3.3V Differential LVPECL to LVTTL Translator

The MC100EPT21 is a Differential LVPECL to LVTTL translator. Because LVPECL (Positive ECL) levels are used only +3.3 V and ground are required. The small outline 8-lead SOIC package makes the EPT21 ideal for applications which require the translation of a clock or data signal.

The V_{BB} output allows this EPT21 to be cap coupled in either single-ended or differential input mode. When single-ended cap coupled, V_{BB} output is tied to the \overline{D} input and D is driven for a non-inverting buffer, or V_{BB} output is tied to the D input and \overline{D} is driven for an inverting buffer. When cap coupled differentially, V_{BB} output is connected through a resistor to each input pin. If used, the V_{BB} pin should be bypassed to V_{CC} via a 0.01 μF capacitor. For additional information see AND8020. For a single-ended direct connection use an external voltage reference source such as a resistor divider. Do not use V_{BB} for a single-ended direct connection or port to another device.

- 1.4 ns Typical Propagation Delay
- Maximum Frequency > 275 MHz Typical
- 24 mA TTL outputs
- Operating Range: $V_{CC} = 3.0 \text{ V}$ to 3.6 V with GND = 0 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at GND
- The 100 Series Contains Temperature Compensation
- V_{BB} Output
- New Differential Input Common Mode Range



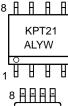
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SO-8 D SUFFIX CASE 751





TSSOP-8 DT SUFFIX CASE 948R



A = Assembly Location

L = Wafer Lot

Y = Year

W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT21D	SO-8	98 Units/Rail
MC100EPT21DR2	SO-8	2500 Tape & Reel
MC100EPT21DT	TSSOP-8	100 Units/Rail
MC100EPT21DTR2	TSSOP-8	2500 Tape & Reel

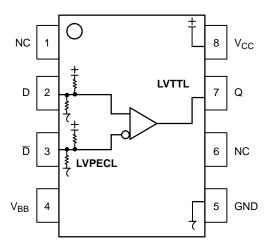
PIN

D**, \overline{D} **

 V_{CC}

 V_{BB}

GND



NC No Connect

Ground

** Pins will default to V_{CC}/2 when left open.

PIN DESCRIPTION

Differential LVPECL Input Pair

Output Reference Voltage

FUNCTION

LVTTL Output

Positive Supply

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

ATTRIBUTES

Characteris	Value	
Internal Input Pulldown Resistor	75 kΩ	
Internal Input Pullup Resistor	37.5 kΩ	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1.5 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time C	Level 1	
Flammability Rating	UL 94 V-0 @ 0.125 in	
Transistor Count	81 Devices	
Meets or exceeds JEDEC Spec EIA/s	JESD78 IC Latchup Test	

^{1.} For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Power Supply	GND = 0 V		3.8	V
V _{IN}	PECL Input Voltage	GND = 0 V	$V_{I} \leq V_{CC}$	0 to 3.8	V
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
$\theta_{\sf JA}$	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W
θ JC	Thermal Resistance (Junction-to-Case)	std bd	8 TSSOP	41 to 44	°C/W
T _{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

^{2.} Maximum Ratings are those values beyond which device damage may occur.

PECL INPUT DC CHARACTERISTICS $V_{CC} = 3.3 \text{ V, GND} = 0.0 \text{ V (Note 3)}$

Symbol	Characteristic			-40 °C			25°C			85°C		Unit
		Ī	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
V _{IH}	Input HIGH Voltage (Single-Ended)		2075		2420	2075		2420	2075		2420	mV
V _{IL}	Input LOW Voltage (Single-Ended)		1355		1675	1355		1675	1355		1675	mV
V _{BB}	Output Voltage Reference		1775	1875	1975	1775	1875	1975	1775	1875	1975	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4)		2.0		3.3	2.0		3.3	2.0		3.3	V
I _{IH}	Input HIGH Current				150			150			150	μΑ
I _{IL}		D D	-150		0.5	-150		0.5	-150		0.5	μΑ

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

TTL OUTPUT DC CHARACTERISTICS $V_{CC} = 3.3 \text{ V}$, GND = 0.0 V, $T_A = -40 ^{\circ}\text{C}$ to $85 ^{\circ}\text{C}$

Symbol	Characteristic	Condition	Min	Тур	Max	Unit
V _{OH}	Output HIGH Voltage (Note 5)	I _{OH} = -3.0 mA	2.4			V
V _{OL}	Output LOW Voltage (Note 5)	I _{OL} = 24 mA			0.5	V
I _{CCH}	Power Supply Current	Outputs set to HIGH	5	12	20	mA
I _{CCL}	Power Supply Current	Outputs set to LOW	8	18	26	mA
Ios	Output Short Circuit Current		-130		-80	mA

^{5.} All loading with 500 Ω to GND.

AC CHARACTERISTICS $V_{CC} = 3.0 \text{ V}$ to 3.6 V, GND = 0.0 V (Note 6)

				-40 °C 25°C								
Symbol	Characteristic		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{max}	Maximum Frequency (See Figure 2. F _{max} /JITTER)		275	350		275	350		275	350		MHz
t _{PLH} , t _{PHL}	Propagation Delay to Output Differential		1200 1200	1450 1400	1800 1800	1200 1200	1450 1400	1800 1800	1300 1200	1450 1400	1900 1900	ps
t _{SK++} t _{SK} t _{SKPP}	Output-to-Output Skew++ Output-to-Output Skew- Part- to- Part Skew (Note 7)				60 25 500			60 25 500			60 25 500	ps
t _{JITTER}	Cycle-to-Cycle Jitter (See Figure 2 F _{max} /JITTER)			0.2	< 1		0.2	< 1		0.2	< 1	ps
V _{PP}	Input Voltage Swing (Differential)		150	800	1200	150	800	1200	150	800	1200	mV
t _r t _f	Output Rise/Fall Times (0.8V - 2.0V)	Q, \overline{Q}	330	500	900	330	500	900	330	500	900	ps

^{6.} Measured with a 750 mV 50% duty-cycle clock source. R_L = 500 Ω to GND and C_L = 20 pF to GND. Refer to Figure 3.

Input parameters vary 1:1 with V_{CC}.
 V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

^{7.} Skews are measured between outputs under identical transitions.

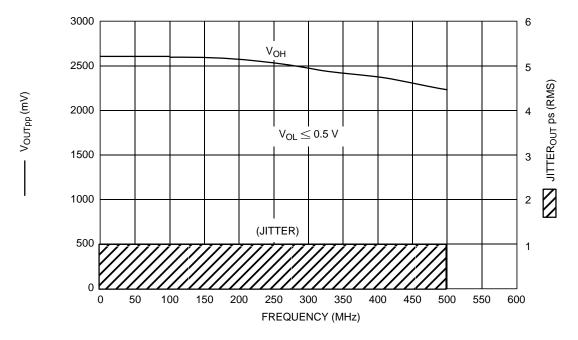


Figure 2. F_{max}/Jitter

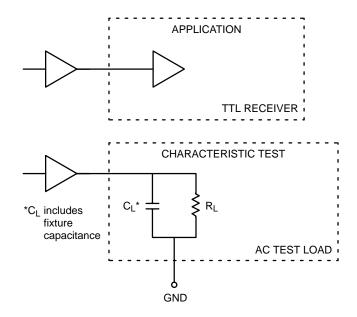


Figure 3. TTL Output Loading Used For Device Evaluation

Resource Reference of Application Notes

AN1404 - ECLinPS Circuit Performance at Non-Standard V_{IH} Levels

AN1405 - ECL Clock Distribution Techniques

AN1406 - Designing with PECL (ECL at +5.0 V)

AN1504 - Metastability and the ECLinPS Family

AN1568 - Interfacing Between LVDS and ECL

AN1650 - Using Wire-OR Ties in ECLinPS Designs

AN1672 - The ECL Translator Guide
AND8001 - Odd Number Counters Design

AND8002 - Marking and Date Codes

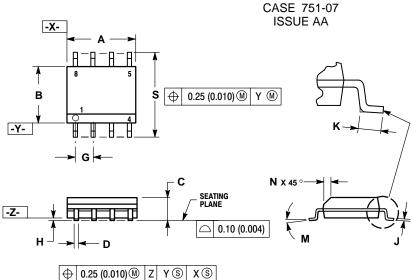
AND8009 - ECLinPS Plus Spice I/O Model Kit

AND8020 - Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.

PACKAGE DIMENSIONS

SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07

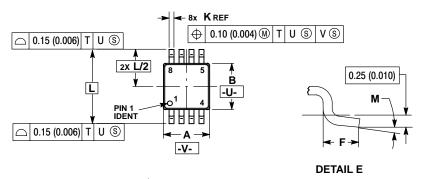


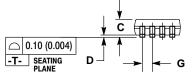
- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDAARD IS 751-07

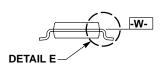
	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.80	5.00	0.189	0.197
В	3.80	4.00	0.150	0.157
C	1.35	1.35 1.75		0.069
D	0.33	0.33 0.51		0.020
G	1.27	7 BSC	0.05	0 BSC
Н	0.10	0.10 0.25		0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	5.80 6.20		0.244

PACKAGE DIMENSIONS

TSSOP-8 **DT SUFFIX** PLASTIC TSSOP PACKAGE CASE 948R-02 **ISSUE A**







NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

 5. TERMINAL NI IMBERS ARE SHOWN FOR

- PER SIDE.
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE W–.

	MILLIN	IETERS	INCHES			
DIM	MIN	MAX	MIN	MAX		
Α	2.90	3.10	0.114	0.122		
В	2.90	3.10	0.114	0.122		
С	0.80	1.10	0.031	0.043		
D	0.05 0.15		0.002	0.006		
F	0.40	0.70	0.016	0.028		
G	0.65	BSC	0.026	BSC		
K	0.25 0.40 0.010		0.010	0.016		
L	4.90	BSC	0.193			
M	0°	6 °	0°	6°		

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