MC100EPT22

3.3V Dual LVTTL/LVCMOS to Differential LVPECL Translator

The MC100EPT22 is a dual LVTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Positive ECL) levels are used only +3.3 V and ground are required. The small outline 8-lead package and the single gate of the EPT22 makes it ideal for those applications where space, performance, and low power are at a premium. Because the mature MOSAIC 5 process is used, low cost and high speed can be added to the list of features.

- 420 ps Typical Propagation Delay
- Maximum Frequency > 1.1 GHz Typical
- Operating Range: V_{CC} = 3.0 V to 3.6 V with GND = 0 V
- PNP LVTTL Inputs for Minimal Loading
- Q Output Will Default HIGH with Inputs Open
- The 100 Series Contains Temperature Compensation.

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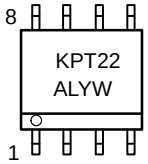
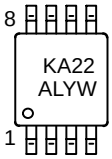
MARKING DIAGRAMS*

SO-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R

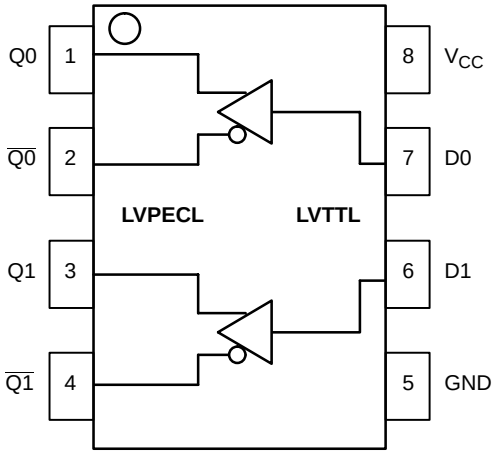


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EPT22D	SO-8	98 Units/Rail
MC100EPT22DR2	SO-8	2500 Tape & Reel
MC100EPT22DT	TSSOP-8	100 Units/Rail
MC100EPT22DTR2	TSSOP-8	2500 Tape & Reel



PIN DESCRIPTION

PIN	FUNCTION
Q0, Q1, $\overline{Q0}$, $\overline{Q1}$	LVPECL Differential Outputs
D0, D1	LVTTL Inputs
V_{CC}	Positive Supply
GND	Ground

Figure 1. 8-Lead Pinout (Top View) **and Logic Diagram**

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		N/A
Internal Input Pullup Resistor		N/A
ESD Protection	Human Body Model Machine Model Charged Device Model	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		164 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Power Supply	GND = 0 V		6	V
V_I	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	8 TSSOP	41 to 44	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

TTL INPUT DC CHARACTERISTICS V_{CC}= 3.3 V, GND= 0.0 V, T_A= -40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V			20	μA
I_{IHH}	Input HIGH Current MAX	V_{IN} = V_{CC}			100	μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V			-0.6	mA
V_{IK}	Input Clamp Voltage	I_{IN} = -18 mA			-1.0	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V

PECL OUTPUT DC CHARACTERISTICS V_{CC} = 3.3 V, GND = 0.0 V (Note 3)

		-40 °C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	Power Supply Current	32	43	55	35	45	60	37	46	62	mA
V_{OH}	Output HIGH Voltage (Note 4)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 4)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

3. Output parameters vary 1:1 with V_{CC}.
4. All loading with 50 Ω to V_{CC}- 2.0 V.

AC CHARACTERISTICS V_{CC}= 3.0 V to 3.6 V, GND= 0.0 V (Note 5)

		-40 °C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Frequency (See Figure 2. F_{max}/JITTER)	0.8	1.1		0.8	1.1		0.8	1.1		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	250	400	650	250	420	675	300	500	700	ps
t_{skew}	Within-Device Skew (Note 6) Device-to-Device Skew (Note 7)		50 200	100 400		50 200	100 425		50 200	100 400	ps
t_{JITTER}	Random Clock Jitter (See Figure 2. F_{max}/JITTER)		0.2	< 1		0.2	< 1		0.2	< 1	ps
t_r t_f	Output Rise/Fall Times (20% - 80%) Q, $\overline{Q}$	50	110	200	60	120	220	70	140	250	ps

5. Measured using a 2.4 V source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V.
6. Skew is measured between outputs under identical transitions and conditions on any one device.
7. Device-to-Device Skew for identical transitions at identical V_{CC} levels.

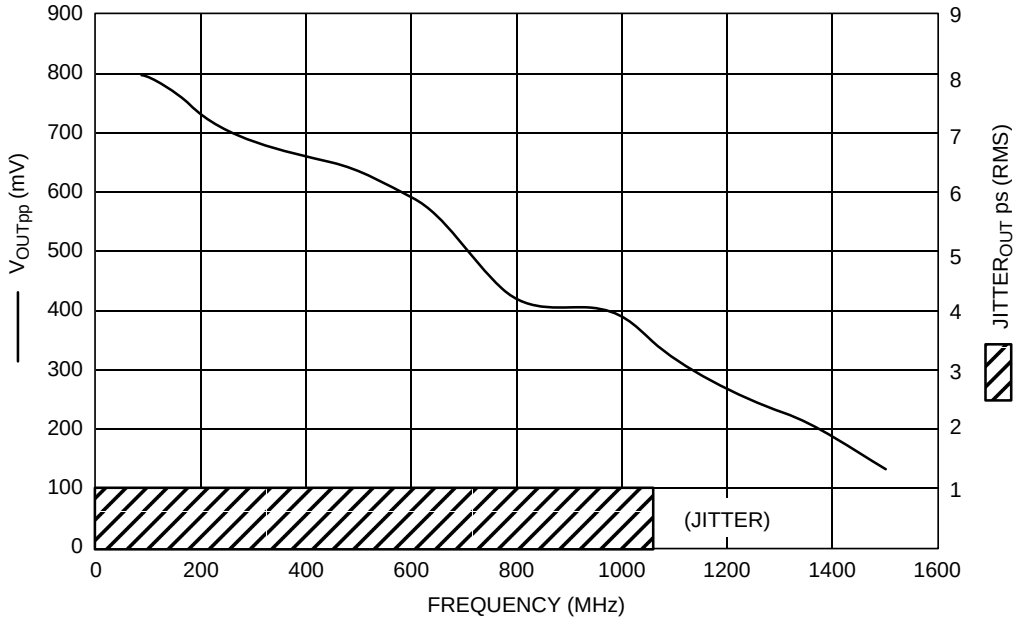


Figure 2. F_{max}/Jitter

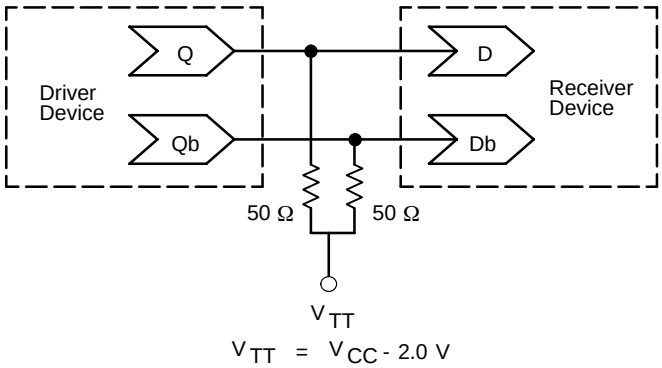


Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 - Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 - ECLinPS Circuit Performance at Non-Standard V_{IH} Levels

AN1405 - ECL Clock Distribution Techniques

AN1406 - Designing with PECL (ECL at +5.0 V)

AN1504 - Metastability and the ECLinPS Family

AN1568 - Interfacing Between LVDS and ECL

AN1650 - Using Wire-OR Ties in ECLinPS Designs

AN1672 - The ECL Translator Guide

AND8001 - Odd Number Counters Design

AND8002 - Marking and Date Codes

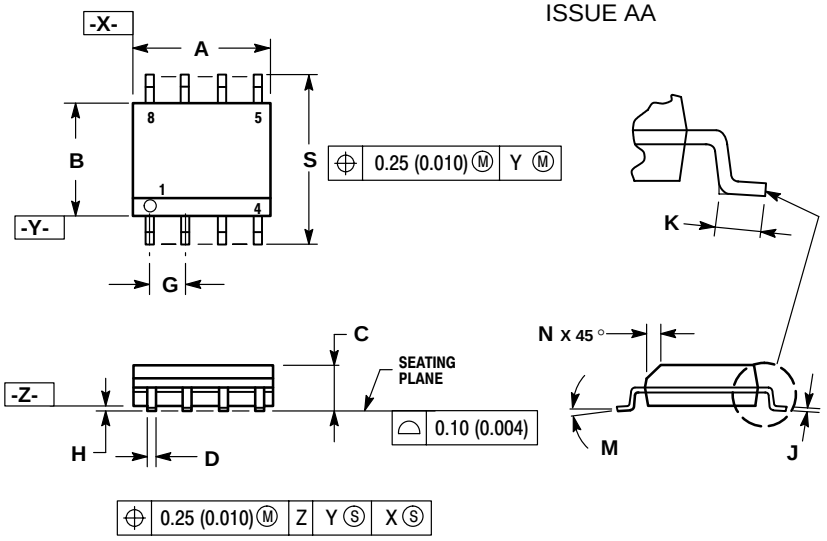
AND8009 - ECLinPS Plus Spice I/O Model Kit

AND8020 - Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.

PACKAGE DIMENSIONS

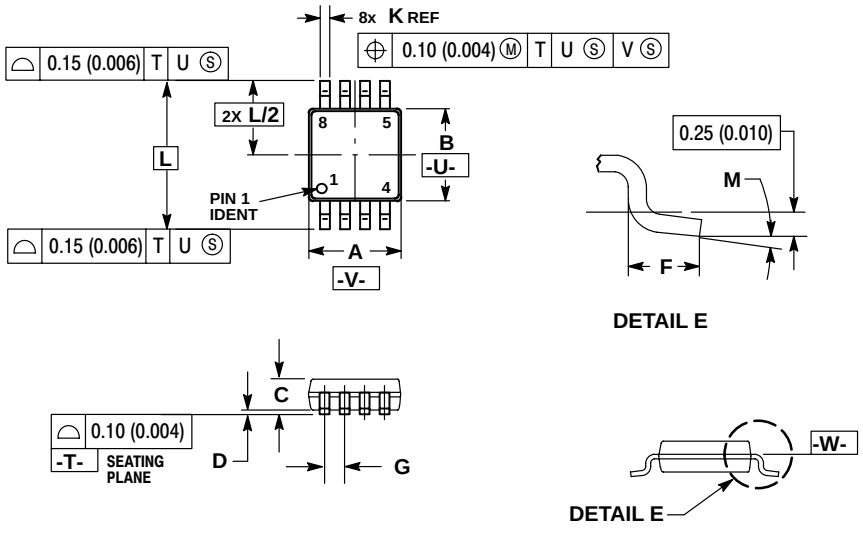
SO-8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-07
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751–01 THRU 751–06 ARE OBSOLETE. NEW STANDAARD IS 751–07

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

TSSOP-8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R-02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0 °	6 °	0 °	6 °

Notes

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