NB7L216

2.5V/3.3V, 12Gb/s Multi Level Clock/Data Input to RSECL, High Gain Receiver/Buffer/Translator with Internal Termination

The NB7L216 is a differential receiver/driver with high gain output targeted for high frequency applications. The device is functionally equivalent to the NBSG16 but with much higher gain output. This highly versatile device provides 35 dB of gain up to 7 GHz.

Inputs incorporate internal 50 Ω termination resistors and accept Negative ECL (NECL), Positive ECL (PECL), LVTTL, LVCMOS, CML, or LVDS. Outputs are Reduced Swing ECL (RSECL), 400 mV.

The V_{BB} pin is internally generated voltage supply available to this device only. The V_{BB} is used as a reference voltage for single−ended NECL or PECL inputs. For all single−ended input conditions, the unused complementary differential input should be connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} output should be left open.

Application notes, models and support documentation are available at www.onsemi.com.

Features

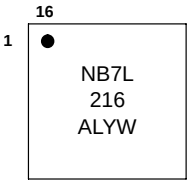
- High Gain of 35 dB from DC to 7 GHz Typical
- High IIP3: 0 dB Typical
- 20 mV Minimum Input Voltage Swing
- Maximum Input Clock Frequency up to 8.5 GHz
- Maximum Input Data Rate up to 12 Gb/s Typical
- <0.5 ps of RMS Clock Jitter
- <9 ps of Data Dependent Jitter
- 120 ps Typical Propagation Delay
- 30 ps Typical Rise and Fall Times
- RSPECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.465 V
- RSECL Output Level (400 mV Peak−to−Peak Output),
- 50 Ω Internal Input Termination Resistors (Temperature−Coefficient of < 6.38 mΩ/°C)
- V_{BB} – ECL Reference Voltage Output
- Pb−Free Packages are Available

ON Semiconductor®

http://onsemi.com

QFN−16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional marking information, refer to Application Note AND8002/D.

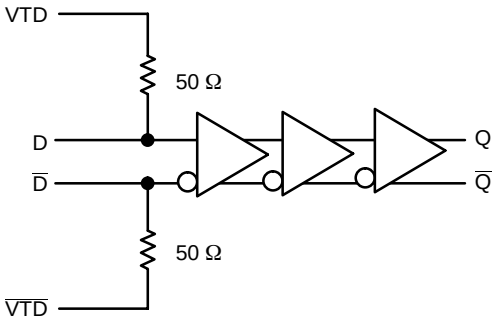


Figure 1. Functional Block Diagram

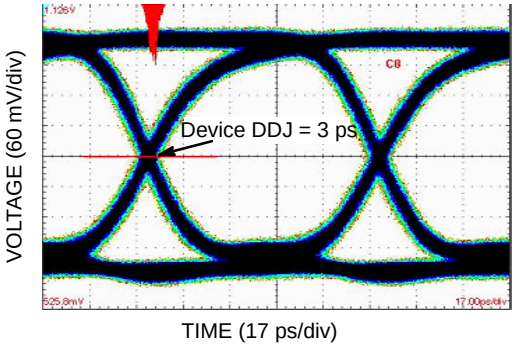


Figure 2. Typical Output Waveform at 12 Gb/s with PRBS 2^{23}–1 (V_{INPP} = 400 mV, Input Signal DDJ = 12 ps)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

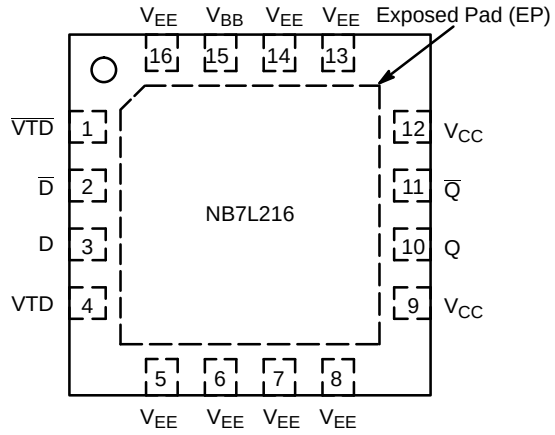


Figure 3. QFN−16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	$\overline{VTD}$	−	Internal 50 Ω termination pin. See Table 7. Note 1
2	$\overline{D}$	LVPECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted differential input. Note 1.
3	D	LVPECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted differential input. Note 1.
4	VTD	−	Internal 50 Ω termination pin. See Table 7. Note 1.
15	V_{BB}	−	Internally generated ECL reference voltage supply.
5, 6, 7, 8, 13, 14, 15	V_{EE}	−	Negative supply voltage. All V_{EE} pins must be externally connected to power supply to guarantee proper operation.
9, 12	V_{CC}	−	Positive supply voltage. All V_{CC} pins must be externally connected to power supply to guarantee proper operation
10	Q	RSECL Output	Noninverted differential output. Typically receiver terminated with 50 Ω resistor to $V_{TT} = V_{CC} - 2.0$ V.
11	$\overline{Q}$	RSECL Output	Inverted differential output. Typically receiver terminated with 50 Ω resistor to $V_{TT} = V_{CC} - 2.0$ V.
−	EP	−	Exposed pad (EP). Thermally exposed pad on the package bottom must be attached to a heat sinking conduit. It is recommended to connect the EP to the lower potential, V_{EE}.

1. In the differential configuration when the input termination pins (VTD, $\overline{VTD}$) are connected to a common termination voltage and if no signal is applied on D/$\overline{D}$ input then the device will be susceptible to self−oscillation.

Table 2. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model Charged Device Model	> 500 kV > 50 V > 4 kV
Moisture Sensitivity (Note 2)	QFN−16	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		164
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test.		

2. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS (Note 3)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		−3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	V_I = V_{CC} V_I = V_{EE}	3.6 −3.6	V V
V_{INPP}	Differential Input Voltage $\lvert D - \overline{D} \rvert$			2.8	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{OUT}	Output Current	Continuous Surge		25 50	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 4)	0 lfpm 500 lfpm	QFN−16 QFN−16	42 35	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	1S2P (Note 4)	QFN−16	4	°C/W
T_{sol}	Wave Solder Pb Pb−Free	<2 Sec @ 248°C <2 Sec @ 260°C		265 265	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

3. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
4. JEDEC standard multilayer board − 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 4. DC CHARACTERISTICS, CLOCK INPUTS, CML OUTPUTS V_{CC} = 2.375 V to 3.465 V, V_{EE} = 0 V

Symbol	Characteristic	−40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current (VTD/$\overline{VTD}$ open)		27	35		27	35		27	35	mA
V_{OH}	Output HIGH Voltage (Note 5 and 6)	V_{CC} −1040	V_{CC} −980	V_{CC} −940	V_{CC} −1000	V_{CC} −950	V_{CC} −900	V_{CC} –950	V_{CC} −900	V_{CC} −850	mV
V_{OL}	Output LOW Voltage (Note 5 and 6)	V_{CC} −1520	V_{CC} −1430	V_{CC} −1320	V_{CC} −1470	V_{CC} −1370	V_{CC} −1270	V_{CC} –1440	V_{CC} −1340	V_{CC} −1240	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (see Figures 14 and 16)											
V_{TH}	Input Threshold Reference Voltage Range (Note 7 and 8)	1100		V_{CC} −10	1100		V_{CC} −10	1100		V_{CC} −10	mV
V_{IH}	Single−ended Input HIGH Voltage (Note 8)	V_{th} +10		V_{CC}	V_{th} + 10		V_{CC}	V_{th} +10		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage (Note 8)	V_{EE}		V_{th} −10	V_{EE}		V_{th} −10	V_{EE}		V_{th} −10	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 15 and 17)											
V_{IHD}	Differential Input HIGH Voltage (Note 9)	1105		V_{CC}	1105		V_{CC}	1105		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage (Note 9)	V_{EE}		V_{CC} −10	V_{EE}		V_{CC} −10	V_{EE}		V_{CC} −10	mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 9 and 10)	1100		V_{CC} −5	1100		V_{CC} –5	1100		V_{CC} –5	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	10		2500	10		2500	10		2500	mV
V_{IO}	Input Offset Voltage (Note 11)	−5	0	+5	−5	0	+5	−5	0	+5	mV
V_{BB}	Internally Generated Reference Voltage Supply (Only 3 V – 3.6 V Supply Load with −100 μA)	V_{CC} −1425	V_{CC} −1345	V_{CC} −1265	V_{CC} −1425	V_{CC} −1345	V_{CC} −1265	V_{CC} −1425	V_{CC} −1345	V_{CC} −1265	mV
I_{IH}	Input HIGH Current D/Db (VTD/$\overline{VTD}$ Open)	0	20	100	0	20	100	0	20	100	μA
I_{IL}	Input LOW Current D/Db (VTD/$\overline{VTD}$ Open)	−25	10	75	−25	10	75	−25	10	75	μA
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
R_{T_Coef}	Internal Input Termination Resistor Temperature Coefficient		6.38			6.38			6.38		mΩ/°C

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Outputs evaluated with 50 Ω resistors to $V_{TT} = V_{CC}$ − 2.0 V for proper operation.
6. Input and output parameters vary 1:1 with V_{CC}.
7. V_{TH} is applied to the complementary input when operating in single−ended mode.
8. V_{IH}, V_{IL} and V_{TH} parameters must be complied simultaneously.
9. V_{IHD}, V_{ILD} and V_{CMR} parameters must be complied simultaneously.
10. V_{CMR} min varies 1:1 with V_{EE}, V_{CMR} max varies 1:1 with V_{CC}.
11. Typical standard deviation of input offset voltage is 1.76 mV.

Table 5. AC CHARACTERISTICS V_{CC} = 2.375 V to 3.465 V, V_{EE} = 0 V; (Note 12)

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \le 7.0$ GHz (See Figure 4) $f_{in} \le 8.5$ GHz	275 100	380 250		275 100	380 250		275 100	380 250		mV
f_{DATA}	Maximum Operating Data Rate	10	12		10	12		10	12		Gb/s
|S21|	Power Gain DC to 7 GHz		35			35			35		dB
|S11|	Input Return Loss @ 7 GHz		−10			−10			−10		dB
|S22|	Output Return Loss @ 7 GHz		−5			−5			−5		dB
|S12|	Reverse Isolation (Differential Configuration)		−25			−25			−25		dB
IIP3	Input Third Order Intercept		0			0			0		dBm
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential @ 1 GHz	60	120	180	60	120	180	60	120	180	ps
t_{SKEW}	Duty Cycle Skew (Note 12) Device to Device Skew (Note 17)		2 5	10 20		2 5	10 20		2 5	10 20	ps
t_{JITTER}	RMS Random Clock Jitter $f_{in} \le 8.5$ GHz (Note 15) Peak−to−Peak Data Dependent Jitter (Note 16) f_{DATA} = 3.5 Gb/s f_{DATA} = 5.0 Gb/s f_{DATA} = 10 Gb/s f_{DATA} = 12 Gb/s		0.1 1 3 4 4	0.5 7 9 9 9		0.1 1 3 4 4	0.5 7 9 9 9		0.1 1 3 4 4	0.5 7 9 9 9	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 14 and Figure 12)	20		2500	20		2500	20		2500	mV
t_r t_f	Output Rise/Fall Times @ 0.5 GHz (20% − 80%) Q, $\overline{Q}$		30	45		30	45		30	45	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

12. Measured by forcing $V_{INPPmin}$ from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{TT} = V_{CC} − 2.0 V. Input edge rates 40 ps (20% − 80%).
13. Duty cycle skew is measured between differential outputs using the deviations of the sum of Tpw− and Tpw+ @ 1 GHz.
14. V_{INPP} (MAX) cannot exceed V_{CC} − V_{EE}. Input voltage swing is a single−ended measurement operating in differential mode.
15. Additive RMS jitter with 50% duty cycle clock signal.
16. Additive peak−to−peak data dependent jitter with input NRZ data at PRBS 2^{23}−1.
17. Device to device skew is measured between outputs under identical transition @ 1 GHz.

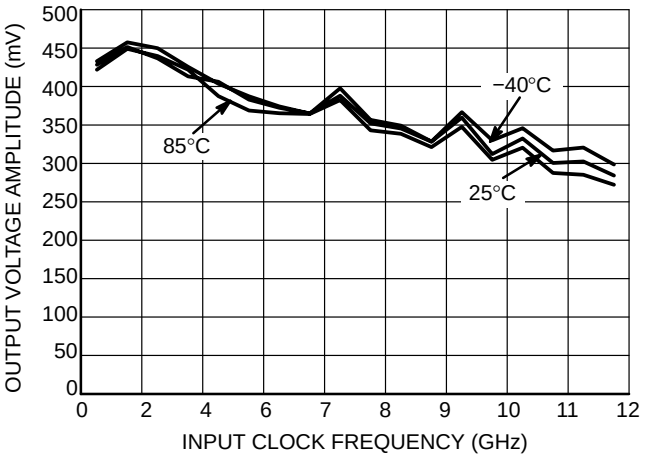


Figure 4. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{IN}) and Temperature (V_{INPP} = 400 mV, V_{CC} = 3.3 V and V_{EE} = 0 V)

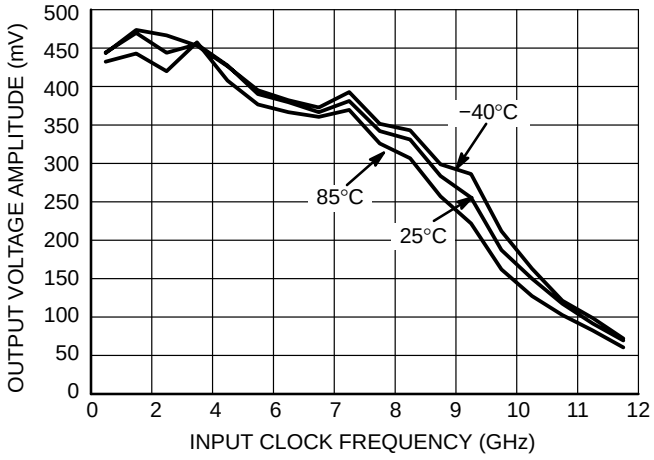


Figure 5. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{IN}) and Temperature (V_{INPP} = 20 mV, V_{CC} = 3.3 V and V_{EE} = 0 V)

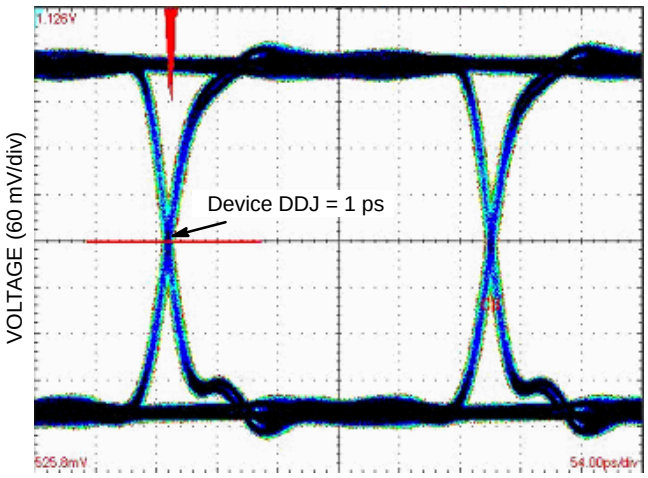


Figure 6. Typical Output Waveform at 2.488 Gb/s with PRBS 2^{23}–1 (V_{INPP} = 400 mV, Input Signal DDJ = 12 ps)

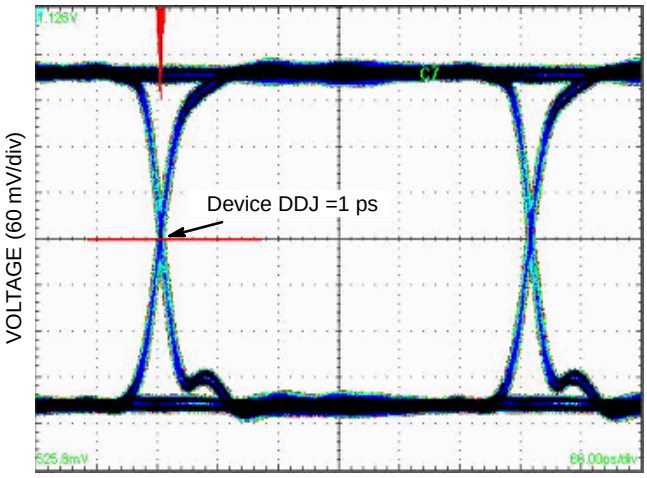


Figure 7. Typical Output Waveform at 3.5 Gb/s with PRBS 2^{23}–1 (V_{INPP} = 400 mV, Input Signal DDJ = 12 ps)

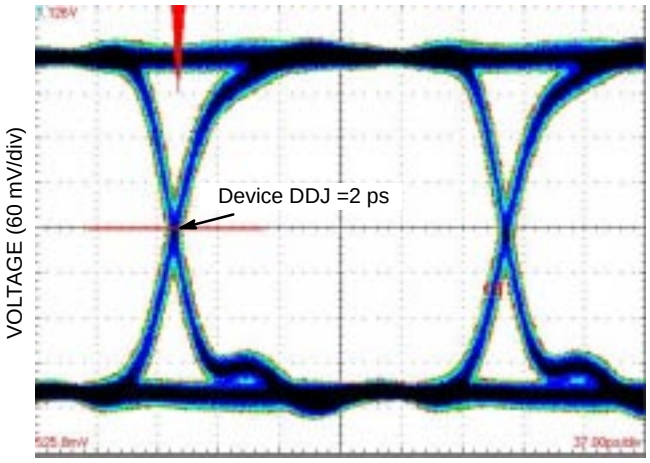


Figure 8. Typical Output Waveform at 5 Gb/s with PRBS 2^{23}–1 (V_{INPP} = 400 mV, Input Signal DDJ = 12 ps)

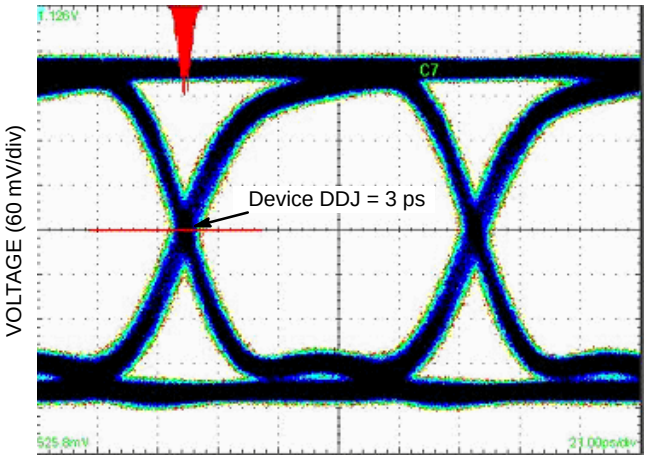


Figure 9. Typical Output Waveform at 10 Gb/s with PRBS 2^{23}–1 (V_{INPP} = 400 mV, Input Signal DDJ = 12 ps)

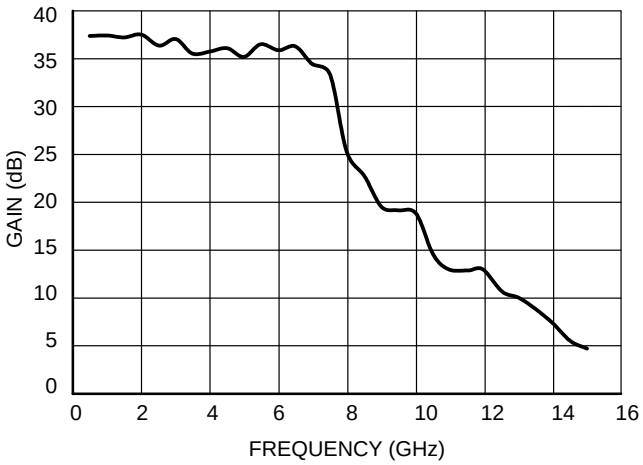


Figure 10. Small Signal Gain – S21 Magnitude*

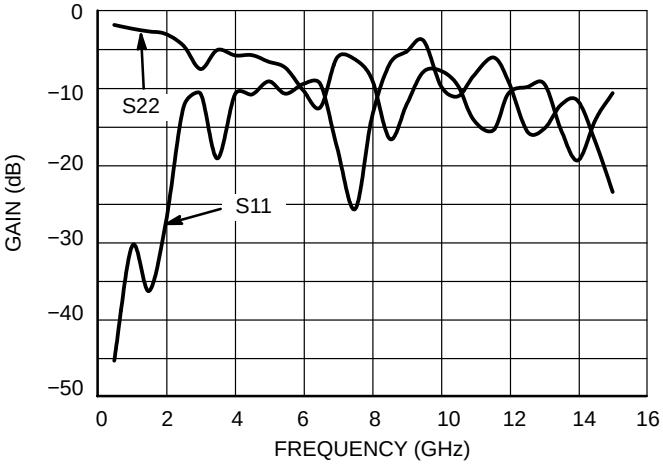


Figure 11. Input and Output Reflection – S11 and S22 Magnitude*

*T_A = +25°C, V_{CC} = 3.3 V, V_{EE}=0 V, P_{IN} = −44 dBm,Z_S = Z_L = 50 Ω, input and output matching network is not included.

Table 6. TYPICAL DEVICE S−PARAMETERS

Frequency (Hz)	S11			S21			S12			S22		
	dbS11	|S11|	∠S11	dbS21	|S21|	∠S21	dbS12	|S12|	∠S12	dbS22	|S22|	∠S22
4.97E+08	−45.2	0.005	−88.5	37.2	72.799	−33.2	−72.3	0.001	−139.1	−2.5	0.749	157.4
1.02E+09	−30.4	0.030	−134.7	37.3	73.145	−68.4	−45.8	0.005	129.8	−2.9	0.714	154.3
1.51E+09	−36.2	0.015	−146.5	37.1	71.433	−105.4	−43.3	0.007	98.5	−2.9	0.717	132.8
2.00E+09	−27.4	0.042	25.7	37.4	74.061	−139.0	−37.1	0.014	91.8	−3.5	0.666	107.1
2.52E+09	−12.3	0.244	−27.7	36.2	64.810	−179.5	−29.9	0.032	54.4	−4.4	0.599	92.1
3.01E+09	−10.6	0.295	−83.8	36.9	70.102	144.5	−26.1	0.050	9.4	−6.3	0.485	77.3
3.50E+09	−19.0	0.112	−22.1	35.4	58.933	99.9	−28.3	0.038	25.9	−5.0	0.566	67.9
4.02E+09	−10.6	0.294	−120.3	35.6	60.437	73.8	−24.8	0.058	−32.6	−7.6	0.417	54.2
4.51E+09	−10.7	0.291	167.4	36.0	62.843	41.1	−22.5	0.075	−68.3	−13.9	0.201	70.2
4.99E+09	−9.0	0.354	87.1	35.1	56.576	14.2	−25.2	0.055	−107.2	−8.7	0.367	81.2
5.48E+09	−10.6	0.294	62.7	36.4	65.812	−16.1	−24.3	0.061	−121.4	−8.0	0.398	50.4
6.01E+09	−9.3	0.341	108.2	35.8	61.327	−72.8	−24.5	0.060	−125.7	−8.0	0.397	−0.9
6.49E+09	−9.4	0.340	59.4	36.2	64.212	−119.4	−21.9	0.080	−152.4	−12.5	0.237	−27.2
6.98E+09	−17.5	0.133	25.5	34.3	52.039	−141.5	−22.7	0.073	177.5	−7.4	0.428	−32.2
7.51E+09	−25.6	0.053	107.9	33.2	45.861	164.6	−24.4	0.060	165.7	−7.0	0.445	−37.9
7.99E+09	−13.7	0.206	146.5	25.2	18.093	133.6	−21.5	0.084	152.8	−7.6	0.416	−54.7
8.52E+09	−6.7	0.462	117.9	22.6	13.434	116.2	−19.4	0.107	120.7	−12.1	0.249	−73.7
9.00E+09	−5.2	0.552	106.2	19.4	9.336	102.0	−19.0	0.112	109.9	−12.2	0.246	−62.5
9.49E+09	−3.7	0.652	71.1	19.0	8.937	61.1	−19.4	0.107	62.0	−11.5	0.267	−100.2
1.00E+10	−9.7	0.326	46.2	18.7	8.595	18.6	−24.0	0.063	50.6	−10.4	0.301	−117.0
1.05E+10	−11.0	0.283	35.8	14.5	5.298	−13.3	−25.9	0.051	12.9	−10.8	0.288	−172.0
1.10E+10	−8.3	0.384	7.2	12.9	4.408	−9.6	−29.4	0.034	21.1	−13.4	0.213	74.0
1.15E+10	−5.9	0.506	−0.4	12.7	4.339	−33.7	−21.4	0.085	36.3	−21.4	0.085	−148.6
1.20E+10	−9.0	0.356	−23.8	12.9	4.395	−63.4	−19.4	0.107	−9.5	−13.4	0.214	159.5
1.25E+10	−15.6	0.166	−46.9	10.5	3.360	−97.8	−21.0	0.089	−39.0	−12.4	0.239	169.2
1.30E+10	−15.1	0.175	−83.0	9.9	3.121	−119.7	−24.0	0.063	−39.9	−11.3	0.272	171.6
1.35E+10	−12.0	0.250	−96.5	8.7	2.728	−148.9	−22.0	0.079	−39.1	−14.9	0.181	177.8
1.40E+10	−11.5	0.265	−105.9	7.3	2.314	−167.1	−18.6	0.118	−74.2	−18.4	0.120	140.3
1.45E+10	−17.0	0.140	−97.8	5.4	1.856	167.6	−20.1	0.099	−107.0	−15.7	0.163	98.2
1.50E+10	−23.4	0.068	−108.9	4.6	1.695	145.0	−20.2	0.098	−128.1	−11.2	0.274	96.1

NOTE: T_A = +25°C, V_{CC}=3.3V, V_{EE} = 0 V, P_{IN} = −44 dBm, Z_S = Z_L = 50 Ω, input and output matching network is not included.

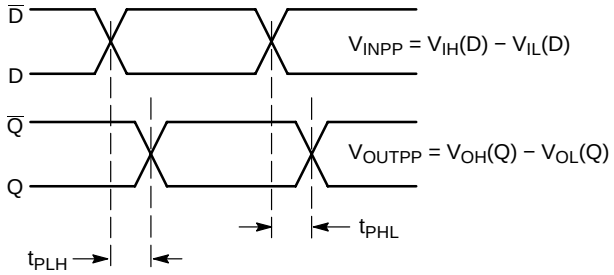


Figure 12. AC Reference Measurement

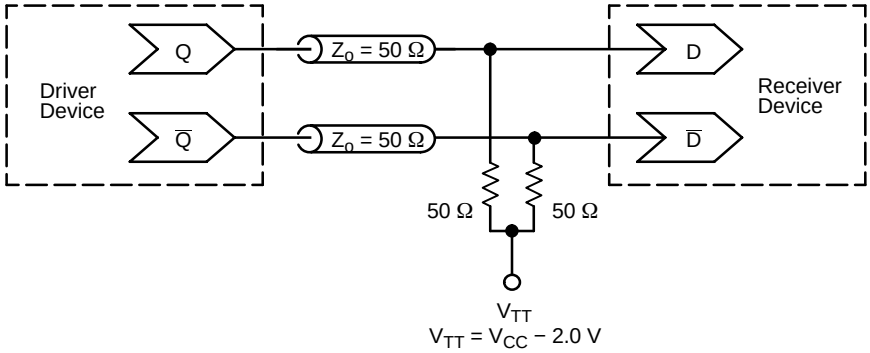


Figure 13. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

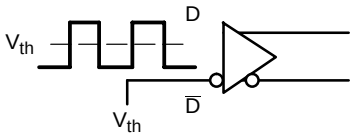


Figure 14. Differential Input Driven Single−Ended

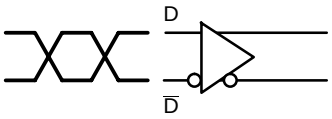


Figure 15. Differential Inputs Driven Differentially

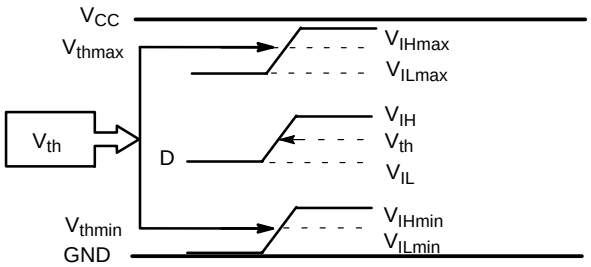
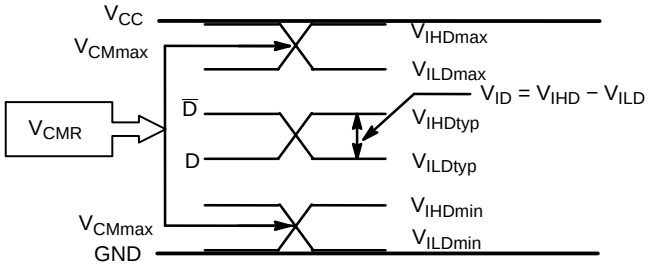


Figure 16. V_{th} Diagram



NOTE: $V_{EE} \le V_{IN} \le V_{CC}$; $V_{IH} > V_{IL}$

Figure 17. V_{CMR} Diagram

APPLICATION INFORMATION

All NB7L216 inputs can accept PECL, CML, LVTTL, LVCMOS and LVDS signal levels. The limitations for differential input signal (LVDS, PECL, or CML) are minimum input swing of 75 mV and the maximum input swing of 2500 mV. Within these conditions, the input voltage can range from V_{CC} to 1.2 V. Examples interfaces are illustrated below in a 50 Ω environment (Z = 50 Ω). For output termination and interface, refer to application note AND8020/D.

Table 7. INTERFACING OPTIONS

Interfacing Options	Connections
CML	Connect VTD and $\overline{VTD}$ to V_{CC} (See Figure 18)
LVDS	Connect VTD and $\overline{VTD}$ Together (See Figure 20)
AC−COUPLED	Bias VTD and $\overline{VTD}$ Inputs within Common Mode Range (V_{CMR}) (See Figure 19)
RSECL, PECL, NECL	Standard ECL Termination Techniques (See Figure 13)
LVTTL, LVCMOS	An External Voltage (V_{THR}) should be Applied to the Unused Complementary Differential Input. Nominal V_{THR} is 1.5 V for LVTTL and V_{CC} / 2 for LVCMOS Inputs. This Voltage must be within the V_{THR} Specification. (See Figure 21)

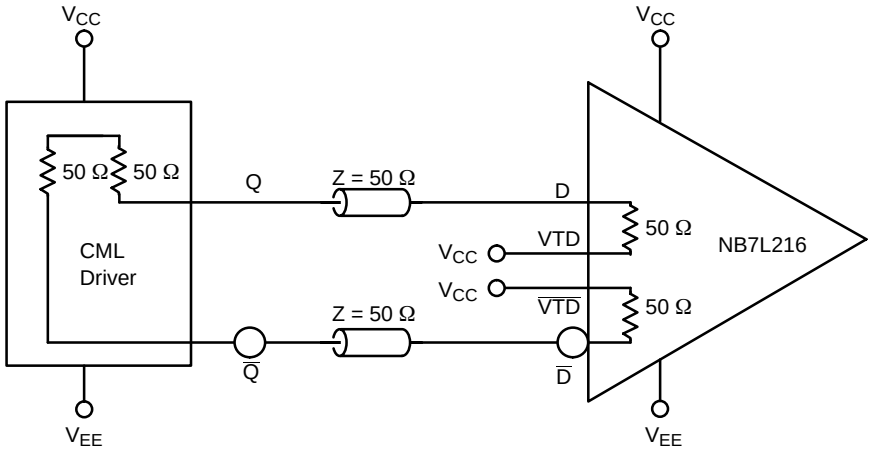
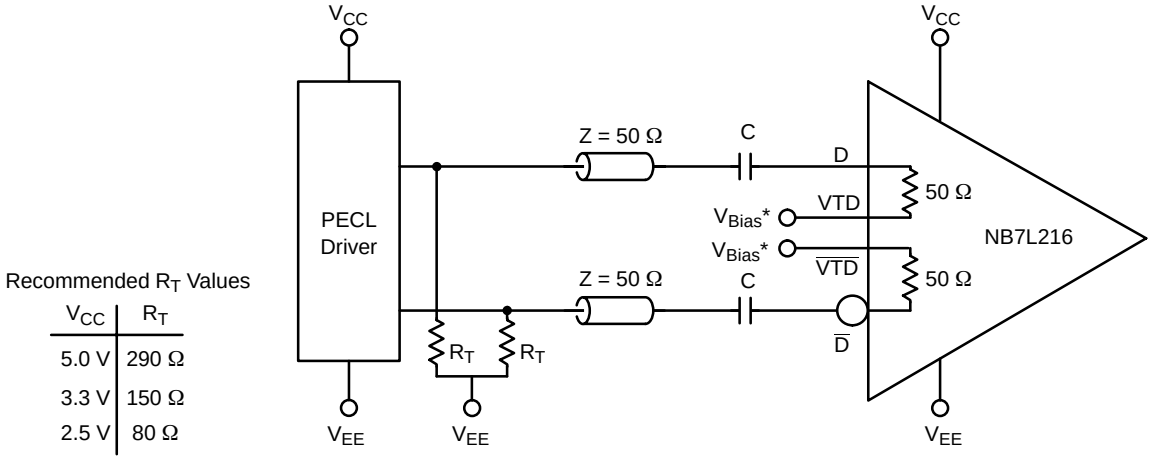


Figure 18. CML to NB7L216 Interface



Recommended R_T Values

V_{CC}	R_T
5.0 V	290 Ω
3.3 V	150 Ω
2.5 V	80 Ω

*V_{Bias} must be within common mode range limits (V_{CMR})

Figure 19. PECL to NB7L216 Interface

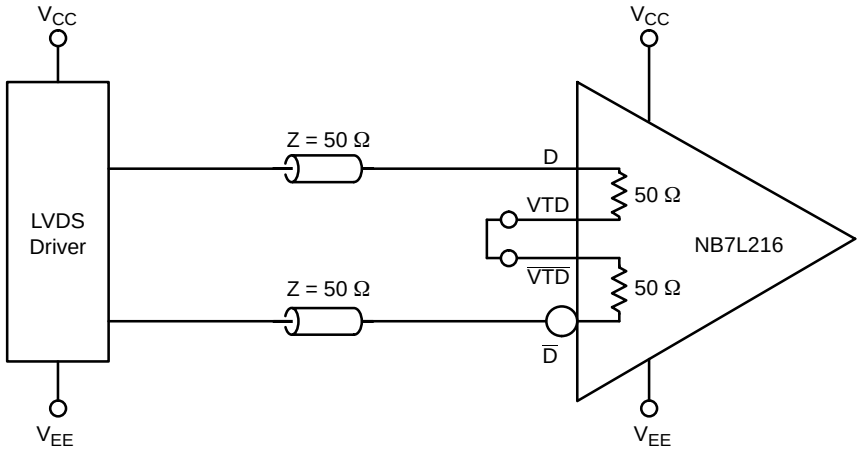


Figure 20. LVDS to NB7L216 Interface

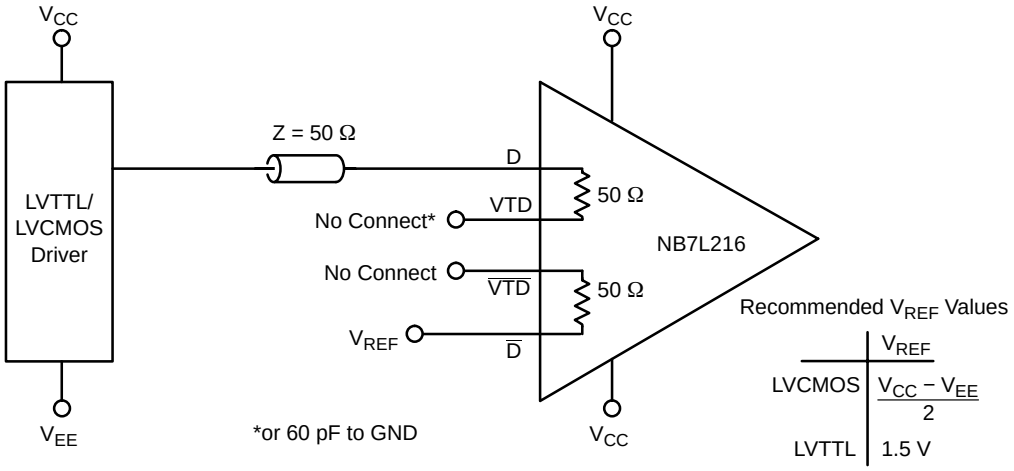


Figure 21. LVCMOS/LVTTL to NB7L216 Interface

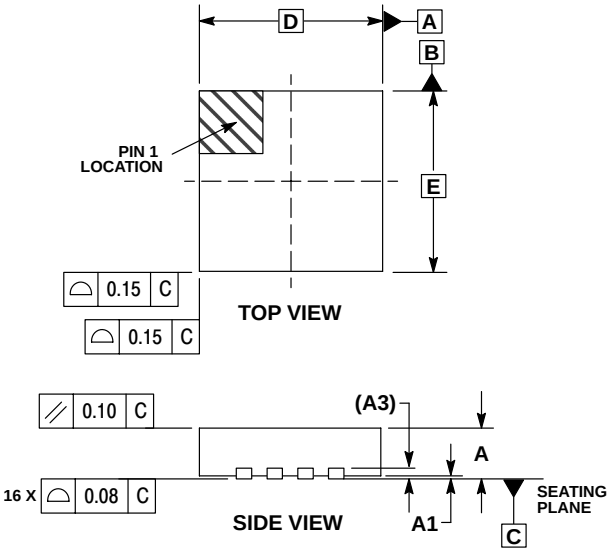
ORDERING INFORMATION

Device	Package	Shipping†
NB7L216MN	QFN−16	123 Units / Rail
NB7L216MNG	QFN−16 (Pb−Free)	123 Units / Rail
NB7L216MNR2	QFN−16	3000 / Tape & Reel
NB7L216MNR2G	QFN−16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

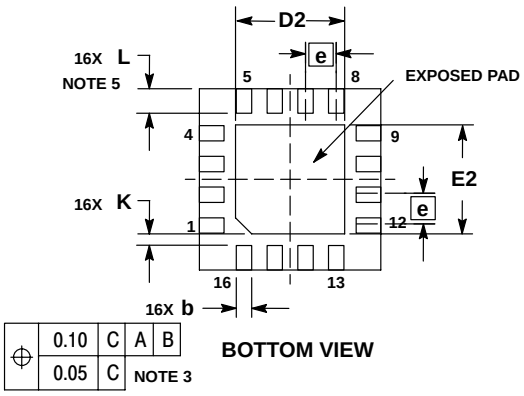
PACKAGE DIMENSIONS

16 PIN QFN
CASE 485G−01
ISSUE B

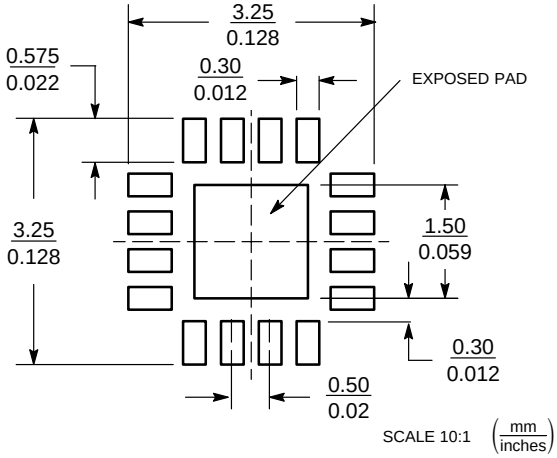


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50



SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.