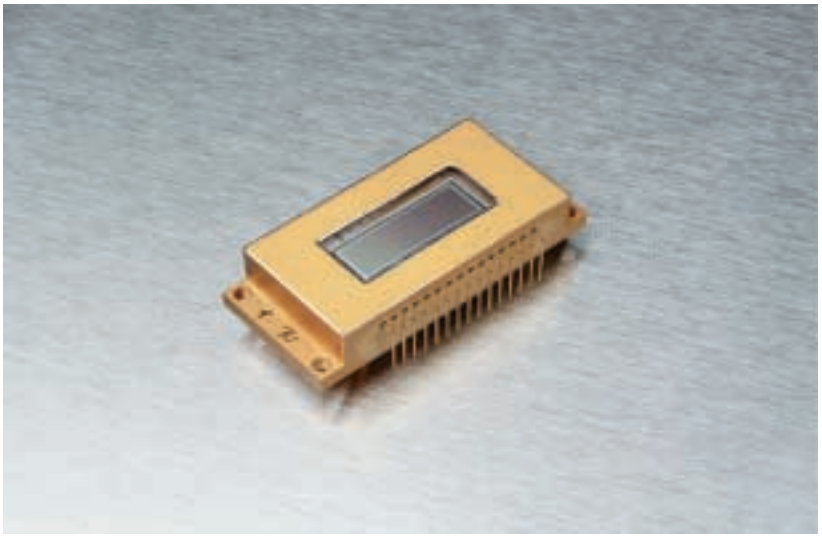
DATASHEET

RETICON®

RA1133J Full Frame CCD Image Sensor

24 µm square pitch, 1100 x 330 pixel configuration



Description

The RA1133J is a full frame CCD sensor with reset capabilities designed specifically for use in spectroscopy, biomedical imaging and related scientific imaging applications. The package for the array is designed with an integrated two stage thermoelectric cooler. This enables the device to be run 40° C below ambient temperature, -15° C when compared to room temperature. Its combination of very low noise and low dark current make it ideal for low light, high dynamic range and high resolution applications.

The imager is structured with a single output register at one end of the imaging columns. A lateral reset drain is located adjacent to this readout register which enables the dumping of accumulated charge from the array. Two phase clocks are needed to drive the readout register. Three phase clocks are needed to drive imaging cells. The array is available in a 30-pin metal package with an integrated TE cooler as shown in Figure 1. Package dimensions are shown in Figure 8.

MPP Operation

A major source of dark current in devices such as this originates in surface states at the Si-SiO2 interface. A unigue design and process enables the RA1133J to be run in "multi-pinned phase" or MPP mode of operation. This helps eliminate dark current generation in the interface surface states. By holding the vertical clocks at negative potential during integration and horizontal signal readout, the surface will not be depleted and the surface state will not generate dark current.

Caution: While the RA1133J imagers have been designed to resist electrostatic discharge (ESD), they can be damaged from such discharges. Always observe proper ESD precautions when handling and storing these sensors.

Features

- 363,000 picture elements (pixels) in a 1100 x 330 configuration
- 24 µm square pixels
- 2-phase buried channel process
- On-chip amplifier for low noise and high speed readout
- Dynamic range greater than 25,000:1
- On-chip temperature sensor
- Two stage TE cooler integrated into the package
- Hermetically sealed
- 100% fill factor
- 10 MHz data rate

PerkinElmer™ optoelectronics

Imaging Area

The imaging area is an array of 1100 columns (vertical CCD shift registers). Each column has 330 picture elements. The pixel size is 24 µm by 24 µm. The total imaging area is 26.4 mm by 7.92 mm. Typical spectral response as a function of wavelength is shown in Figure 2. This is for both the standard array and an array coated with lumogen, an UV phosphor that extends the range of the detector into the ultraviolet.

In the vertical direction, each pixel corresponds to one stage (three electrodes) of the shift register. The three electrode groups are driven by three-phases (Ø1V - Ø3V) brought in from both edges of the array to improve clock electrode response time. Charge packets (imaging data) in the vertical register can be shifted to the horizontal readout by clocking the three phases (Ø1V, Ø2V and Ø3V). A transfer gate (ØTG) is provided at the interface of the vertical register. The transfer gate controls the transferring of charge into the horizontal readout register. Charge flow is from Ø3 gate of the vertical shift register into Ø1 gate of the horizontal readout register. The control function is performed by pulsing the transfer gate high to permit the charge flow from the vertical register into the horizontal register for readout. When the potential of the vertical register electrodes is held steady, a potential well is created beneath the storage gates Ø1V and Ø2V. When an image impinges on the sensing area, an electrical signal of the scene will be collected in the potential well during this integration period.

Following the integration interval, the collected charge (signal) in the array can be read out as a full frame image by transferring the charge, one or more rows at a time, into the horizontal shift register. From here, the charge can be shifted serially to the output amplifier. A mechanical shutter is needed to shield the array from incident light during the readout process. A strobe illumination could be used to stimulate the shuttered mode of operation. Image smearing degrades the performance, particularly at low data rates, unless shuttering is provided.

Horizontal Register

The horizontal shift register is driven by two phase clocks (Ø1H and Ø2H). The horizontal register has 1100 stages plus an extension of 35 stages (3 dummy stages, 16 leading isolation stages and 16 trailing isolation stages). As a result, amplifier power is dissipated more efficiently and dark current generation by localized heating is minimized.

Figure 1. Pinout Configuration

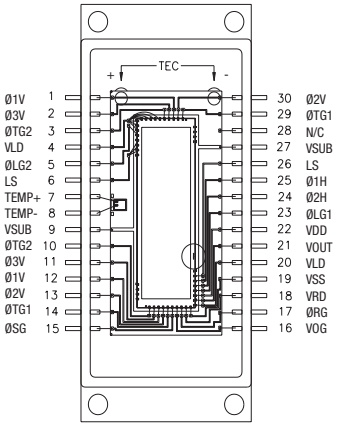


Figure 2. Quantum Efficiency

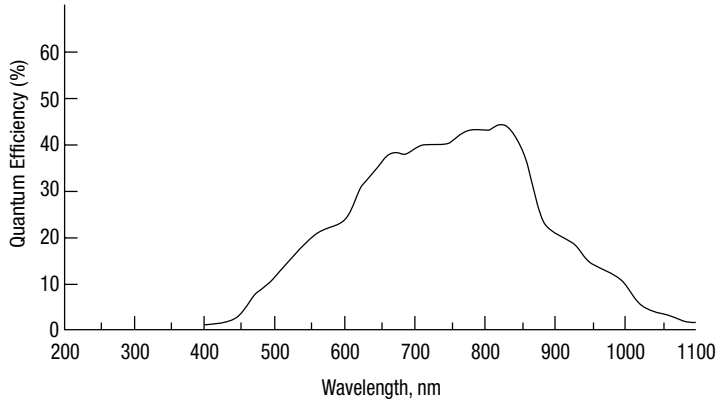
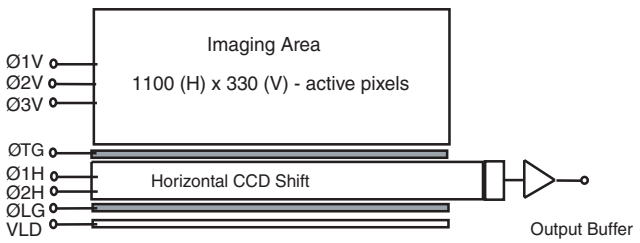


Figure 3. Functional Diagram



Summing Mode

At the end of the horizontal register, there is an ouput summing well which can be clocked to allow multiple-pixel summation of the scene. This summing well is located after the 19 extra stages of the horizontal register and prior to the DC biased gate (VOG) as shown in Figure 5. The summing gate (ØSG) can be clocked with one of the horizontal clock phases or with its own clock generator (see Figure 4a for summing gate timing). For example, two parallel lines of charge are additively transferred into the serial register, then the summing gate is pulsed low after the charge from two serial pixels has been transferred into the summing well. Thus, the resulting signal represents the sum of charges in four (2x2) contiguous pixels from the imaging region. It effectively reduces the 1100 x 330 device to a 550 x 165 array and increases the pixel size by four times. Other variations of this technique can be useful for low-light level situations, i.e., scenes with low contrast or a low signal-to-noise ratio. There is, of course, a loss in resolution that accompanies the gain in effective pixel size.

Output Amplifier

There is an on-chip amplifier that is located at the end of the extended shift register. The amplifier is a two stage buried channel transistor amplifier as shown in Figure 5. It is designed to operate with data rates in excess of 10 MHz. It has a bandwidth of approximately 60 MHz with a 10 pF load.

Temperature Monitoring

The RA1133J device has a temperature sensor integrated into the package for monitoring array temperature.

Timing Requirements

The timing recommended to run the RA1133J imager in the low speed and low noise mode of operation is shown in Figures 4A, 4B, and 4C. A 50% duty cycyle, two phase clock will drive the horizontal register to its highest speed. Figure 4a shows the timing of the horizontal two phase clocks, summing well clock and reset clock. To achieve high charge transfer, serial clocks must cross between 10% and 90% of the peak voltage. In addition, the rise and fall times of the two phase clocks need to be more than 50 ns in order to prevent the injection of spurious charge into the CCD channel.

Figure 4C. Horizontal CCD Shift Register Timing

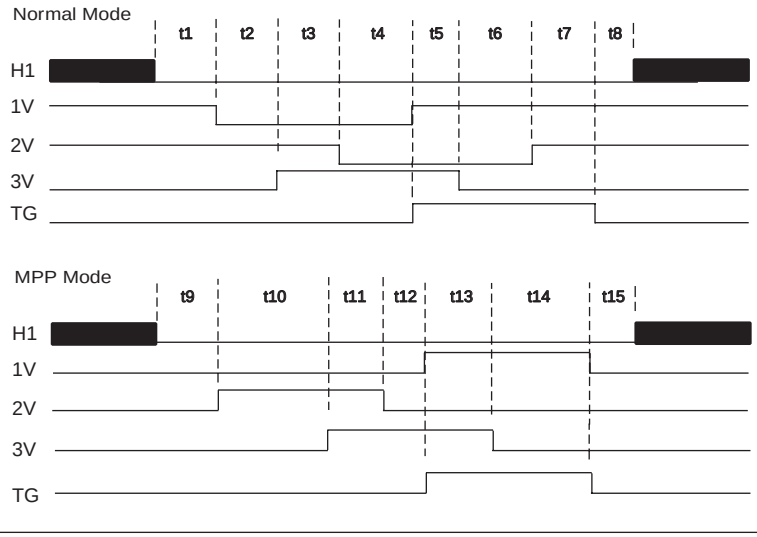
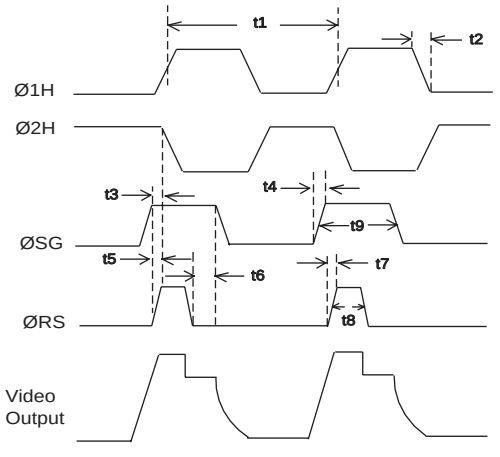


Table 2. Vertical Timing Diagram Characteristics

Item	Sym	Min	Typ	Max	Units
FE H1 to FE 1V	t1		2.6		µs
FE 1V to RE 3V	t2		2.6		µs
RE 3V to FE 2V	t3		2.6		µs
FE 2V to RE 1V	t4		5.2		µs
RE 1V to FE 3V	t5		1.4		µs
FE 3V to RE 2V	t6		1.4		µs
RE 2V to FE TG	t7		4.6		µs
FE TG to RE H1	t8		2.6		µs
FE H1 to RE 2V	t9		2.6		µs
RE 2V to RE 3V	t10		5.2		µs
RE 3V to FE 2V	t11		2.6		µs
FE 2V to RE 1V	t12		2.6		µs
RE 1V to FE 3V	t13		2.8		µs
FE 3V to FE TG	t14		4.6		µs
FE TG to RE H1	t14		2.6		µs

Figure 4a. Horizontal CCD Shift Register Timing



Timing Requirements (cont.)

The timing shown in Figure 4a is repeated 1100 + 35 (or more) times to allow the readout of one complete line of the image.

Figure 4b shows the timing requirements for the vertical register. Overlapping of the vertical clocks are normally longer than 5 µs. Rise and fall times of all clocks need to be 3 µs or longer in order to prevent spurious charge into the CCD channel. All vertical clock transitions should occur when the horizontal clocks are held steady.

Timing for MPP and normal mode is shown. The difference between the two modes is that during integration, all clocks must be held low for MPP mode.

Array Cooling

Both the dark current and the noise performance of the array can be improved by cooling. The dark current will be reduced by 50% for approximately every 6 - 8 °C reduction in array temperature. Cooling can be achieved via the integrated thermoelectric cooler. The bias supplies TEC+ and TEC- electronically control this cooler. This is a two-stage cooler capable of reducing the temperature of the array 40° C from the ambient temperature. Additional cooling can be achieved by decreasing the ambient temperature or by cooling the heat sink on the TE cooler as shown in Figure 6 and Figure 7.

Region of Interest

Rapid access to regions of interest is facilitated by use of a lateral charge drain. The drain is constructed adjacent to the horizontal CCD (HCCD) shift register. Unwanted lines of data are quickly disposed without the requirement for horizontal transfer. In this manner, entire lines of image data can be disposed of by a single vertical shift sequence, with a time penalty of 20 µs. This is to be contrasted with the normal read sequence which includes both the vertical shift (20 µs), plus readout of the 1130 horizontal elements (2260 µs). As the unwanted lines are transferred from storage region into the HCCD, the horizontal phases are held high to maintain a surface potential which is more positive than the low state channel potential of the transfer gate. Similar to a lateral antiblooming drain, charge will spill preferentially into the rapid discharge drain. Due to the fixed potential barrier, the HCCD cannot be completely cleared of charge and thus one horizontal shift sequence is required before resumption of valid data read.

Table 1. Timing Diagram Characteristics

Item	Sym	Min	Typ	Max	Units
$Ø_{1,2H}$ rise/fall time	T1		50		ns
$Ø_{1,2H}$ clock period	T2			100	ns
$Ø_{SG}$ delay from $Ø_{H2}$ edge	T3	+0			ns
$Ø_{SG}$ rise/fall time	T4		50		ns
$Ø_{RG}$ delay from $Ø_{SG}$ edge	T5	+0			ns
$Ø_{SG}$ delay from $Ø_{RG}$ edge	T6	+0			ns
$Ø_{RG}$ rise/fall time	T7		50		ns
$Ø_{RG}$ pulse duration	T8	10			ns
$Ø_{SG}$ pulse duration	T9			100	ns

Figure 4b. Vertical CCD Shift Register Timing and Its Relationship to Horizontal Clocks in Normal and MPP Mode

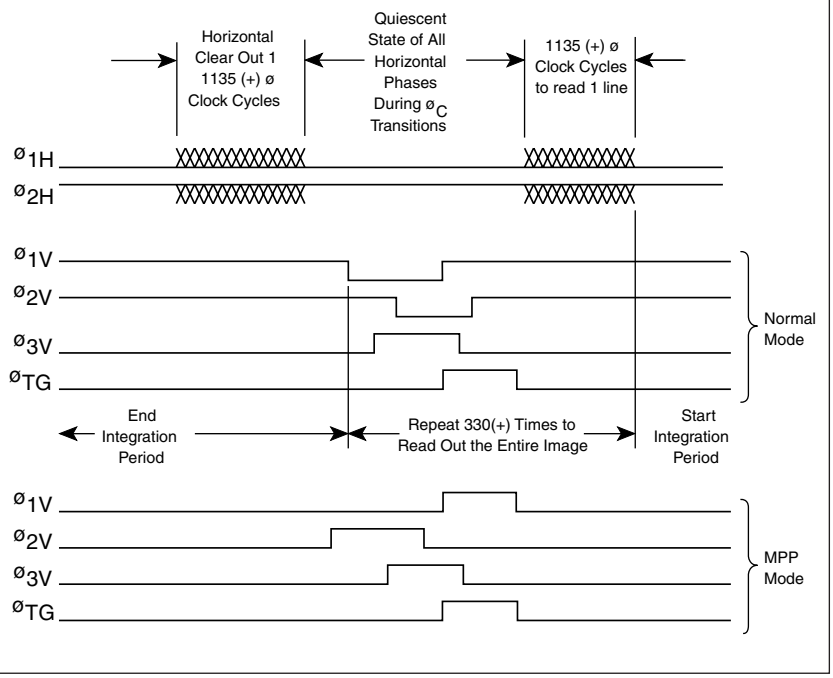


Figure 5. Output Structure

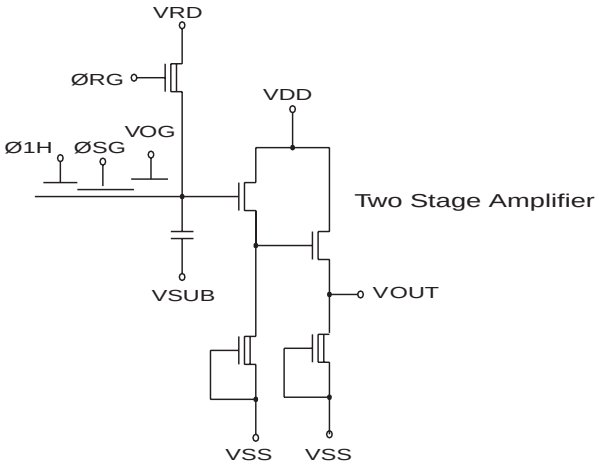


Figure 6. TEC Current vs. Chip Temperature (Ambient Temperature)

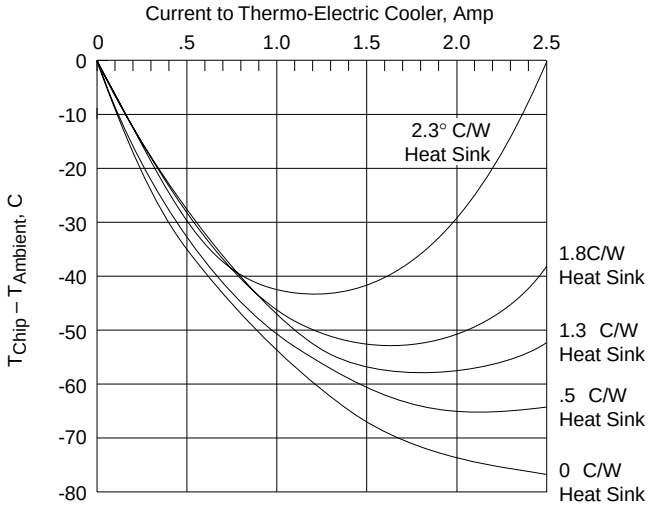


Figure 7. Heat Sink Temperature vs. Chip Temperature

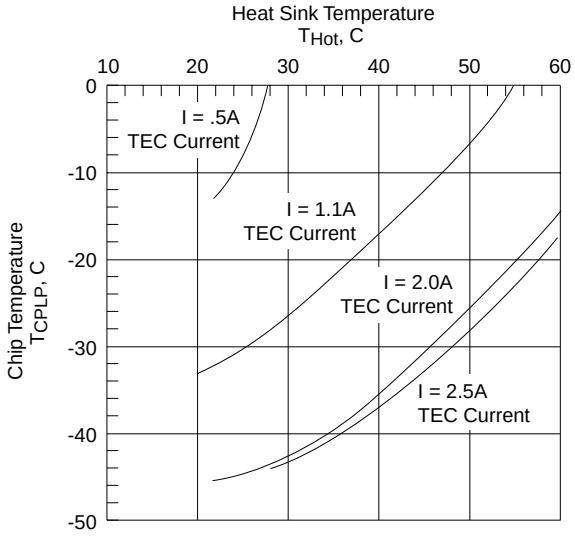


Figure 8. Package Dimensions

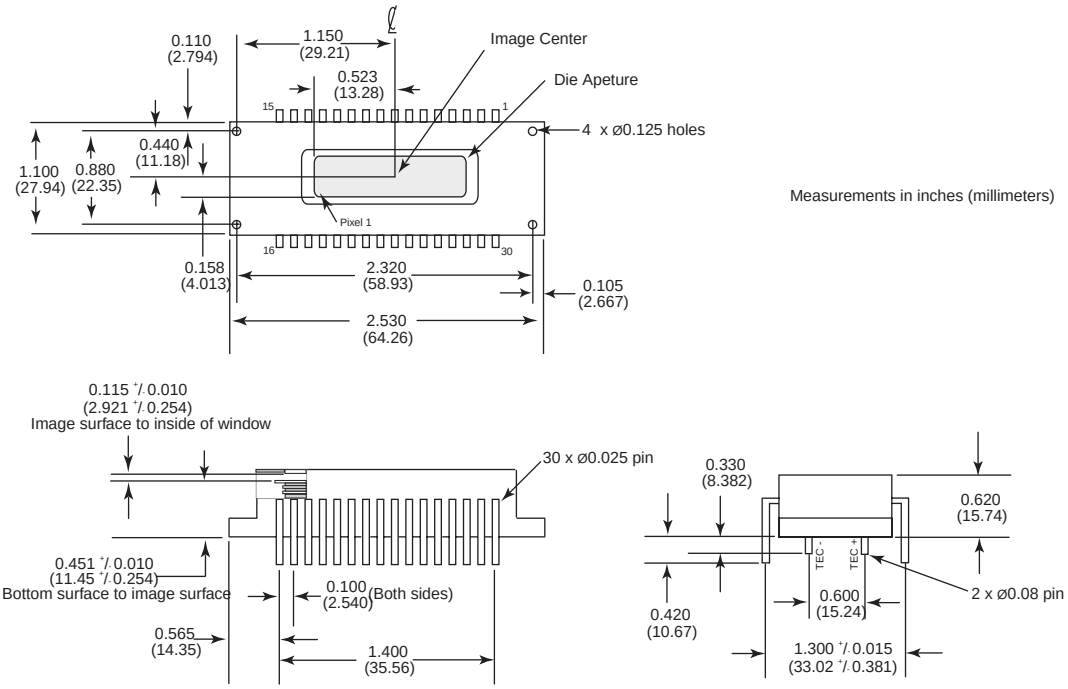


Table 3. Absolute Maximum Ratings

	Min	Max
Storage Temperature	- 55C	+ 85C
Operating Temperature	- 55C	+ 85C

Table 4. Typical Device Specifications

Parameter	Sym	Min	Typ	Max	Units
Format			1100 x 330		
Pixel Size			24 x 24		µm
Imaging Area			26.4 x 7.92		mm
Dynamic Range [1]	DR		25,000:1		
Full Well Charge [2]	Q_{SAT}	250	300		Ke-
Saturation Voltage	V_{SAT}	1000	1200		mV
Dark Current MPP [3]	DL		1	3	pA/cm2
Photo Response Non Uniformity	PRNU		5	10	±%
Dark Signal Uniformity	DSNU		2	5	±%
Charge Transfer Efficiency	CTE	0.9999	0.99995		
Output Amplifier Gain			4		µV/e-
Operating Frequency	fclock			15	MHz
Read Noise [4]			10		e-

Notes:

1. Full well/read noise, MPP mode
2. RLoad = 5.1 kOhms, MPP mode
3. MPP mode at -15 ℃
4. Measured at 500 kHz at -15 ℃

Table 5. Recommended Operating Conditions

Pin #	Signal	Function		Typ	Tolerance
24, 25	Ø1H, Ø2H	Horizontal Clocks	High Low	5 0	±5%
3, 29	ØTG	Transfer Gate Clock	High Low	4 -8	±10%
15	ØSG	Summing Gate Clock	High Low	5 0	±5%
1, 12	Ø1V (MPP)	Vertical Clock (MPP Phase)	High Low	4 -9	±5%
2, 11, 13, 30	Ø2V, Ø3V	Vertical Clocks	High Low	2 -11	±5%
5, 23	ØLG	Lateral Charge Gate	High Low	5 0	±5%
17	ØRG	Reset Gate	High Low	8 0	±10%
16	VOG	Output Gate		3	±5%
22	VDD	Amplifier Voltage Supply		14	±5%
4, 20	VLD	Lateral Charge Drain		13	±5%
18	VRD	Amplifier Reset Drain		10	±5%
6, 26	LS	Light Shield		GND	±5%
19	VSS	Video Amplifier Source		GND	±5%
9, 27	VSUB	Substrate Bias		-2	±5%

Table 6. Pinout Descriptions

Pin #	Sym	Function	Pin #	Sym	Function
1	$Ø_{1V}$	Vertical Phase 1	16	V_{OG}	Output Gate
2	$Ø_{3V}$	Vertical Phase 3	17	$Ø_{RG}$	Reset Gate
3	$Ø_{TG2}$	Transfer Gate 2	18	V_{RD}	Reset Drain
4	V_{LD}	Lateral Charge Drain	19	V_{SS}	Video Amplifier Source
5	$Ø_{LG2}$	Lateral Charge Gate 2	20	V_{LD}	Lateral Charge Drain
6	LS	Light Shield	21	V_{OUT}	Video Output
7	TEMP+	Temp+	22	V_{DD}	Video Amplifier Drain
8	TEMP-	Temp-	23	$Ø_{LG1}$	Lateral Charge Gate 1
9	V_{SUB}	Substrate	24	$Ø_{2H}$	Horizontal Phase 2
10	$Ø_{TG2}$	Transfer Gate 2	25	$Ø_{1H}$	Horizontal Phase 1
11	$Ø_{3V}$	Vertical Phase 3	26	LS	Light Shield
12	$Ø_{1V}$	Vertical Phase 1	27	V_{SUB}	Substrate
13	$Ø_{2V}$	Vertical Phase 2	28	N/C	No Connection
14	$Ø_{TG1}$	Transfer Gate 1	29	$Ø_{TG1}$	Transfer Gate 1
15	$Ø_{SG}$	Summing Gate	30	$Ø_{2V}$	Vertical Phase 2

Ordering Information

While the information provided in this data sheet is intended to describe the form, fit and function for this product, PerkinElmer reserves the right to make changes without notice.

Table 7. Ordering Information

Part Number	RA1133JAS-912

For more information e-mail us at opto@perkinelmer.com or visit our web site at **www.perkinelmer.com/opto**. All values are nominal; specifications subject to change without notice.

Table 8. Sales Offices

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