

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4067 16-channel analog multiplexer/demultiplexer

Product specification
File under Integrated Circuits, IC06

September 1993

16-channel analog multiplexer/demultiplexer

74HC/HCT4067

FEATURES

- Low "ON" resistance:
80 Ω (typ.) at $V_{CC} = 4.5$ V
70 Ω (typ.) at $V_{CC} = 6.0$ V
60 Ω (typ.) at $V_{CC} = 9.0$ V
typical "break before make" built-in
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4067 are high-speed Si-gate CMOS devices and are pin compatible with the "4067" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4067 are 16-channel analog multiplexers/demultiplexers with four address inputs (S_0 to S_3), an active LOW enable input ($\bar{E}$), sixteen independent inputs/outputs (Y_0 to Y_{15}) and a common input/output (Z). The "4067" contains sixteen bidirectional analog switches, each with one side connected to an independent input/output (Y_0 to Y_{15}) and the other side connected to a common input/output (Z).

With $\bar{E}$ LOW, one of the sixteen switches is selected (low impedance ON-state) by S_0 to S_3 . All unselected switches are in the high impedance OFF-state. With $\bar{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_0 to S_3 .

The analog inputs/outputs (Y_0 to Y_{15} , and Z) can swing between V_{CC} as a positive limit and GND as a negative limit. V_{CC} to GND may not exceed 10 V.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PZL} / t _{PZH}	turn-on time E̅ to V _{OS} S _n to V _{OS}	C _L = 15 pF; R _L = 1 kΩ; V _{CC} = 5 V	26	32	ns
			29	33	ns
t _{PLZ} / t _{PHZ}	turn-off time E̅ to V _{OS} S _n to V _{OS}		27	26	ns
			29	30	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per switch	notes 1 and 2	29	29	pF
C _S	max. switch capacitance independent (Y) common (Z)		5	5	pF
			45	45	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \} \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$ = sum of outputs

C_L = output load capacitance in pF

C_S = max. switch capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5$ V

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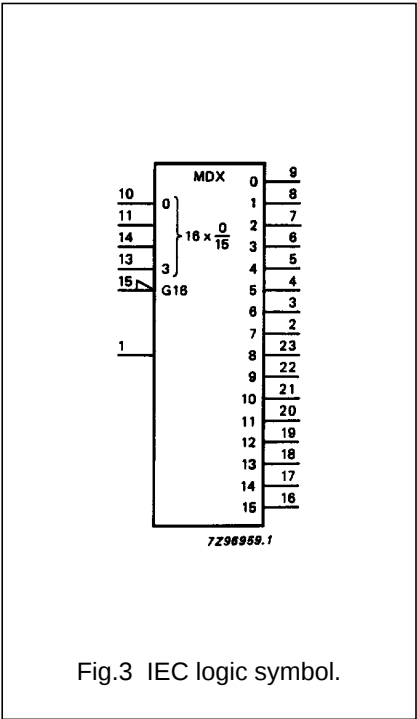
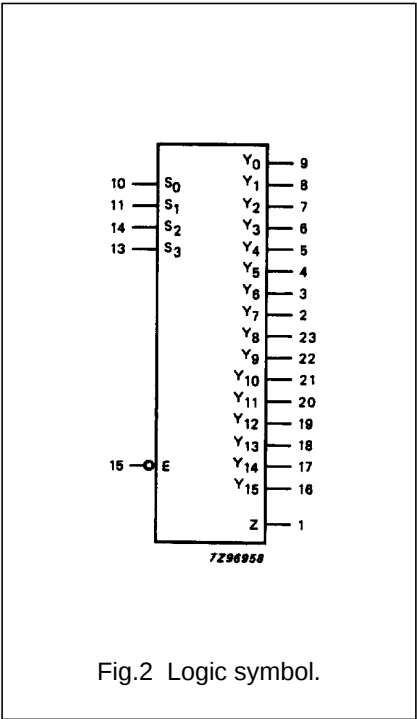
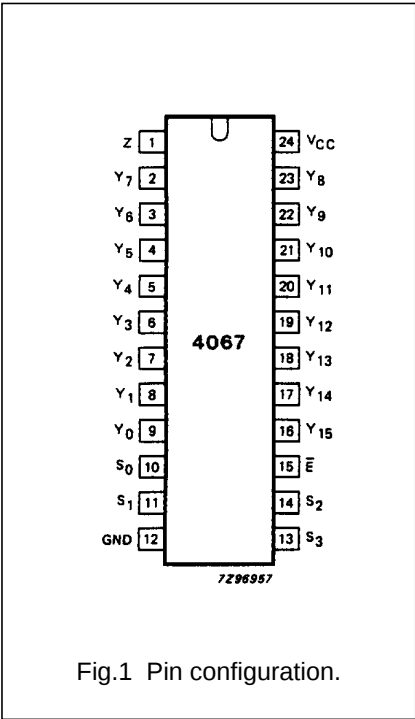
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ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	Z	common input/output
9, 8, 7, 6, 5, 4, 3, 2, 23, 22, 21, 20, 19, 18, 17, 16	Y ₀ to Y ₁₅	independent inputs/outputs
10, 11, 14, 13	S ₀ to S ₃	address inputs
12	GND	ground (0 V)
15	$\overline{E}$	enable input (active LOW)
24	V _{CC}	positive supply voltage

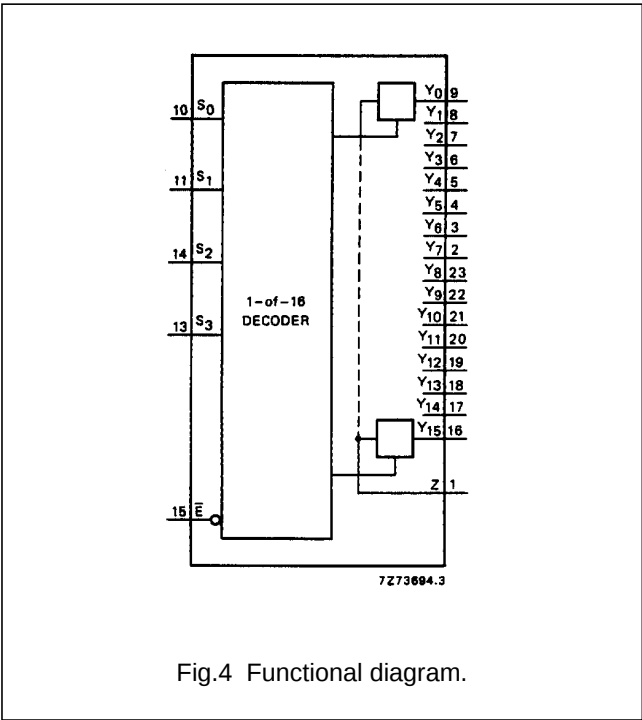


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APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

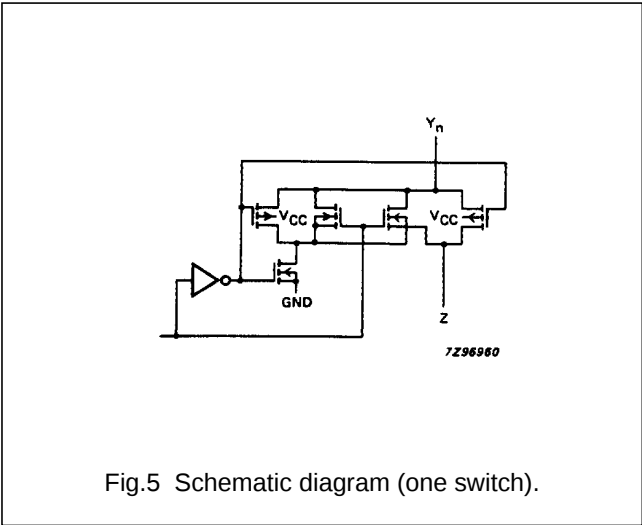


FUNCTION TABLE

INPUTS					CHANNEL ON
$\overline{E}$	S_3	S_2	S_1	S_0	
L	L	L	L	L	$Y_0 - Z$
L	L	L	L	H	$Y_1 - Z$
L	L	L	H	L	$Y_2 - Z$
L	L	L	H	H	$Y_3 - Z$
L	L	H	L	L	$Y_4 - Z$
L	L	H	L	H	$Y_5 - Z$
L	L	H	H	L	$Y_6 - Z$
L	L	H	H	H	$Y_7 - Z$
L	H	L	L	L	$Y_8 - Z$
L	H	L	L	H	$Y_9 - Z$
L	H	L	H	L	$Y_{10} - Z$
L	H	L	H	H	$Y_{11} - Z$
L	H	H	L	L	$Y_{12} - Z$
L	H	H	L	H	$Y_{13} - Z$
L	H	H	H	L	$Y_{14} - Z$
L	H	H	H	H	$Y_{15} - Z$
H	X	X	X	X	none

Notes

1. H = HIGH voltage level
L = LOW voltage level
X = don't care



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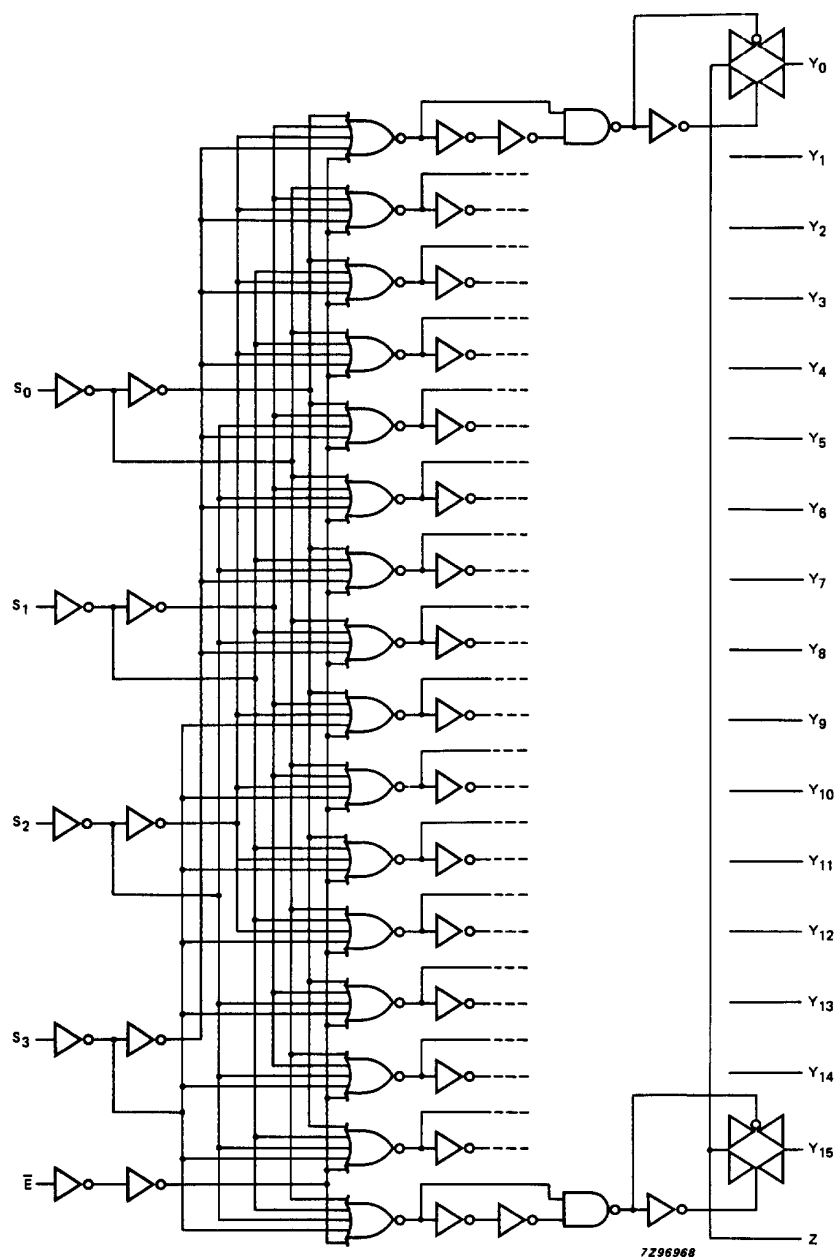


Fig.6 Logic diagram.

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{CC}; \pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	-65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note

1. To avoid drawing V_{CC} current out of terminal Z, when switch current flows in terminals Y_n , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no V_{CC} current will flow out of terminals Y_n . In this case there is no limit for the voltage drop across the switch, but the voltages at Y_n and Z may not exceed V_{CC} or GND.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	10.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	GND		V_{CC}	GND		V_{CC}	V	
T_{amb}	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTER- ISTICS
T_{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V $V_{CC} = 10.0$ V

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DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: $V_{CC} - GND = 2.0, 4.5, 6.0$ and 9.0 VFor 74HCT: $V_{CC} - GND = 4.5$ V

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS			
		74HC/HCT									V _{CC} (V)	I _S (μA)	V _{is}	V _I
		+25			−40 to +85		−40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
R _{ON}	ON-resistance (peak)		— 110 95 75	— 180 160 130		— 225 200 165		— 270 240 195	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	V _{CC} to GND	V _{IH} or V _{IL}	
R _{ON}	ON-resistance (rail)		150 90 80 70	— 160 140 120		— 200 175 150		— 240 210 180	Ω Ω Ω Ω	2.0 4.5 6.0 9.0	100 1000 1000 1000	GND or V _{CC}	V _{IH} or V _{IL}	
ΔR _{ON}	maximum variation of ON-resistance between any two channels		— 9 8 6						Ω Ω Ω Ω	2.0 4.5 6.0 9.0		V _{CC} to GND	V _{IH} or V _{IL}	

Notes

- At supply voltages ($V_{CC} - GND$) approaching 2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring R_{ON} see Fig.7.

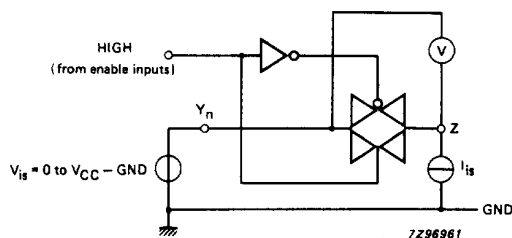
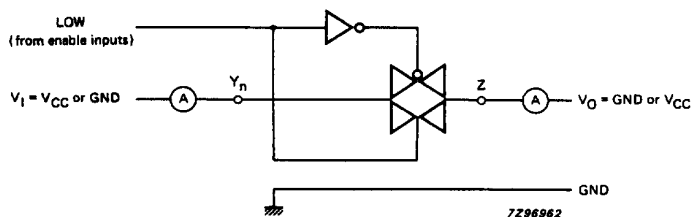
Fig.7 Test circuit for measuring ON-resistance (R_{ON}).

Fig.8 Test circuit for measuring OFF-state current.

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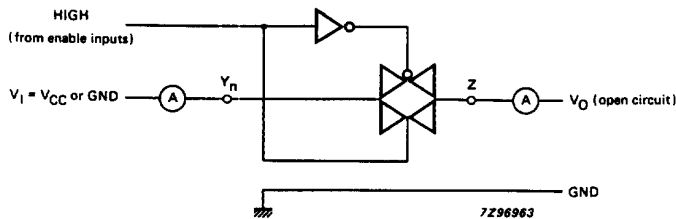


Fig.9 Test circuit for measuring ON-state current.

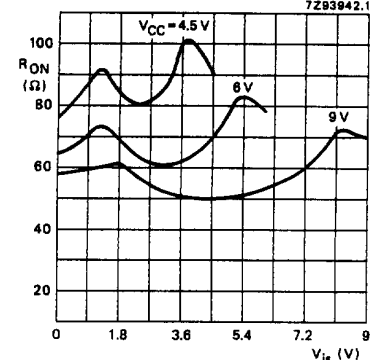


Fig.10 Typical ON-resistance (R_{ON}) as a function of input voltage (V_{IS}) for $V_{IS} = 0$ to $V_{CC} - GND$.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS		
		74HC									V _{CC} (V)	V _I	OTHER
		+25			−40 to +85		−40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V _{IH}	HIGH level input voltage	1.5	1.2		1.5		1.5		V	2.0			
		3.15	2.4		3.15		3.15			4.5			
		4.2	3.2		4.2		4.2			6.0			
		6.3	4.7		6.3		6.3			9.0			
V _{IL}	LOW level input voltage		0.8	0.50		0.50		0.50	V	2.0			
			2.1	1.35		1.35		1.35		4.5			
			2.8	1.80		1.80		1.80		6.0			
			4.3	2.70		2.70		2.70		9.0			
±I _I	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	μA	6.0 10.0	V _{CC} or GND		
±I _S	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	V _{IH} or V _{IL}	V _S = V _{CC} – GND (see Fig.8)	
±I _S	analog switch OFF-state current all channels			0.8		8.0		8.0	μA	10.0	V _{IH} or V _{IL}	V _S = V _{CC} – GND (see Fig.9)	
±I _S	analog switch ON-state current			0.8		8.0		8.0	μA	10.0	V _{IH} or V _{IL}	V _S = V _{CC} – GND (see Fig.9)	
I _{CC}	quiescent supply current			8.0 16.0		80.0 160		160 320	μA	6.0 10.0	V _{CC} or GND	V _{IS} = GND or V _{CC} ; V _{OS} = V _{CC} or GND	

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AC CHARACTERISTICS FOR 74HCGND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V _{CC} (V)	OTHER	
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay V _{is} to V _{os} ; Y _n to Z		25 9 7 5	75 15 13 9		95 19 16 11		110 22 19 14	ns	2.0 4.5 6.0 9.0	R _L = ∞; C _L = 50 pF (see Fig.16)	
t _{PHL} / t _{PLH}	propagation delay V _{is} to V _{os} ; Z to Y _n		18 6 5 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 9.0		
t _{PHZ} / t _{PLZ}	turn-off time E to Y _n		74 27 22 20	250 50 43 38		315 63 54 48		375 75 64 57	ns	2.0 4.5 6.0 9.0		R _L = 1 kΩ; C _L = 50 pF (see Fig.17)
t _{PHZ} / t _{PLZ}	turn-off time S _n to Y _n		83 30 24 21	250 50 43 38		315 63 54 48		375 75 64 57	ns	2.0 4.5 6.0 9.0		
t _{PHZ} / t _{PLZ}	turn-off time E̅ to Z		85 31 25 24	275 55 47 42		345 69 59 53		415 83 71 63	ns	2.0 4.5 6.0 9.0		
t _{PHZ} / t _{PLZ}	turn-off time S _n to Z		94 34 27 25	290 58 47 45		365 73 62 56		435 87 74 68	ns	2.0 4.5 6.0 9.0		
t _{PZH} / t _{PZL}	turn-on time E̅ to Y _n		80 29 23 17	275 55 47 42		345 69 59 53		415 83 71 63	ns	2.0 4.5 6.0 9.0		
t _{PZH} / t _{PZL}	turn-on time S _n to Y _n		88 32 26 18	300 60 51 45		375 75 64 56		450 90 77 68	ns	2.0 4.5 6.0 9.0		
t _{PZH} / t _{PZL}	turn-on time E̅ to Z		85 31 25 18	275 55 47 42		345 69 59 53		415 83 71 63	ns	2.0 4.5 6.0 9.0		
t _{PZH} / t _{PZL}	turn-on time S _n to Z		94 34 27 19	300 60 51 45		375 75 64 56		450 90 77 68	ns	2.0 4.5 6.0 9.0		

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Note to AC CHARACTERISTICS FOR 74HC

- Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCY								V _{CC} (V)	V _I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V _{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V _{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
±I _I	input leakage current			0.1		1.0		1.0	μA	5.5	V _{CC} or GND	
± I _S	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	5.5	V _{IH} or V _{IL}	V _S = V _{CC} – GND (see Fig.8)
±I _S	analog switch OFF-state current all channels			0.8		8.0		8.0	μA	5.5	V _{IH} or V _{IL}	V _S = V _{CC} – GND (see Fig.9)
±I _S	analog switch ON-state current			0.8		8.0		8.0	μA	5.5	V _{IH} or V _{IL}	V _S = V _{CC} – GND (see Fig.9)
I _{CC}	quiescent supply current			8.0		80.0		160	μA	4.5 to 5.5	V _{CC} or GND	V _{is} = GND or V _{CC} ; V _{os} = V _{CC} or GND
ΔI _{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V _{CC} –2.1 V	other inputs at V _{CC} or GND

Note

- The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\bar{E}$	0.6
S_n	0.5

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AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay V _{is} to V _{os} ; Y _n to Z		9	15		19		22	ns	4.5	R _L = ∞; C _L = 50 pF (see Fig.16)
t _{PHL} / t _{PLH}	propagation delay V _{is} to V _{os} ; Z to Y _n		6	12		15		18	ns	4.5	
t _{PHZ} / t _{PLZ}	turn-off time E̅ to Y _n		26	55		69		83	ns	4.5	R _L = 1 kΩ; C _L = 50 pF (see Fig.17)
t _{PHZ} / t _{PLZ}	turn-off time S _n to Y _n		31	55		69		83	ns	4.5	
t _{PHZ} / t _{PLZ}	turn-off time E̅ to Z		30	60		75		90	ns	4.5	
t _{PHZ} / t _{PLZ}	turn-off time S _n to Z		35	60		75		90	ns	4.5	
t _{PZH} / t _{PZL}	turn-on time E̅ to Y _n		32	60		75		90	ns	4.5	
t _{PZH} / t _{PZL}	turn-on time S _n to Y _n		35	60		75		90	ns	4.5	
t _{PZH} / t _{PZL}	turn-on time E̅ to Z		38	65		81		98	ns	4.5	
t _{PZH} / t _{PZL}	turn-on time S _n to Z		38	65		81		98	ns	4.5	

Note

- Due to higher Z terminal capacitance (16 switches versus 1) the delay figures to the Z terminal are higher than those to the Y terminal.

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ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; $t_r = t_f = 6$ ns

SYMBOL	PARAMETER	TYP.	UNIT	V _{CC} (V)	V _{is(p-p)} (V)	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	4.5 9.0	4.0 8.0	R _L = 10 k Ω ; C _L = 50 pF (see Fig.14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	4.5 9.0	4.0 8.0	R _L = 10 k Ω ; C _L = 50 pF (see Fig.14)
	switch "OFF" signal feed-through	-50 -50	dB dB	4.5 9.0	note 3	R _L = 600 Ω ; C _L = 50 pF f = 1 MHz (see Figs 11 and 15)
f _{max}	minimum frequency response (-3 dB)	90 100	MHz MHz	4.5 9.0	note 4	R _L = 50 Ω ; C _L = 10 pF (see Figs 12 and 13)
C _S	maximum switch capacitance independent (Y) common (Z)	5 45	pF pF			

Notes

1. V_{is} is the input voltage at Y_n or Z terminal, whichever is assigned as an input.
2. V_{os} is the output voltage at Y_n or Z terminal, whichever is assigned as an output.
3. Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
4. Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

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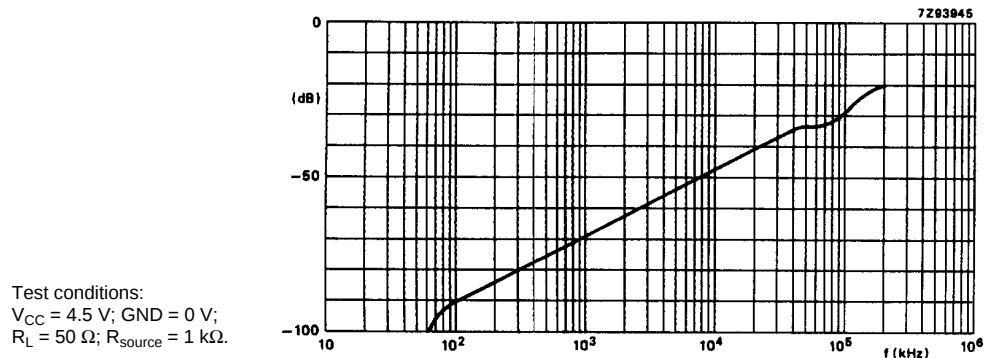


Fig.11 Typical switch "OFF" signal feed-through as a function of frequency.

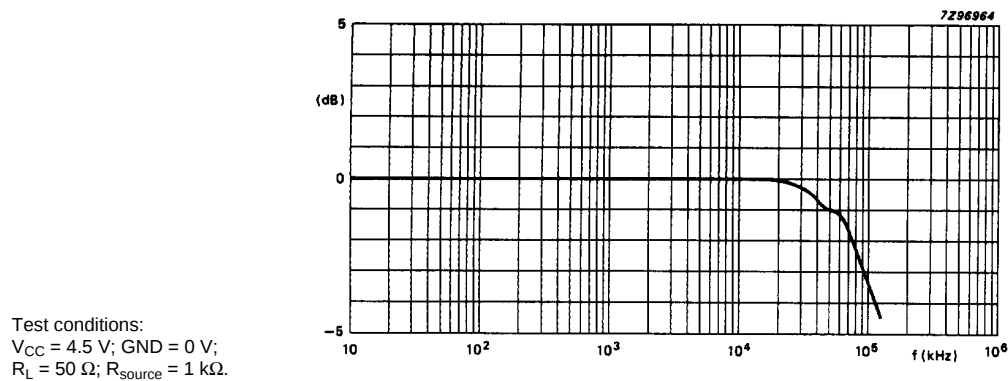


Fig.12 Typical frequency response.

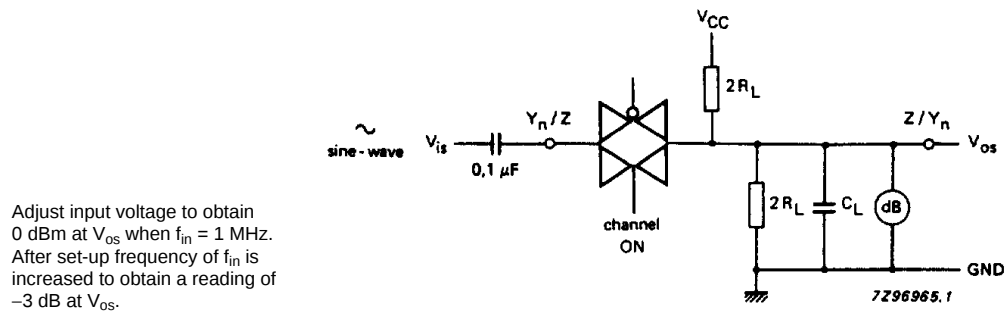


Fig.13 Test circuit for measuring minimum frequency response.

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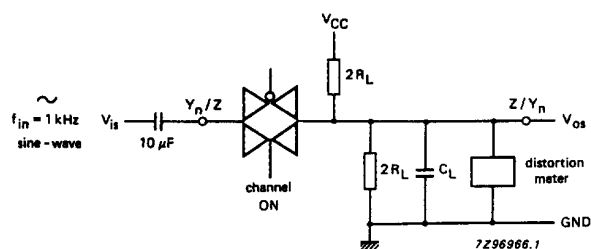


Fig.14 Test circuit for measuring sine-wave distortion.

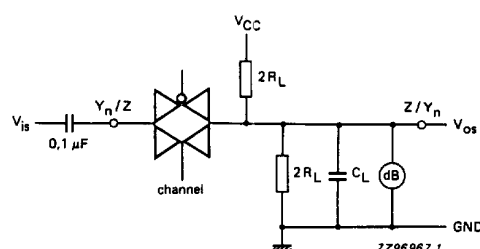


Fig.15 Test circuit for measuring switch "OFF" signal feed-through.

AC WAVEFORMS

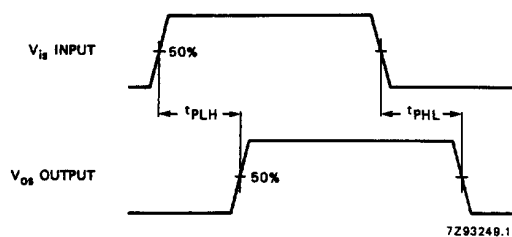
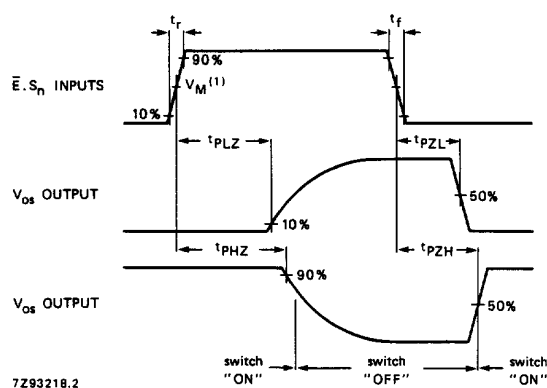


Fig.16 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.



- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT : $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.17 Waveforms showing the turn-on and turn-off times.

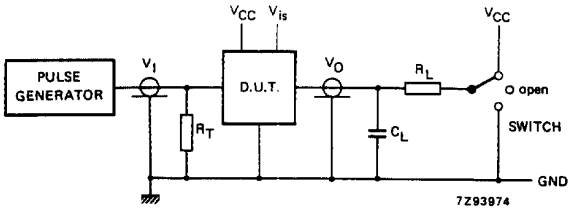
16-channel analog
multiplexer/demultiplexer

74HC/HCT4067

TEST CIRCUIT AND WAVEFORMS

Conditions

TEST	SWITCH	V _{is}
t _{PZH}	GND	V _{CC}
t _{PZL}	V _{CC}	GND
t _{PHZ}	GND	V _{CC}
t _{PLZ}	V _{CC}	GND
others	open	pulse



- C_L

=

load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
- R_T

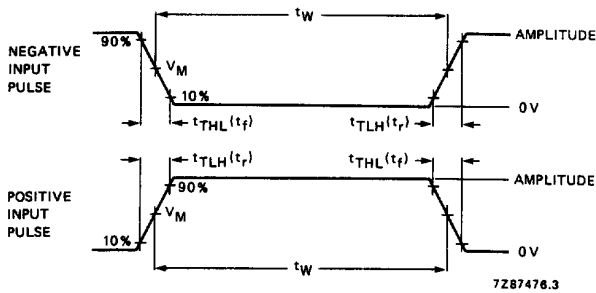
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termination resistance should be equal to the output impedance Z_O of the pulse generator.
- t_r

=

t_f = 6 ns, when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

Fig.18 Test circuit for measuring AC performance.



FAMILY	AMPLI-TUDE	V _M	t _r , t _f	
			f _{max} ; PULSE WIDTH	OTHER
74HC	V _{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Fig.19 Input pulse definitions.

PACKAGE OUTLINES

See *“74HC/HCT/HCU/HCMOS Logic Package Outlines”*.