

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT573

Octal D-type transparent latch;  
3-state

Product specification  
File under Integrated Circuits, IC06

December 1990

## Octal D-type transparent latch; 3-state

## 74HC/HCT573

## FEATURES

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors/microcomputers
- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the "563" and "373"
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT573 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT573 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications.

A latch enable (LE) input and an output enable ( $\overline{OE}$ ) input are common to all latches.

The "573" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at

the D<sub>n</sub> inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When  $\overline{OE}$  is LOW, the contents of the 8 latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches.

The "573" is functionally identical to the "563" and "373", but the "563" has inverted outputs and the "373" has a different pin arrangement.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

| SYMBOL                              | PARAMETER                               | CONDITIONS                                    | TYPICAL |     | UNIT |
|-------------------------------------|-----------------------------------------|-----------------------------------------------|---------|-----|------|
|                                     |                                         |                                               | HC      | HCT |      |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay                       | C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V |         |     |      |
|                                     | D <sub>n</sub> to Q <sub>n</sub>        |                                               | 14      | 17  | ns   |
|                                     | LE to Q <sub>n</sub>                    |                                               | 15      | 15  | ns   |
| C <sub>I</sub>                      | input capacitance                       |                                               | 3.5     | 3.5 | pF   |
| C <sub>PD</sub>                     | power dissipation capacitance per latch | notes 1 and 2                                 | 26      | 26  | pF   |

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF; V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>; for HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

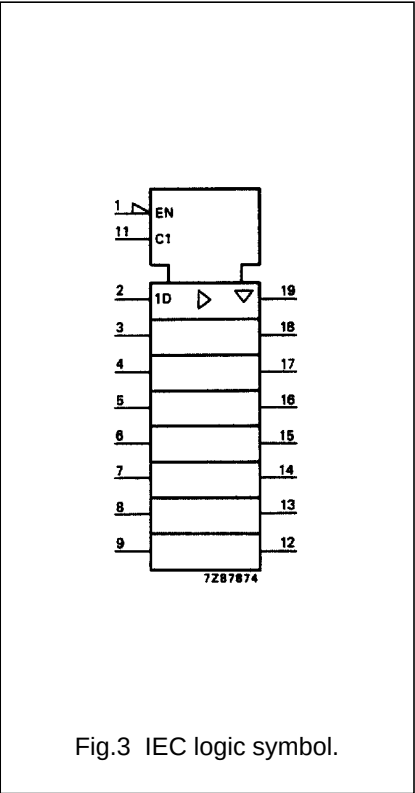
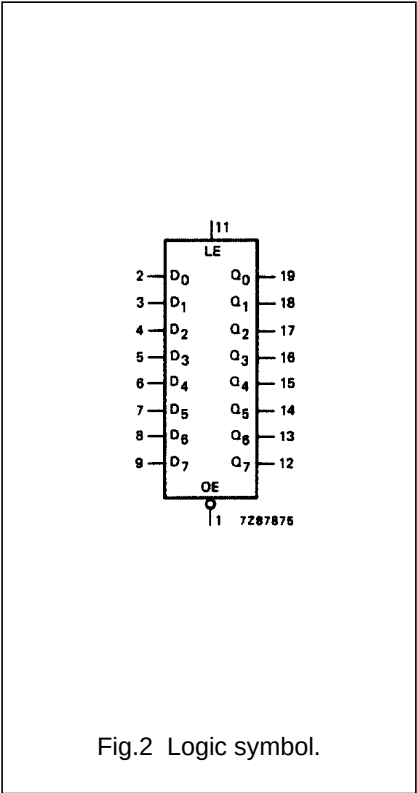
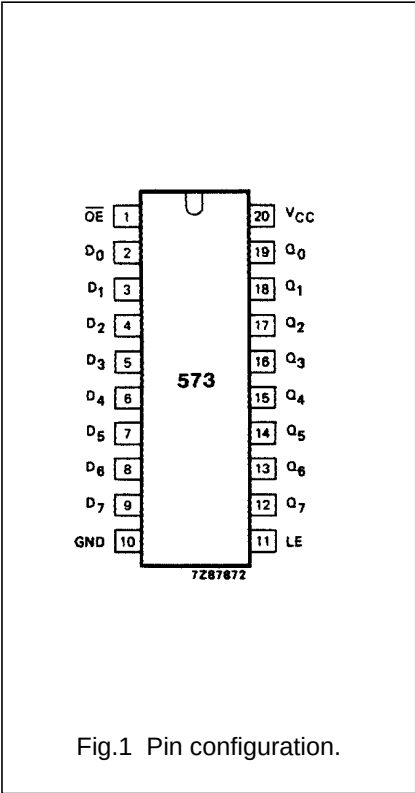
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Octal D-type transparent latch; 3-state

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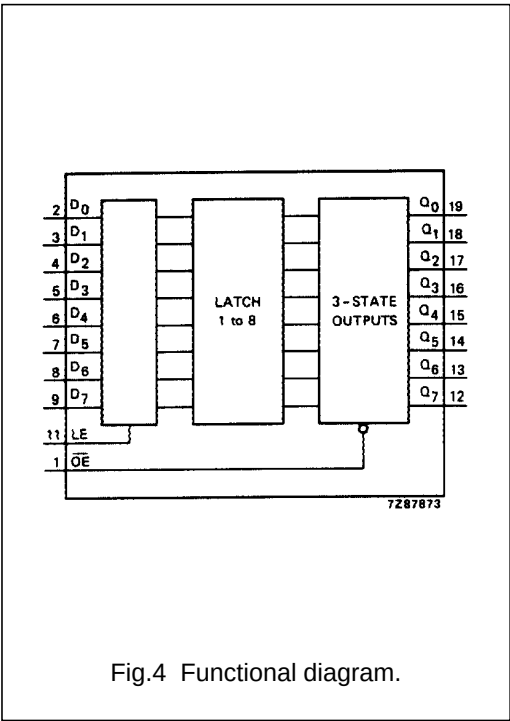
PIN DESCRIPTION

| PIN NO.                        | SYMBOL                           | NAME AND FUNCTION                        |
|--------------------------------|----------------------------------|------------------------------------------|
| 2, 3, 4, 5, 6, 7, 8, 9         | D <sub>0</sub> to D <sub>7</sub> | data inputs                              |
| 11                             | LE                               | latch enable input (active HIGH)         |
| 1                              | $\overline{\text{OE}}$           | 3-state output enable input (active LOW) |
| 10                             | GND                              | ground (0 V)                             |
| 19, 18, 17, 16, 15, 14, 13, 12 | Q <sub>0</sub> to Q <sub>7</sub> | 3-state latch outputs                    |
| 20                             | V <sub>CC</sub>                  | positive supply voltage                  |



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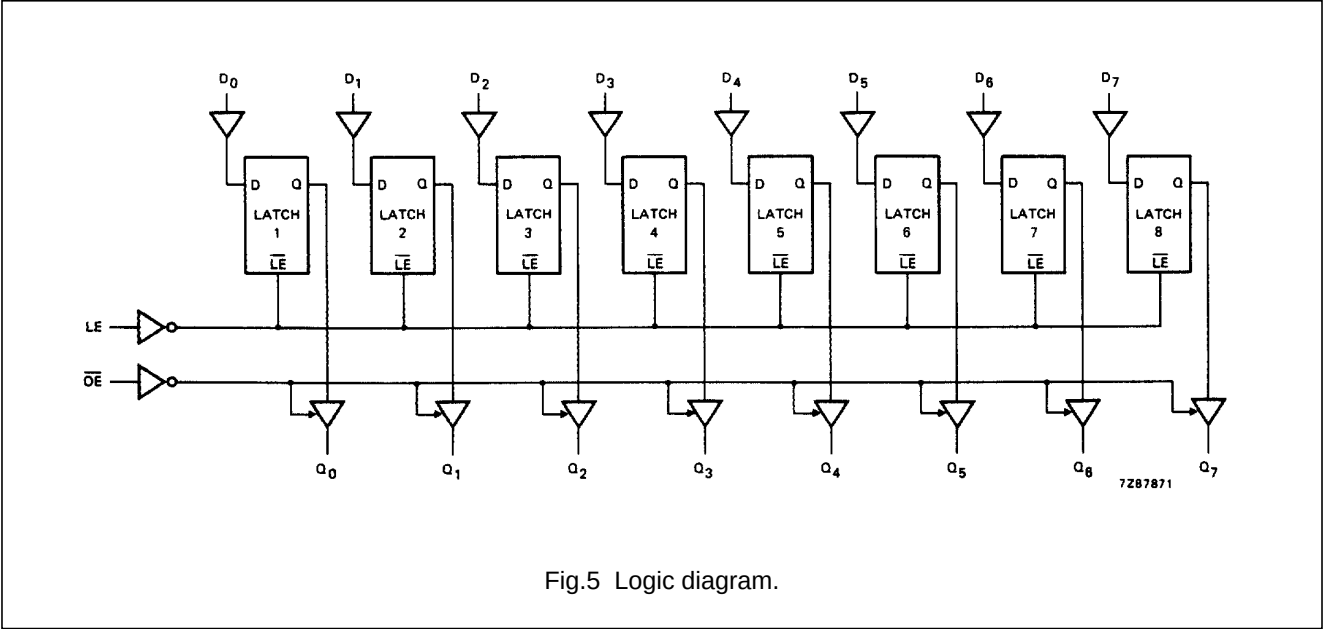


FUNCTION TABLE

| OPERATING MODES                             | INPUTS |    |    | INTERNAL LATCHES | OUTPUTS                          |
|---------------------------------------------|--------|----|----|------------------|----------------------------------|
|                                             | OE     | LE | DN |                  | Q <sub>0</sub> to Q <sub>7</sub> |
| enable and read register (transparent mode) | L      | H  | L  | L                | L                                |
|                                             | L      | H  | H  | H                | H                                |
| latch and read register                     | L      | L  | L  | L                | L                                |
|                                             | L      | L  | h  | H                | H                                |
| latch register and disable outputs          | H      | L  | L  | L                | Z                                |
|                                             | H      | L  | h  | H                | Z                                |

Notes

- 1. H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
- L = LOW voltage level
- l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
- Z = high impedance OFF-state



## Octal D-type transparent latch; 3-state

## 74HC/HCT573

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                                        | T <sub>amb</sub> (°C) |                |                 |                 |                 |                 |                 | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|------------------------------------------------------------------|-----------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|-----------|
|                                     |                                                                  | 74HC                  |                |                 |                 |                 |                 |                 |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                                  | +25                   |                |                 | −40 to +85      |                 | −40 to +125     |                 |      |                        |           |
|                                     |                                                                  | min.                  | typ.           | max.            | min.            | max.            | min.            | max.            |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>D <sub>n</sub> to Q <sub>n</sub>            |                       | 47<br>17<br>14 | 150<br>30<br>26 |                 | 190<br>38<br>33 |                 | 225<br>45<br>38 | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>LE to Q <sub>n</sub>                        |                       | 50<br>18<br>14 | 150<br>30<br>26 |                 | 190<br>38<br>33 |                 | 225<br>45<br>38 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable<br>time OE to Q <sub>n</sub>               |                       | 44<br>16<br>13 | 140<br>28<br>24 |                 | 175<br>35<br>30 |                 | 210<br>42<br>36 | ns   | 2.0<br>4.5<br>6.0      | Fig.8     |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable<br>time $\overline{OE}$ to Q <sub>n</sub> |                       | 55<br>20<br>16 | 150<br>30<br>26 |                 | 190<br>38<br>33 |                 | 225<br>45<br>38 | ns   | 2.0<br>4.5<br>6.0      | Fig.8     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                           |                       | 14<br>5<br>4   | 60<br>12<br>10  |                 | 75<br>15<br>13  |                 | 90<br>18<br>15  | ns   | 2.0<br>4.5<br>6.0      | Fig.6     |
| t <sub>w</sub>                      | enable pulse width<br>HIGH                                       | 80<br>16<br>14        | 14<br>5<br>4   |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>su</sub>                     | set-up time<br>D <sub>n</sub> to LE                              | 50<br>10<br>9         | 11<br>4<br>3   |                 | 65<br>13<br>11  |                 | 75<br>15<br>13  |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.9     |
| t <sub>h</sub>                      | hold time<br>D <sub>n</sub> to LE                                | 5<br>5<br>5           | 3<br>1<br>1    |                 | 5<br>5<br>5     |                 | 5<br>5<br>5     |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.9     |

## Octal D-type transparent latch; 3-state

## 74HC/HCT573

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT           | UNIT LOAD COEFFICIENT |
|-----------------|-----------------------|
| D <sub>n</sub>  | 0.35                  |
| LE              | 0.65                  |
| $\overline{OE}$ | 1.25                  |

**AC CHARACTERISTICS FOR 74HCT**

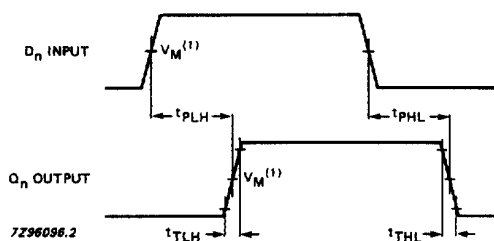
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                              | T <sub>amb</sub> (°C) |      |      |            |      |             |      | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|--------------------------------------------------------|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------|
|                                     |                                                        | 74HCT                 |      |      |            |      |             |      |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                        | +25                   |      |      | −40 to +85 |      | −40 to +125 |      |      |                        |           |
|                                     |                                                        | min.                  | typ. | max. | min.       | max. | min.        | max. |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>D <sub>n</sub> to Q <sub>n</sub>  |                       | 20   | 35   |            | 44   |             | 53   | ns   | 4.5                    | Fig.6     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>LE to Q <sub>n</sub>              |                       | 18   | 35   |            | 44   |             | 53   | ns   | 4.5                    | Fig.7     |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable<br>time<br>OE to Q <sub>n</sub>  |                       | 17   | 30   |            | 38   |             | 45   | ns   | 4.5                    | Fig.8     |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable<br>time<br>OE to Q <sub>n</sub> |                       | 18   | 30   |            | 38   |             | 45   | ns   | 4.5                    | Fig.8     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                 |                       | 5    | 12   |            | 15   |             | 18   | ns   | 4.5                    | Fig.6     |
| t <sub>W</sub>                      | enable pulse width<br>HIGH                             | 16                    | 5    |      | 20         |      | 24          |      | ns   | 4.5                    | Fig.7     |
| t <sub>su</sub>                     | set-up time<br>D <sub>n</sub> to LE                    | 13                    | 7    |      | 16         |      | 20          |      | ns   | 4.5                    | Fig.9     |
| t <sub>h</sub>                      | hold time<br>D <sub>n</sub> to LE                      | 9                     | 4    |      | 11         |      | 14          |      | ns   | 4.5                    | Fig.9     |

## Octal D-type transparent latch; 3-state

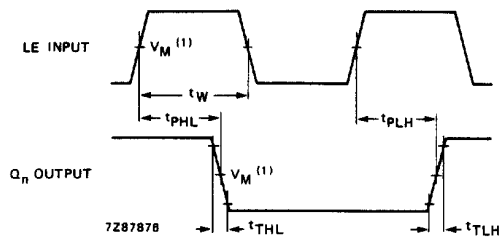
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## AC WAVEFORMS



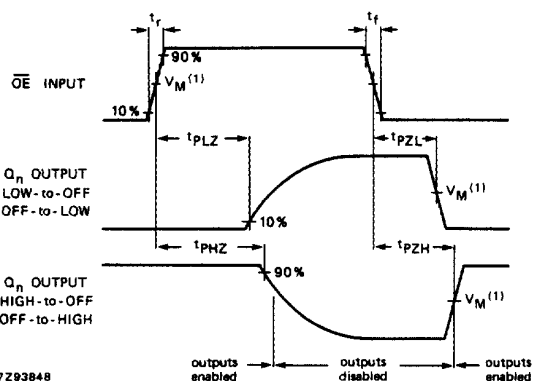
(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.6 Waveforms showing the data input ( $D_n$ ) to output ( $Q_n$ ) propagation delays and the output transition times.



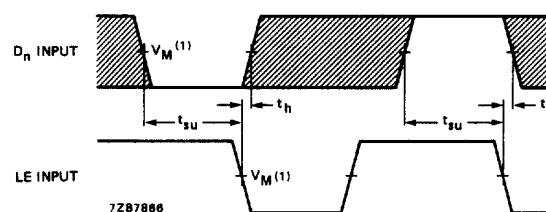
(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output ( $Q_n$ ) propagation delays and the output transition times.



(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.8 Waveforms showing the 3-state enable and disable times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.9 Waveforms showing the data set-up and hold times for  $D_n$  input to LE input.

## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".