

## 750kHz – 800MHz Low Phase Noise Multiplier VCXO

Universal Low Phase Noise IC's

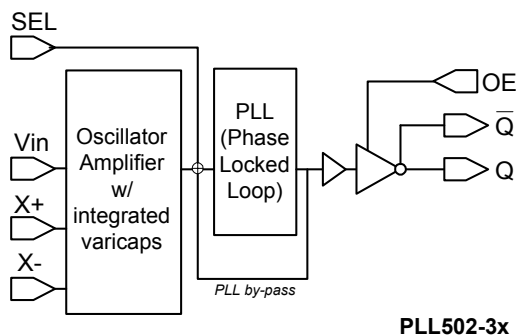
### FEATURES

- Selectable 750kHz to 800MHz range.
- Low phase noise output (@ 10kHz frequency offset, -142dBc/Hz for 19.44MHz, -125dBc/Hz for 155.52MHz, -115dBc/Hz for 622.08MHz).
- CMOS (PLL502-37), PECL (PLL502-35 and PLL502-38) or LVDS (PLL502-39) output.
- 12 to 25MHz crystal input.
- No external load capacitor or varicap required.
- Output Enable selector.
- Wide pull range (+/-200 ppm)
- Selectable 1/16 to 32x frequency multiplier.
- 3.3V operation.
- Available in 16-Pin (TSSOP or 3x3mm QFN).

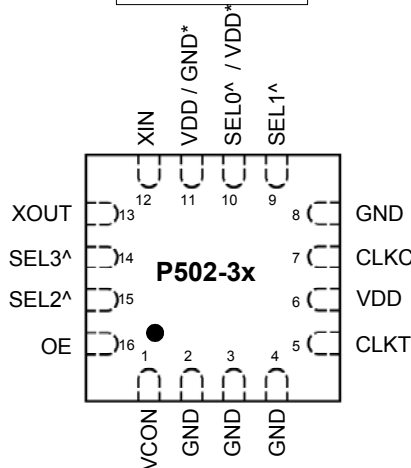
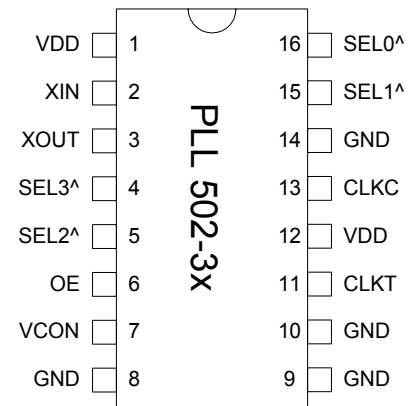
### DESCRIPTION

The PLL502-35 (PECL with inverted OE), PLL502-37 (CMOS), PLL502-38 (PECL), and PLL502-39 (LVDS) are high performance and low phase noise VCXO IC chips. They provide phase noise performance as low as -125dBc at 10kHz offset (at 155MHz), by multiplying the input crystal frequency up to 32x. The wide pull range (+/- 200 ppm) and very low jitter make them ideal for a wide range of applications, including SONET/SDH and FEC. They accept fundamental parallel resonant mode crystals from 12 to 25MHz.

### BLOCK DIAGRAM



### PIN CONFIGURATION (Top View)



<sup>^</sup>: Internal pull-up

\*: On 3x3 package, PLL502-35/-38 do not have SEL0 available: Pin 10 is VDD, pin 11 is GND. However, PLL502-37/-39 have SEL0 (pin 10), and pin11 is VDD. See pin assignment table for details.

### OUTPUT ENABLE LOGICAL LEVELS

Part #	OE	State
PLL502-38	0 (Default)	Output enabled
	1	Tri-state
PLL502-35 PLL502-37 PLL502-39	0	Tri-state
	1 (Default)	Output enabled

OE input: Logical states defined by PECL levels for PLL502-38  
Logical states defined by CMOS levels for PLL502-37/-39

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### FREQUENCY SELECTION TABLE

SEL3	SEL2	SEL1	SEL0	Selected Multiplier
0	0	1	1	Fin x 32
0	1	1	0	Fin / 8
0	1	1	1	Fin x 2
1	0	0	1	Fin / 2
1	0	1	0	Fin / 16
1	0	1	1	Fin x 4
1	1	0	0	Fin / 4
1	1	0	1	Fin x 8
1	1	1	0	Fin x 16
1	1	1	1	No multiplication

**Note:** SEL0 is not available (always "1") for PLL502-35 and PLL502-38 in 3x3mm package

### PIN DESCRIPTIONS PLL502-35 and PLL502-38 (see next page of PLL502-37/-39)

Name	TSSOP Pin number	3x3mm QFN Pin number	Type	Description
XIN	2	12	I	Crystal input. See Crystal Specification on page 4.
XOUT	3	13	I	Crystal output. See Crystal Specification on page 4.
OE	6	16	I	Output enable pin (see OE logic state table on page 1).
VCON	7	1	I	Voltage Control input.
GND	8,9,10,14	2,3,4,8,11	P	Ground.
CLKT	11	5	O	True output PECL
CLKC	13	7	O	Complementary output PECL.
SEL0	16	Not available	I	Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND.
SEL1	15	9	I	
SEL2	5	15	I	
SEL3	4	14	I	
VDD	1, 12	6,10	P	+3.3V power supply.

### PIN DESCRIPTIONS PLL502-37/-39 (see previous page of PLL502-35/-38)

Name	TSSOP Pin number	3x3mm QFN Pin number	Type	Description
XIN	2	12	I	Crystal input. See Crystal Specification on page 4.
XOUT	3	13	I	Crystal output. See Crystal Specification on page 4.
OE	6	16	I	Output enable pin (see OE logic state table on page 1).
VCON	7	1	I	Voltage Control input.
GND	8,9,10,14	2,3,4,8	P	Ground.
CLKT	11	5	O	True output LVDS (PLL502-39) (N/C for PLL502-37)
CLKC	13	7	O	Complementary output LVDS (PLL502-39) (CMOS out for PLL502-37).
SEL0	16	10	I	Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND.
SEL1	15	9	I	
SEL2	5	15	I	
SEL3	4	14	I	
VDD	1, 12	6,11	P	+3.3V power supply.

## ELECTRICAL SPECIFICATIONS

### 1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		4.6	V
Input Voltage, dc	$V_I$	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature*	$T_A$	-40	85	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

\* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

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### 2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	$F_{XIN}$	Parallel Fundamental Mode	12		25	MHz
Crystal Loading Rating	$C_{L(xtal)}$	At VCON = 1.65V		9.5		pF
Crystal Pullability	$C_0/C_1(xtal)$	AT cut			250	-
Recommended ESR	$R_E$	AT cut			30	$\Omega$

**Note:** Crystal Loading rating: 9.5pF is the loading the crystal sees from the VCXO chip at VCON = 1.65V. It is assumed that the crystal will be at nominal frequency at this load. If the crystal requires more load to be at nominal frequency, the additional load must be added externally. This however may reduce the pull range.

### 3. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		$F_{XIN} = 12 - 25\text{MHz};$ XTAL $C_0/C_1 < 250$ $0V \leq VCON \leq 3.3V$		500		ppm
CLK output pullability		VCON=1.65V, $\pm 1.65V$	$\pm 200$			ppm
VCXO Tuning Characteristic				150		ppm/V
Pull range linearity					10	%
VCON pin input impedance			2000			k $\Omega$
VCON modulation BW		$0V \leq VCON \leq 3.3V, -3\text{dB}$	25			kHz

**Note:** Parameters denoted with an asterisk (\*) represent nominal characterization data and are not production tested to any specific limits.

### 4. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Supply Current, Dynamic (with Loaded Outputs)	$I_{DD}$	PECL/LVDS/CMOS	$F_{out} < 24\text{MHz}$			60/28/15	mA
			$24\text{MHz} < F_{out} < 96\text{MHz}$			65/45/30	
			$96\text{MHz} < F_{out} < 800\text{MHz}$			100/80/40	
Operating Voltage	$V_{DD}$		2.97		3.63	V	
Output Clock Duty Cycle		@ 50% $V_{DD}$ (CMOS)	45	50	55	%	
		@ 1.25V (LVDS)	45	50	55		
		@ $V_{DD} - 1.3V$ (PECL)	45	50	55		
Short Circuit Current				$\pm 50$		mA	

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### 5. Jitter Specifications

PARAMETERS	CONDITIONS	FREQUENCY	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	19.44MHz		2.2		ps
		77.76MHz		4.5		
		155.52MHz		4.5		
		622.08MHz		5.0		
Period jitter Peak-to-Peak <sup>1</sup>	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	19.44MHz		17		ps
		77.76MHz		25		
		155.52MHz		27		
		622.08MHz		35		
Integrated jitter RMS <sup>2</sup>	Integrated 12 kHz to 20 MHz	155.52MHz		2.5	4	ps
		622.08MHz		2.5	4	

### 6. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier (typical)	19.44MHz	-80	-108	-132	-142	-150	dBc/Hz
	77.76MHz	-72	-103	-122	-130	-125	
	155.52MHz	-65	-95	-120	-125	-121	
	622.08MHz	-55	-85	-109	-115	-110	

Note: Phase Noise measured at VCON = 0V

### 7. CMOS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output drive current	I <sub>OH</sub>	V <sub>OH</sub> = V <sub>DD</sub> -0.4V, V <sub>DD</sub> =3.3V	10			mA
	I <sub>OL</sub>	V <sub>OL</sub> = 0.4V, V <sub>DD</sub> = 3.3V	10			mA
Output Clock Rise/Fall Time		0.3V ~ 3.0V with 15 pF load		2.4		ns

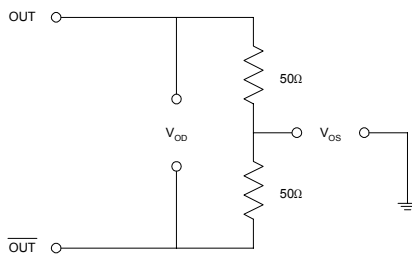
**8. LVDS Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	$V_{OD}$	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
$V_{DD}$ Magnitude Change	$\Delta V_{OD}$		-50		50	mV
Output High Voltage	$V_{OH}$			1.4	1.6	V
Output Low Voltage	$V_{OL}$		0.9	1.1		V
Offset Voltage	$V_{OS}$		1.125	1.2	1.375	V
Offset Magnitude Change	$\Delta V_{OS}$		0	3	25	mV
Power-off Leakage	$I_{OXD}$	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		$\pm 1$	$\pm 10$	$\mu A$
Output Short Circuit Current	$I_{OSD}$			-5.7	-8	mA

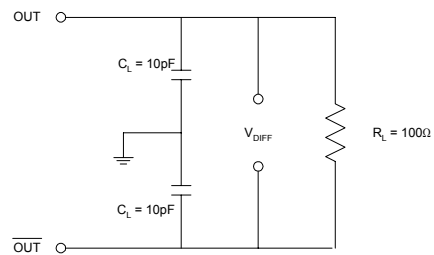
**9. LVDS Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	$t_r$	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	$t_f$		0.2	0.7	1.0	ns

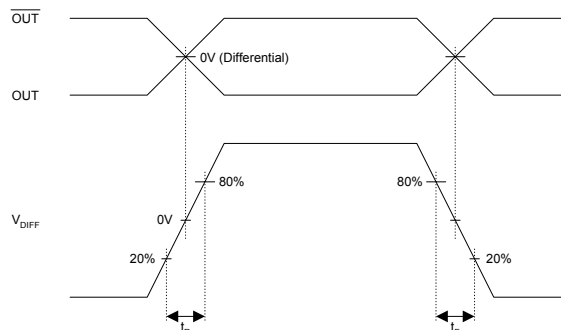
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



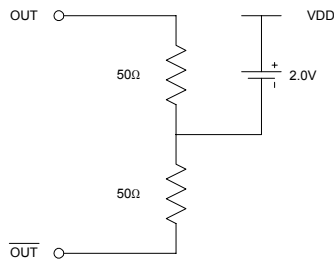
**10. PECL Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	$V_{OH}$	$R_L = 50 \Omega$ to $(V_{DD} - 2V)$ (see figure)	$V_{DD} - 1.025$		V
Output Low Voltage	$V_{OL}$			$V_{DD} - 1.620$	V

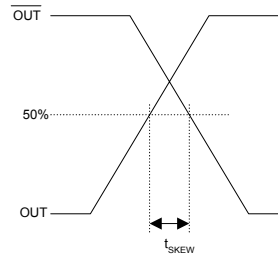
**11. PECL Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	$t_r$	20%~80% of Waveform		0.6	1.5	ns
Clock Fall Time	$t_f$	20%~80% of Waveform		0.6	1.5	ns

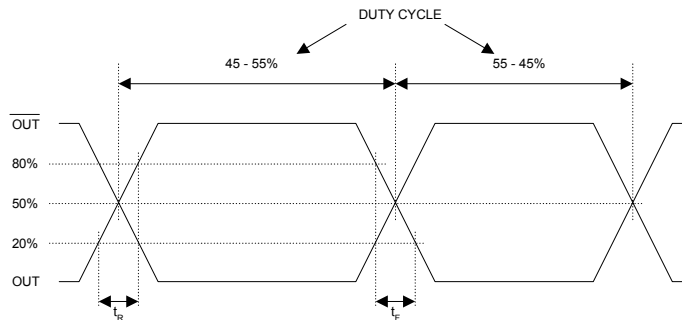
PECL Levels Test Circuit



PECL Output Skew



PECL Transition Time Waveform



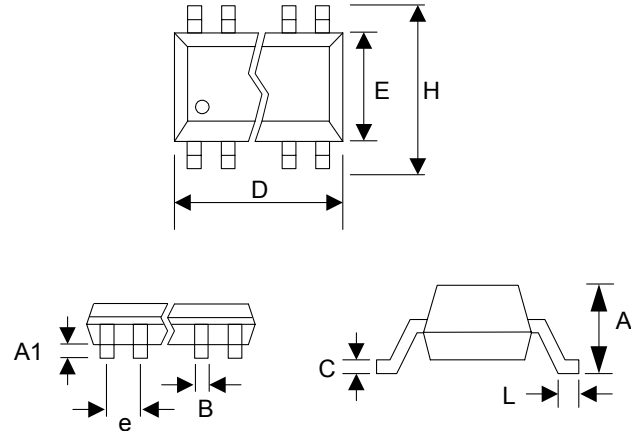
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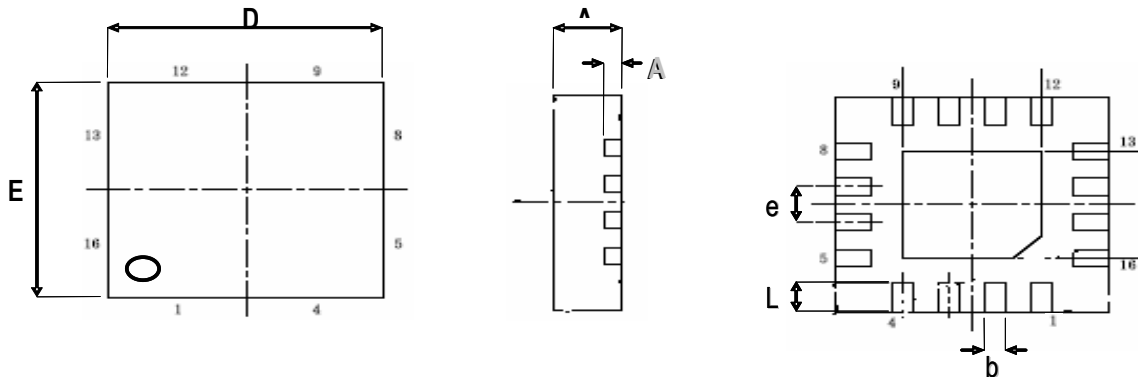
**PACKAGE INFORMATION**

**16 Pin TSSOP**

Dimensions in ( mm )		
Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



**16 Pin 3x3 QFN**



Symbol	Dimension in MM		Dimension in inch	
	Min.	Max.	Min.	Max.
A	0.70	0.80	0.028	0.032
A1	0.203 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020



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**ORDERING INFORMATION**

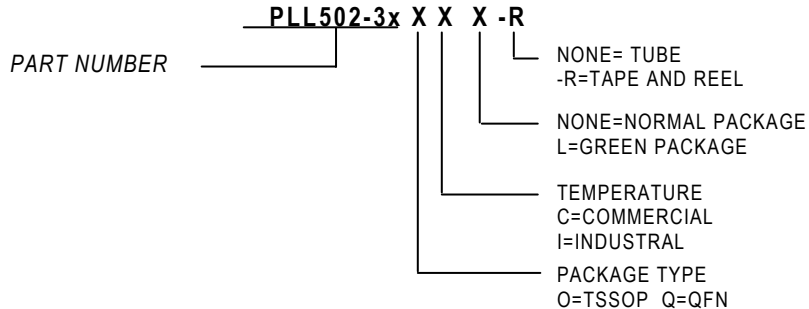
**For part ordering, please contact our Sales Department:**

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:  
Device number, Package type, Operating temperature range, shipping method



Order Number	Marking	Package Option
PLL502-35OC	P502-35OC	16-Pin TSSOP (Tube)
PLL502-35OC-R	P502-35OC	16-Pin TSSOP (Tape and Reel)
PLL502-35QC	P502-35QC	16-Pin 3x3 QFN (Tube)
PLL502-35QC-R	P502-35QC	16-Pin 3x3 QFN (Tape and Reel)
PLL502-35OCL	P502-35OCL	16-Pin TSSOP (Tube)
PLL502-35OCL-R	P502-35OCL	16-Pin TSSOP (Tape and Reel)
PLL502-35QCL	P502-35QCL	16-Pin 3x3 QFN (Tube)
PLL502-35QCL-R	P502-35QCL	16-Pin 3x3 QFN (Tape and Reel)
PLL502-37OC	P502-37OC	16-Pin TSSOP (Tube)
PLL502-37OC-R	P502-37OC	16-Pin TSSOP (Tape and Reel)
PLL502-37QC	P502-37QC	16-Pin 3x3 QFN (Tube)
PLL502-37QC-R	P502-37QC	16-Pin 3x3 QFN (Tape and Reel)
PLL502-37OCL	P502-37OCL	16-Pin TSSOP (Tube)
PLL502-37OCL-R	P502-37OCL	16-Pin TSSOP (Tape and Reel)
PLL502-37QCL	P502-37QCL	16-Pin 3x3 QFN (Tube)
PLL502-37QCL-R	P502-37QCL	16-Pin 3x3 QFN (Tape and Reel)
PLL502-38OC	P502-38OC	16-Pin TSSOP (Tube)
PLL502-38OC-R	P502-38OC	16-Pin TSSOP (Tape and Reel)
PLL502-38QC	P502-38QC	16-Pin 3x3 QFN (Tube)
PLL502-38QC-R	P502-38QC	16-Pin 3x3 QFN (Tape and Reel)
PLL502-38OCL	P502-38OCL	16-Pin TSSOP (Tube)
PLL502-38OCL-R	P502-38OCL	16-Pin TSSOP (Tape and Reel)
PLL502-38QCL	P502-38QCL	16-Pin 3x3 QFN (Tube)
PLL502-38QCL-R	P502-38QCL	16-Pin 3x3 QFN (Tape and Reel)
PLL502-39OC	P502-39OC	16-Pin TSSOP (Tube)
PLL502-39OC-R	P502-39OC	16-Pin TSSOP (Tape and Reel)
PLL502-39QC	P502-39QC	16-Pin 3x3 QFN (Tube)
PLL502-39QC-R	P502-39QC	16-Pin 3x3 QFN (Tape and Reel)
PLL502-39OCL	P502-39OCL	16-Pin TSSOP (Tube)
PLL502-39OCL-R	P502-39OCL	16-Pin TSSOP (Tape and Reel)
PLL502-39QCL	P502-39QCL	16-Pin 3x3 QFN (Tube)
PLL502-39QCL-R	P502-39QCL	16-Pin 3x3 QFN (Tape and Reel)

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