PLL502-39U

750kHz – 800MHz Low Phase Noise Multiplier VCXO

Universal Low Phase Noise IC's

FEATURES

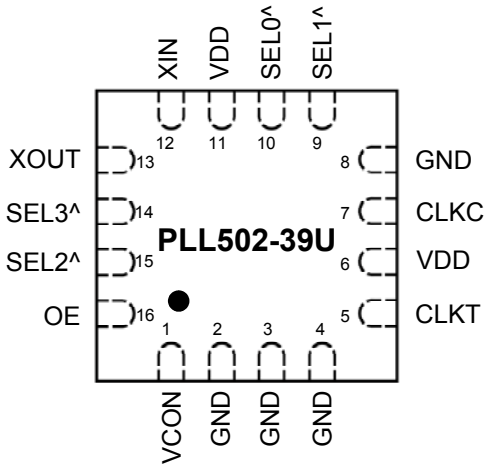
- Selectable 750kHz to 800MHz range.
- Low phase noise output (@ 10kHz frequency offset, -142dBc/Hz for 19.44MHz, -125dBc/Hz for 155.52MHz, -115dBc/Hz for 622.08MHz).
- 12 to 25MHz crystal input.
- No external load capacitor or varicap required.
- Inverted LVDS signal Output Enable selector.
- Wide pull range (+/-200 ppm)
- Selectable 1/16 to 32x frequency multiplier.
- 3.3V operation.
- Available in 16-Pin (TSSOP or 3x3mm QFN).

DESCRIPTION

The PLL502-39U (LVDS) is a high performance and low phase noise VCXO clock IC. It provides phase noise performance as low as –125dBc at 10kHz offset (at 155MHz), by multiplying the input crystal frequency up to 32x. The wide pull range (+/- 200 ppm) and very low jitter makes this ideal for a wide range of applications, including SONET/SDH and FEC. PLL502-39 accepts fundamental parallel resonant mode crystals input from 12 to 25MHz.

PIN CONFIGURATION

(Top View)

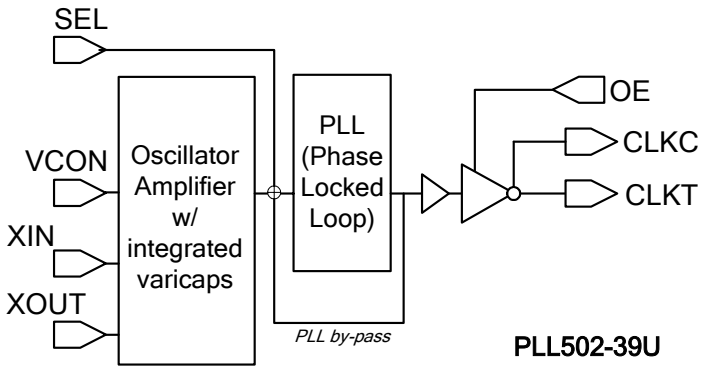


Note: ^ designates Internal pull-up

OUTPUT ENABLE LOGICAL LEVELS

Part #	OE	State
PLL502-39U	1	Tri-state
	0 (Default)	Output enabled

BLOCK DIAGRAM



PLL502-39U

FREQUENCY SELECTION TABLE

SEL3	SEL2	SEL1	SEL0	Selected Multiplier
0	0	1	1	Fin x 32
0	1	1	0	Fin / 8
0	1	1	1	Fin x 2
1	0	0	1	Fin / 2
1	0	1	0	Fin / 16
1	0	1	1	Fin x 4
1	1	0	0	Fin / 4
1	1	0	1	Fin x 8
1	1	1	0	Fin x 16
1	1	1	1	No multiplication

PIN DESCRIPTIONS

Name	3x3mm QFN Pin number	Type	Description
VCON	1	I	Voltage Control input.
GND	2,3,4,8	P	Ground connection.
CLKT	5	O	LVDS Output
VDD	6	P	+3.3V power supply.
CLKC	7	O	Complementary LVDS output
SEL1	9	I	Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND.
SEL0	10	I	
VDD	11	P	+3.3V power supply.
XIN	12	I	Crystal input. See Crystal Specification on page 3.
XOUT	13	I	Crystal output. See Crystal Specification on page 3.
SEL3	14	I	Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND.
SEL2	15	I	
OE	16	I	Output enable pin (see OE logic state table on page 1).

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode	12		25	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$	At VCON = 1.65V		9.5		pF
Crystal Pullability	$C_0/C_{1\ (xtal)}$	AT cut			250	-
Recommended ESR	R_E	AT cut			30	Ω

Note: Crystal Loading rating: 9.5pF is the loading the crystal sees from the VCXO chip at VCON = 1.65V. It is assumed that the crystal will be at nominal frequency at this load. If the crystal requires more load to be at nominal frequency, the additional load must be added externally. This however may reduce the pull range.

3. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		F_{XIN} = 12 – 25MHz; XTAL C_0/C_1 < 250 0V ≤ VCON ≤ 3.3V		500		ppm
CLK output pullability		VCON=1.65V, ±1.65V	±200			ppm
VCXO Tuning Characteristic				150		ppm/V
Pull range linearity					10	%
VCON pin input impedance			2000			kΩ
VCON modulation BW		0V ≤ VCON ≤ 3.3V, -3dB	25			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

4. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic (with Loaded Outputs)	I_{DD}	Fout<24MHz			25	mA
		24MHz<Fout<96MHz			45	
		96MHz<Fout<800MHz			80	
Operating Voltage	V_{DD}		2.97		3.63	V
Output Clock Duty Cycle		@ 1.25V	4	50	55	%
Short Circuit Current				±50		mA

5. Jitter Specifications

PARAMETERS	CONDITIONS	FREQUENCY	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	19.44MHz		2.2		ps
		77.76MHz		4.5		
		155.52MHz		4.5		
		622.08MHz		5.0		
Period jitter Peak-to-Peak[1]	With capacitive decoupling between VDD and GND. Over 10,000 cycles.	19.44MHz		17		ps
		77.76MHz		25		
		155.52MHz		27		
		622.08MHz		35		
Integrated jitter RMS	Integrated 12 kHz to 20 MHz	155.52MHz		2.5	4	ps
		622.08MHz		2.5	4	

6. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier (typical)	19.44MHz	-80	-108	-132	-142	-150	dBc/Hz
	77.76MHz	-72	-103	-122	-130	-125	
	155.52MHz	-65	-95	-120	-125	-121	
	622.08MHz	-55	-85	-109	-115	-110	

Note: Phase Noise measured at VCON = 0V

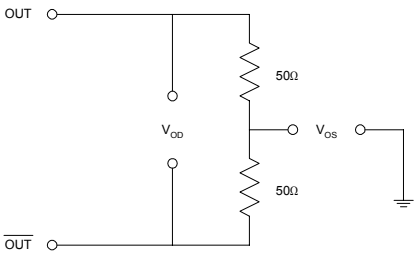
8. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

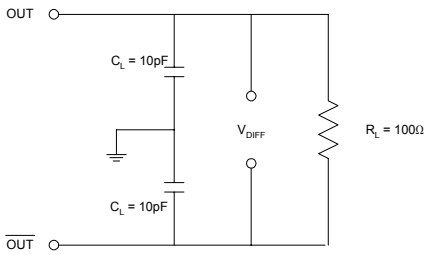
9. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

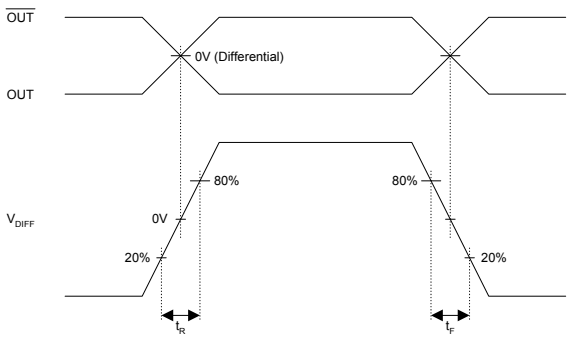
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



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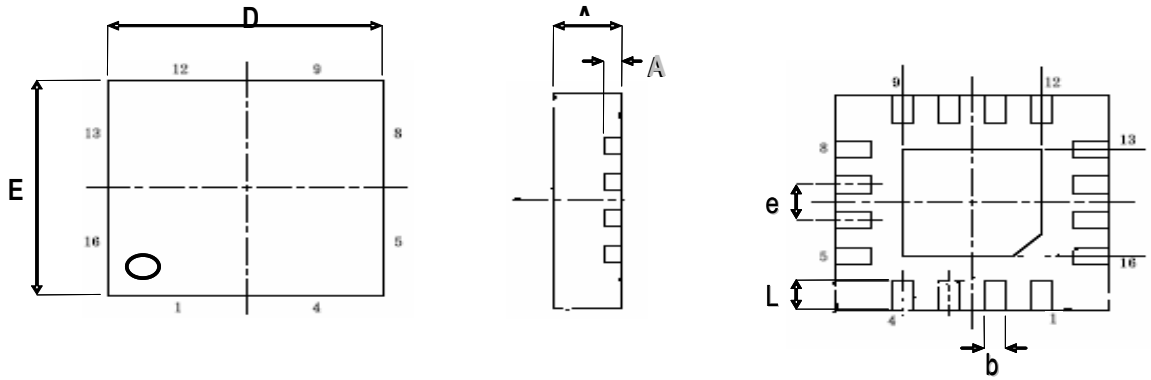
PACKAGE INFORMATION

16 Pin 3x3 QFN



Symbol	Dimension in MM		Dimension in inch	
	Min.	Max.	Min.	Max.
A	0.70	0.80	0.028	0.032
A1	0.203 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:

Device number, Package type, Operating temperature range, shipping method

PLL502-39U X X- R

PART NUMBER

PACKAGE TYPE
Q=QFN

NONE= TUBE
-R=TAPE AND REEL

TEMPERATURE
C=COMMERCIAL
I=INDUSTRAL

Order Number	Marking	Package Option
PLL502-39UQC	P502-39UQC	16-Pin 3x3 QFN (Tube)
PLL502-39UQC-R	P502-39UQC	16-Pin 3x3 QFN (Tape and Reel)