Description

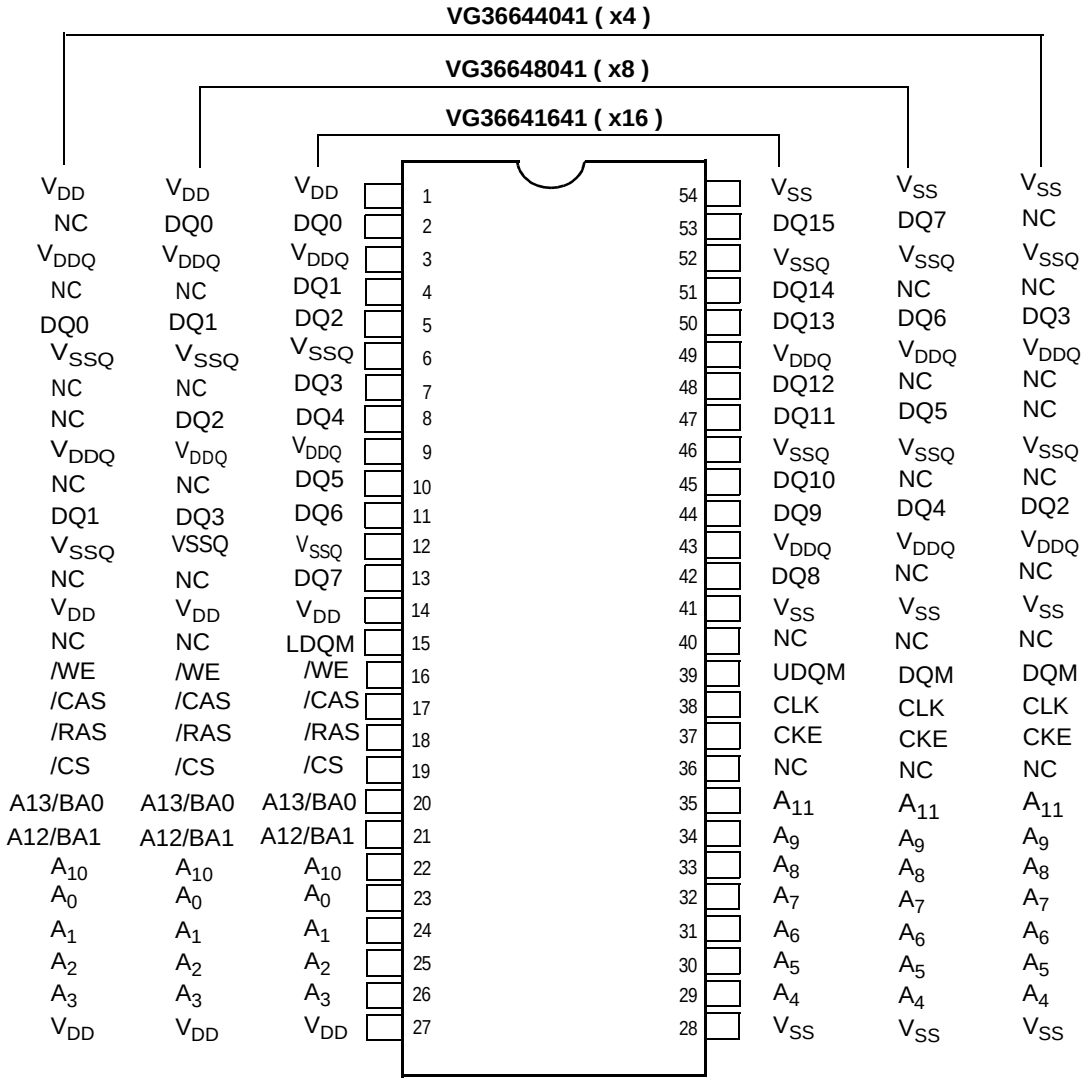
The VG36644041D, VG36648041D and VG36641641D are high-speed 67,108,864-bit synchronous dynamic random-access memories, organized as 4,194,304 x 4 x 4, 2,097,152 x 8 x 4 and 1,048,576 x 16 x 4 (word x bit x bank), respectively.

The synchronous DRAMs achieve high-speed data transfer using the pipeline architecture. All input and outputs are synchronized with the positive edge of the clock.The synchronous DRAMs are compatible with Low Voltage TTL (LVTTL).These products are packaged in 54-pin TSOPII.

Features

- Single 3.3V (±0.3V) power supply
- High speed clock cycle time
  - -5L : 183MHz<3-3-3>, available only on 4Mx16 option
  - -6 : 166MHz<3-3-3>
  - -7 : 143MHz<3-3-3>, 133MHz<2-3-2>
  - -7L : 133MHz<3-3-3>
  - -8H : 100MHz<2-2-2>
- Fully synchronous operation referenced to clock rising edge
- Possible to assert random column access in every cycle
- Quad internal banks controlled by A12 & A13 (Bank Select)
- Byte control by LDQM and UDQM for VG36641641D
- Programmable wrap sequence (Sequential / Interleave)
- Programmable burst length (1, 2, 4, 8 and full page)
- Programmable /CAS latency (2 and 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- X4, X8, X16 organization
- LVTTL compatible inputs and outputs
- 4,096 refresh cycles / 64ms
- Burst termination by Burst stop and Precharge command

Pin Configurations



Pin Descriptions

Pin Name	Function	Pin Name	Function
CLK	Master Clock	DQM	DQ Mask Enable
CKE	Clock Enable	A0-11	Address Input
/CS	Chip Select	BA0,1	Bank Address
/RAS	Row Address Strobe	V_{DD}	Power Supply
/CAS	Column Address Strobe	V_{DDQ}	Power Supply for DQ
/WE	Write Enable	V_{SS}	Ground
DQ0 ~ DQ15	Data I/O	V_{SSQ}	Ground for DQ

Pin Function

Symbol	Input	Function
CLK	Input	Other input signals are referenecd to the CLK rising edge
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank).
/CS	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
/RAS, /CAS, /WE	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
A0 - A13	Input	Address Inputs: Provide the row address for ACTIVE command, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. The row address is specified by A0-A11. The column address is specified by A0-A9 (X4) / A0-A8 (X8) / A0-A7 (X16)
BA0,BA1	Input	Bank Address Inputs: BA0 and BA1 define which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied to.
DQM, UDQM , LDQM	Input	Din Mask / Output Disable: When DQM is high in burst write, Din for the current cycle is masked. When DQM is is high in burst read, Dout is disable at the next but one cycle.
DQ0 - DQ15	I/O	Data Input / Output: Data bus
V_{DD}, V_{SS}	Supply	Power Supply for the memory array and peripheral circuitry
V_{DDQ}, V_{SSQ}	Supply	Power Supply are supplied to the output buffers only

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit
Supply Voltage	V_{DD}	with respect to V_{SS}	-0.5 to 4.6	V
Supply Voltage for Output	V_{DDQ}	with respect to V_{SSQ}	-0.5 to 4.6	V
Input Voltage	V_I	with respect to V_{SS}	-0.5 to V_{DD}+0.5	V
Output Voltage	V_O	with respect to V_{SSQ}	-0.5 to V_{DDQ}+0.5	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D	T_a = 25 °C	1	W
Operating temperature	T_{OPT}		0 to 70	°C
Storage temperature	T_{STG}		-65 to 150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (T_a = 0 ~ 70 °C, unless otherwise noted)

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Supply Voltage for DQ	V_{DDQ}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Ground for DQ	V_{SSQ}	0	0	0	V
High Level Input Voltage (all inputs)	V_{IH}	2.0		V_{DD} + 0.3	V
Low Level Input Voltage (all inputs)	V_{IL}	-0.3		0.8	V

Pin Capacitance (Ta = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.3±0.3V , V_{SS} = V_{SSQ} = 0V, unless otherwise noted)

Parameter	Symbol	Min	Max	Unit
Input Capacitance, address & control pin	C_{IN}	2.5	3.8	pF
Input Capacitance, CLK pin	C_{CLK}	2.5	3.5	pF
Data input / output capacitance	$C_{I/O}$	4.0	6.5	pF

DC Characteristics 1

(Ta = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.3± 0.3V, V_{SS} = V_{SSQ} = 0V, Ouput Open, unless otherwise noted)

Parameter	Symbol	Test Conditions	Organization	Limits (max.)					Unit	Notes
				-5L	-6	-7	-7L	-8H		
Operating current	I_{CC1}	One bank active t_{RC} = $t_{RC(MIN)}$, t_{CLK} = $t_{CLK(MIN)}$, BL = 1, CL=3	x4	-	-	75	75	70	mA	1, 2
			x8	-	-	75	75	70		
			x16	100	95	85	85	80		
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL(MAX)}$, t_{CK} = 15ns	x4/x8/x16	2					mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL(MAX)}$, CLK ≤ $V_{IL(MAX)}$	x4/x8/x16	1					mA	
Precharge standby current in non power down mode	$I_{CC2}N$	$\overline{CS}$ ≥ V_{CC} - 0.2V t_{CK} = 15ns, CKE ≥ $V_{IH(MIN)}$	x4/x8/x16	20					mA	3
	$I_{CC2}NS$	$\overline{CS}$ ≥ V_{CC} - 0.2V CLK ≤ $V_{IL(MAX)}$, CKE≥$V_{IH(MIN)}$ All input signals are stable.	x4/x8/x16	20					mA	
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL(MAX)}$, t_{CK} = 10ns	x4/x8/x16	7					mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL(MAX)}$, CLK ≤ $V_{IL(MAX)}$	x4/x8/x16	5						
Active standby current in Nonpower down mode	$I_{CC3}N$	$\overline{CS}$ ≥ V_{CC} - 0.2V t_{CK} = 15ns, CKE ≥ $V_{IH(MIN)}$	x4/x8/x16	35					mA	3
	$I_{CC3}NS$	$\overline{CS}$ ≥ V_{CC} - 0.2V CLK ≤ $V_{IL(MAX)}$, CKE≥$V_{IH(MIN)}$ All input signals are stable.	x4/x8/x16	35					mA	
Operating current (Burst mode)	I_{CC4}	All banks active t_{CK} = $t_{CK(MIN)}$, BL=4, CL=3 All banks active	x4	-	-	90	90	70	mA	
			x8	-	-	90	90	70		
			x16	140	130	100	100	80		
Refresh current	I_{CC5}	t_{RC} = $t_{RC(MIN)}$, t_{CLK} = $t_{CLK(MIN)}$	x4/x8/x16	160	150	130	130	110	mA	
Self refresh current	I_{CC6}	CKE ≤ 0.2V	x4/x8/x16	1					mA	4
				0.5					mA	5

NOTES

1. $I_{CC(max)}$ is specified at the output open condition.
2. -5L grade are available only on 4MX16 option.
3. Input signals are changed one time during 30ns.
4. Normal version: VG366440(80/16)41DT
5. Low power version: VG366440(80/16)41DTL

DC Characteristics 2

(Ta = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.3±0.3V , V_{SS} = V_{SSQ} = 0V, unless otherwise noted)

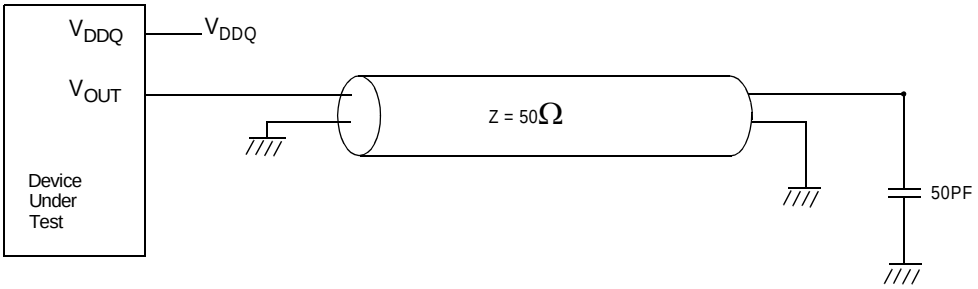
Parameter	Symbol	Test Condition	Min	Max	Unit
Input leakage current (Inputs)	$I_{I(L)}$	$0 \leq V_{IN} \leq V_{DD(MAX)}$ Pins not under test = 0V	-5	5	uA
Output leakage current (I/O pins)	$I_{O(L)}$	$0 \leq V_{OUT} \leq V_{DD(MAX)}$ DQ# in H - Z., D_{OUT} is disabled	-5	5	uA
High level output voltage	V_{OH}	I_{OH} = -2mA	2.4		V
Low level output voltage	V_{OL}	I_{OL} = 2mA		0.4	V

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.3±0.3V , V_{SS} = V_{SSQ} = 0V, unless otherwise noted)

AC input Levels (V_{IH}/V_{IL})	2.0 / 0.8V	Input timing reference level / Output timing reference level	1.4V
Input rise and fall time	1ns	Output load condition	50pF

Note): 1.if clock rising time is longer than 1ns, (tr/2-0.5ns) should be added to the parameter.

Output Load Conditions



A.C. Characteristics (Ta = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.3±0.3V , V_{SS} = V_{SSQ} = 0V, unless otherwise noted)

Parameter		Sym-bol	Limits										Unit	Note
			-5L*1		-6 *1		-7		-7L		-8H			
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CL = 3	t_{CK3}	5.5		6		7		7.5		8		ns	
	CL = 2	t_{CK2}	7.5		7.5		7.5		10		10		ns	
CLK to valid output delay	CL = 3	t_{AC3}		5		5		5.4		5.4		6	ns	*2
	CL = 2	t_{AC2}		6		6		6		6		6	ns	*2
CLK high pulse width		t_{CH}	2.3		2.5		2.5		2.5		3		ns	
CLK low pulse width		t_{CL}	2.3		2.5		2.5		2.5		3		ns	
CKE setup time		t_{CKS}	1.5		1.5		1.5		1.5		2		ns	
CKE hold time		t_{CKH}	0.8		0.8		0.8		0.8		1		ns	
Address setup time		t_{AS}	1.5		1.5		1.5		1.5		2		ns	
Address hold time		t_{AH}	0.8		0.8		0.8		0.8		1		ns	
Command setup time		t_{CMS}	1.5		1.5		1.5		1.5		2		ns	
Command hold time		t_{CMH}	0.8		0.8		0.8		0.8		1		ns	
Data input setup time		t_{DS}	1.5		1.5		1.5		1.5		2		ns	
Data input hold time		t_{DH}	0.8		0.8		0.8		0.8		1		ns	
Output data hold time	CL = 3	t_{OH3}	2		2.5		2.7		2.7		3		ns	*2
	CL = 2	t_{OH2}	2		2.5		2.7		3		3		ns	*2
CLK to output in low - Z		t_{LZ}	0		0		0		0		0		ns	
CLK to output in H - Z		t_{HZ}	2	5	2.5	5	2.7	5.4	2.7	5.4	3	6	ns	
ROW cycle time		t_{RC}	55		60		63		67.5		70		ns	
ROW active time		t_{RAS}	38.5	100K	42	100K	42	100K	45	100K	50	100K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}	16.5		18		20		20		20		ns	
Row precharge time		t_{RP}	15		15		15		20		20		ns	
Row active to active delay		t_{RRD}	11		12		14		15		20		ns	
Data in to precharge		t_{DPL}	11		12		14		15		20		ns	
Data in to ACT command		t_{DAL}	tDPL + tRP		tDPL + tRP		tDPL + tRP		tDPL + tRP		tDPL + tRP		ns	
Transition time		t_T	1	10	1	10	1	10	1	10	1	10	ns	
Mode reg. set cycle		t_{RSC}	2		2		2		2		2		tck	
Refresh time		t_{REF}		64		64		64		64		64	ms	

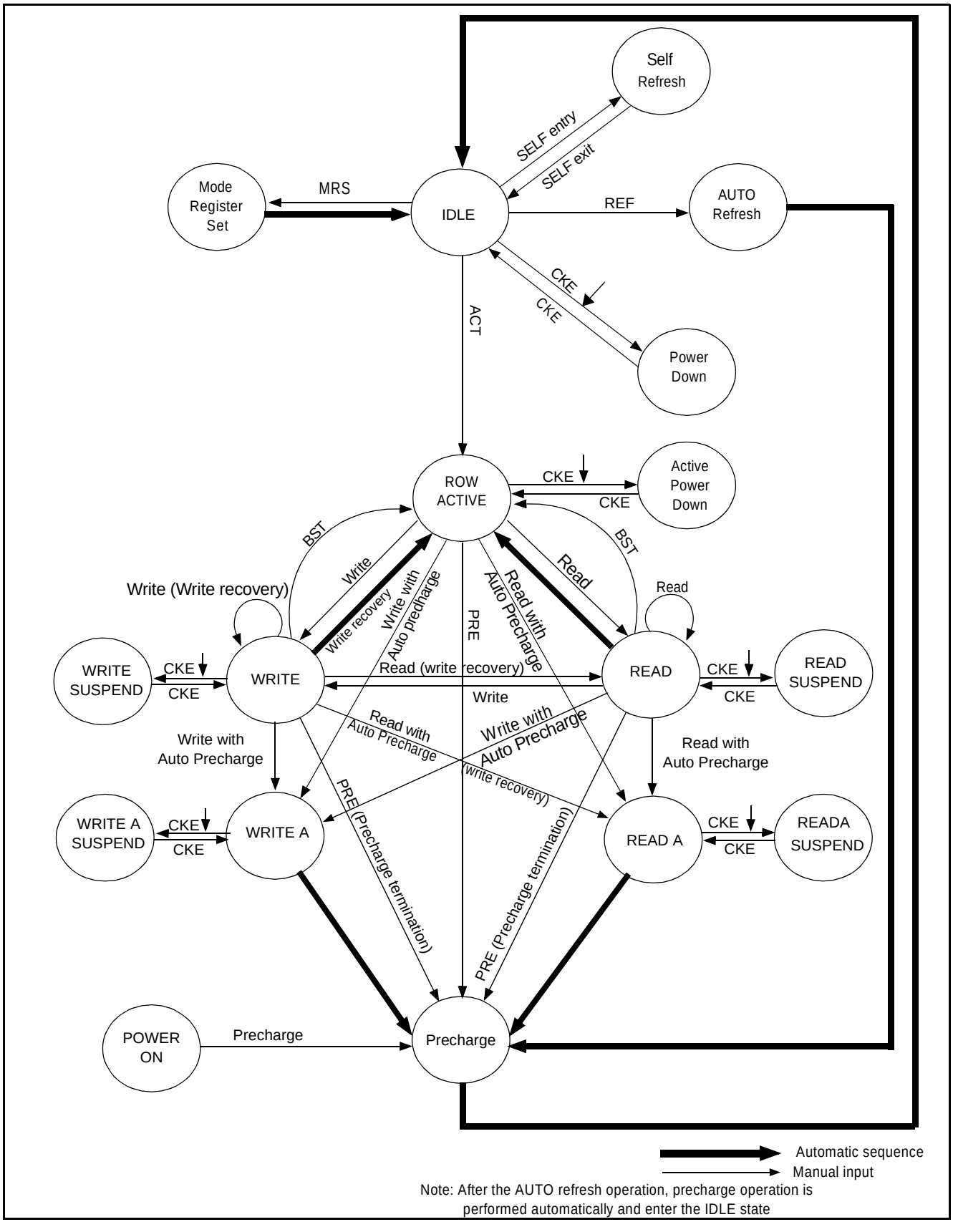
Notes

1. -5L grade are available only on 4MX16 option.

2. if clock rising time is longer than 1ns, (tr/2-0.5ns) should be added to the parameter.

Basic Features and Function Description

1. Simplified State Diagram



Note: After the AUTO refresh operation, precharge operation is performed automatically and enter the IDLE state

2.Truth Table

2.1 Command Truth Table

FUNCTION	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10	A11 A9 - A0
		n - 1	n							
Device deselect	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto precharge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	X	L	H	L	L	V	H	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Burst stop	BST	H	X	L	H	H	L	X	X	X
CBR (Auto) refresh	REF	H	H	L	L	L	H	X	X	X
Self refresh	SELF	H	L	L	L	L	H	X	X	X

2.2 DQM Truth Table

FUNCTION	Symbol	CKE		DQM
		n - 1	n - 1	
Data write/output enable	ENB	H	X	L
Data mask/output disable	MASK	H	X	H

2.3 CKE Truth Table

Current State	Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add - ress
			n - 1	n					
Activating	Clock suspend mode entry		H	L	X	X	X	X	X
Any	Clock suspend		L	L	X	X	X	X	X
Clock suspend	Clock suspend mode exit		L	H	X	X	X	X	X
Idle	CBR refresh command	REF	H	H	L	L	L	H	X
Idle	Self refresh entry	SELF	H	L	L	L	L	H	X
Self refresh	Self refresh exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power down entry		H	L	X	X	X	X	X
Power down	Power down exit		L	H	X	X	X	X	X

H : High level, L : Low level

X : High or Low level (Don't care), V : Valid Data input

2.4 Operative Command Table (note 1) (1/3)

HCurrent state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Idle	H	X	X	X	X	DESL	Nop or Power down	2
	L	H	H	X	X	NOP or BST	Nop or Power down	2
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BR, RA	ACT	Row active	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	X	REF/SELF	Refresh or Self refresh	4
	L	L	L	L	Op-Code	MPS	Mode register access	
Row active	H	X	X	X	X	DESL	Nop	
	L	H	H	X	X	NOP or BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read : Determine AP	5
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write : Determine AP	5
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Precharge	6
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	H	X	X	X	X	DESL	Continue burst to end → Row active	
	L	H	H	H	X	NOP	Continue burst to end → Row active	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, new read : Determine AP	7
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, start write : Determine AP	7,8
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharging	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	H	X	X	X	X	DESL	Continue burst to end → write recovering	
	L	H	H	H	X	NOP	Continue burst to end → write recovering	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Term burst, start read : Determine AP	7,8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Term burst, new write : Determine AP	7
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Term burst, precharging	9
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(2/3)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CA}$	$\overline{WE}$	Address	Command	Action	Notes
Read with auto precharge	H	X	X	X	X	DESL	Continue burst to end → Precharging	
	L	H	H	H	X	NOP	Continue burst to end → Precharging	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	11
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3,11
	L	L	L	H	X	PEF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Write with auto precharge	H	X	X	X	X	DESL	Continue burst to end → write recovering with auto precharte	
	L	H	H	H	X	NOP	Continue burst to end → write recovering with auto precharge	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	11
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3,11
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - code	MRS	ILLEGAL	
Precharging	H	X	X	X	X	DESL	Nop → Enter idle after t_{RP}	
	L	H	H	H	X	NOP	Nop → Enter idle after t_{RP}	
	L	H	H	L	X	BST	Nop → Enter idle after t_{RP}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after t_{RP}	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Row activating	H	X	X	X	X	DESL	Nop → Enter row active after t_{RCD}	
	L	H	H	H	X	NOP	Nop → Enter row active after t_{RCD}	
	L	H	H	L	X	BST	Nop → Enter row active after t_{RCD}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	3, 9
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	

(3/3)

Current	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Write recovering	H	X	X	X	X	DESL	Nop → Enter row active after t_{DPL}	
	L	H	H	H	X	NOP	Nop → Enter row active after t_{DPL}	
	L	H	H	L	X	BST	Nop → Enter row active after t_{DPL}	
	L	H	L	H	BA, CA, A10	READ/READA	Start read, Determine AP	8
	L	H	L	L	BA, CA, A10	WRIT/WRITA	New write, Determine AP	
	L	L	H	H	BA, RA	ACT	ILLEGAL	3
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	PEF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Write recovering with auto precharge	H	X	X	X	X	DESL	Nop → Enter precharge after t_{DPL}	
	L	H	H	H	X	NOP	Nop → Enter precharge after t_{DPL}	
	L	H	H	L	X	BST	Nop → Enter precharge after t_{DPL}	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	3,8,11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	3,11
	L	L	H	H	BA, RA	ACT	ILLEGAL	3,11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op - Code	MRS	ILLEGAL	
Auto Refreshing	H	X	X	X	X	DESL	Nop Enter idle after t_{RC}	
	L	H	H	X	X	NOP/BST	Nop Enter idle after t_{RC}	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	H	X	X	ACT/PRE/PALL	ILLEGAL	
	L	L	L	X	X	REF/SELF/MRS	ILLEGAL	
Mode register setting	H	X	X	X	X	DESL	Nop → Enter idle after 2 Clocks	
	L	H	H	H	X	NOP	Nop → Enter idle after 2 Clocks	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/WRITE	ILLEGAL	
	L	L	X	X	X	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL	

Note

1. All entries assume that CKE was active (High level) during the preceding clock cycle.
2. If both banks are idle, and CKE is inactive (Low level), the device will enter Power downmode. All input buffers except CKE will be disabled.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by BankAddress(BA), depending on the state of that bank.
4. If both banks are idle, and CKE is inactive (Low level), the device will enter Self refresh mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RCD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Must mask preceding data which don't satisfy t_{DPL}.
10. Illegal if t_{RRD} is not satisfied.
11. Illegal for single bank, but legal for other banks in multi-bank devices.

2.5 Command Truth Table for CKE (Note 1)

Current state	CKE n - 1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Notes
Self refresh (S.R.)	H	X	X	X	X	X	X	INVALID, CLK (n - 1)would exit S.R.	
	L	H	H	X	X	X	X	S.R. Recovery	2
	L	H	L	H	H	X	X	S.R. Recovery	2
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	Maintain S.R.	
Self refresh recovery	H	H	H	X	X	X	X	Idle after t_{RC}	
	H	H	L	H	H	X	X	Idle after t_{RC}	
	H	H	L	H	L	X	X	ILLEGAL	
	H	H	L	L	X	X	X	ILLEGAL	
	H	L	H	X	X	X	X	Begin clock suspend next cycle	5
	H	L	L	H	H	X	X	Begin clock suspend next cycle	5
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	H	X	X	X	X	X	Exit clock suspend next cycle	2
	L	L	X	X	X	X	X	Maintain clock suspend	
Power down (P.D.)	H	X	X	X	X	X		INVALID, CLK (n - 1) would exit P.D.	
	L	H	X	X	X	X	X	EXIT P.D. $\rightarrow$ Idle	2
	L	L	X	X	X	X	X	Maintain power down mode	
Both banks idle	H	H	H	X	X	X		Refer to operations in Operative Command Table	
	H	H	L	H	X	X		Refer to operations in Operative Command Table	
	H	H	L	L	H	X		Refer to operation in Operative Command Table	
	H	H	L	L	L	H	X	Auto Refresh	
	H	H	L	L	L	L	Op - Code	Refer to operations in Operative Command Table	
	H	L	H	X	X	X		Refer to operations in Operative Command Table	
	H	L	L	H	X	X		Refer to operations in Operative Command Table	
	H	L	L	L	H	X		Refer to operations in Operative Command Table	
	H	L	L	L	L	H	X	Self refresh	3
	H	L	L	L	L	L	Op - Code	Refer to operations in Operative Command Table	
	L	X	X	X	X	X	X	Power down	3
Any state other than listed above	H	H	X	X	X	X	X	Refer to operations in Operative Command Table	
	H	L	X	X	X	X	X	Begin clock suspend next cycle	4
	L	H	X	X	X	X	X	Exit clock suspend next cycle	
	L	L	X	X	X	X	X	Maintain clock suspend	

Note: 1. H : Hight level, L : low level, X : High or low level (Don't care).
2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
3. Power down and Self refresh can be entered only from the both banks idle state.
4. Must be legal command as defined in Operative Command Table.
5. Illegal if t_{SREX} is not satisfied.

3.Initiallization

Before starting normal operation, the following power on sequence is necessary to prevent SDRAM from damged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high , DQN high and NOP condition at the inputs.
2. Maintain stable power, table clock , and NOP input conditions for a minimum of 200us.
3. Issue precharge commands for all bank. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode regiser.

After these sequence, the SDRAM is in idle state and ready for normal operation.

4.Programming the Mode Register

The mode register is programmed by the mode register set command using address bits A13 through A0 as data inputs. The register retains data until it is reprogrammed or the device loses power.

The mode register has four fields;

Options : A13 through A7

$\overline{\text{CAS}}$ latency : A6 through A4

Wrap type : A3

Burst length : A2 through A0

Following mode register programming, no command can be asserted befor at least two clock cycles have elapsed.

$\overline{\text{CAS}}$ Latency

$\overline{\text{CAS}}$ latency is the most critical parameter being set. It tells the device how many clocks must elapse before the data will be available.

The value is determined by the frequency of the clock and the speed grade of the device. The value can be programmed as 2 or 3.

Burst Length

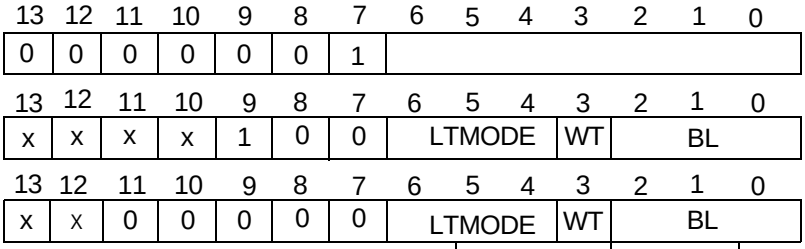
Burst Length is the number of words that will be output or input in read or write cycle. After a read burst is completed, the output bus will become high impedance.

The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. The order is programmable as either “Sequential” or “Interleave”. The method chosen will depend on the type of CPU in the system.

5.Mode Register



Burst length	Bits2 - 0	WT = 0	WT = 1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Fullpage	R

Wrap type		
	0	Sequential
	1	Interleave

Latency mode	Bits 6-4	$\overline{\text{CAS}}$ latency
	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R : Reserved

5.1 Burst Length and Sequence

(Burst of Two)

Starting Address (column address A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

(Burst of Four)

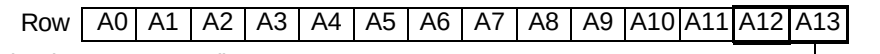
Starting Address (column address A1 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

(Burst of Eight)

Starting Address (column address A2 - A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1 ,2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6 ,7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7 ,0 ,1 ,2 ,3 ,4 ,5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

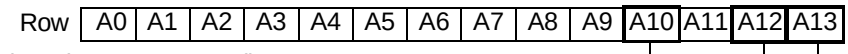
Full page burst is an extension of the above tables of sequential addressing, with the length being 1,024 (for 16Mx4), 512 (for 8M x 8) and 256 (for 4Mx16).

6.Address Bits of Bank-Select and Precharge



(Activate command)

A12	A13	Result
0	0	Select Bank A “Activate “ command
0	1	Select Bank B “Activate” command
1	0	Select Bank C “Activate” command
1	1	Select Bank D “Activate” command

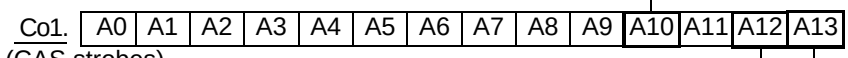


(Precharge command)

A10	A12	A13	Result
0	0	0	Precharge Bank A
0	0	1	Precharge Bank B
0	1	0	Precharge Bank C
0	1	1	Precharge Bank D
1	X	X	Precharge All Banks

X: Don't care

0	Disables Auto-Precharge (End of Burst)
1	Enables Auto - Precharge (End of Burst)



(CAS strobes)

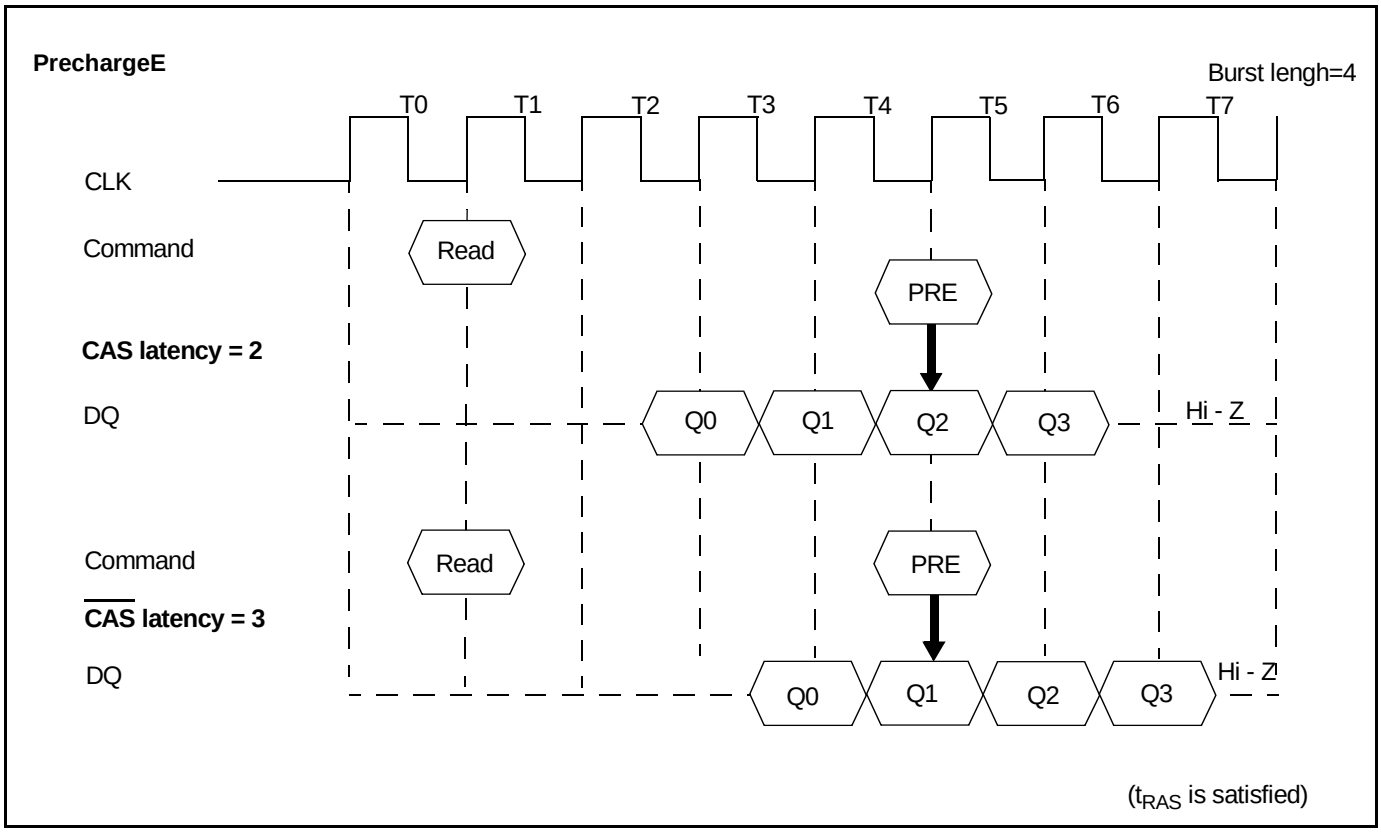
A12	A13	Result
0	0	Enables Read/Write commands for Bank A
0	1	Enables Read/Write commands for Bank B
1	0	Enables Read/Write commands for Bank C
1	1	Enables Read/Write commands for Bank D

7.Precharge

The precharge command can be asserted anytime after $t_{RAS(min.)}$ is satisfied.

Soon after the precharge command is asserted, the precharge operation is performed and the synchronous DRAM enters the idle state after $t_{RP(min.)}$ is satisfied. The parameter t_{RP} is the time required to perform the precharge.

The earliest timing in a read cycle that a precharge command can be asserted without losing any data in the burst is as follows.



In order to write all data to the memory cell correctly, the asynchronous parameter "t_{DPL}" must be satisfied. The $t_{DPL(min.)}$ specification defines the earliest time that a precharge command can be asserted. The minimum number of clocks can be calculated by dividing $t_{DPL(min.)}$ with the clock cycle time.

In summary, the precharge command can be asserted relative to the reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

$\overline{CAS}$ latency	Read	Write
2	-1	+ $t_{DPL(min.)}$
3	-2	+ $t_{DPL(min.)}$

8.Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. If A10 is high in the read or write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins automatically.

In the write cycle, $t_{DAL(min.)}$ must be satisfied before asserting the next activate command to the bank being precharged.

When using auto precharge in the read cycle, knowing when the precharge starts is important because the next activate command to the bank being precharged cannot be executed until the precharge cycle ends. Once auto precharge has started, an activate command to the bank can be asserted after t_{RP} has been satisfied.

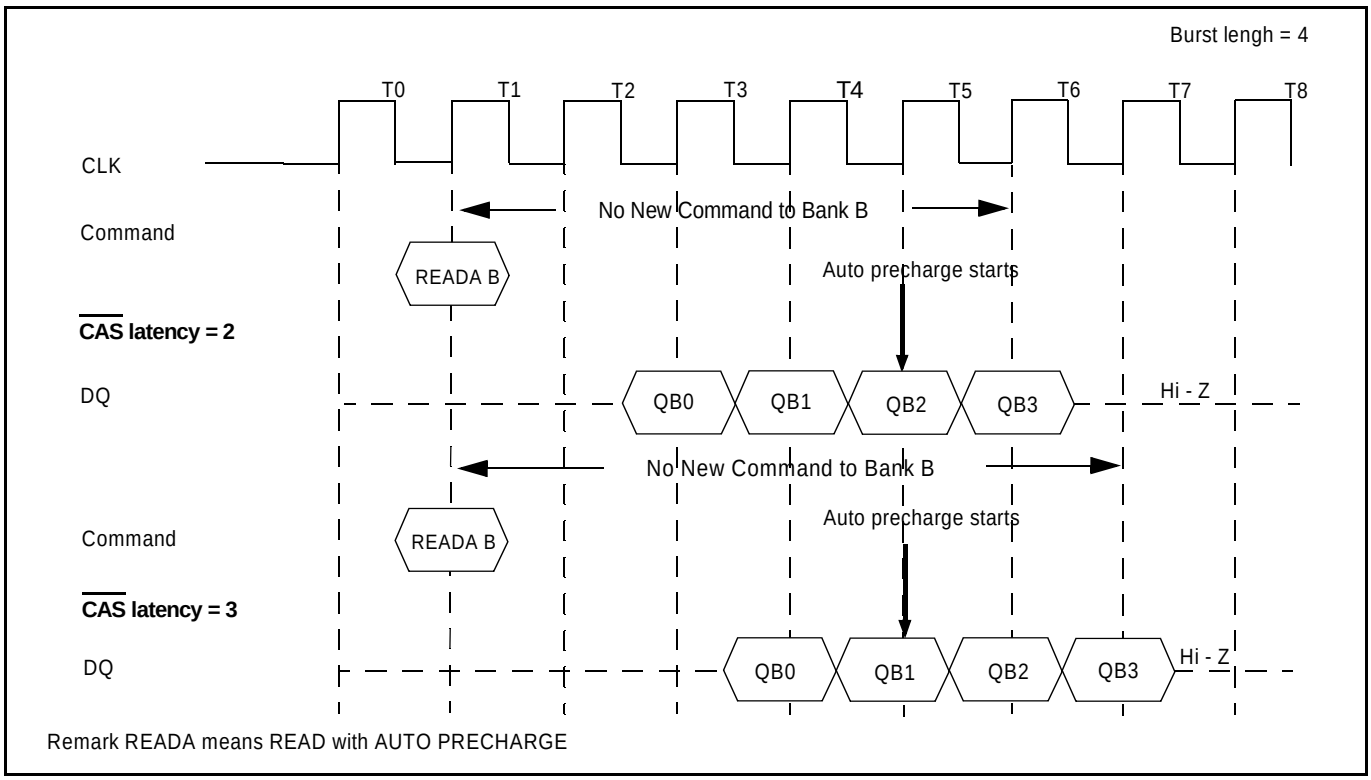
A Read or Write command without auto - precharge can be terminated in the midst of a burst operation. However, a Read or Write command with auto - precharge can not be interrupted by the same bank commands before the entire burst operation is completed. Therefore use of the same bank Read, Write, Precharge or Burst Stop command is prohibited during a read or write cycle with auto - precharge. It should be noted that the device will not respond to the Auto - Precharge command if the device is programmed for full page burst read or write cycles.

The timing when the auto precharge cycle begins depends both on both the $\overline{CAS}$ latency programmed into the mode register and whether the cycle is read or write.

8.1 Read with Auto Precharge

During a READA cycle, the auto precharge begins one clock earlier (CL = 2) or two clocks earlier (CL = 3) than the last word output.

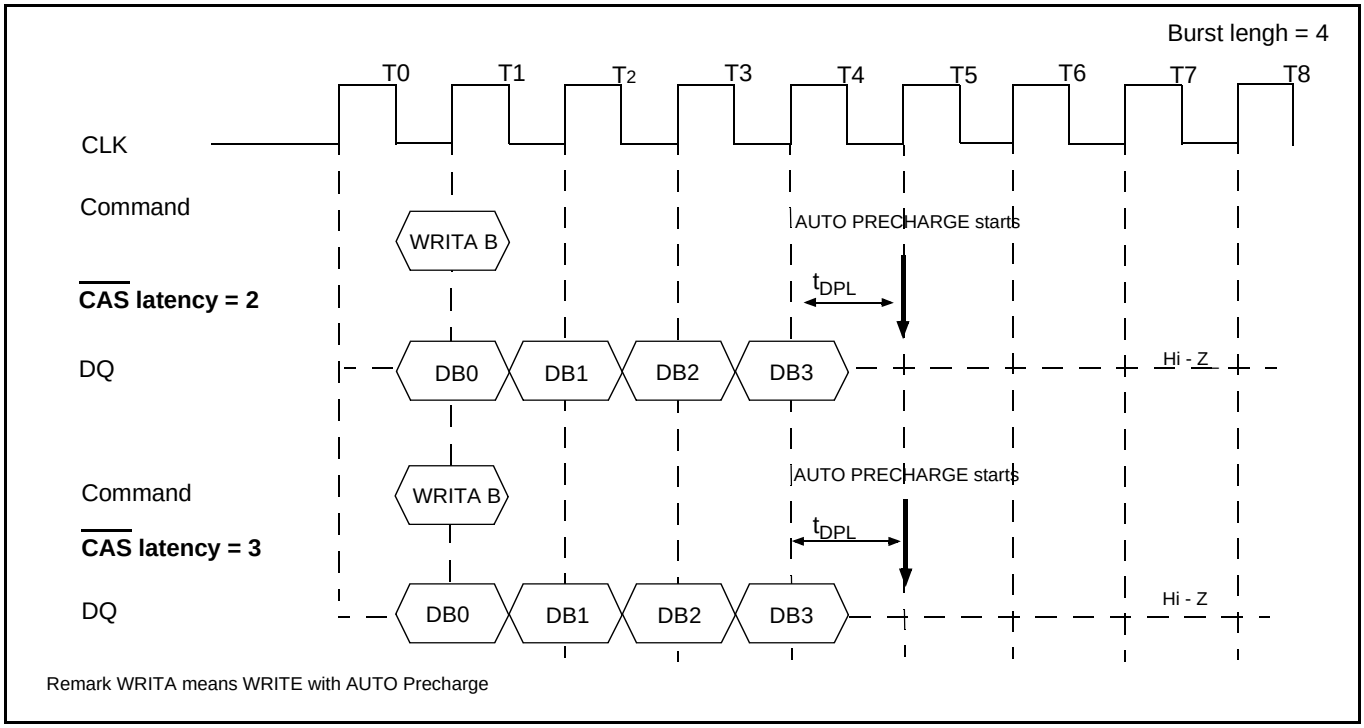
READ with AUTO PRECHARGE



8.2 Write with Auto Precharge

During a write cycle, the auto precharge starts at the timing that is equal to the value of $t_{DPL(min.)}$ after the last data word input to the device.

WRITE with AUTO PRECHRGE



In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid.

In the table below, minus means clocks before the reference; plus means clocks after the reference.

$\overline{\text{CAS}}$ latency	Read	Write
2	-1	+ $t_{DPL(min.)}$
3	-2	+ $t_{DPL(min.)}$

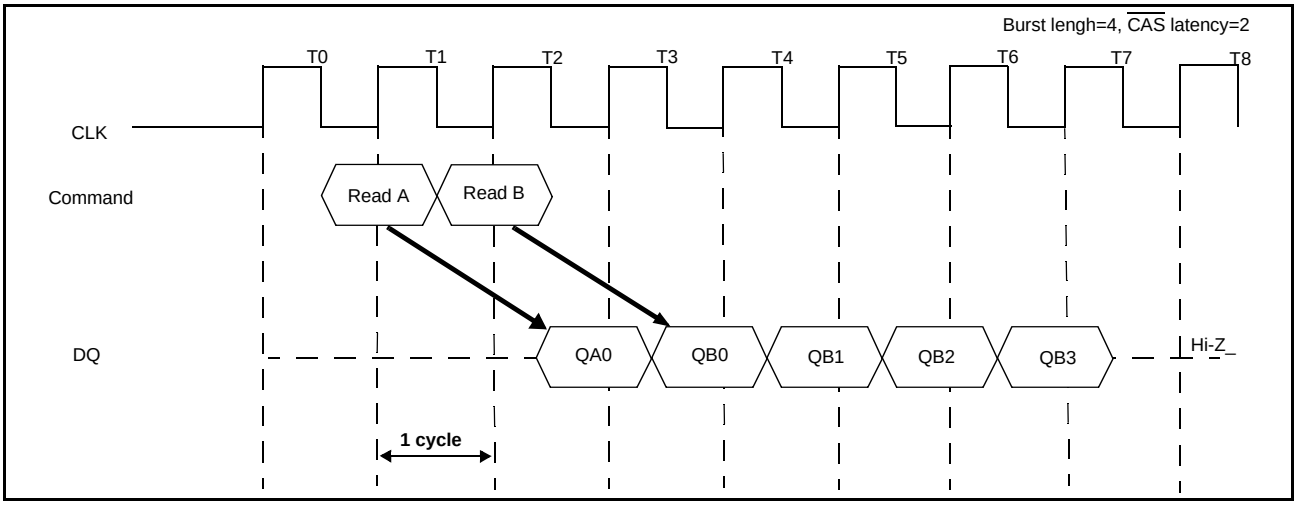
9. Read / Writw Command Interval

9.1 Read to Read Command Interval

During a read cycle when a new read command is asserted, it will be effective after the $\overline{CAS}$ latency, even if the previous read operation has not completed. READ will be interrupted by another READ.

Each read command can be asserted in every clock without any restriction.

READ to READ Command Interval

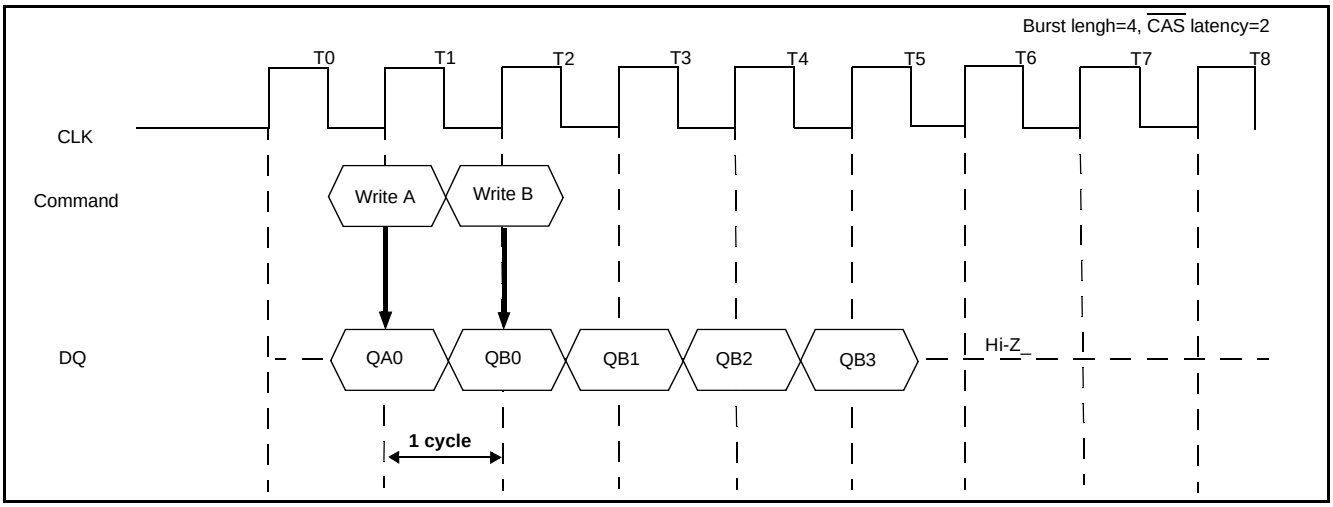


9.2 Write to Write Command Interval

During a write cycle, when a new Write command is asserted, the previous burst will terminated and the new burst will begin with a new write command. WRITE will be interrupted by another WRITE.

Each write command can be asserted in every clock without any restriction.

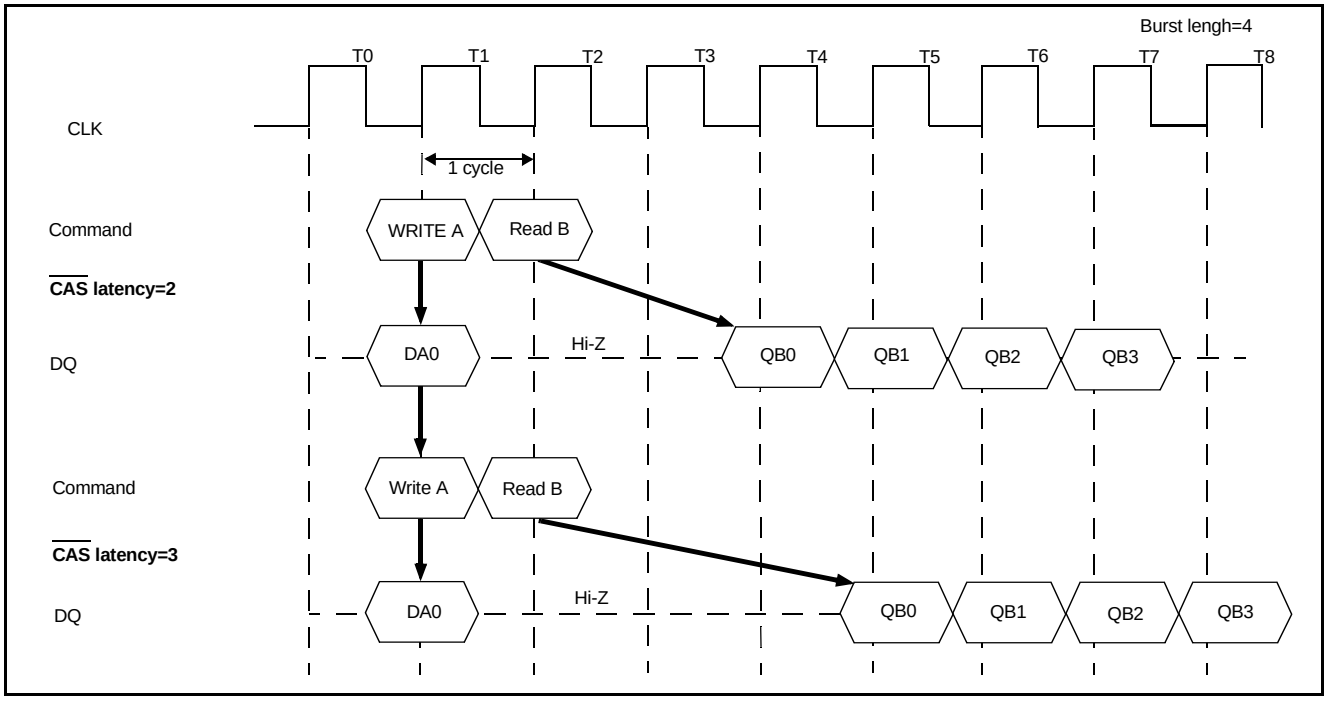
WRITE to WRITE Command Interval



9.3 Write to Read Command Interval

The write command to read command interval is also a minimum of 1 cycle. Only the write data before the read command will be written. The data bus must be Hi-Z at least one cycle prior to the first D_{OUT}.

WRITE to READ Command Interval

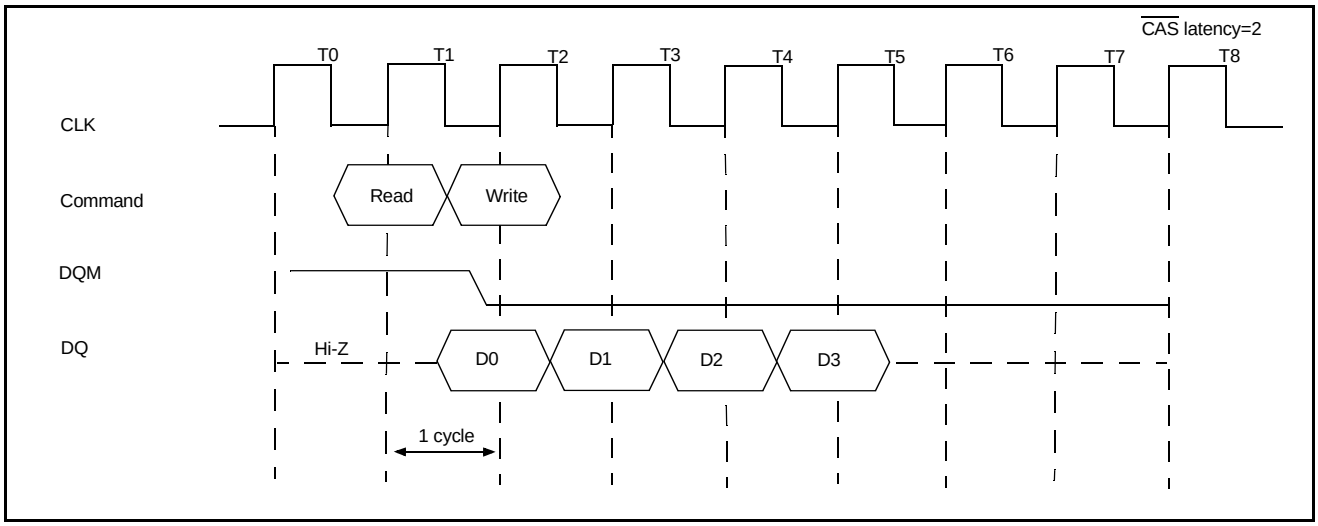


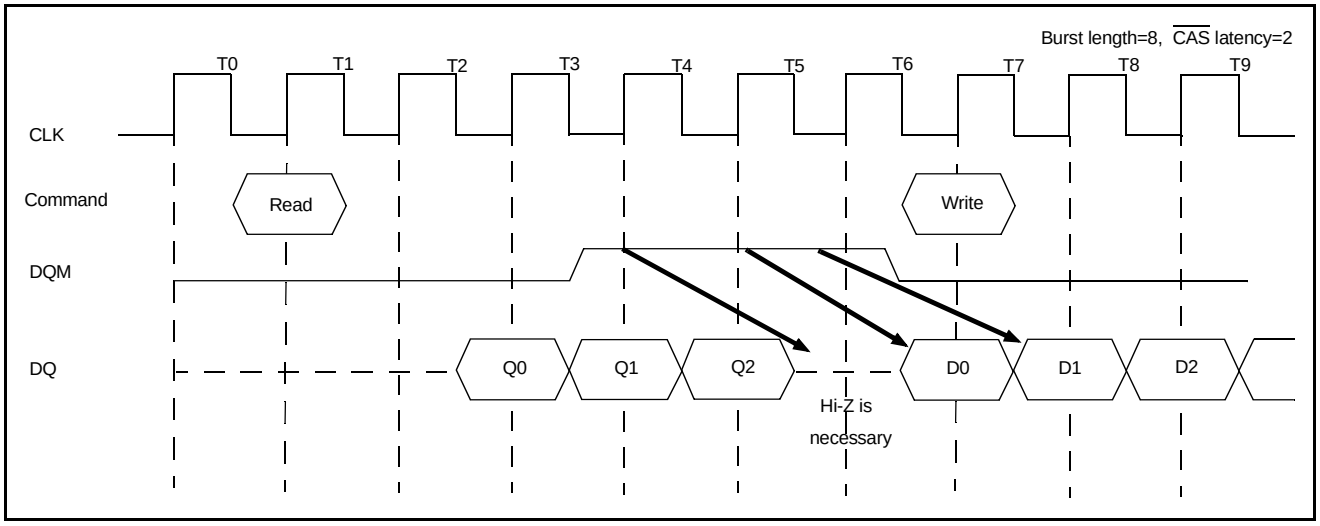
9.4 Read to Write Command Interval

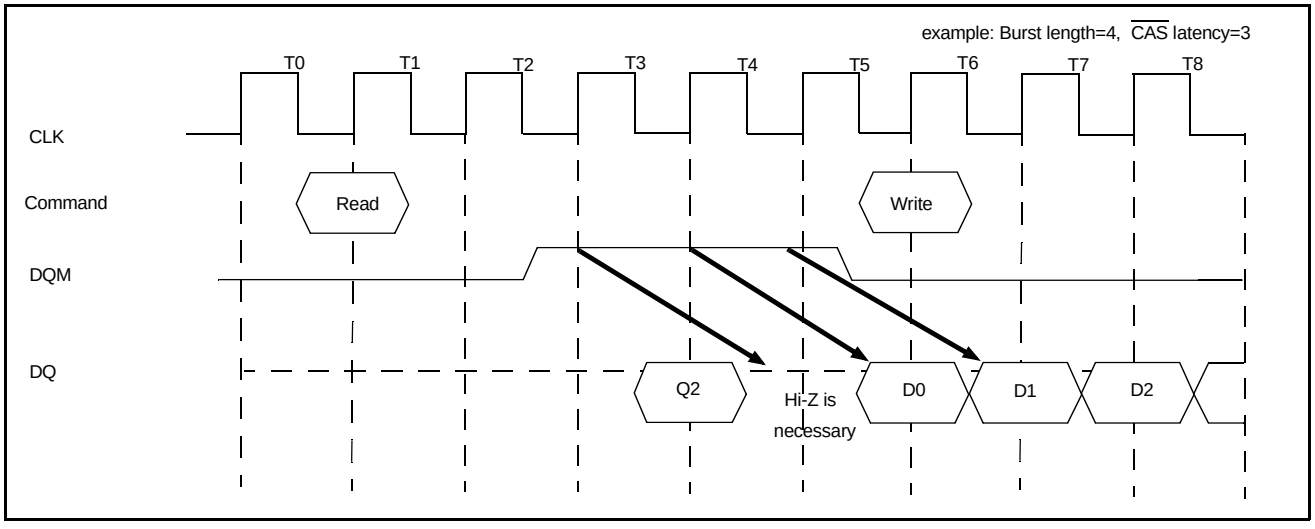
During a read cycle, READ can be interrupted by WRITE.

DQM must be in High at least 3 clocks prior to the write command. There is a restriction to avoid a data conflict. The data bus must be Hi-Z using DQM before Write.

READ to WRITE Command Interval







10.BURST Termination

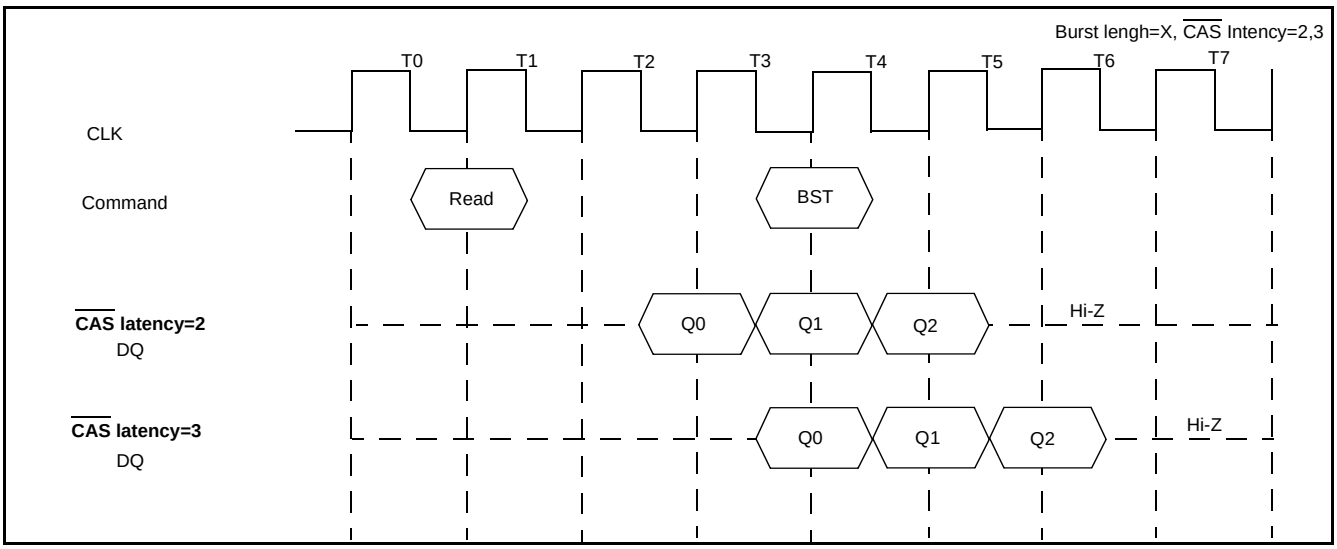
There are two methods to terminate a burst operation other than using a read or a write command. One is the burst stop command and the other is the precharge command.

10.1 BURST Stop Command

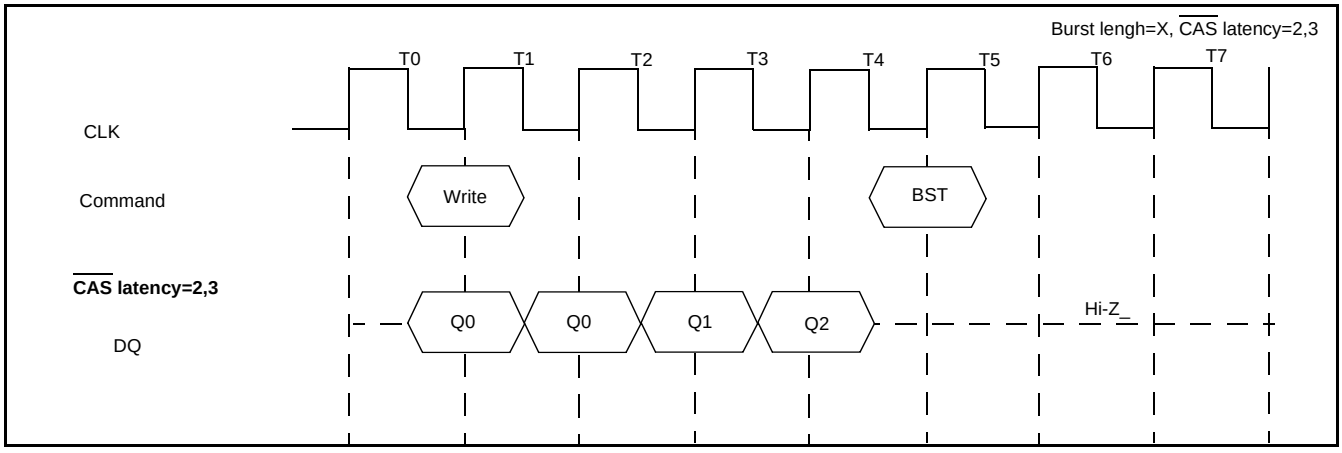
During a read burst, when the burst stop command is issued, the burst read data are terminated and the data bus goes to high-impedance after the $\overline{CAS}$ latency from the burst stop command.

During a write burst, when the burst stop command is issued, the burst write data are termained and data bus goes to Hi-Z at the same clock with the burst stop command.

Burst Termination



Remark BST: Burst stop command



Remark BST: Burst command

10.2 PRECHARGE TERMINATION

10.2.1 PRECHARGE TERMINATION in READ Cycle

During READ cycle, the burst read operation is terminated by a precharge command.

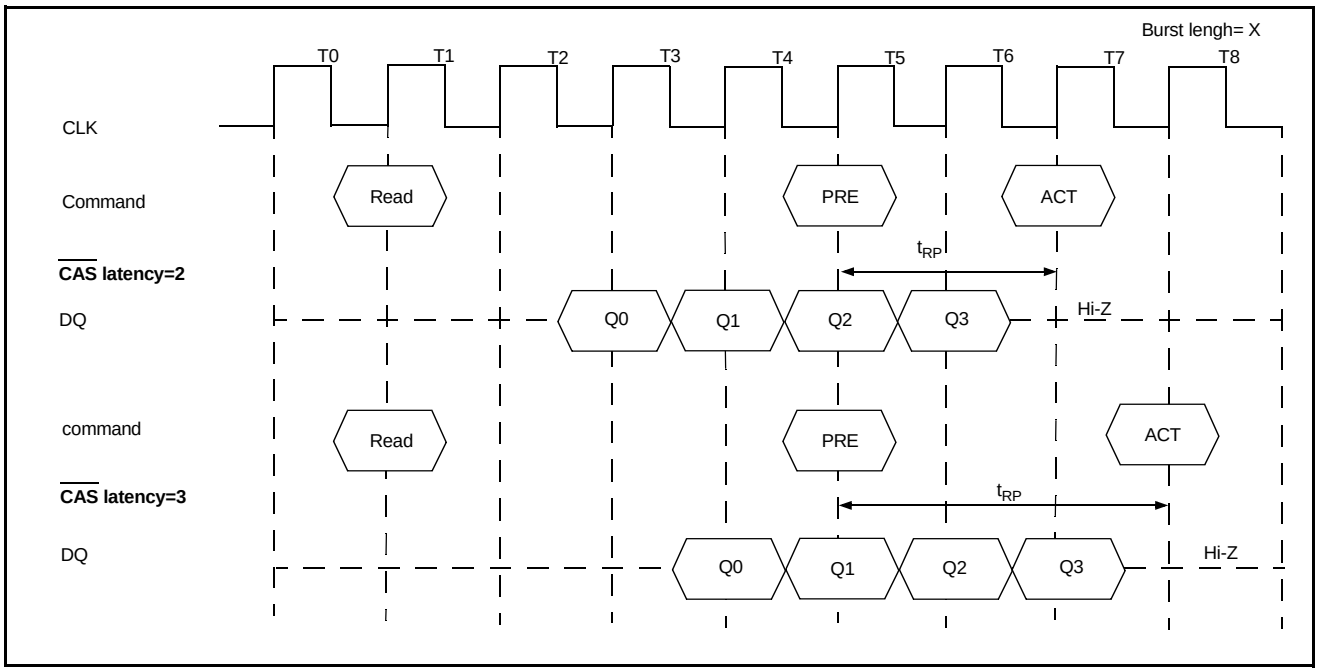
When the precharge command is issued, the burst read operation is terminated and precharge starts.

The same bank can be activated again after t_{RP} from the precharge command.

When CAS latency is 2, the read data will remain valid until one clock after the precharge command.

When CAS latency is 3, the read data will remain valid until two clocks after the precharge command.

Precharge Termination in READ Cycle



10.2.2 Precharge Termination in WRITE Cycle

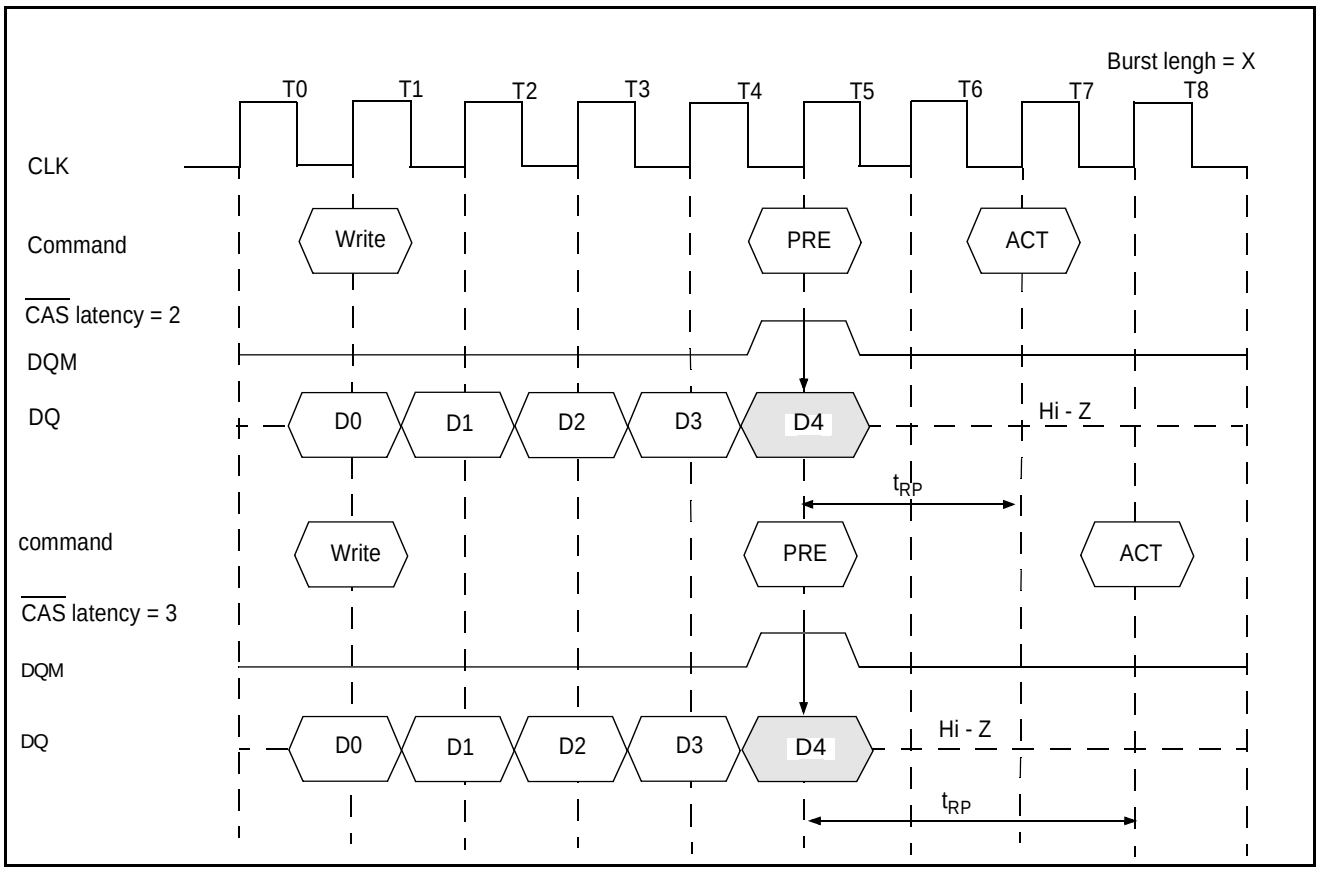
During WRITE cycle, the burst write operation is terminated by a precharge command.

When the precharge command is issued, the burst write operation is terminated and precharge starts.

The same bank can be activated again after t_{RP} from the precharge command. The DQM must be high to mask invalid data in.

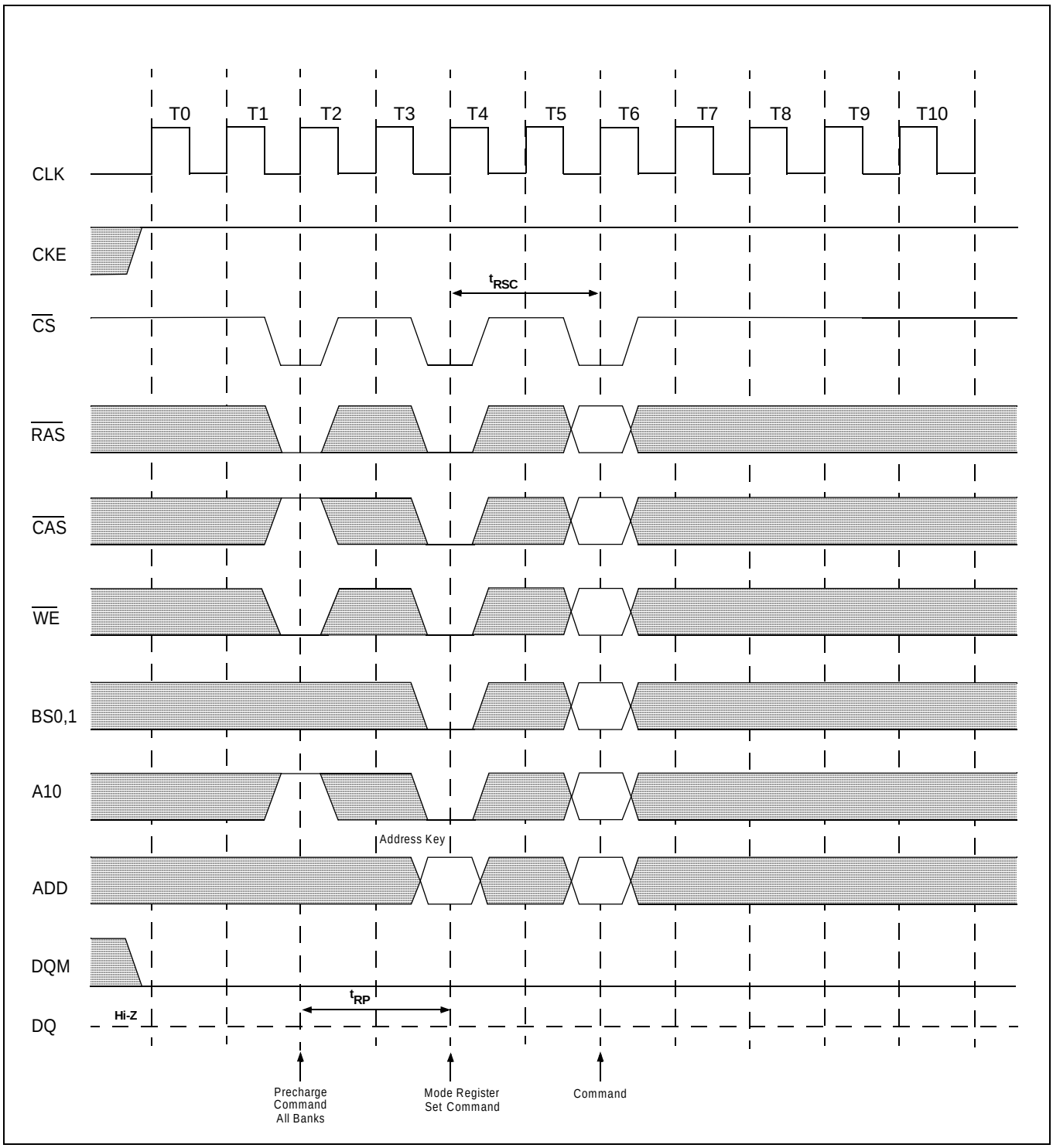
During WRITE cycle, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.

PRECHARGE TERMINATION in WRITE Cycle

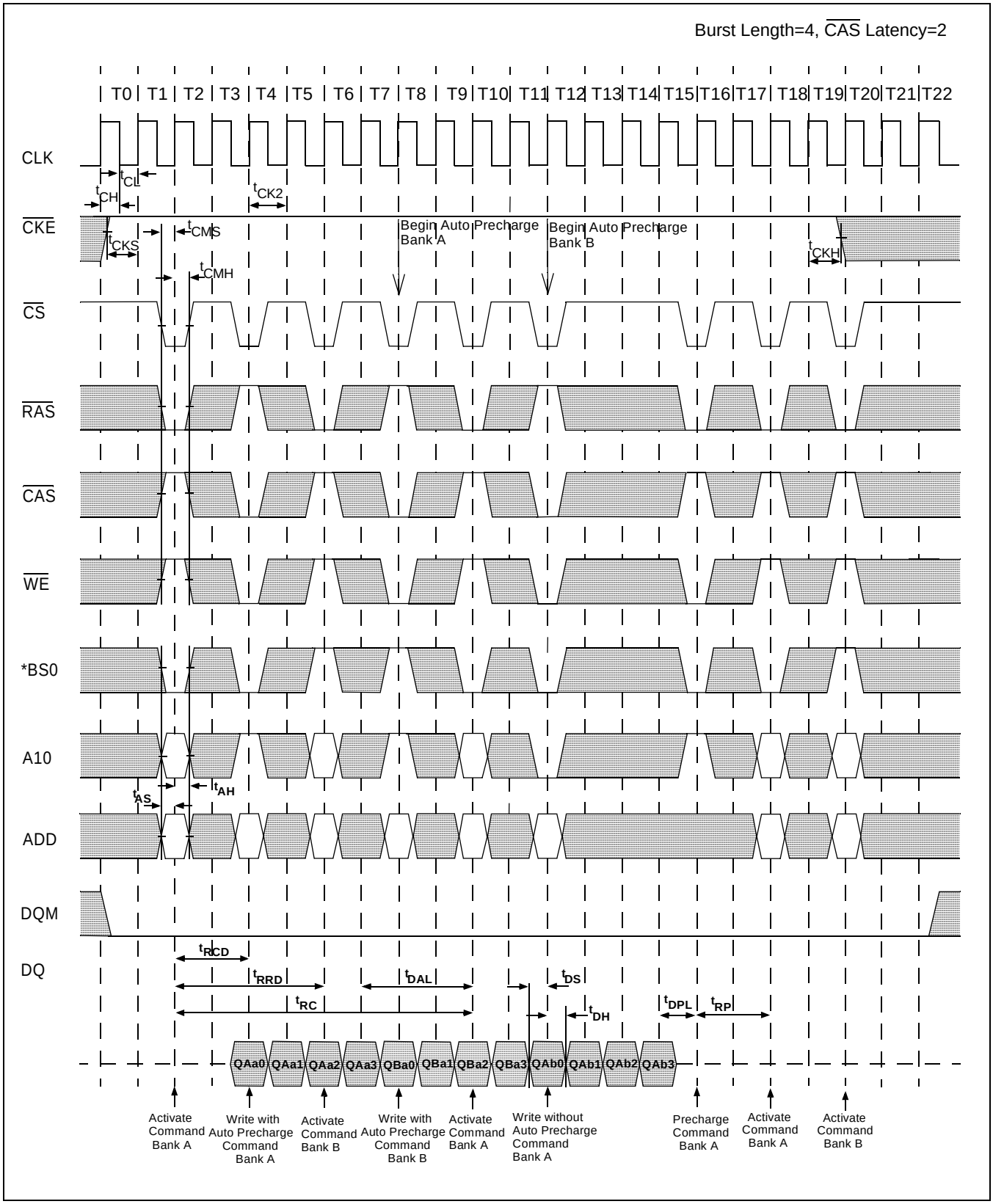


Timing Diagram

Mode Register Set

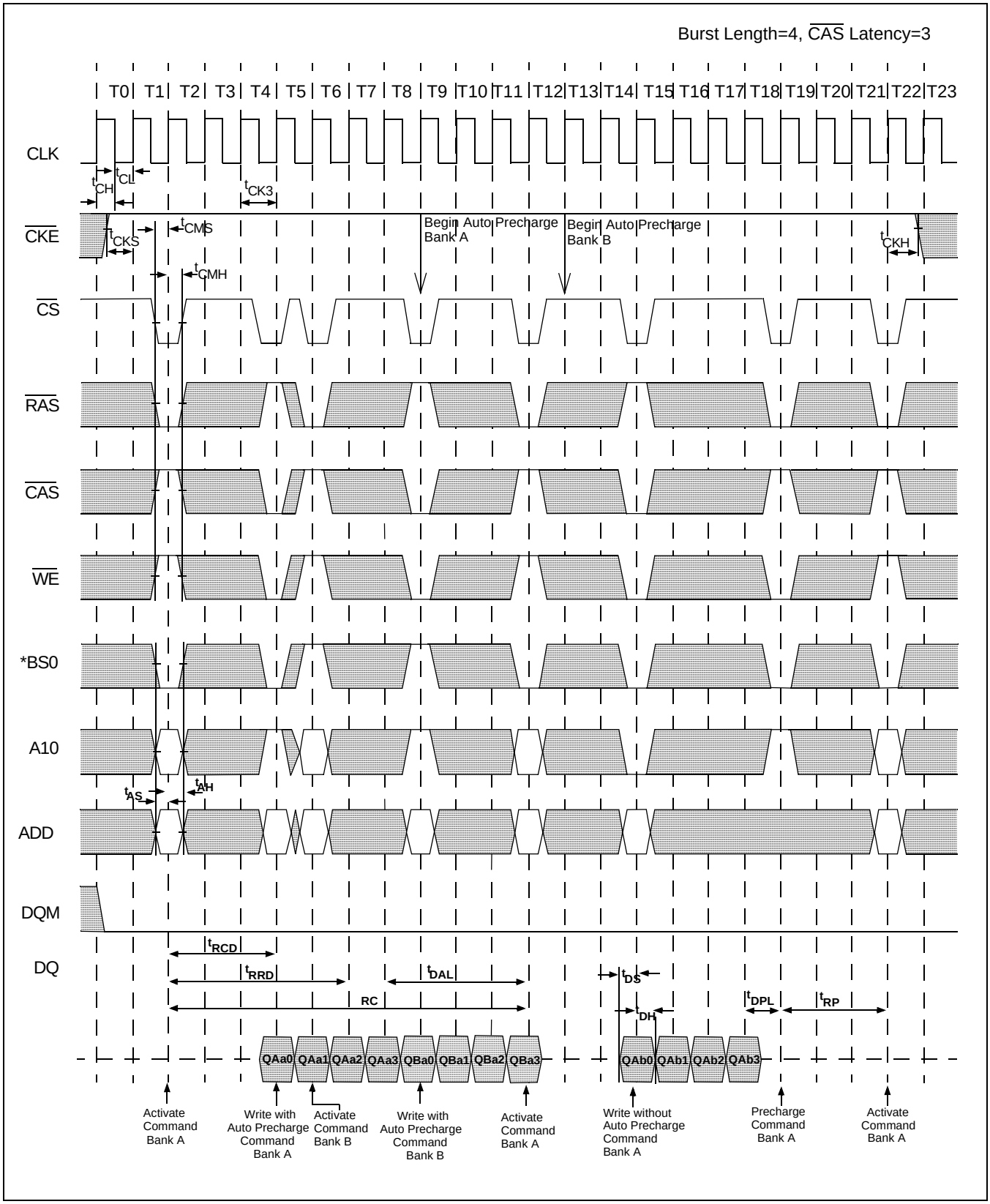


AC Parameters for Write Timing (1 of 2)



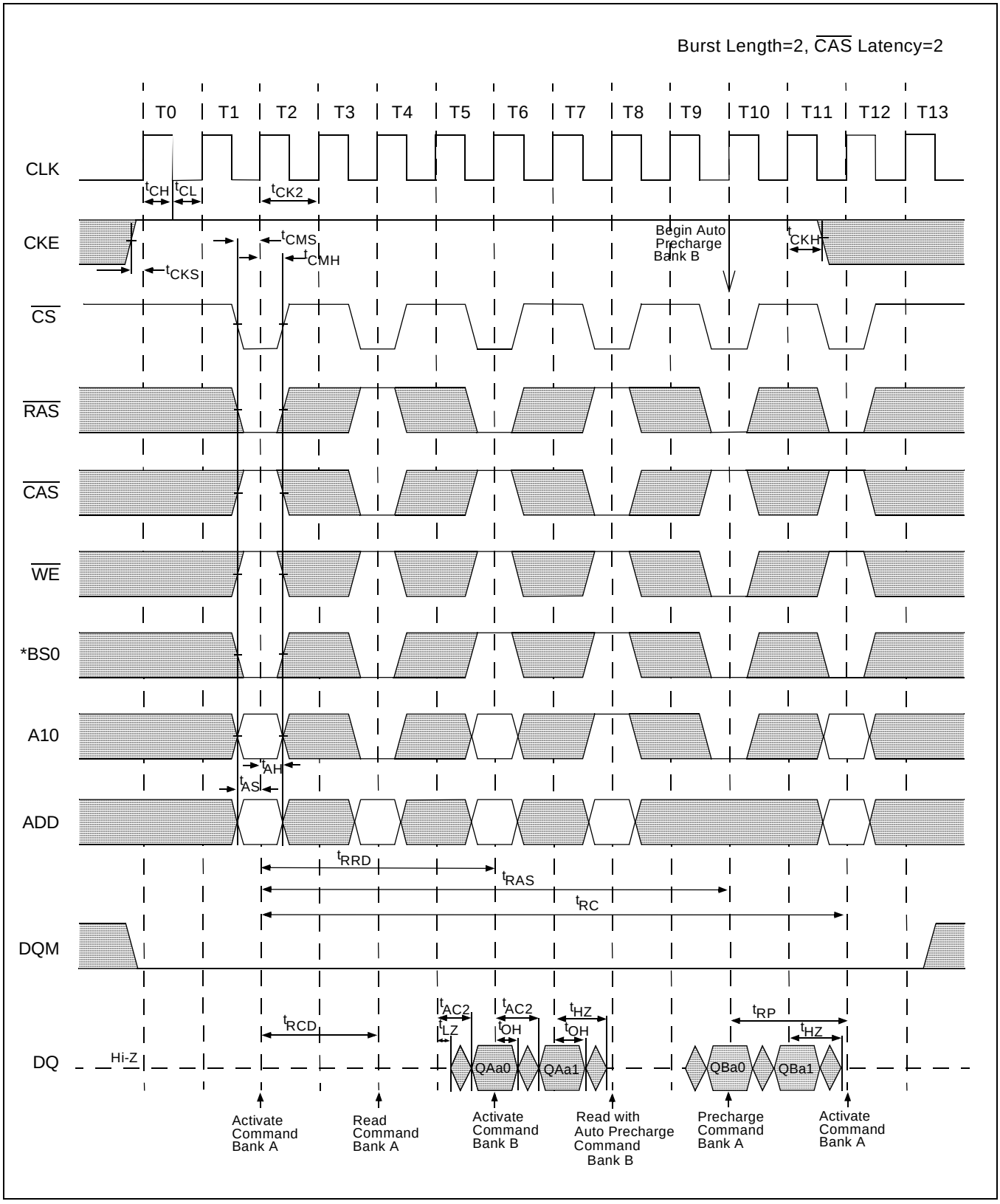
* BS1="L", Bank C,D = Idle

AC Parameters for Write Timing (2 of 2)



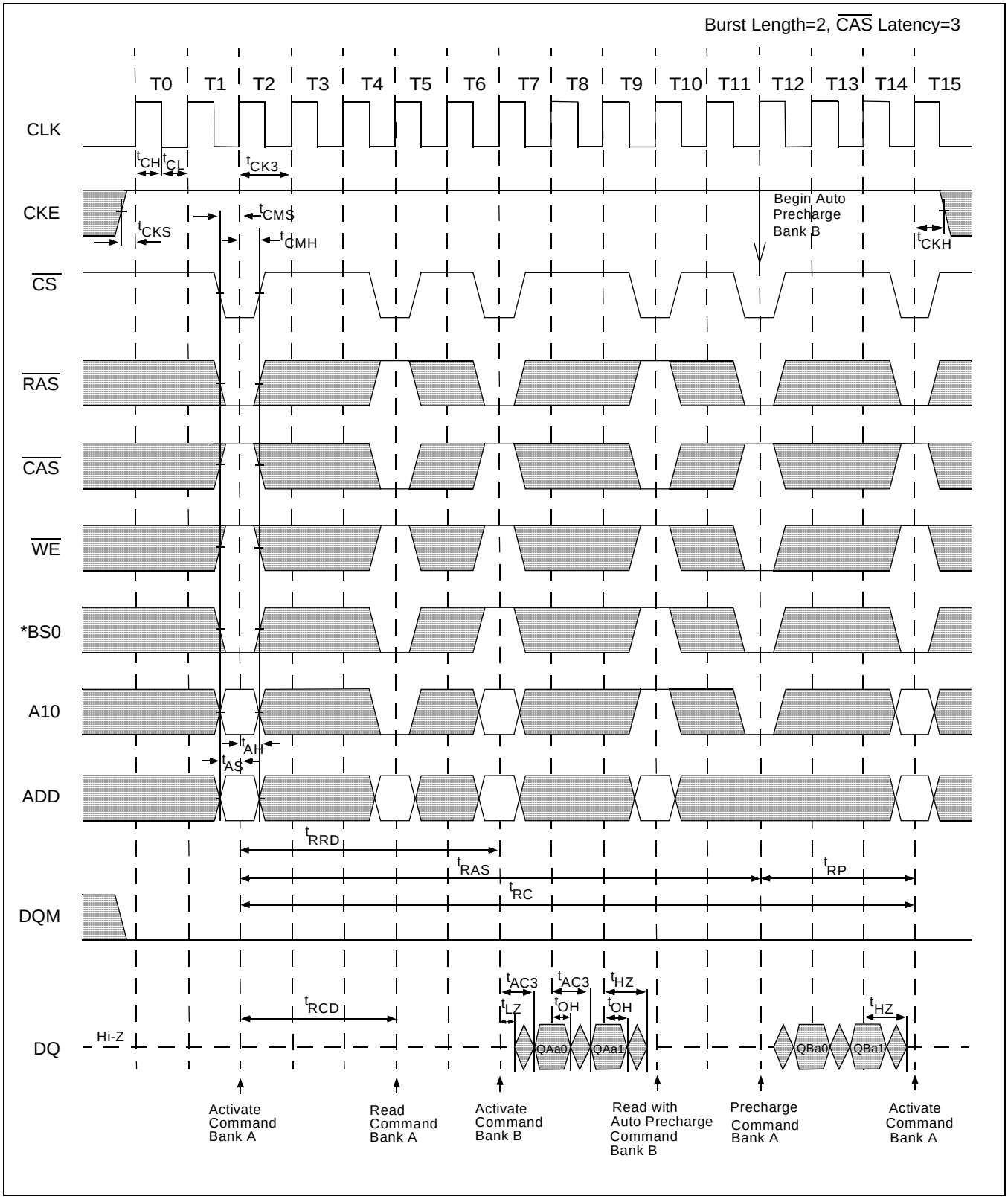
* BS1="L", Bank C,D = Idle

AC Parameters for Read Timing (1 of 2)



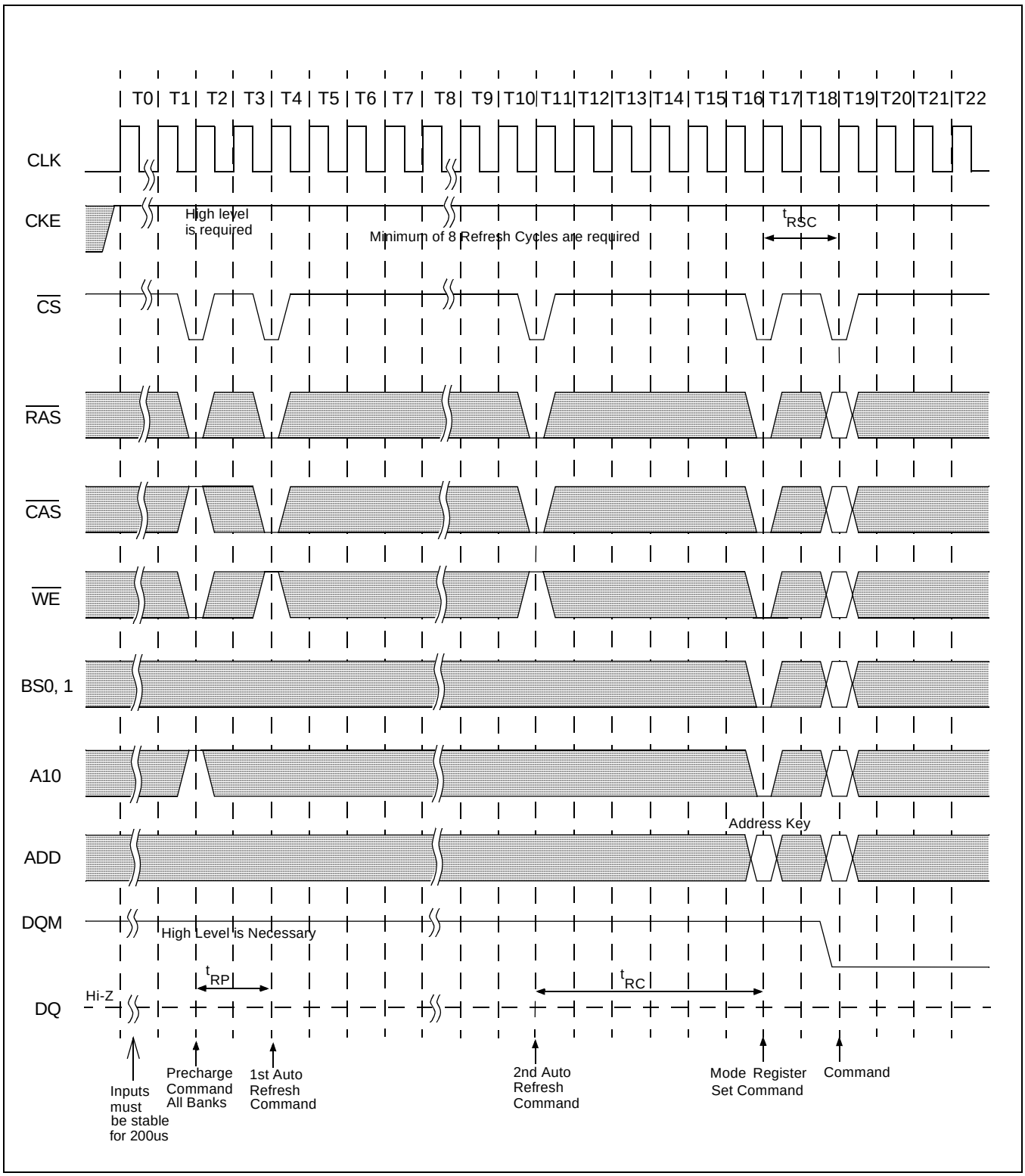
* BS1="L", Bank C,D = Idle

AC Parameters for Read Timing (2 of 2)

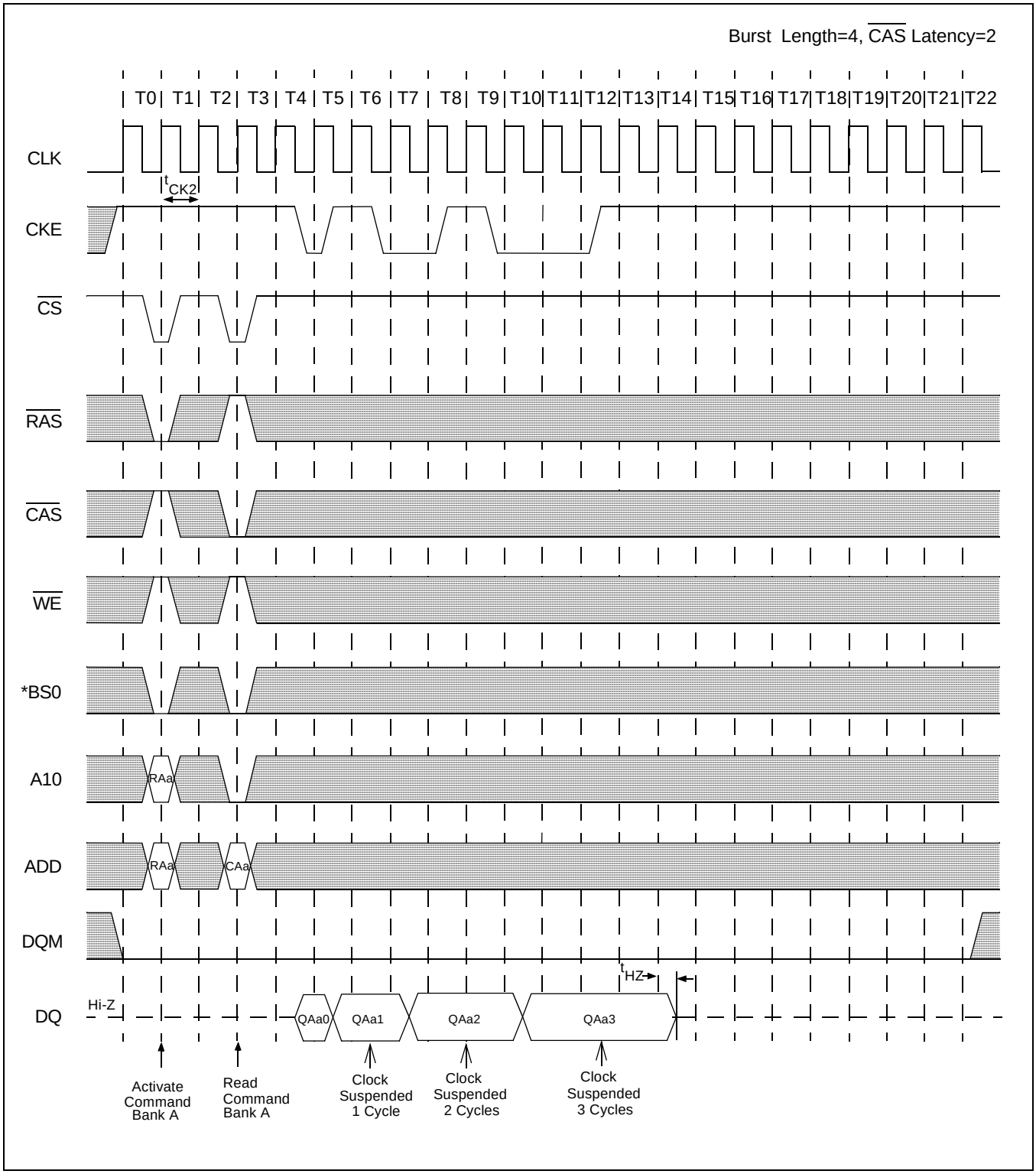


* BS1="L", Bank C,D = Idle

Power on Sequence and Auto Refresh (CBR)

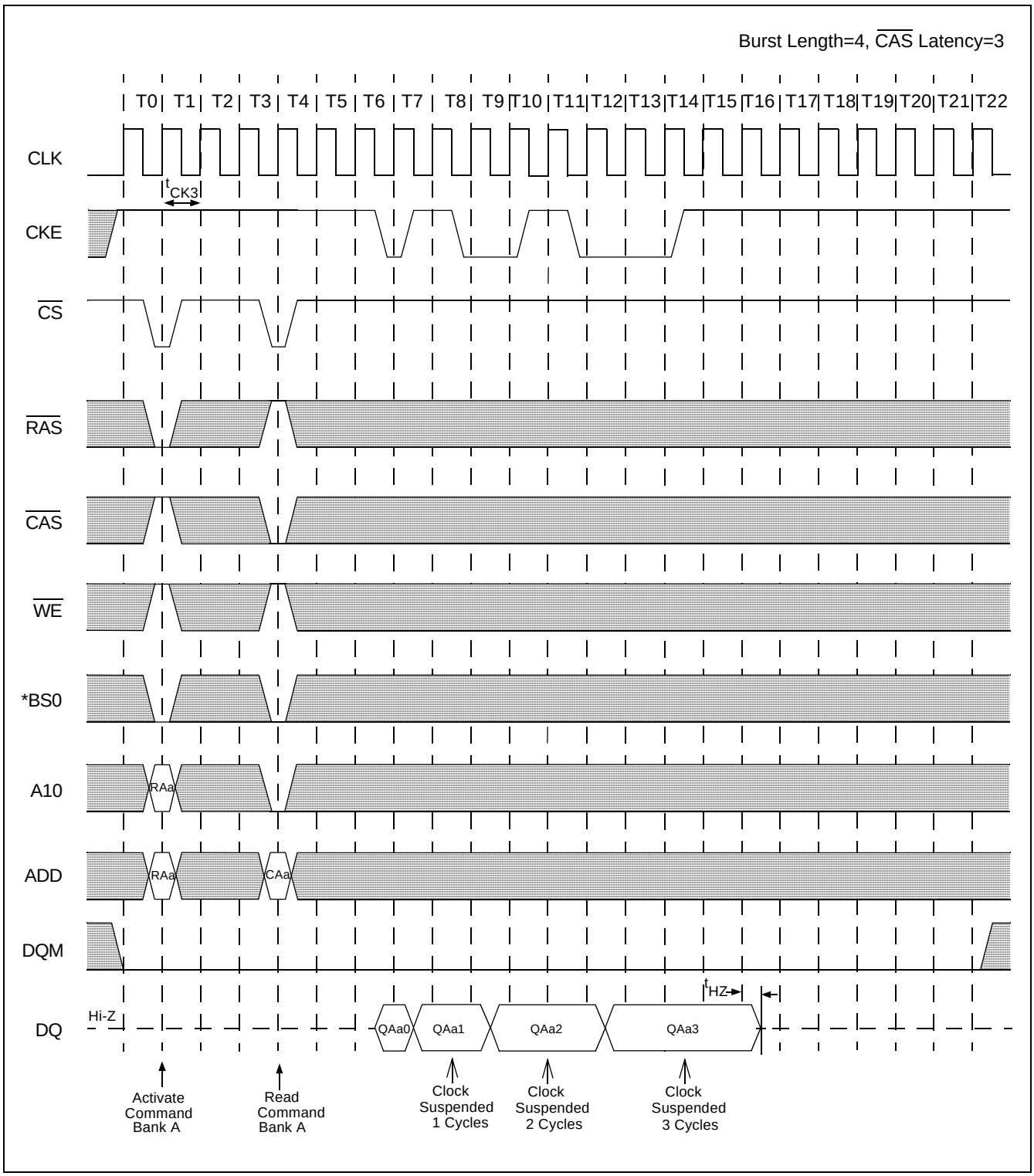


Clock Suspension During Burst Read (Using CKE) (1 of 2)



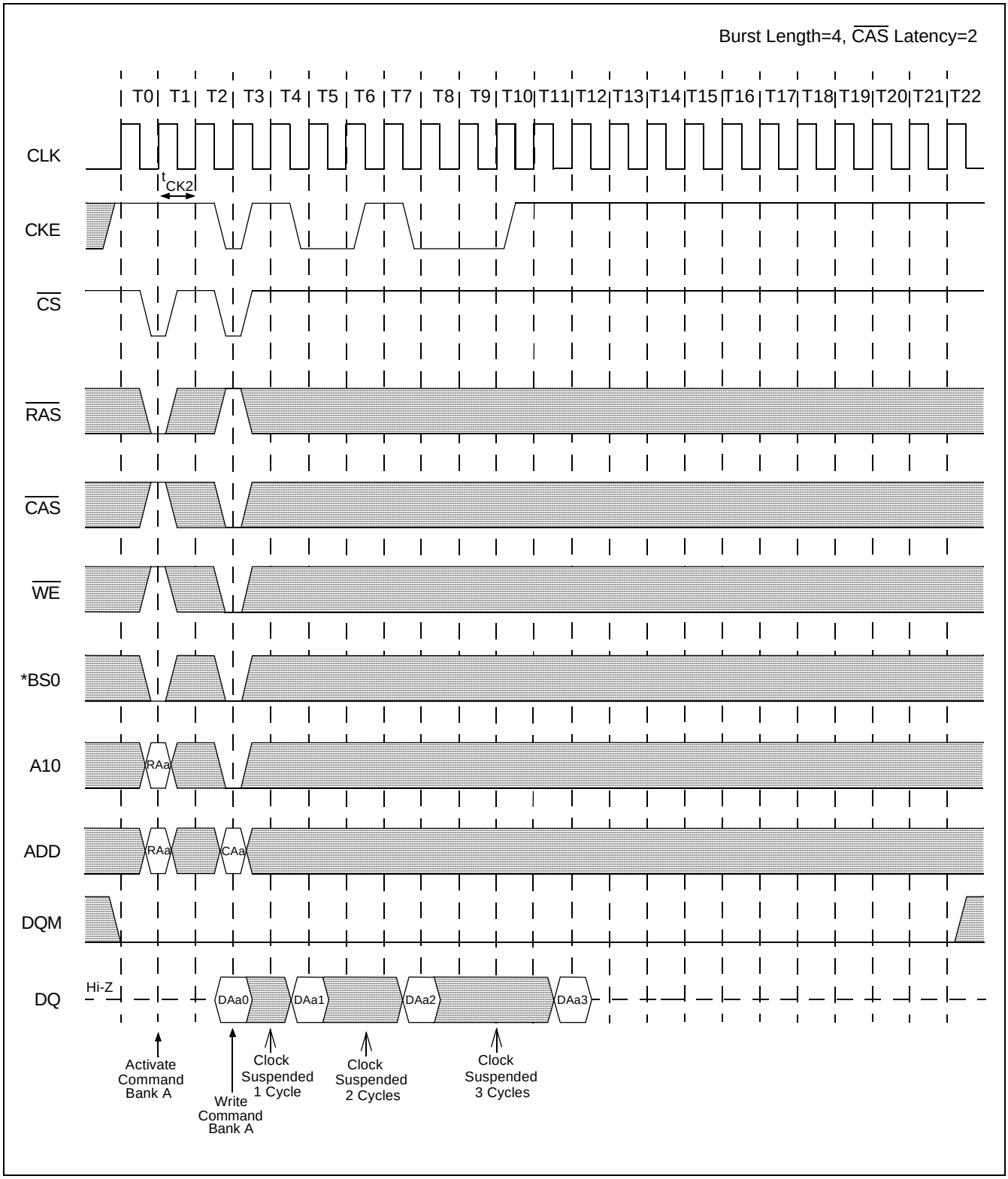
* BS1="L", Bank C,D = Idle

Clock Suspension During Burst Read (Using CKE) (2 of 2)



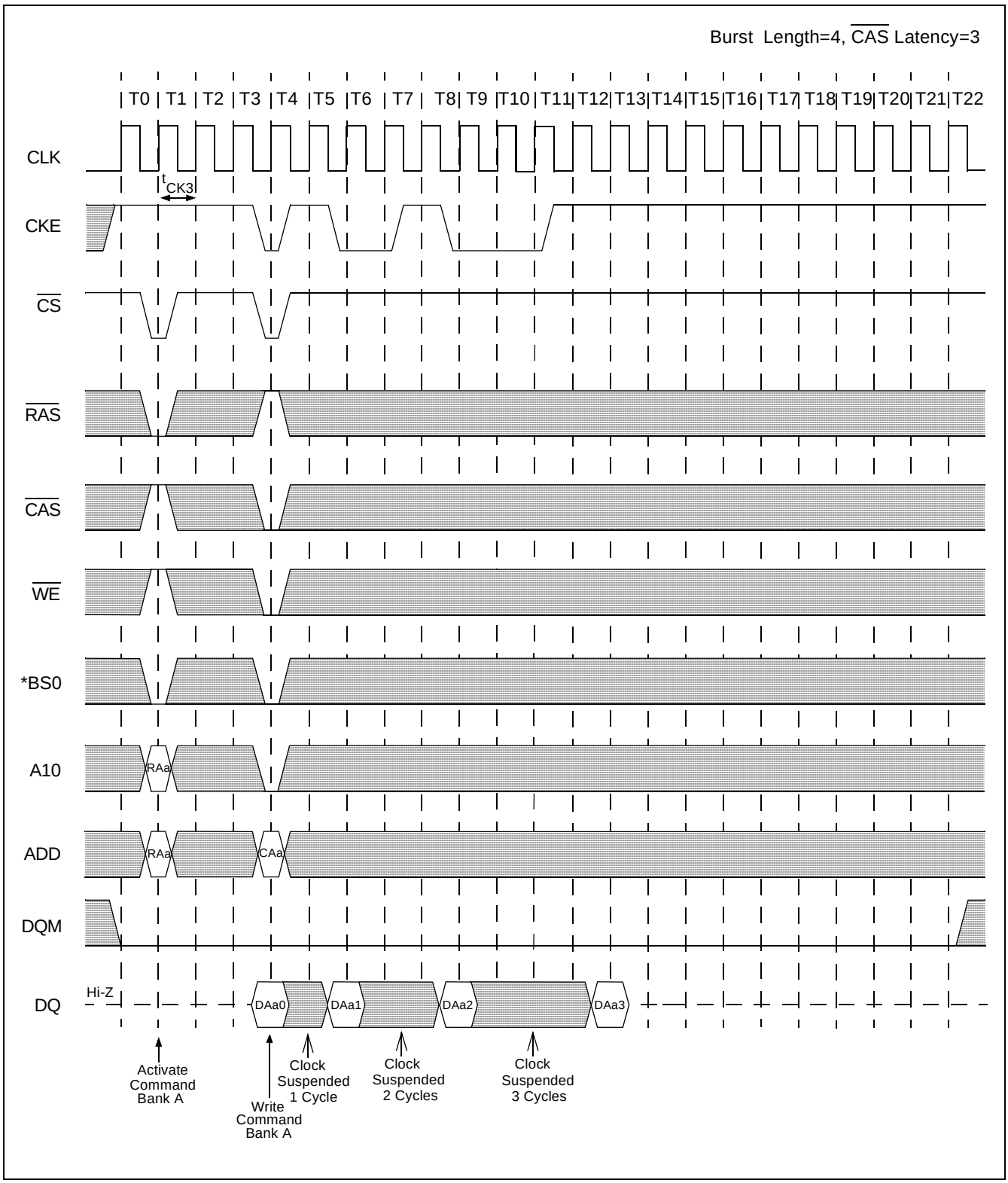
* BS1="L", Bank C,D = Idle

Clock Suspension During Burst Write (Using CKE) (1 of 2)



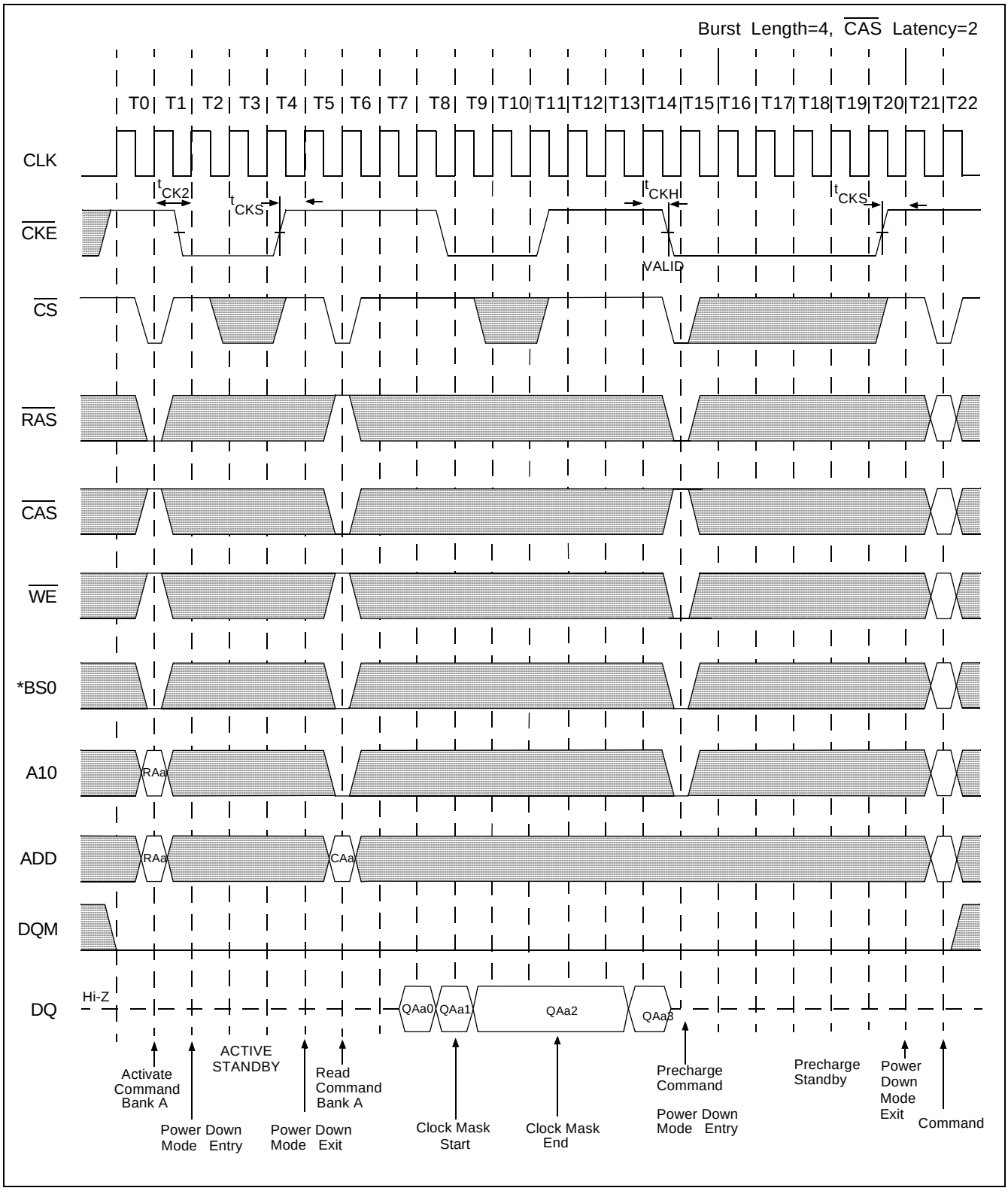
* BS1="L", Bank C,D = Idle

Clock Suspension During Burst Write (Using CKE) (2 of 2)



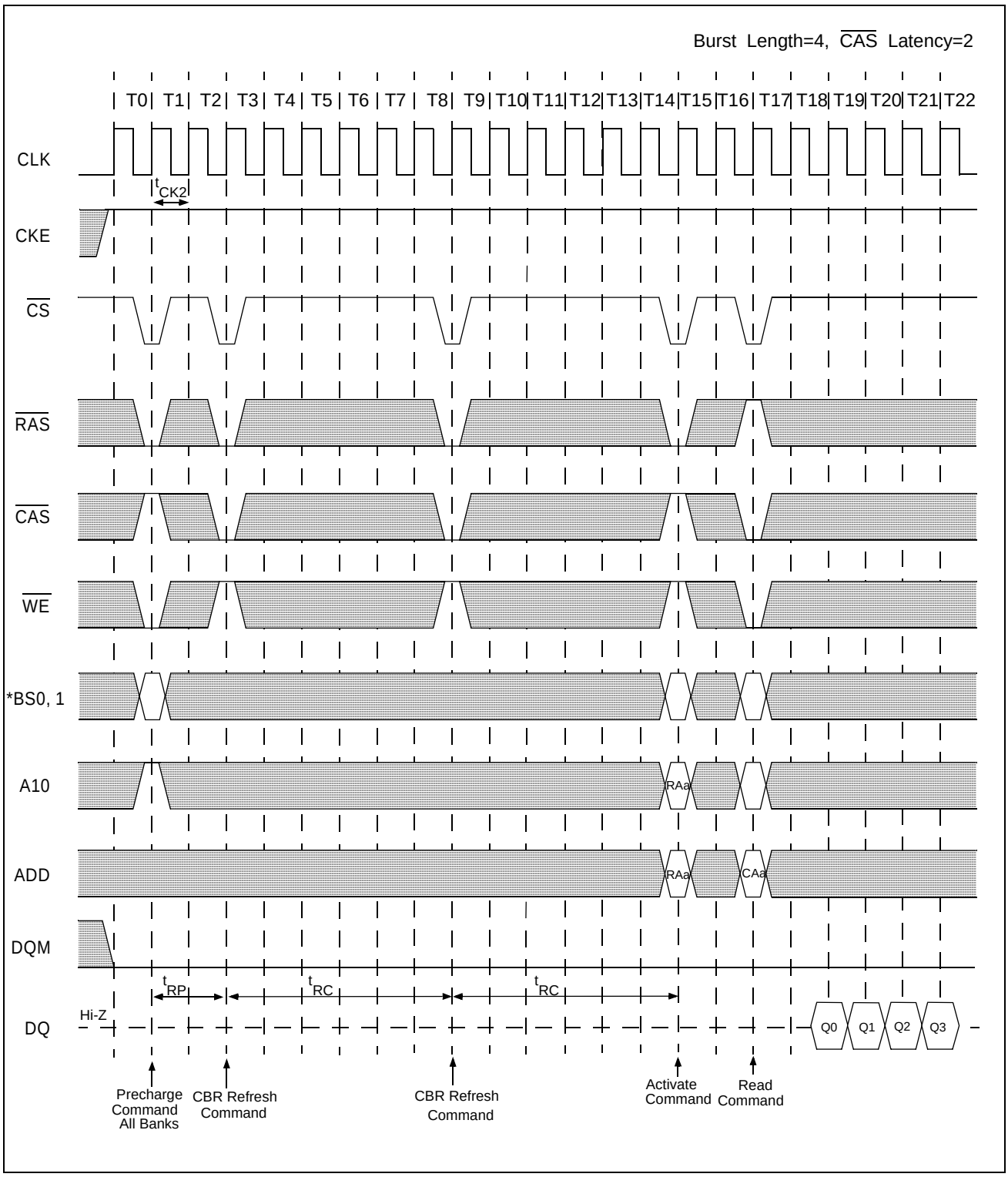
* BS1="L", Bank C,D = Idle

Power Down Mode and Clock Mask



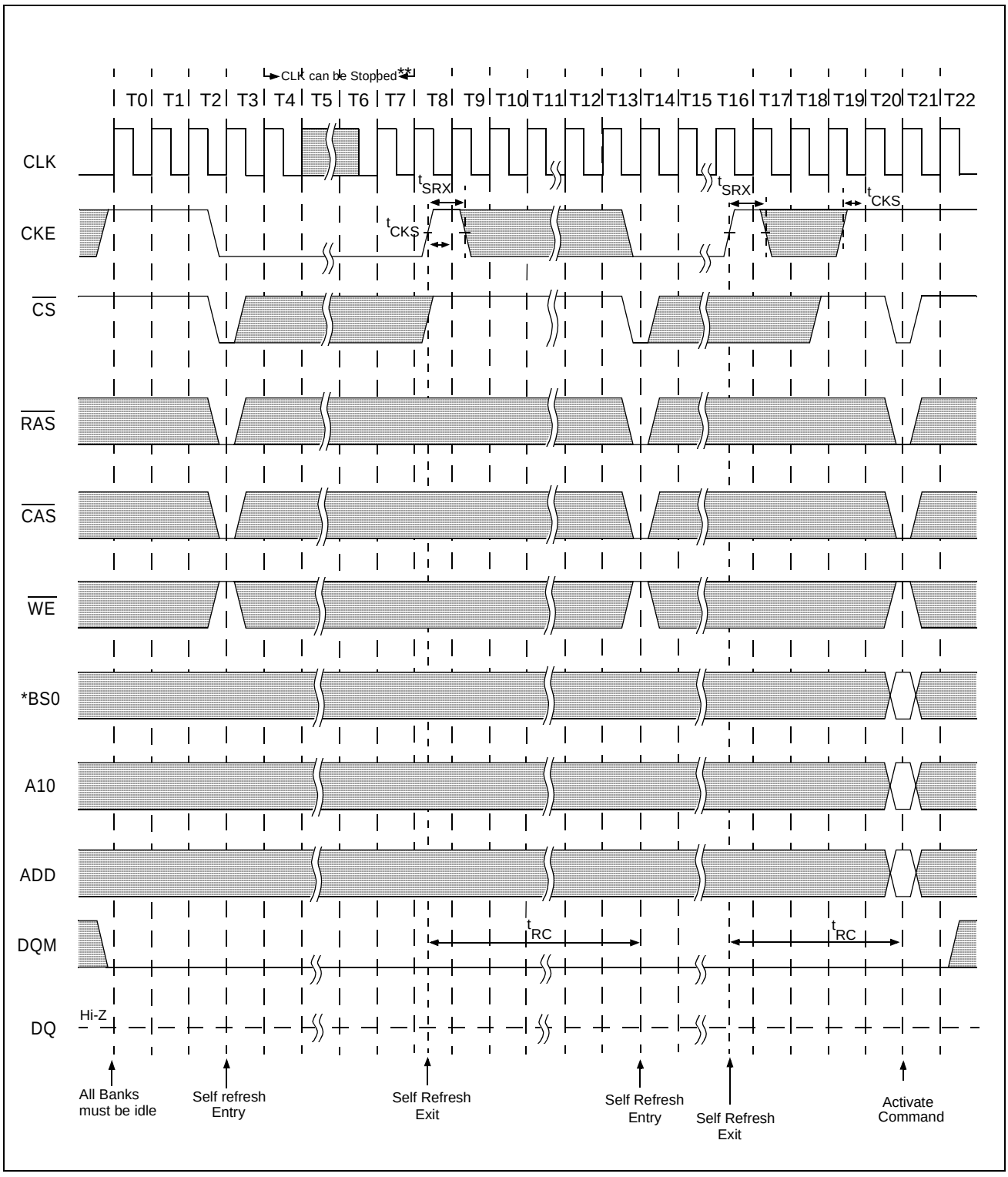
* BS1="L", Bank C,D = Idle

Auto Refresh (CBR)



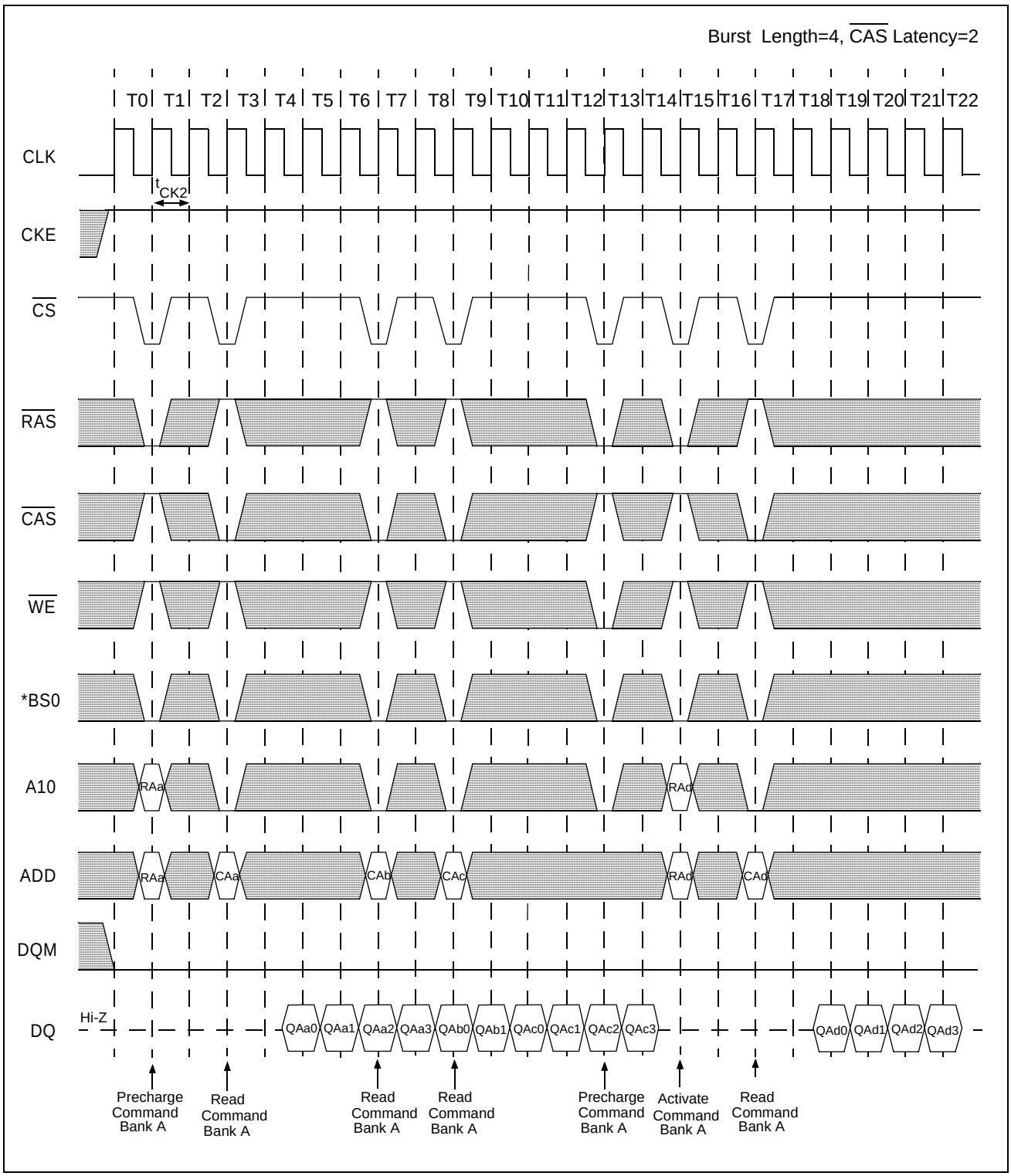
* BS1="L", Bank C,D = Idle

Self Refresh (Entry and Exit)



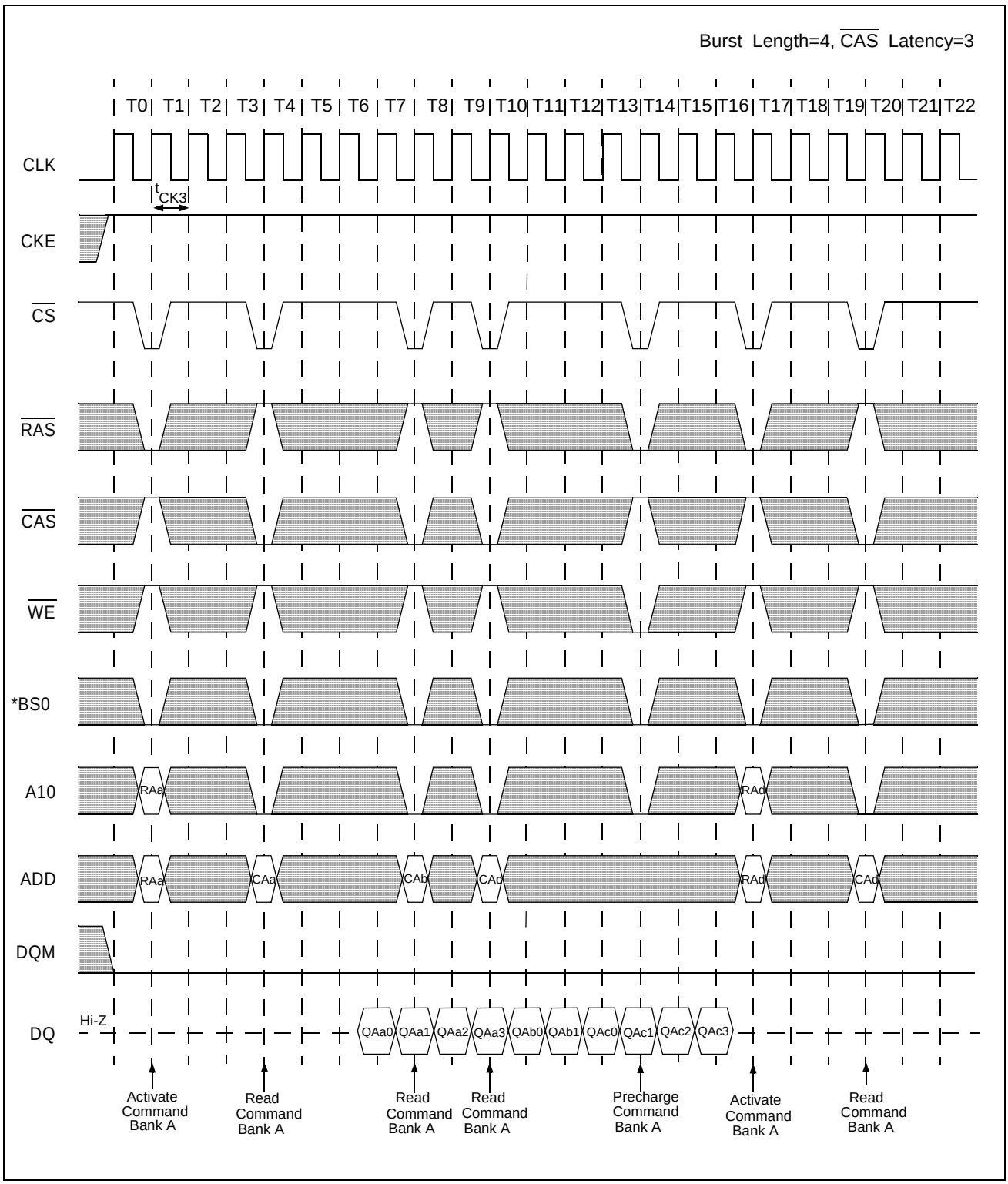
* BS1="L", Bank C,D = Idle
* Clock can be stopped at CKE=Low. If clock is stopped, it must be restarted/stable for 4 clock cycles before CKE=High

Random Column Read (Page With Same Bank) (1 of 2)



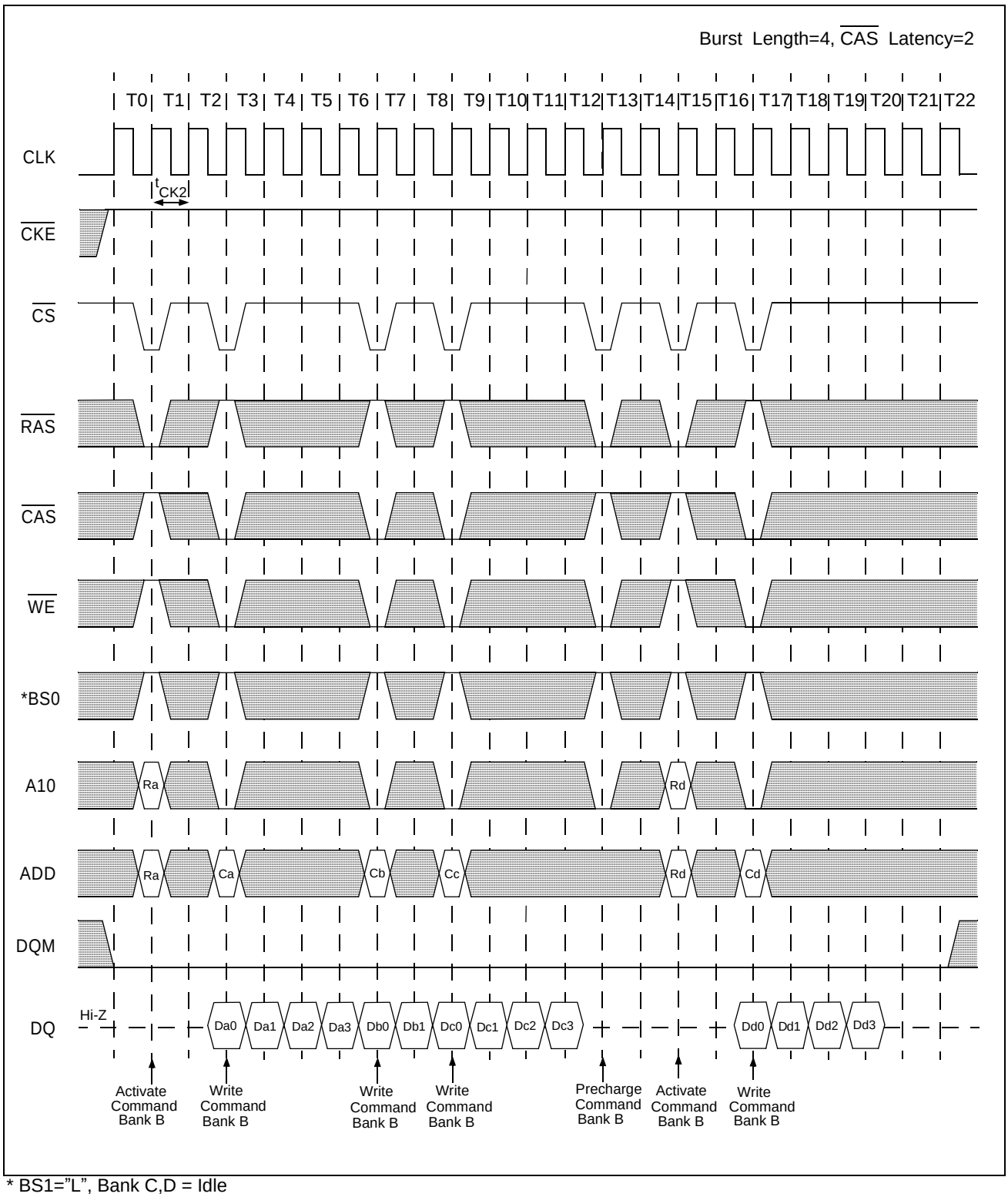
* BS1="L", Bank C,D = Idle

Random Column Read (Page With Same Bank) (2 of 2)



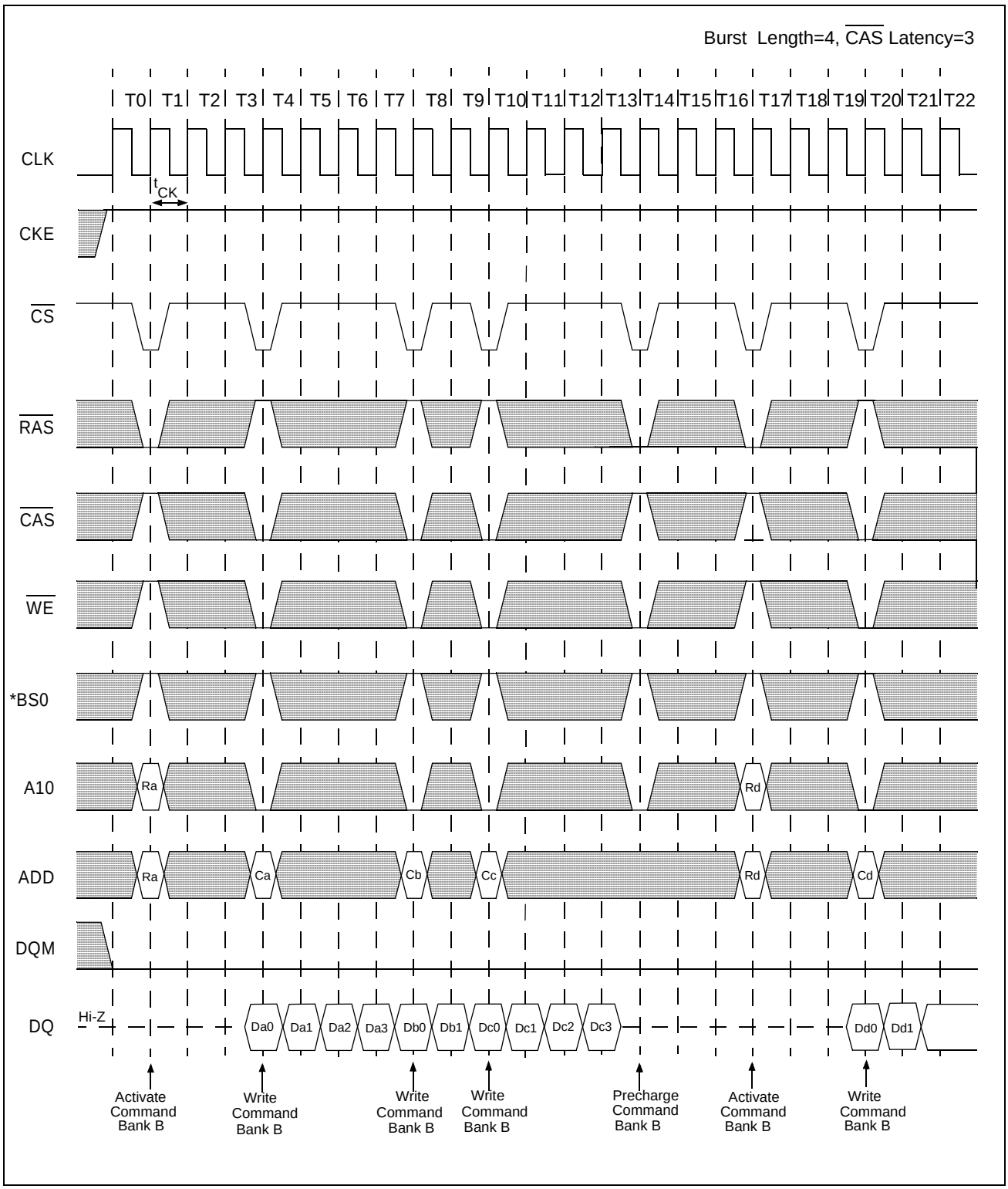
* BS1="L", Bank C,D = Idle

Random Column Write (Page With Same Bank) (1 of 2)



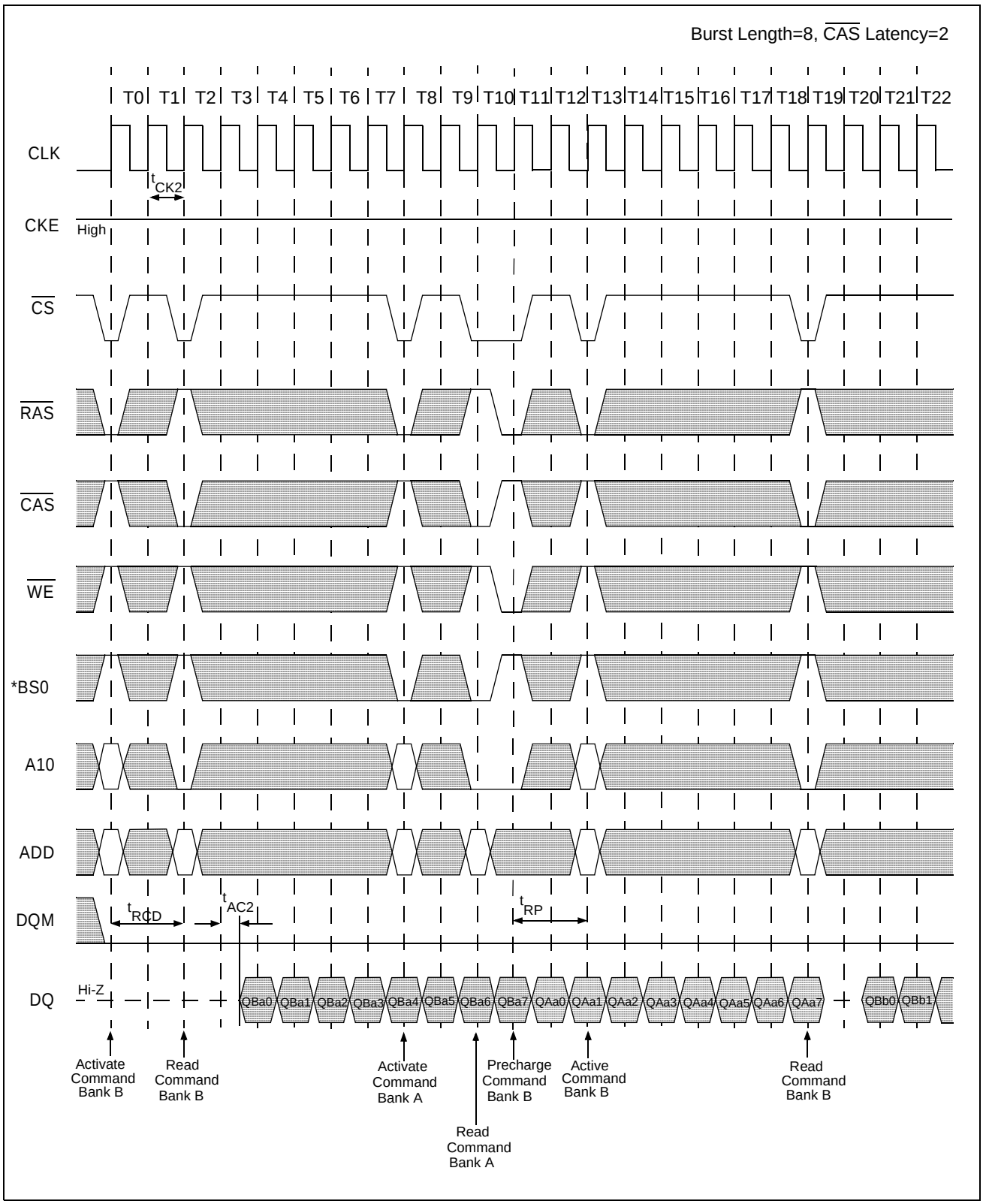
* BS1="L", Bank C,D = Idle

Random Column Write (Page With Same Bank) (1 of 2)



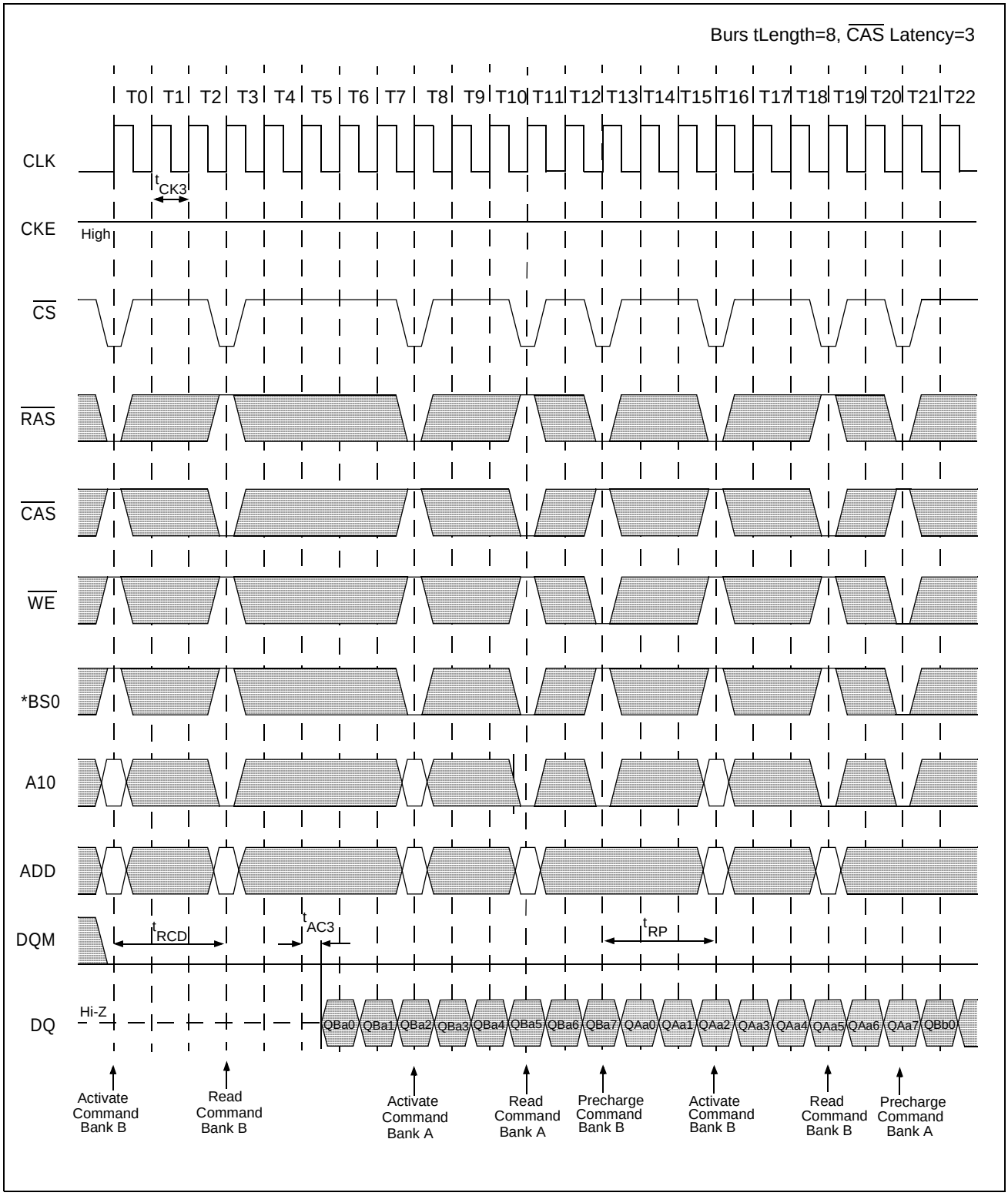
* BS1="L", Bank C,D = Idle

Random Row Read (Interleaving Banks) (1 of 2)



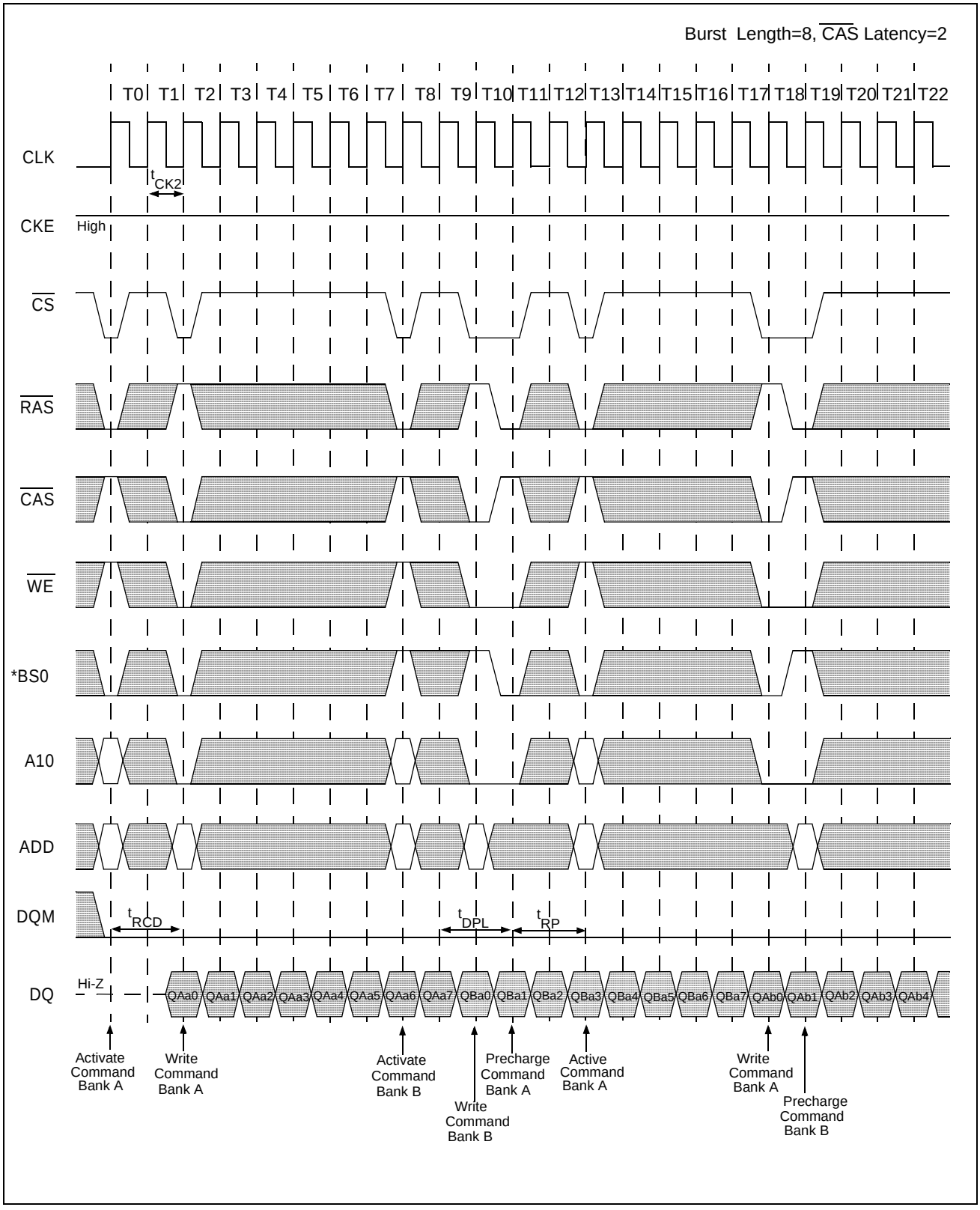
* BS1="L", Bank C,D = Idle

Random Row Read (Interleaving Banks) (2 of 2)



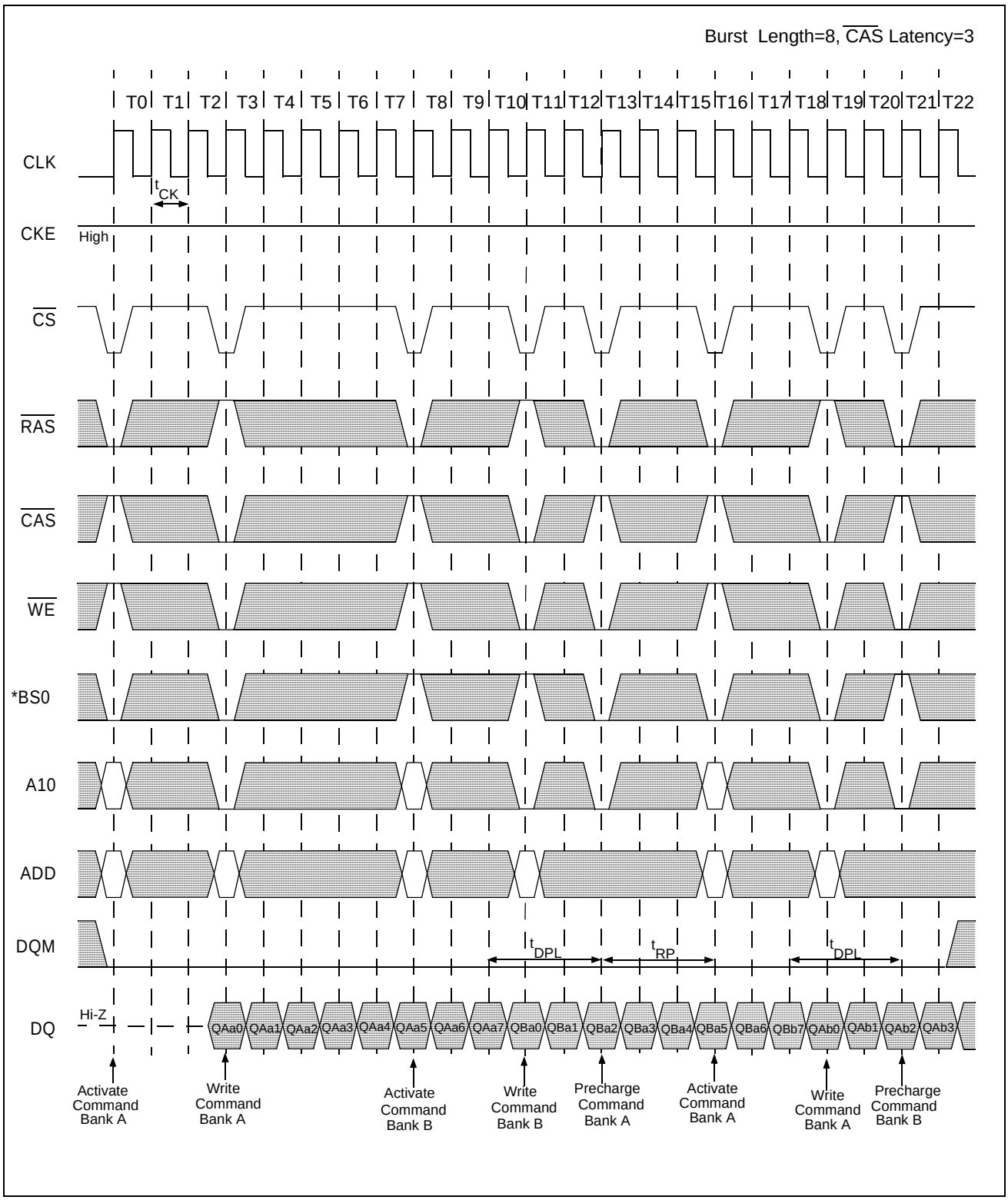
* BS1="L", Bank C,D = Idle

Random Row Write (Interleaving Banks) (1 of 2)



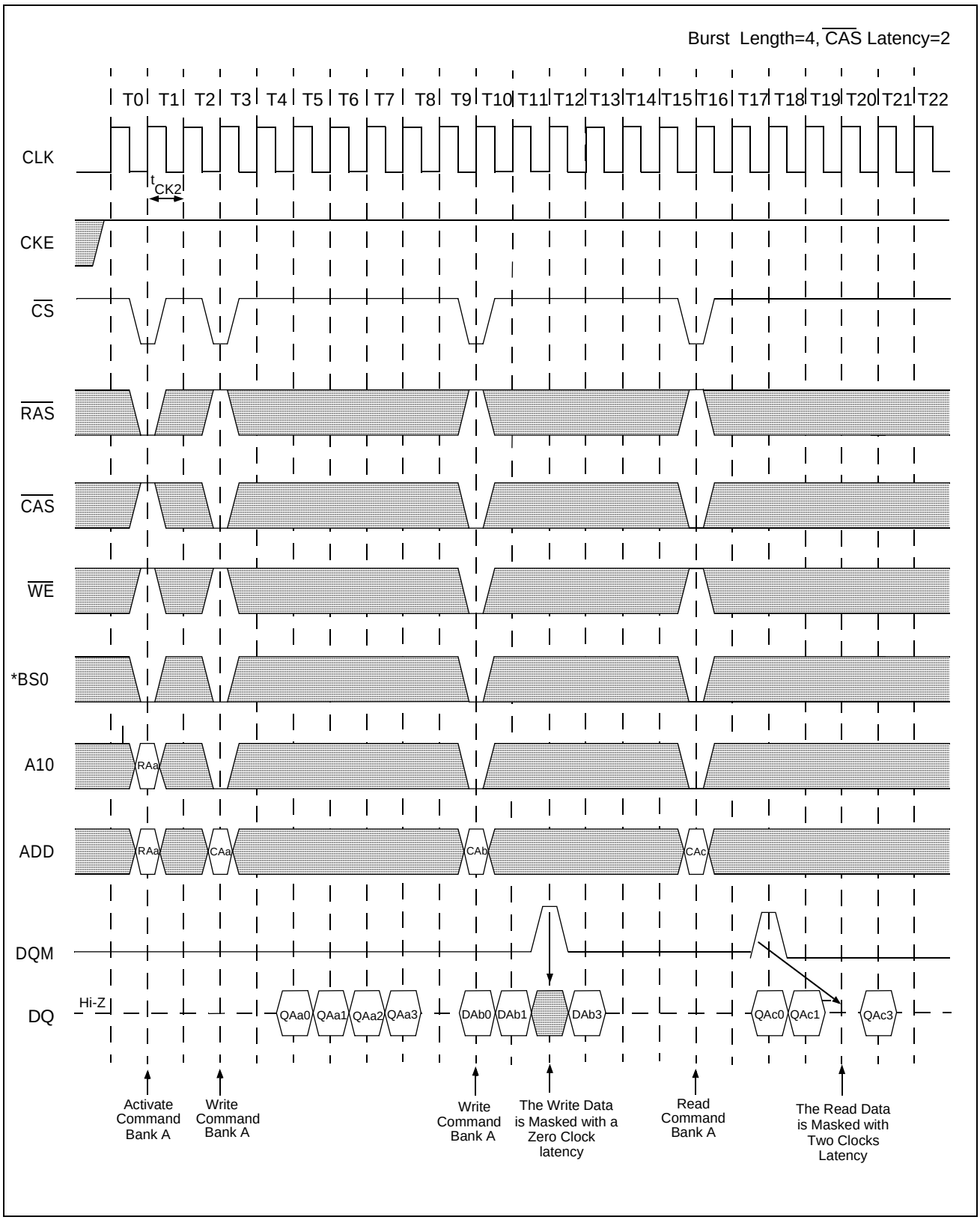
* BS1="L", Bank C,D = Idle

Random Row Write (Interleaving Banks) (2 of 2)



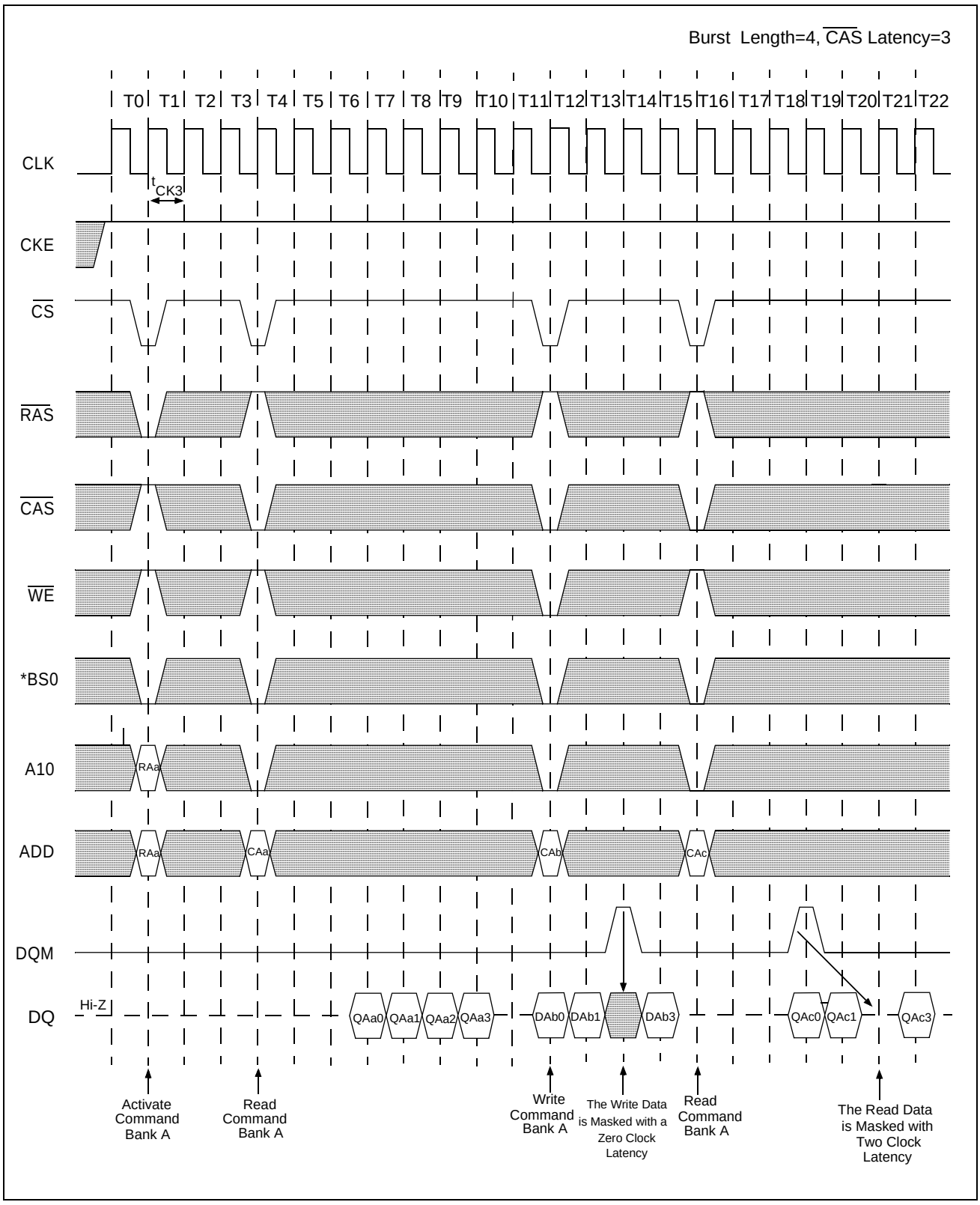
* BS1="L", Bank C,D = Idle

Read and Write Cycle (1 of 2)



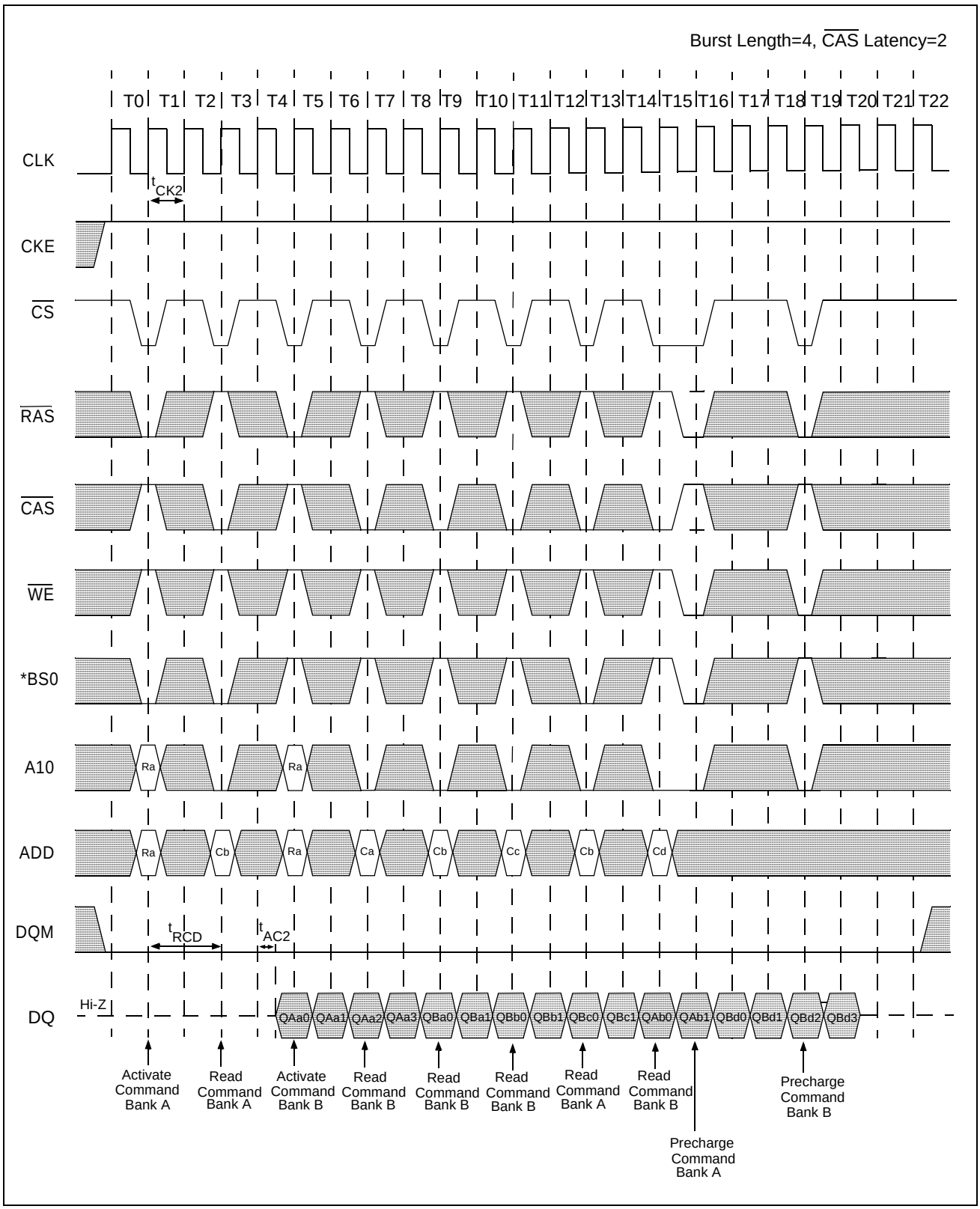
* BS1="L", Bank C,D = Idle

Read and Write Cycle (2 of 2)



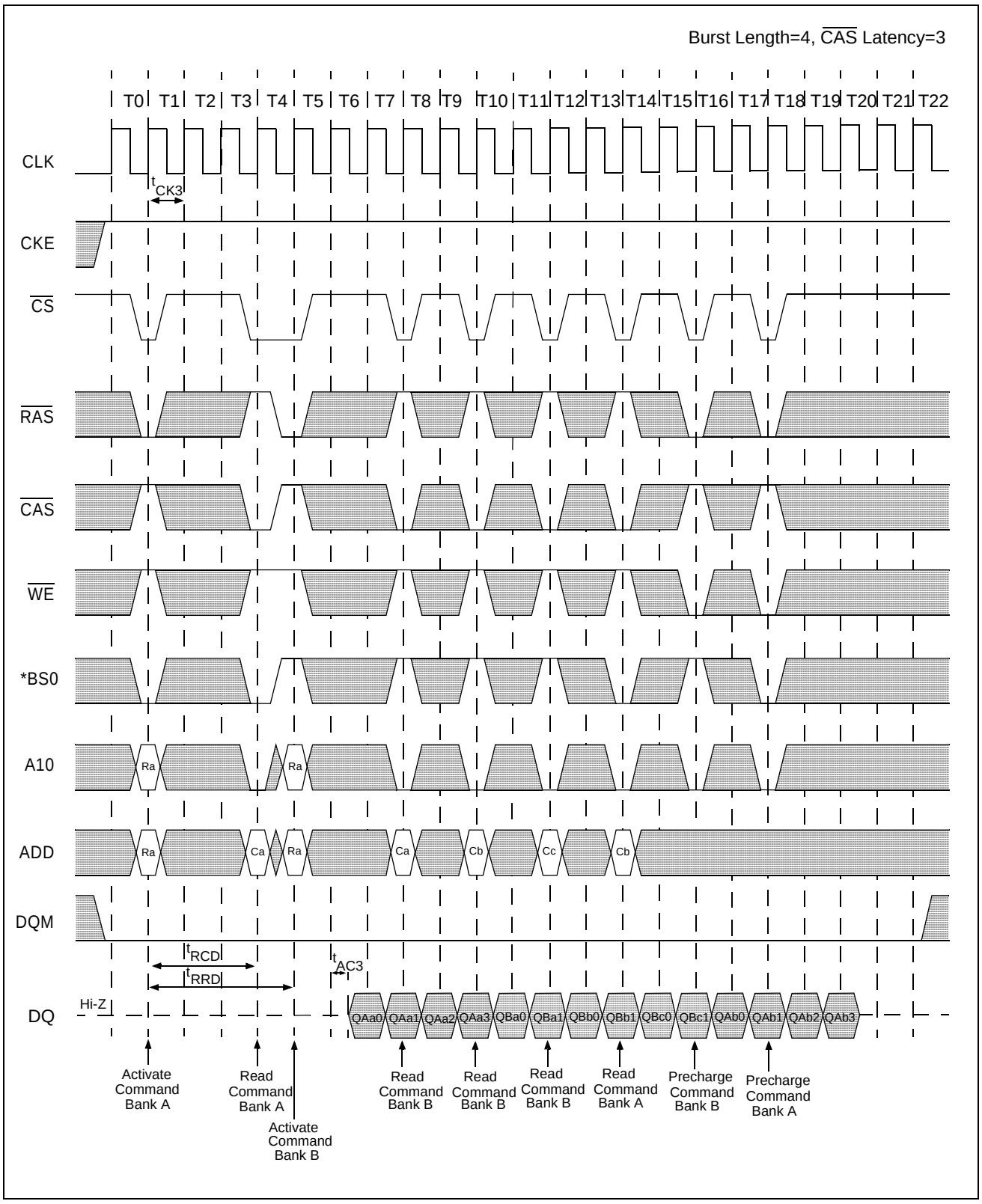
* BS1="L", Bank C,D = Idle

Interleaved Column Read Cycle (1 of 2)



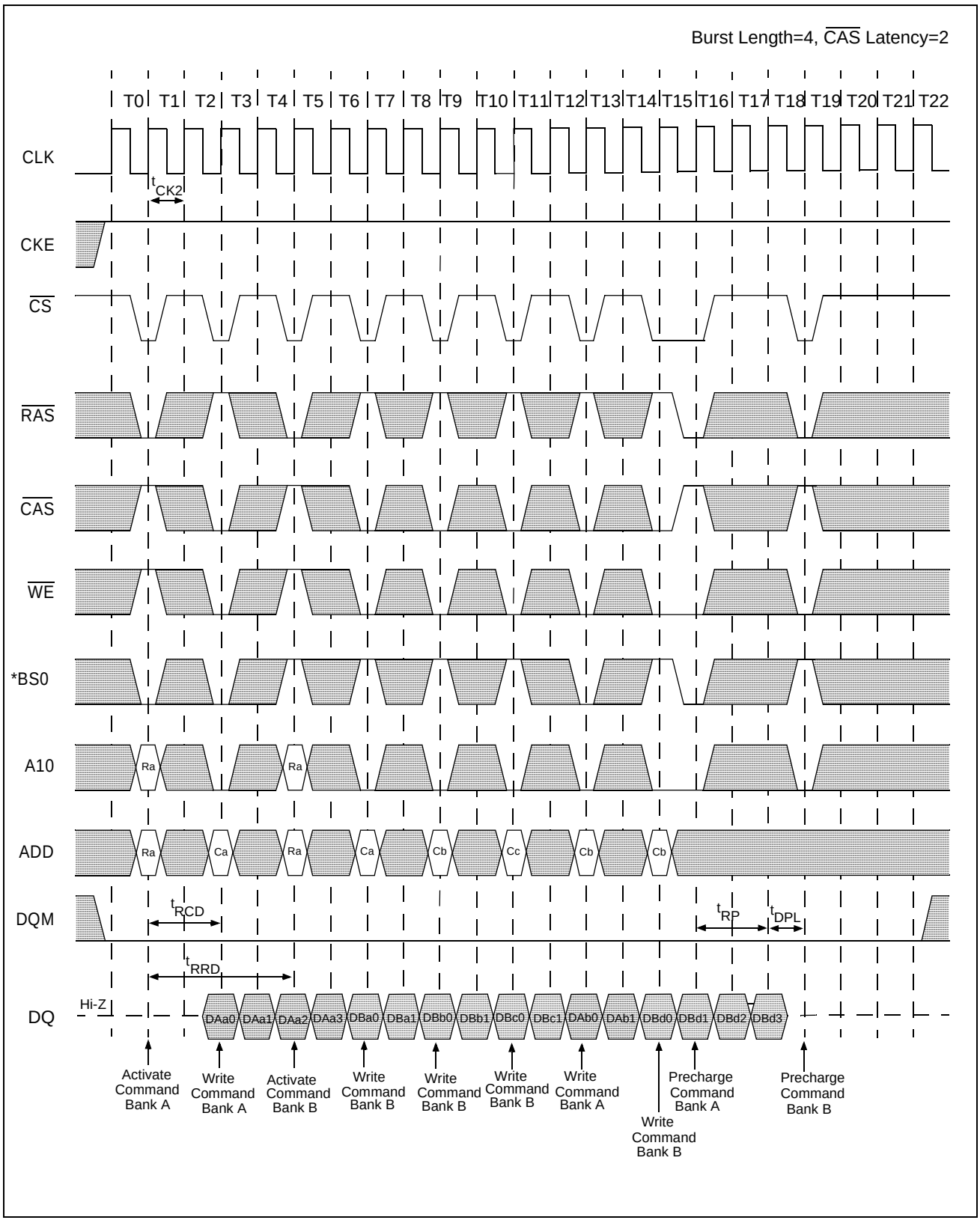
* BS1="L", Bank C,D = Idle

Interleaved Column Read Cycle (2 of 2)



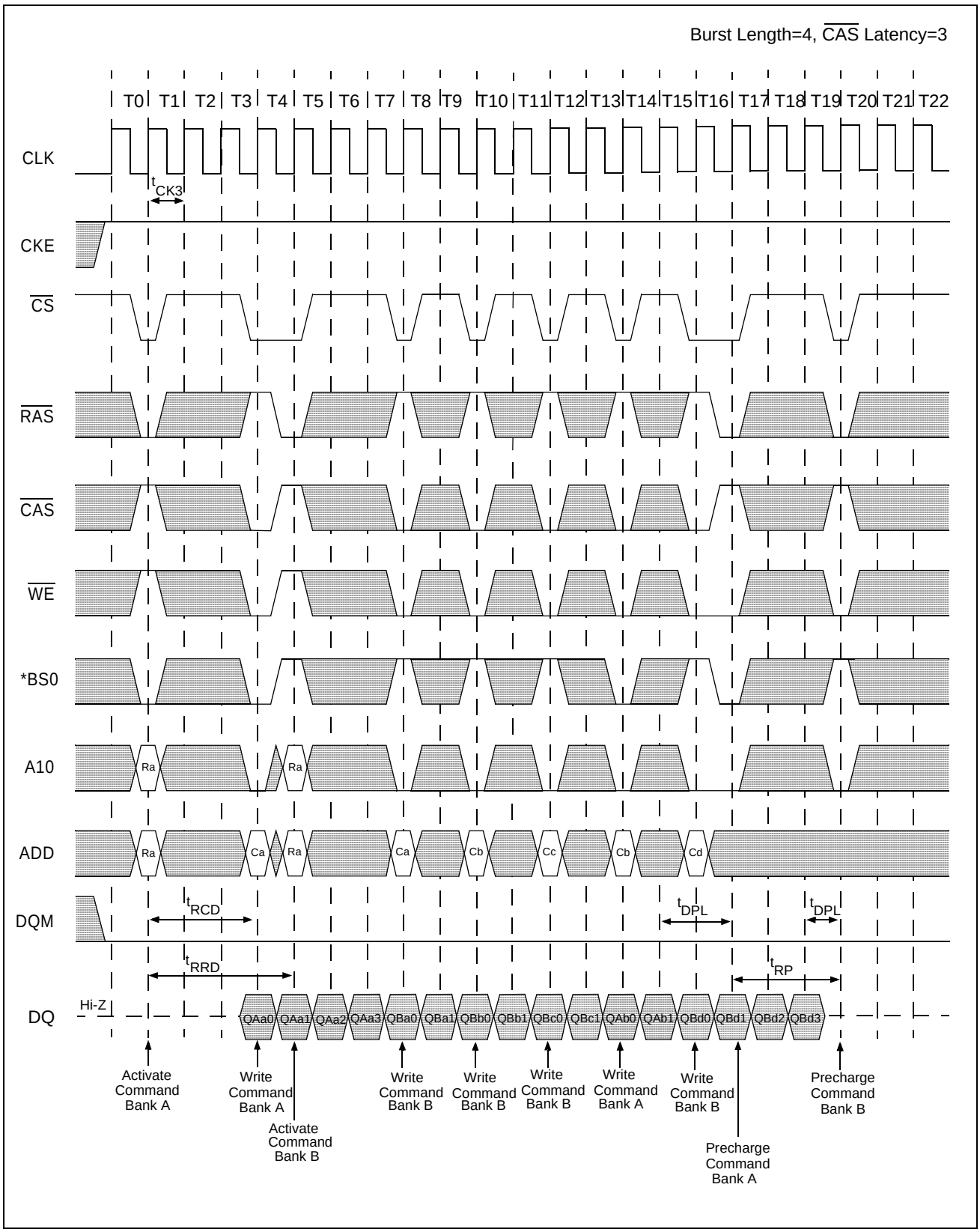
* BS1="L", Bank C,D = Idle

Interleaved Column Write Cycle (1 of 2)



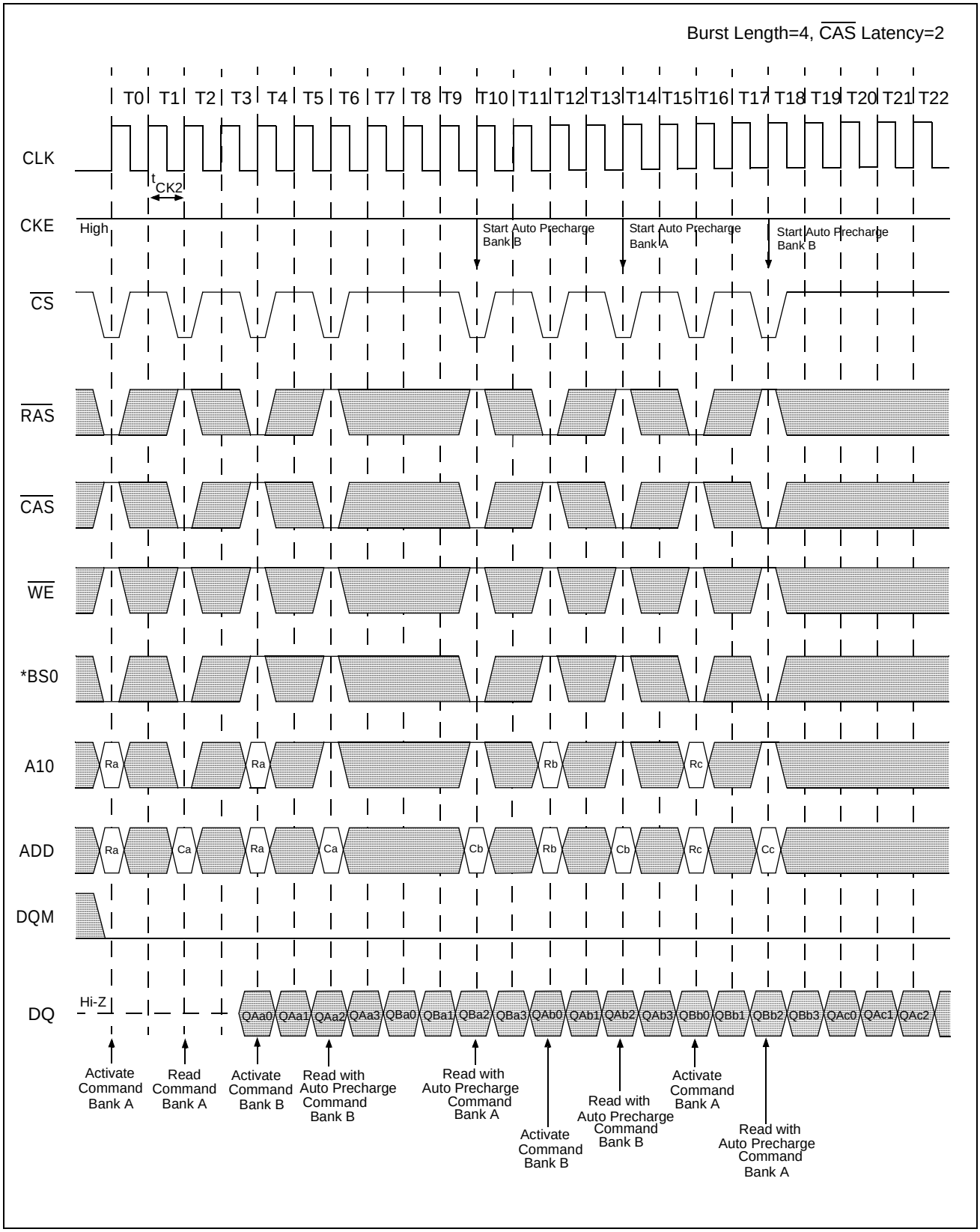
* BS1="L", Bank C,D = Idle

Interleaved Column Write Cycle (2 of 2)



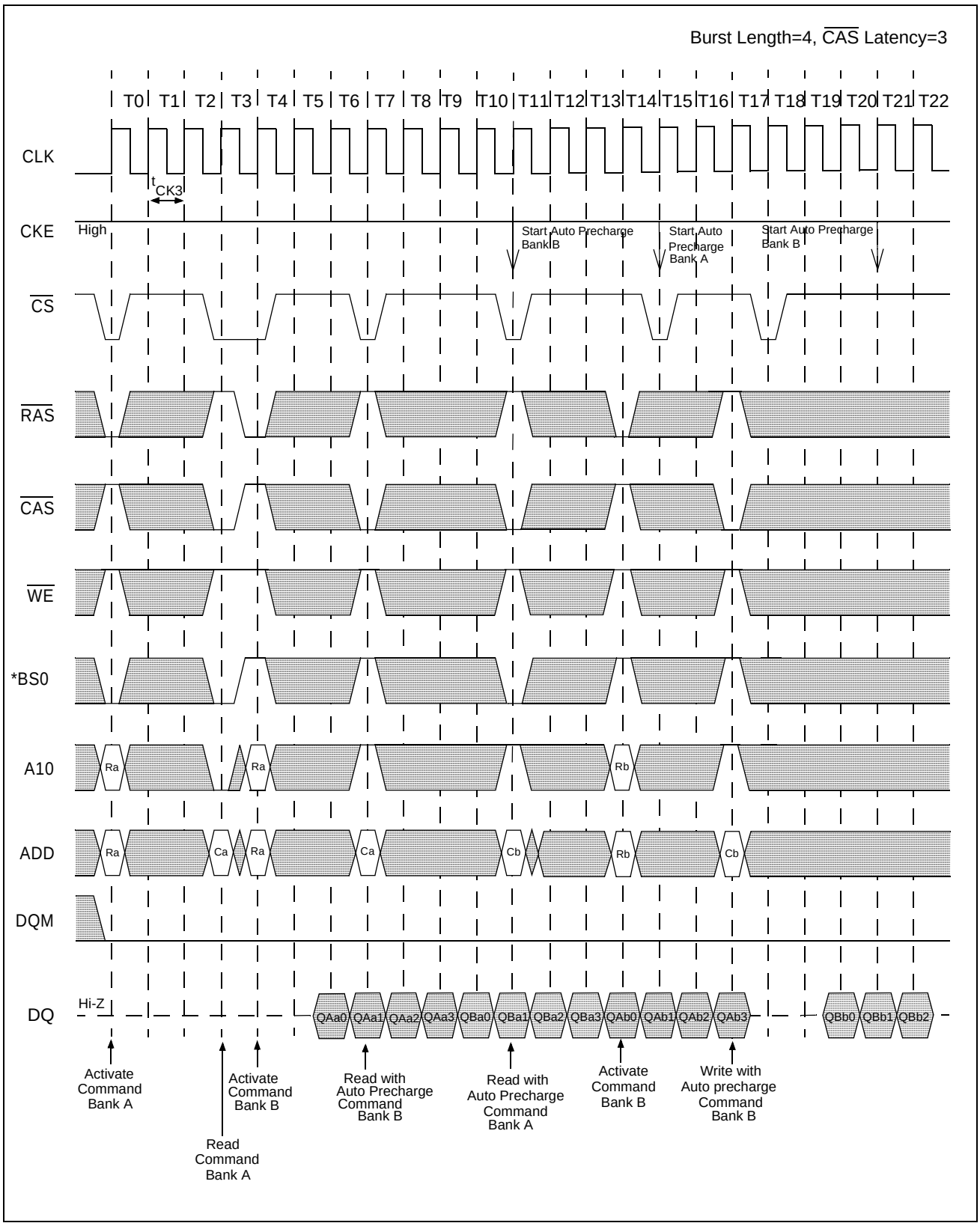
* BS1="L", Bank C,D = Idle

Auto Precharge after Read Burst (1 of 2)



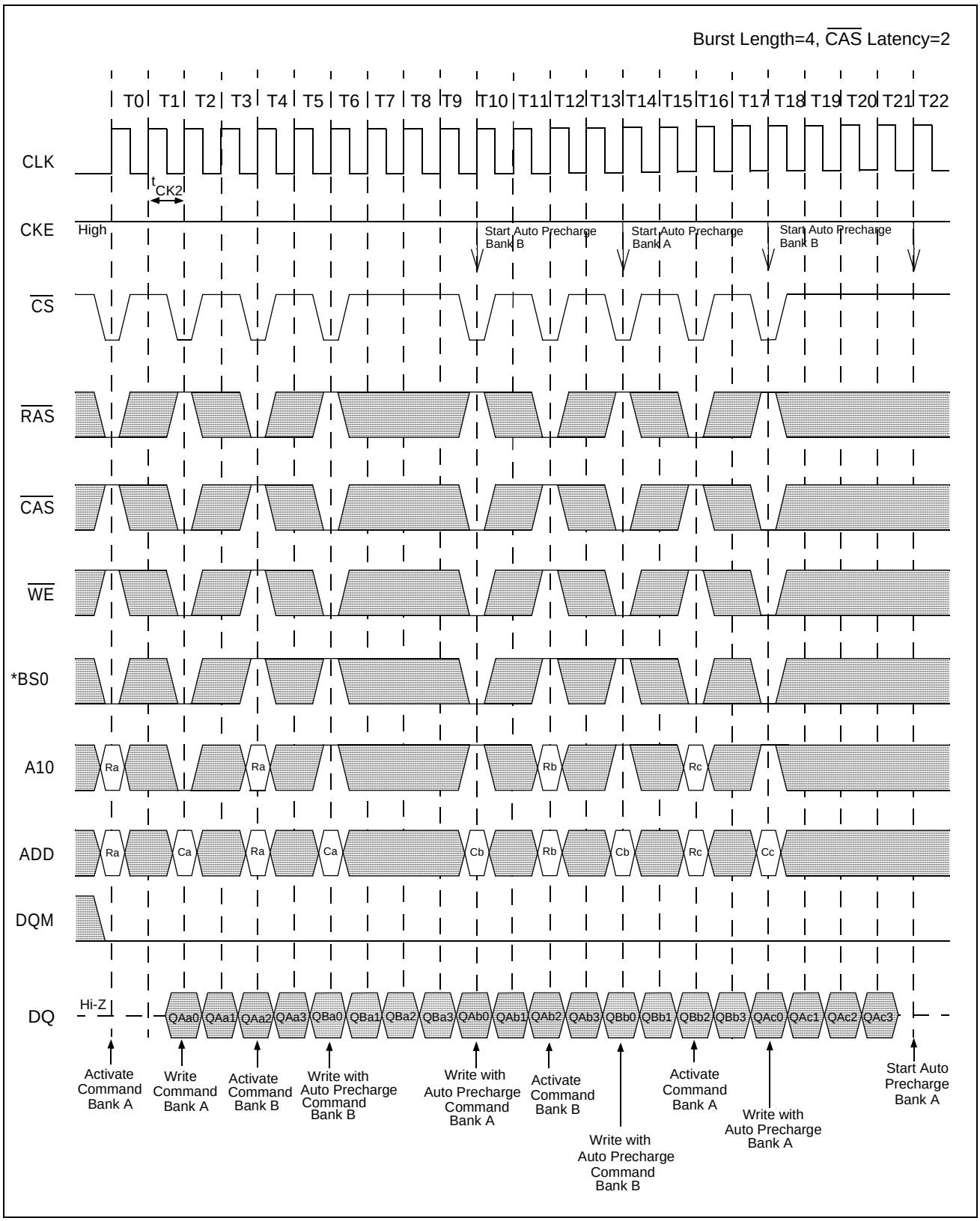
* BS1="L", Bank C,D = Idle

Auto Precharge after Read Burst (2 of 2)



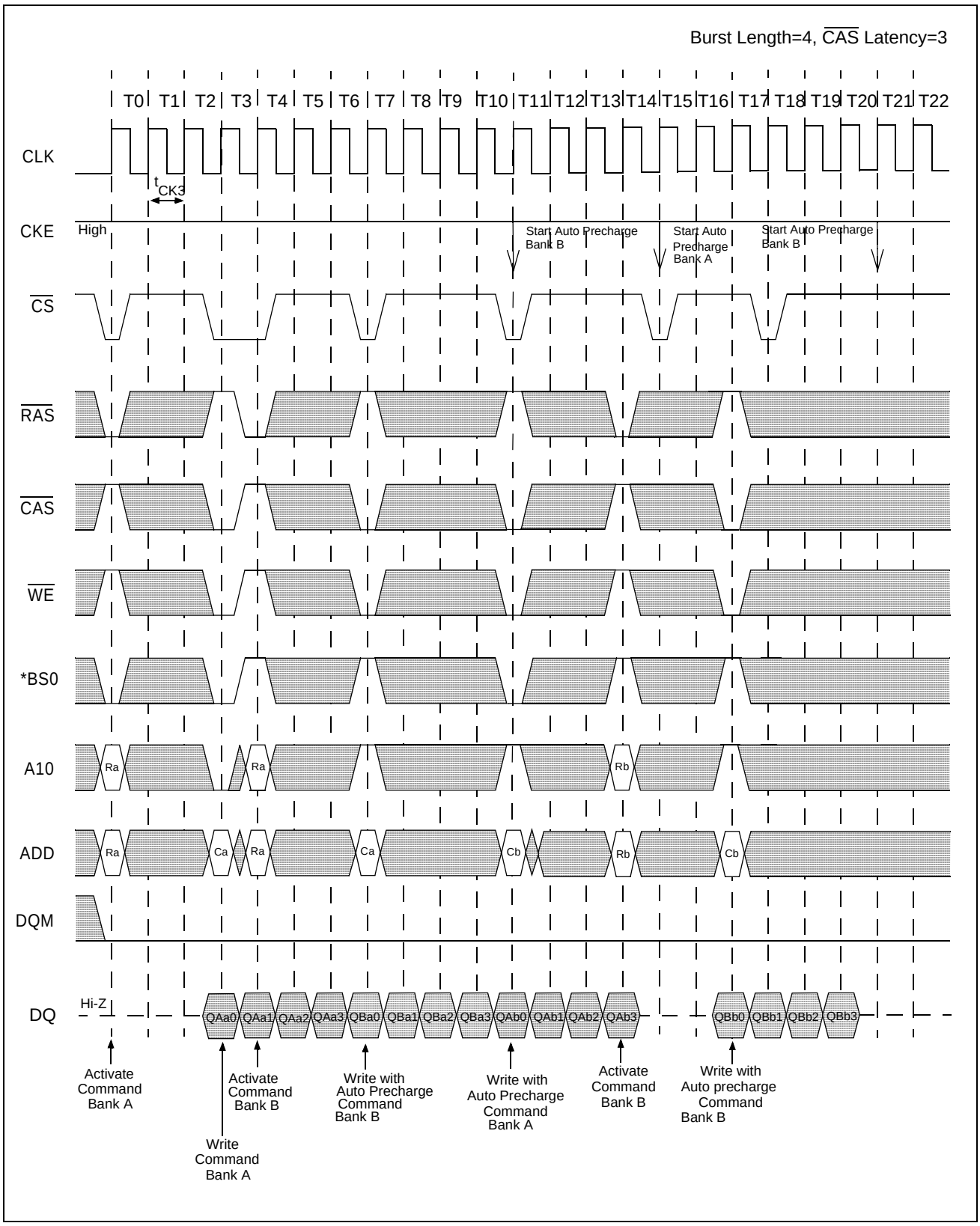
* BS1="L", Bank C,D = Idle

Auto Precharge after Write Burst (1 of 2)



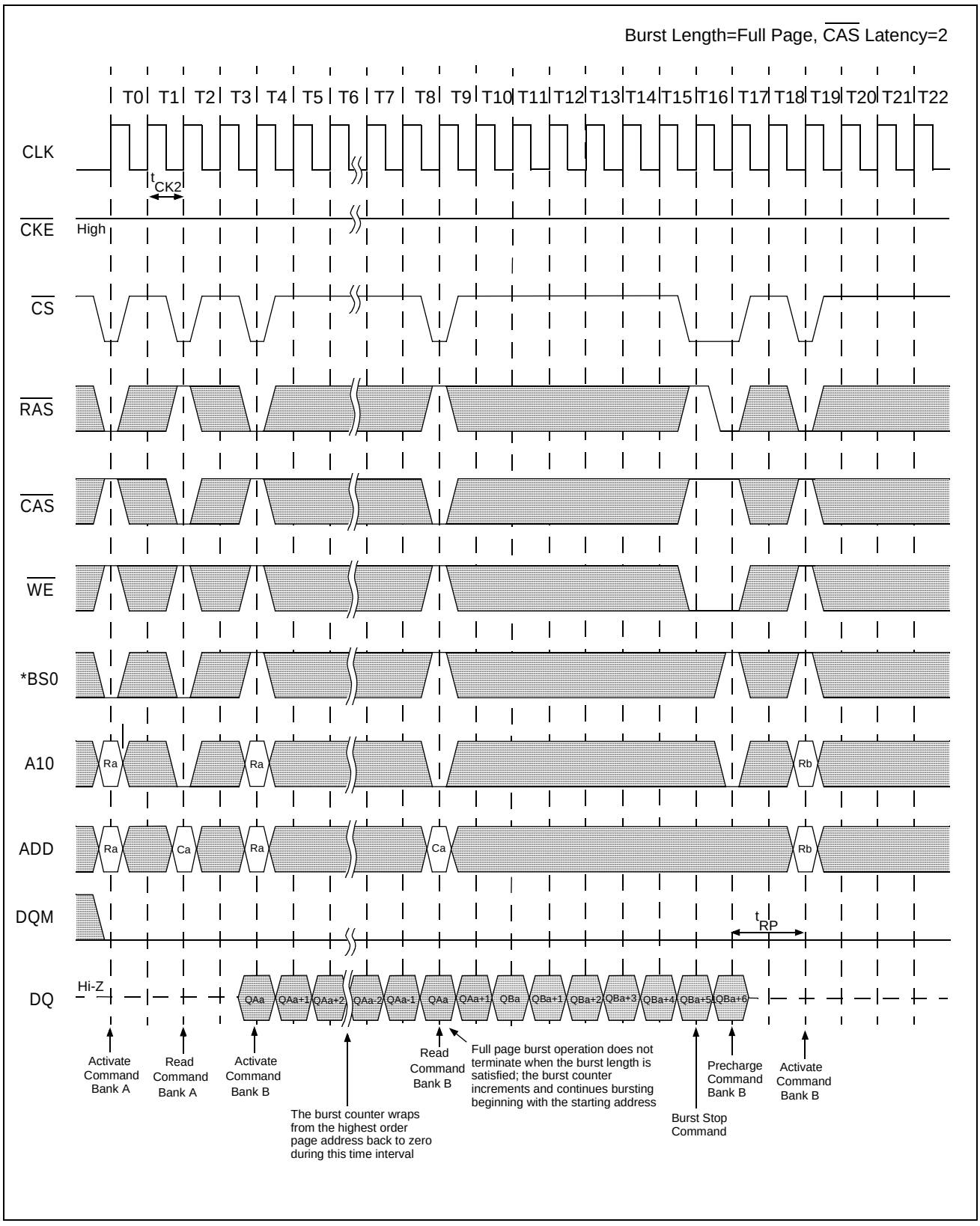
* BS1="L", Bank C,D = Idle

Auto Precharge after Write Burst (2 of 2)



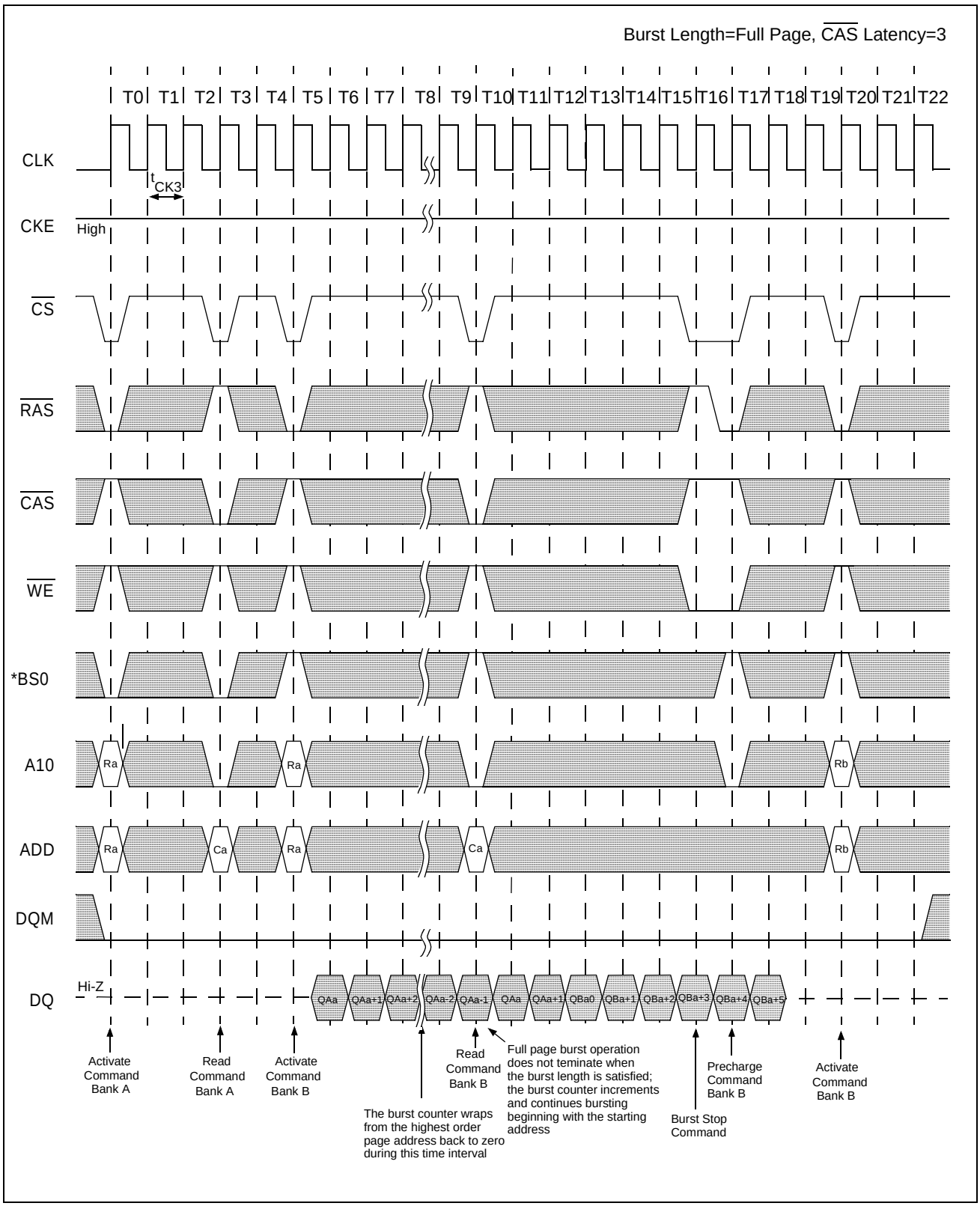
* BS1="L", Bank C,D = Idle

Full Page Read Cycle (1 of 2)



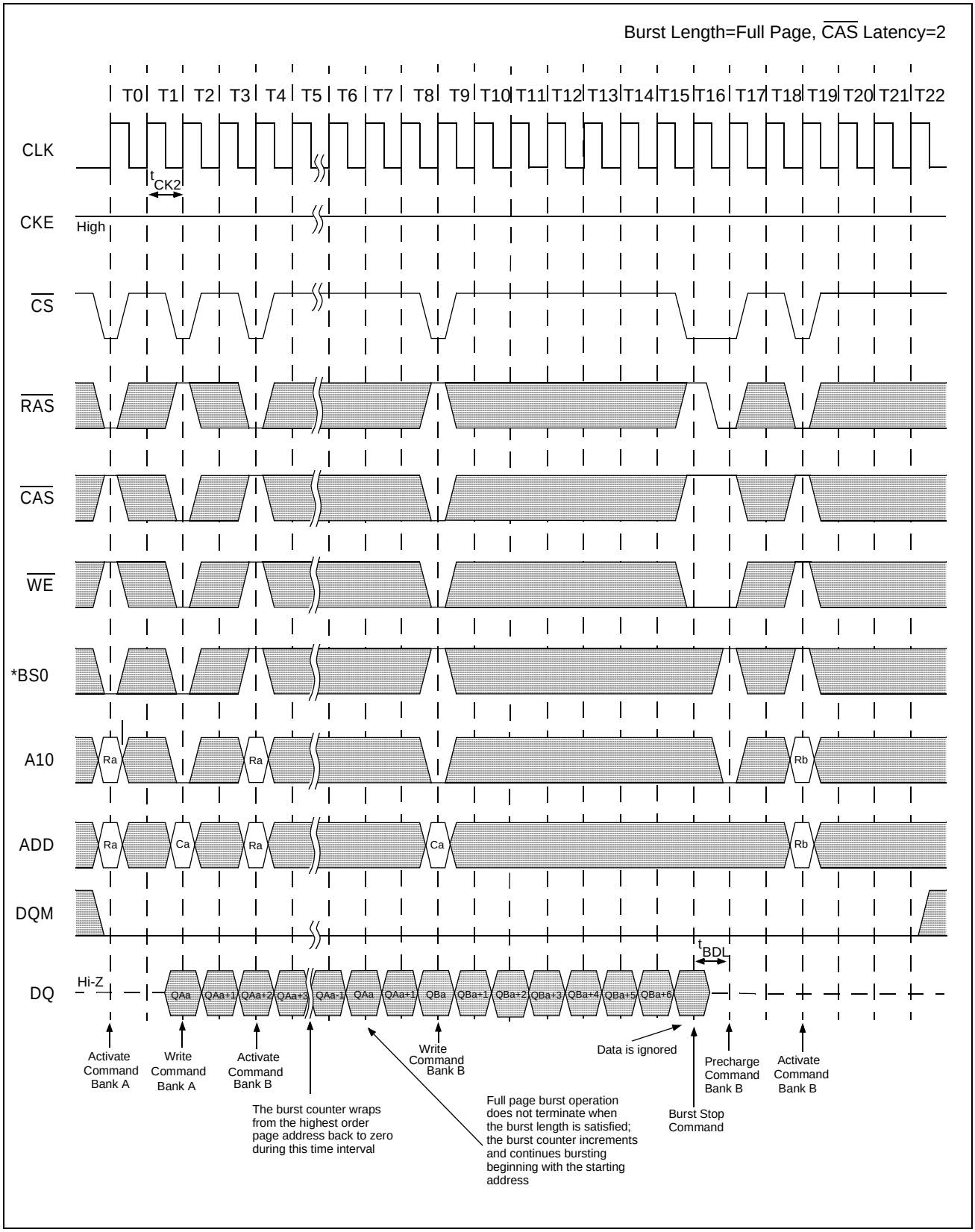
* BS1="L", Bank C,D = Idle

Full Page Read Cycle (2 of 2)



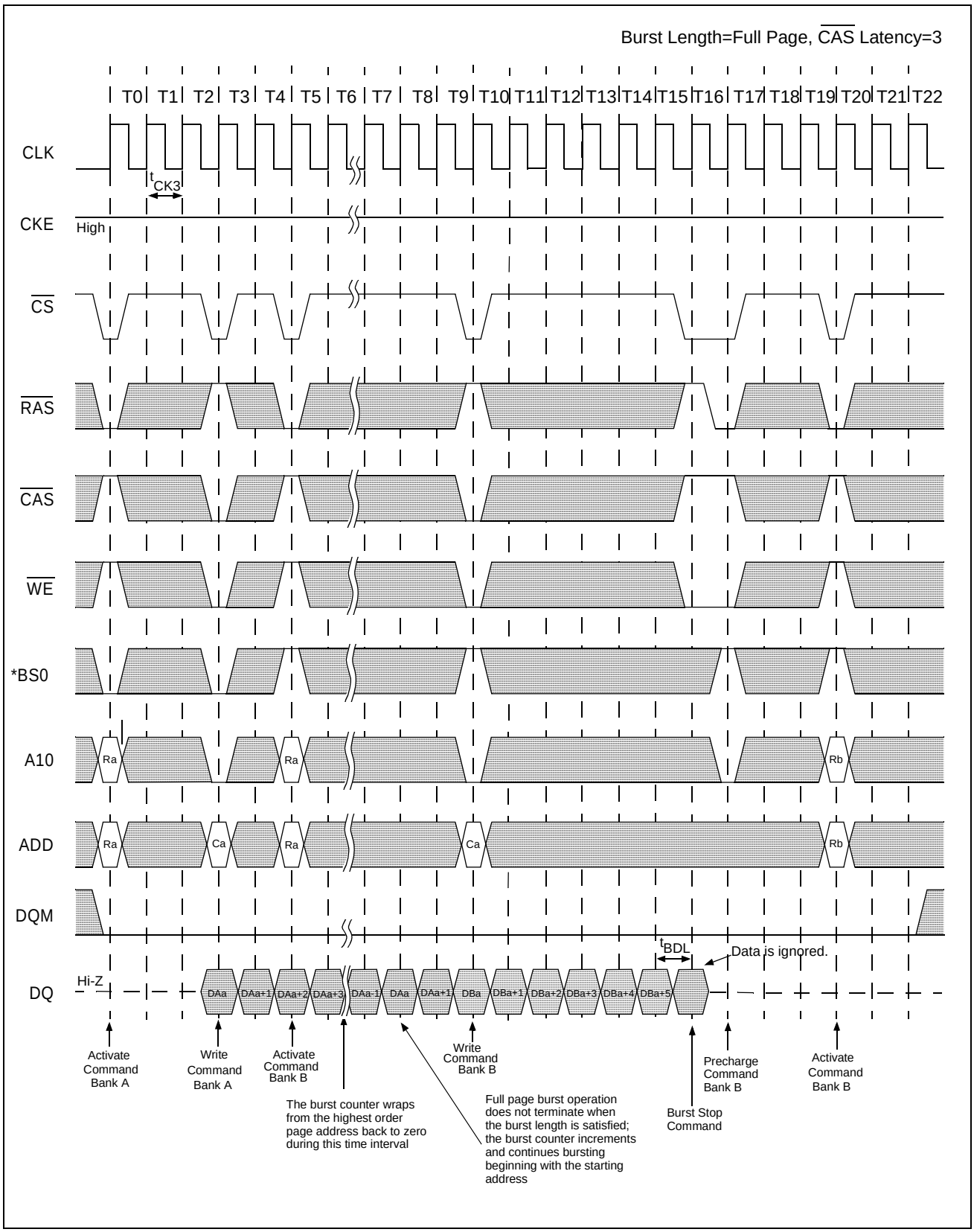
* BS1="L", Bank C,D = Idle

Full Page Write Cycle (1 of 2)



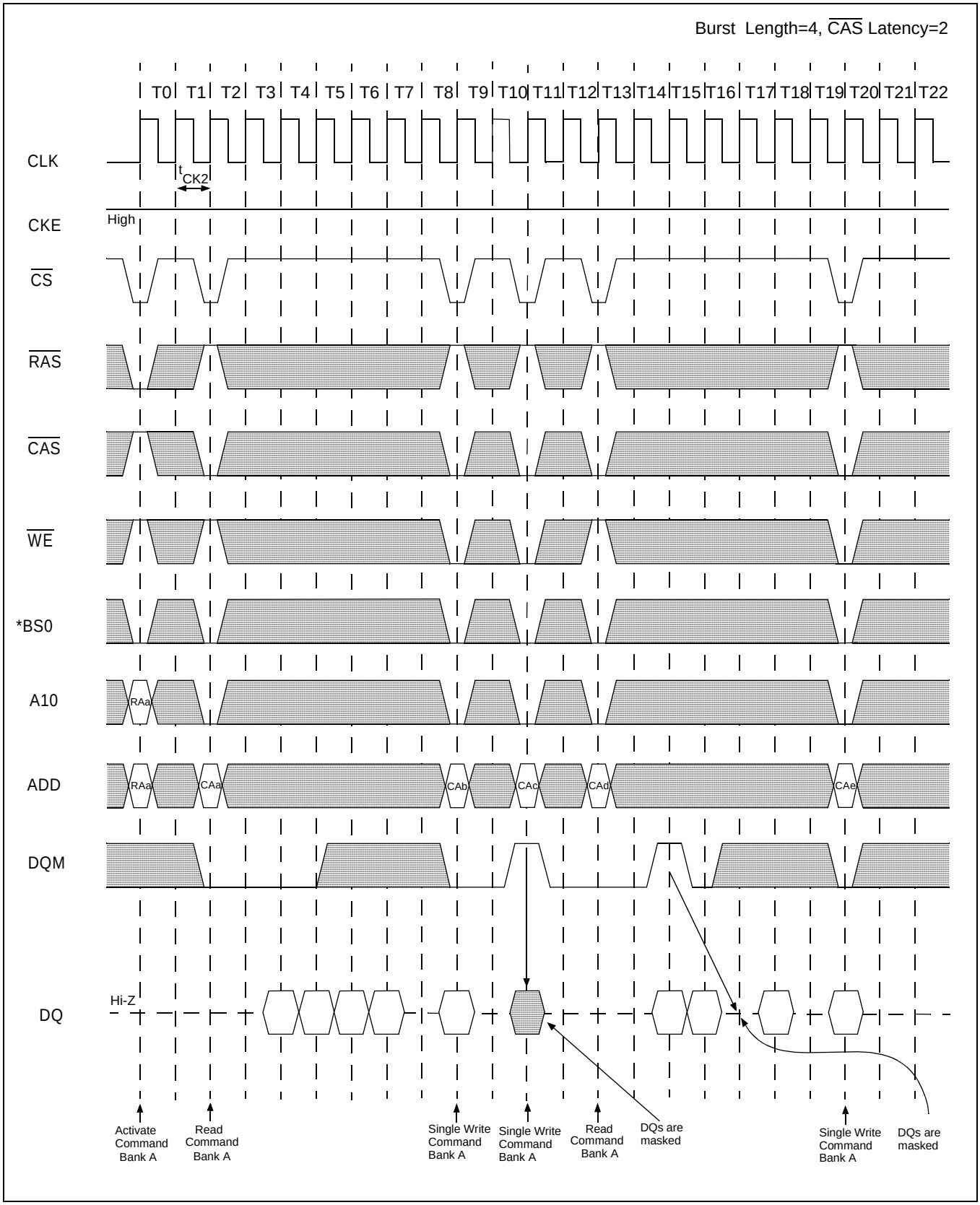
* BS1="L", Bank C,D = Idle

Full Page Write Cycle (2 of 2)



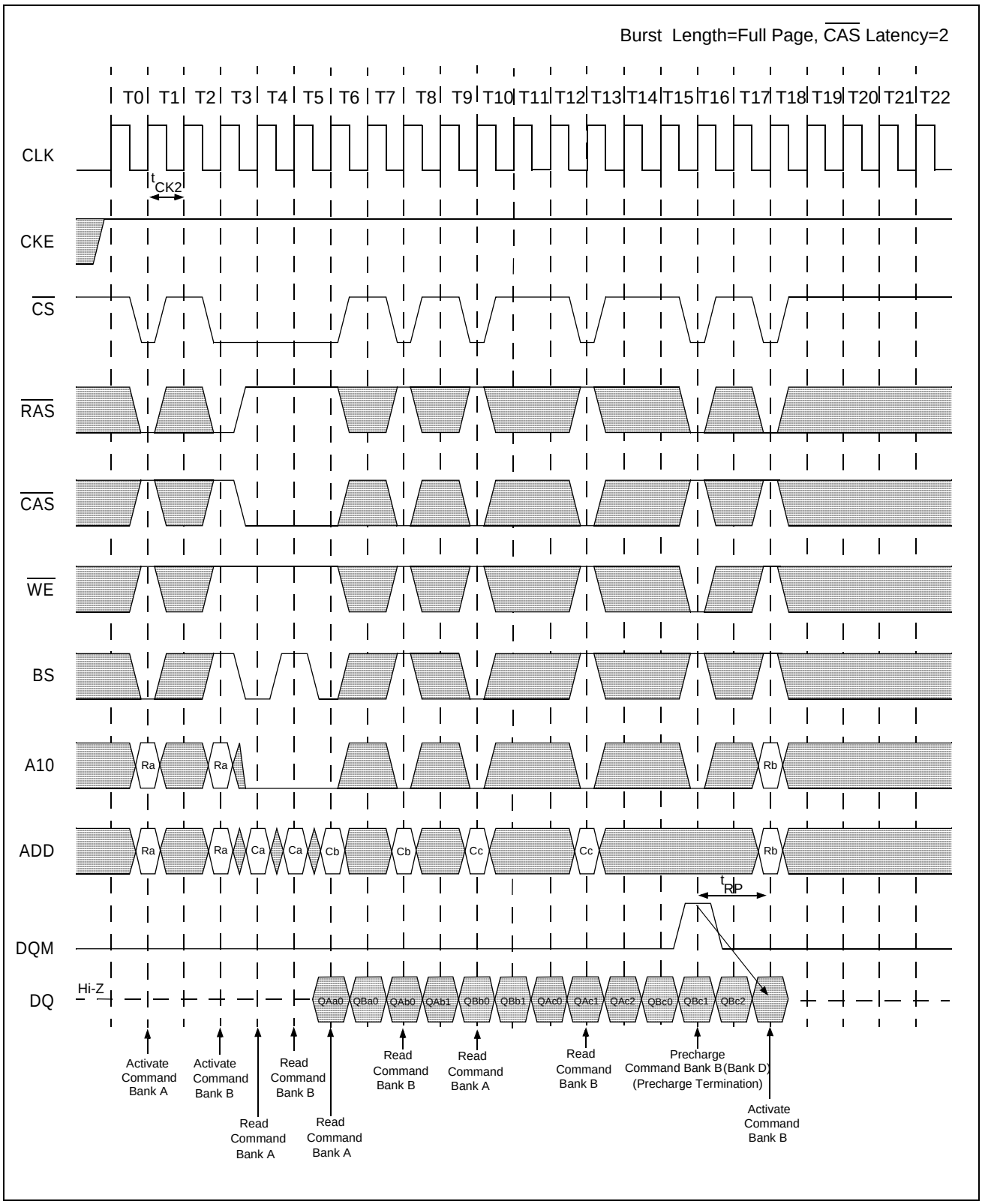
* BS1="L", Bank C,D = Idle

Burst Read and Single Write Operation



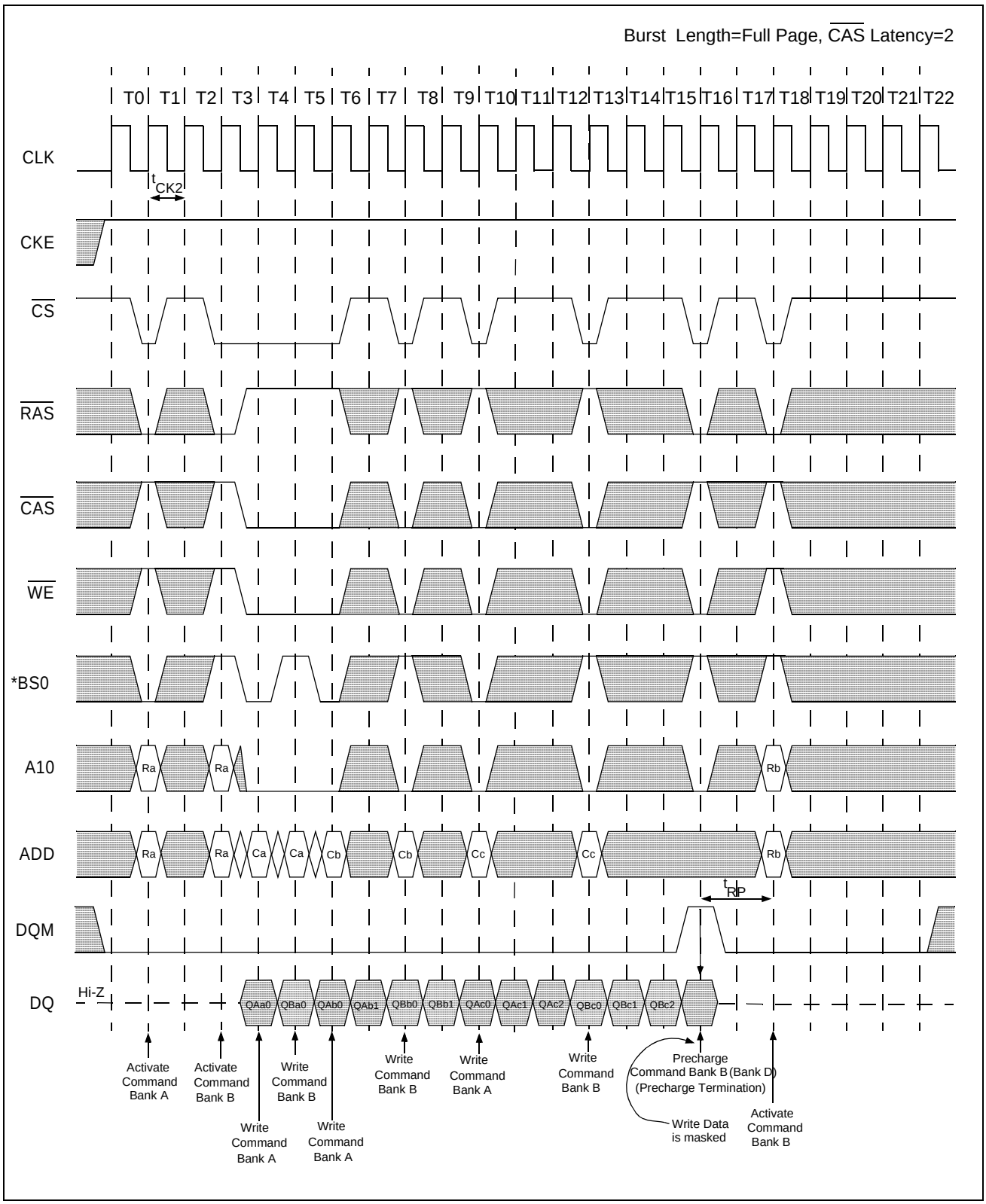
* BS1="L", Bank C,D = Idle

Full Page Random Column Read



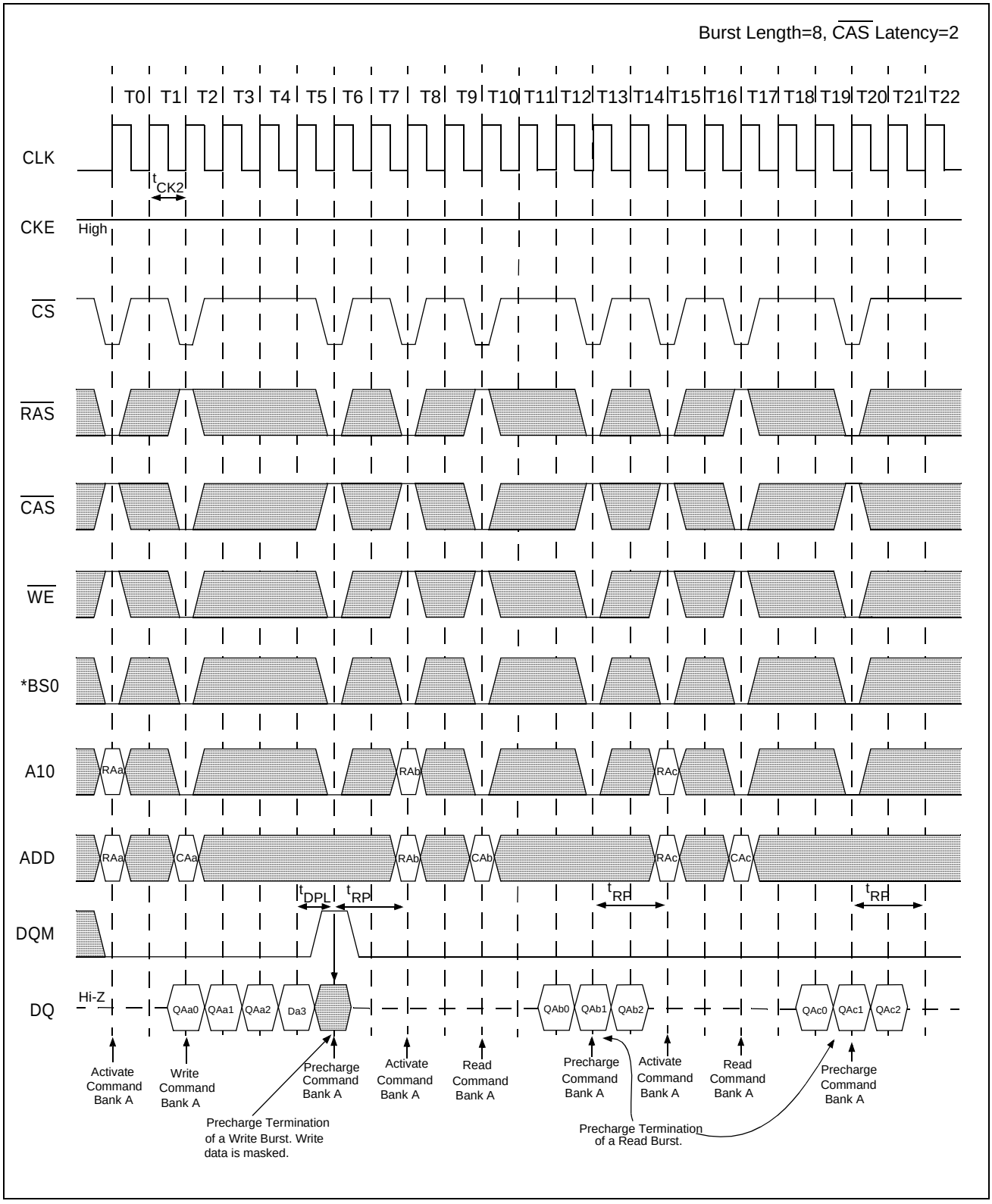
* BS1="L", Bank C,D = Idle

Full Page Random Column Write



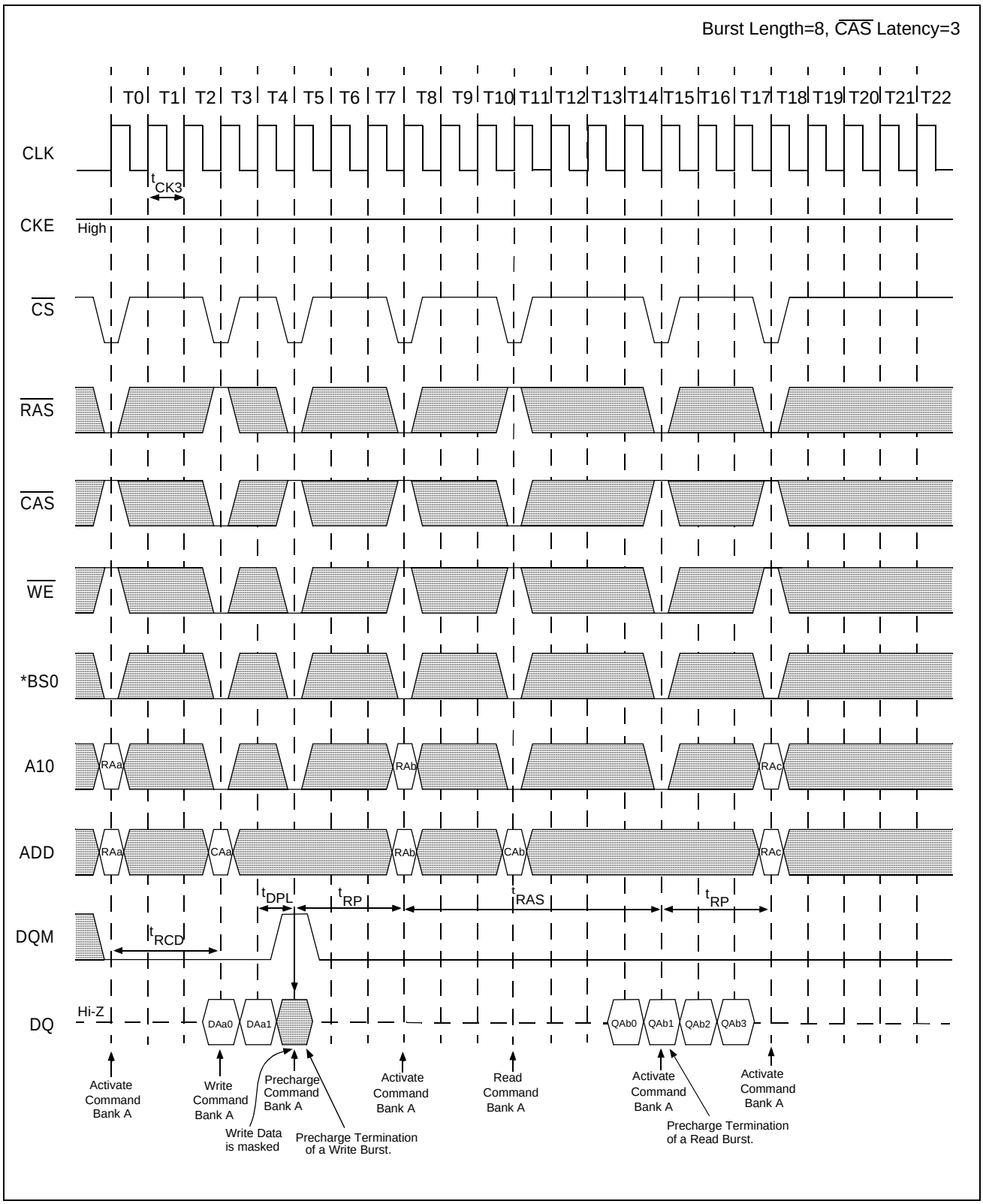
* BS1="L", Bank C,D = Idle

Precharge Termination of a Burst (1 of 2)



* BS1="L", Bank C,D = Idle

Precharge Termination of a Burst (2 of 2)



* BS1="L", Bank C,D = Idle

Ordering information

Part Number	Cycle time	Package
VG366440(80/16)41DT(L)-5L	5.5 ns (183MHz 3/3/3)	400mil, 54-Pin Plastic TSOP
VG366440(80/16)41DT(L)-6	6 ns (166MHz 3/3/3)	
VG366440(80/16)41DT(L)-7	7 ns (143MHz 3/3/3)	
VG366440(80/16)41DT(L)-7L	7.5 ns (133MHz 3/3/3)	
VG366440(80/16)41DT(L)-8H	10 ns (100MHz 2/2/2)	

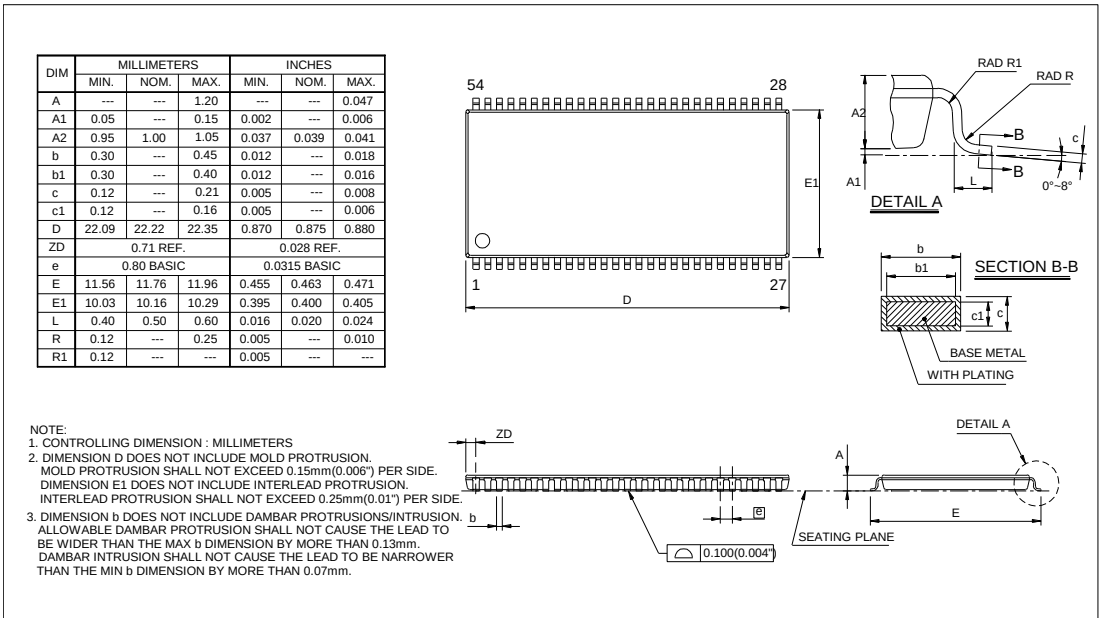
VG36648041DT(L)-7L

- VG : VIS Memory Product
- 36 : Technology/Design Rule
- 64 : 64Mb
- 80 : Device Configuration, 40:x4, 80: x8, 16: x16
- 4 : Device Infernal Banks
- 1 : Interface Type, 1: LVTTL
- D : Mask/Design Version
- T : Package Type, T: TSOP
- L : None: normal version; L:low power version
- 7L : Cycle time; -5L grade is available only on 4M X16 option

Packaging Information

• 400mil, 54-Pin Plastic TSOP

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.20	---	---	0.047
A1	0.05	---	0.15	0.002	---	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	---	0.45	0.012	---	0.018
b1	0.30	---	0.40	0.012	---	0.016
c	0.12	---	0.21	0.005	---	0.008
c1	0.12	---	0.16	0.005	---	0.006
D	22.09	22.22	22.35	0.870	0.875	0.880
ZD	0.71 REF.			0.028 REF.		
e	0.80 BASIC			0.0315 BASIC		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
R	0.12	---	0.25	0.005	---	0.010
R1	0.12	---	---	0.005	---	---



NOTE:
1. CONTROLLING DIMENSION : MILLIMETERS
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15mm(0.006") PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION. INTERLEAD PROTRUSION SHALL NOT EXCEED 0.25mm(0.01") PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD TO BE WIDER THAN THE MAX b DIMENSION BY MORE THAN 0.13mm. DAMBAR INTRUSION SHALL NOT CAUSE THE LEAD TO BE NARROWER THAN THE MIN b DIMENSION BY MORE THAN 0.07mm.