CS9/CSP SERIES: CLOCK OSCILLATOR, PECL, +3.3 VDC or +2.5VDC

DESCRIPTION: A crystal controlled, high frequency, highly stable oscillator, adhering to Positive Emitter Coupled Logic (PECL) Standards. The output can be Tri-stated to facilitate testing or combined multiple clocks. The device is contained in a sub-miniature, very low profile, leadless ceramic SMD package with 6 gold contact pads. This miniature oscillator is ideal for today's automated assembly environments.

APPLICATIONS AND FEATURES:

- **Infiniband; 10GbE; Network Processors; SOHO Routing; Switches; WAN Interfaces**
- **Common Frequencies: 106.25 MHz; 125 MHz; 150 MHz; 155.52 MHz; 156.25 MHz; 161.1328 MHz**
- **+3.3 VDC or +2.5VDC PECL**
- **Frequency Range from 50.000 to 315 MHz**
- **No multiplication**
- **Miniature Ceramic SMD Package Available on Tape and Reel**
- **Lead Free and ROHS Compliant**

■ ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNIT
Operating temperature range	Ta	-40…+85	°C
Storage temperature range	T(stg)	-55…+90	°C
Supply voltage	Vcc	-0.5…+5.0	VDC
Maximum Input Voltage	Vi	Vss-0.5…Vcc+0.5	VDC
Maximum Output Voltage	Vo	Vss-0.5…Vcc+0.5	VDC

■ ELECTRICAL PARAMETERS:

PARAMETER	SYMBOL	TEST CONDITIONS[*1]	VALUE	UNIT
Nominal Frequency	fo		50.000 ~ 315.00**	MHz
Supply Voltage	Vcc		+3.3 or +2.5 ±5%	VDC
Supply Current	Is		80.0 MAX	mA
Output Logic Type			PECL	
Load		Connected between each output and Vcc – 2.0 VDC	50	Ω
Output Voltage Levels	Voh Vol	min max	Vcc-1.025 Vcc-1.620	VDC VDC
Duty Cycle	DC	Measured at 50% of Vcc	40/60 to 60/40 or 45/55 to 55/45	%
Rise / Fall Time	tr / tf	Measured at 20/80% and 80/20% Vcc Levels	0.5 TYP [*2]	ns
Jitter	J	Integrated Phase tji RMS, Fj = 12 kHz…20 MHz	0.3 TYP**	ps
		Integrated Phase RMS tii offset frequency 50KHz to 80MHz	0.5 TYP**	ps
		Deterministic period Jitter tdj using wavecrest analyz.	0.0TYP **	ps
		Random period Jitter trj using wavecrest analyz.	2.5 TYP **	ps
		Peak to Peak Jitter Tp-p using wavecrest analyz.	25 TYP**	ps
Phase Noise typ. @155.52MHz	£(Δf) £(Δf) £(Δf) £(Δf)	Δf=10 Hz Δf=1 KHz Δf=10 KHz Δf= >/=100 KHz	-65 -120 -140 -145	dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Overall Frequency Stability	Δf/fc	Op. Temp., Aging, Load, Supply and Cal. Variations	±20, ±25, ±50, or ±100 MAX[*3]	Ppm
Pin 1 Output Enabled Output Disabled	En Dis	High Voltage or No Connect Ground	0.7•Vcc MIN 0.3•Vcc MAX	VDC VDC

*1 Test Conditions Unless Stated Otherwise: Nominal Vcc, Nominal Load, +25 ±3°C
*2 Frequency Dependent
*3 Not All Stabilities Available With All Temperature Ranges—Please Consult Factory For Availability

■ PART NUMBERING SYSTEM:

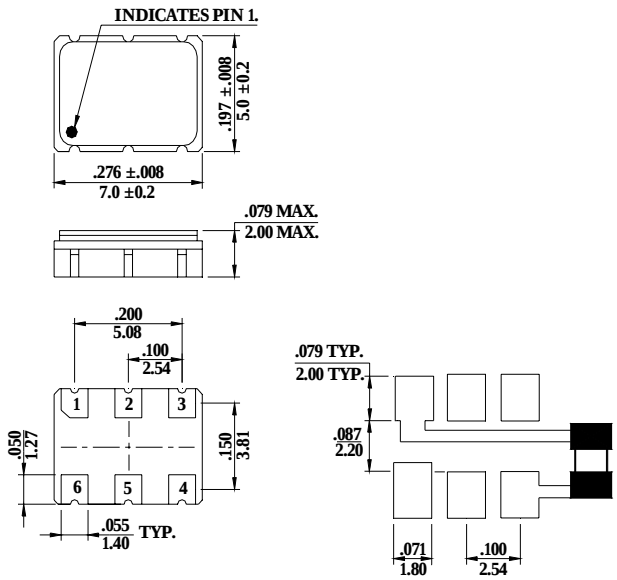
SERIES	SYMMETRY	TEMPERATURE RANGE (°C)	FREQUENCY STABILITY (Overall)	FREQUENCY (MHz)
CS9: +3.3Vdc Clock with PECL Comp. Output CSP: +2.5Vdc Clock with PECL Comp. Output	A: 40/60 to 60/40% T: 45/55 to 55/45%	R: 0…+50 S: 0…+70 U: -20…+70 V: -40…+85**	K: ±20 ppm** I: ±25 ppm** H: ±50 ppm J: ±100 ppm	50.000…315.000

EXAMPLE: CS9ASH-155.520

Clock Oscillator, 7x5mm Package, +3.3 VDC Supply Voltage, PECL Output, Standard Symmetry, 0…+70°C Operating Temperature Range, ±50 ppm Total Frequency Stability, 155.520 MHz

**Above 300MHz extended temp range and ±25ppm stability may not be available, jitter may vary upon spec requirements. Please consult the factory for any custom requirements.

■ MECHANICAL PARAMETERS:



SOLDER PATTERN

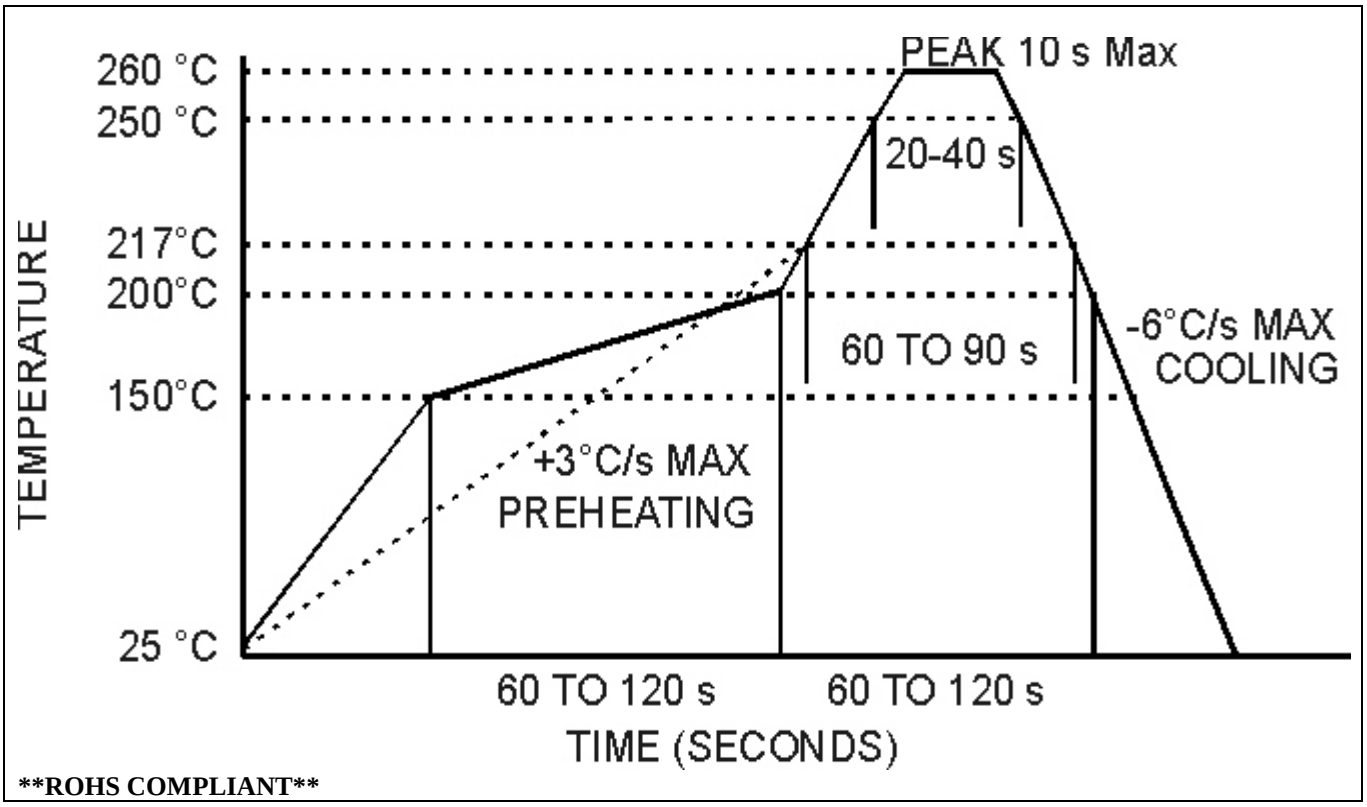
OUTLINE TOLERANCE:
±0.006" / 0.15mm
(Unless otherwise specified)

PIN FUNCTIONS:
[1] ENABLE/ DISABLE
[2] NO CONNECT
[3] CASE GROUND
[4] OUTPUT
[5] COMP. OUTPUT
[6] SUPPLY VOLTAGE

MARKING:
CS9ASH
155.52
RAL D/C

***0.01µF external by-pass filter is recommended as seen on solder pattern.**

■ **REFLOW PROFILE:**



****ROHS COMPLIANT****