Raytheon
RF Components

RMDA29000
27-31 GHz Driver Amplifier MMIC

ADVANCED INFORMATION

Description

The Raytheon RF Components RMDA29000 is a high efficiency driver amplifier designed for use in point to point radio, point to multi-point communications, LMDS and other millimeter wave applications. The RMDA29000 is a 3-stage GaAs MMIC amplifier utilizing Raytheon RF Components' advanced 0.15mm gate length Power PHEMT process and can be used in conjunction with other driver or power amplifiers to achieve the required total power output.

Features

- 22 dB small signal gain (typ.)
- 23 dBm saturated power out (typ.)
- Circuit contains individual source vias
- Chip Size 3.41 mm x 1.62 mm

Absolute Ratings

Parameter	Symbol	Value	Unit
Positive DC Voltage (+5 V Typical)	Vd	+ 6	Volts
Negative DC Voltage	Vg	- 2	Volts
Simultaneous (Vd - Vg)	Vdg	+ 8	Volts
Positive DC Current	I_D	360	mA
RF Input Power (from 50 Ω source)	P_{IN}	+10	dBm
Operating Base plate Temperature	T_C	-30 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Thermal Resistance (Channel to Backside)	R_{jc}	38	°C/W

Electrical Characteristics

(At 25 °C) 50 Ohm system, Vd=+5 V, Quiescent current (Idq)=250 mA

Parameter	Min	Typ	Max	Unit
Frequency Range	27		31	GHz
Gate Voltage[1] (Vg)		-0.4		V
Gain Small Signal	18	22	28	dB
Gain Variation vs. Frequency		+/-1		dB
Power Output at 1 dB Compression		21		dBm
Power Output Saturated: (Pin=+4 dBm)	21	23		dBm

Parameter	Min	Typ	Max	Unit
Drain Current Small Signal mA			250	
Drain Current at P1 dB Compression		270		mA
Power Added Efficiency (PAE): at P1dB		8		%
OIP3[2]		30		dBm
Input Return Loss	5	10		dB
Output Return Loss	5	8		dB

Note:
- Typical range of the negative gate voltages is -0.9 to 0.0 V to set typical Idq of 250 mA.
- 10 MHz tone separation measured at 10 dBm Power Out/tone.

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC Ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012” long corresponding to a typical 2 mil gap between the chip and the substrate material.

Figure 1
Functional Block Diagram

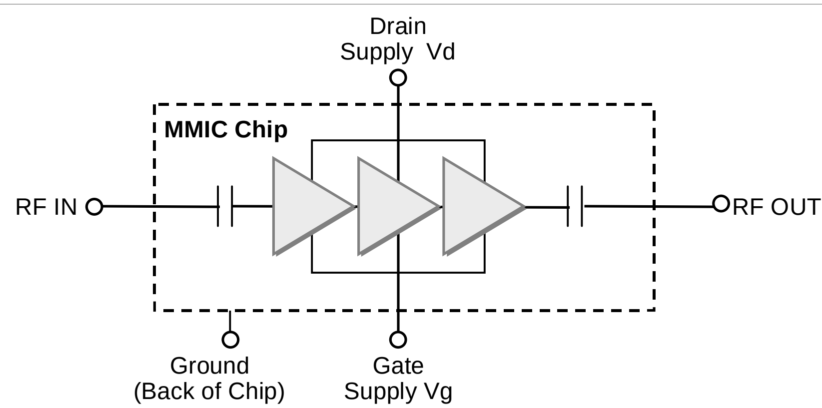

Figure 2
Chip Layout and Bond Pad Locations

(Chip Size=3.405 mm x 1.621 mm x 50 mm. Back of Chip is RF and DC Ground)

Dimensions in mm

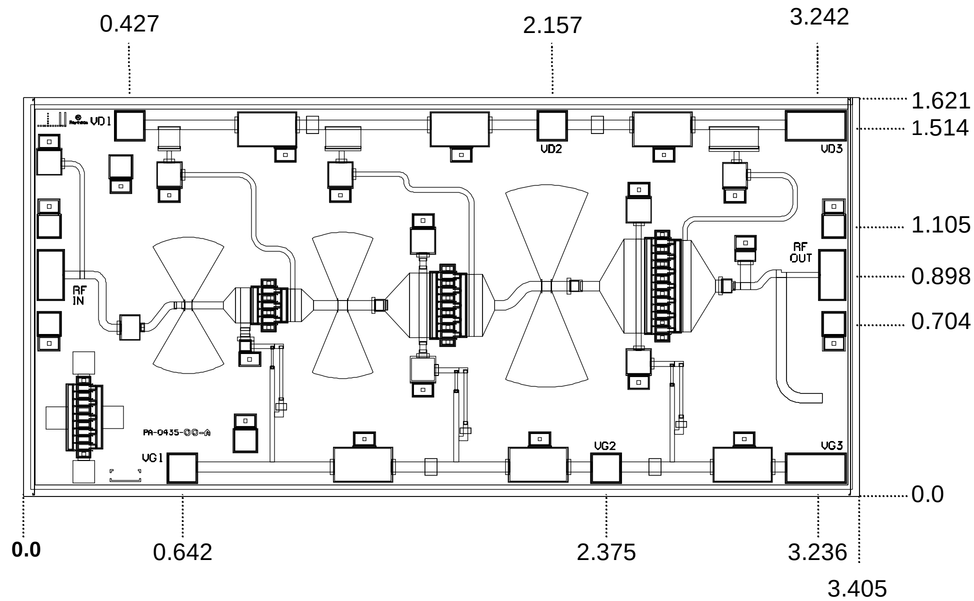

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Figure 3
Recommended Application Schematic Circuit Diagram

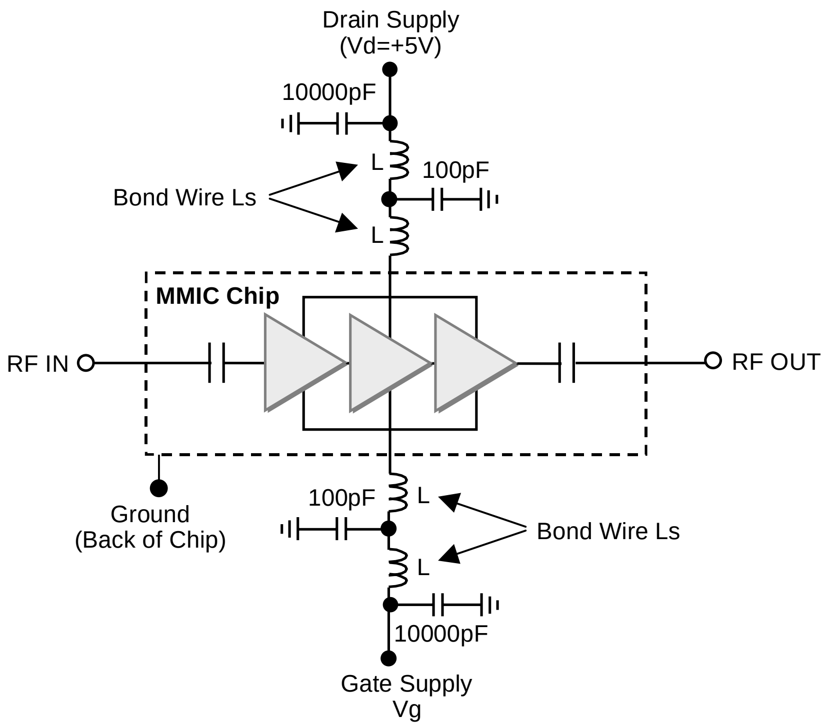
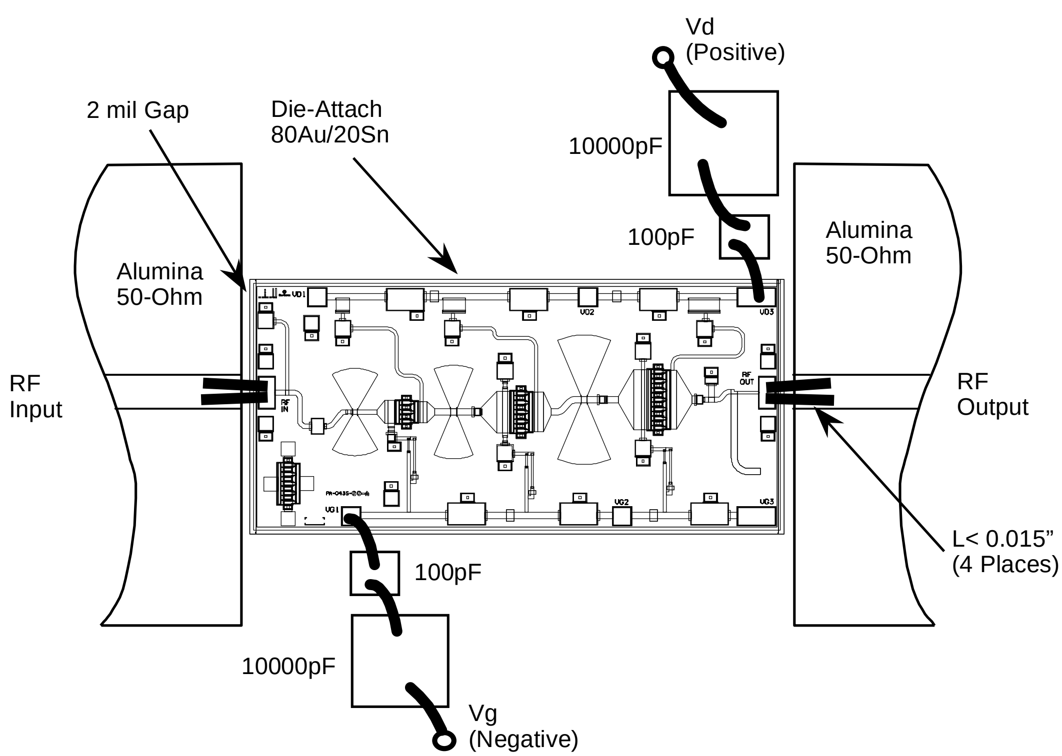


Figure 4
Recommended Assembly Diagram



Note:
Use 0.003" x 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief. Vd should biased from 1 positive supply. Vg should be biased from 1 negative supply.

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Recommended Procedure
for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (Vg) WHILE DRAIN VOLTAGE (Vd) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier.

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the ground of the chip carrier.

Slowly apply negative gate bias supply voltage of -1.5 V to Vg.

Step 3: Slowly apply positive drain bias supply voltage of +5 V to Vd.

Step 4: Adjust gate bias voltage to set the quiescent current of Idq=250 mA.

Step 5: After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band.

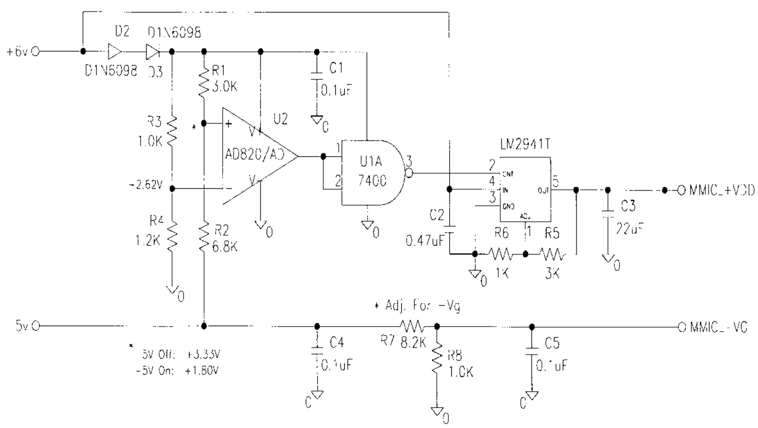
Step 6: Follow turn-off sequence of:

(i) Turn off RF input power.

(ii) Turn down and off drain voltage (Vd).

(iii) Turn down and off gate bias voltage (Vg).

Note:
An example auto bias sequencing circuit to apply negative gate voltage and positive drain voltage for the above procedure is shown below.



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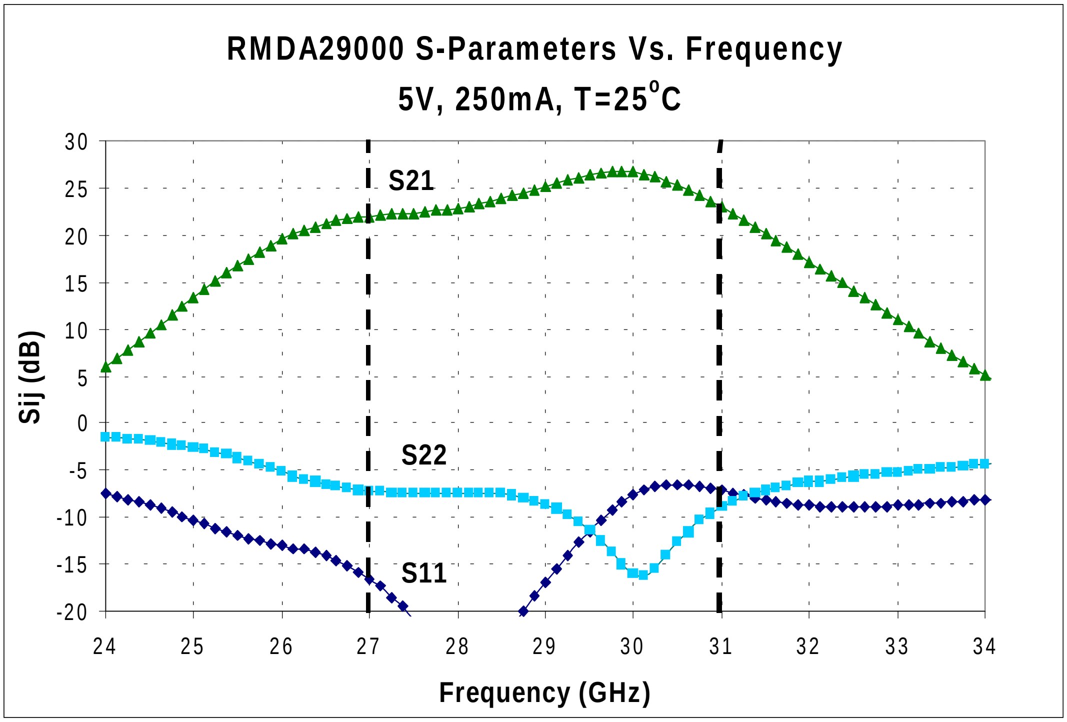
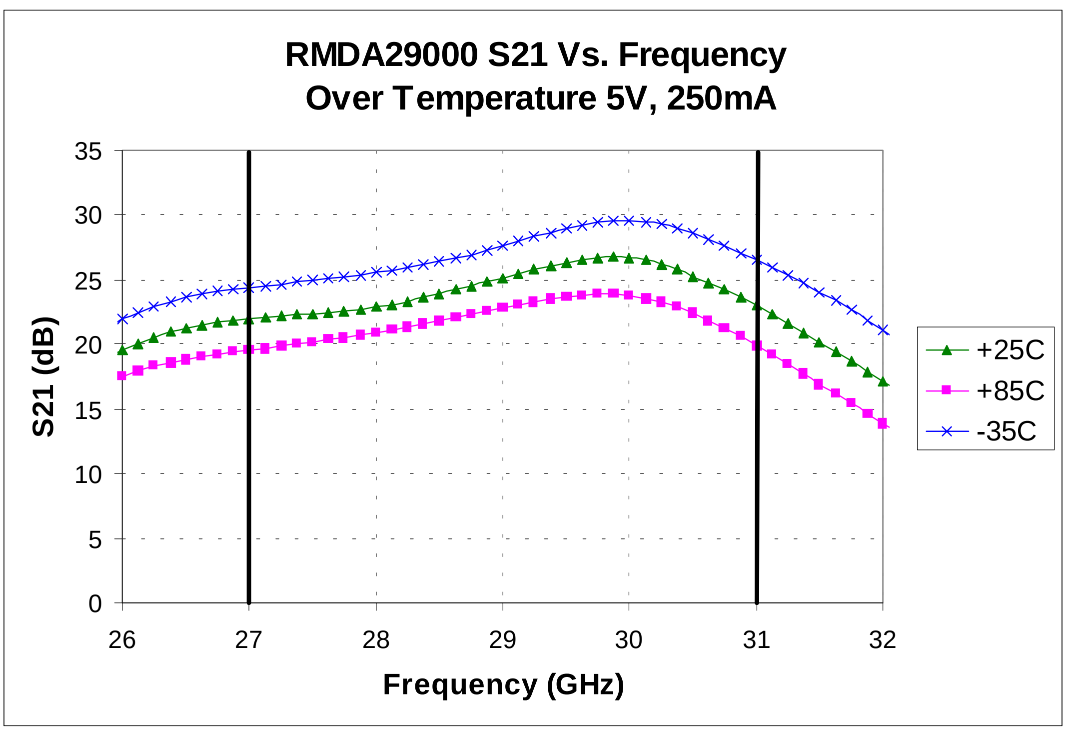
Performance Data





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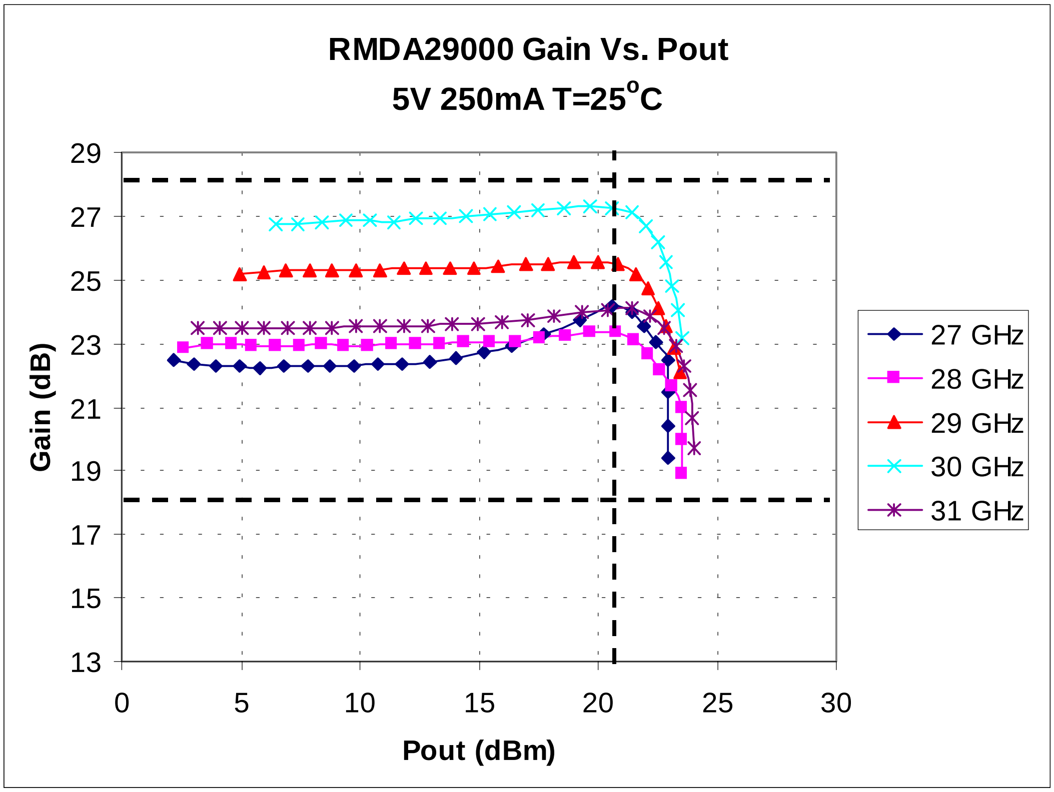

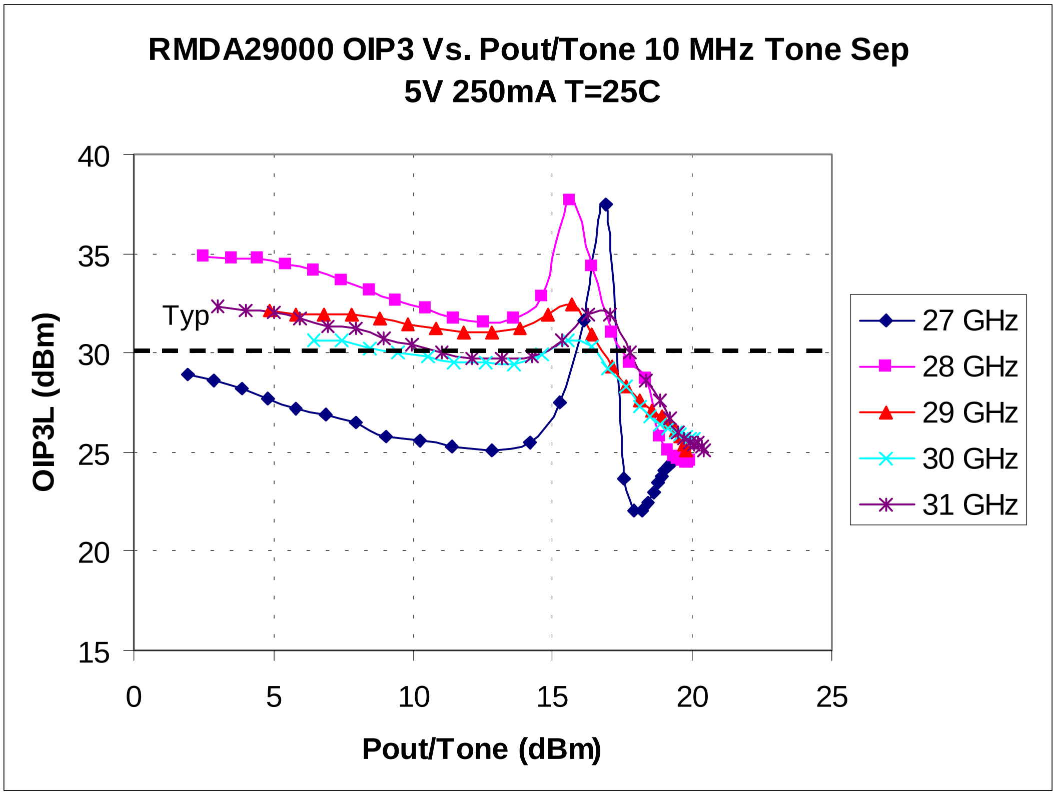

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