Raytheon

RMPA0951A-102
3V Cellular CDMA Power Amplifier Module

PRODUCT INFORMATION

Description

The RMPA0951A-102 is a dual mode, small-outline Power Amplifier Module (PAM) for Cellular CDMA personal communication system applications. The PA is internally-matched to 50 ohms and DC blocked which minimizes the use of external components and reduces circuit complexity for system designers. High AMPS/CDMA efficiency and good linearity are achieved using Raytheon RF Components' InGaP Heterojunction Bipolar Transistor (HBT) process.

Features

- Single positive-supply operation
- High dual-mode (AMPS/CDMA) efficiency
- Excellent linearity
- Small size: 6.0 x 6.0 x 1.5 mm^3 LCC package
- 50-ohm matched input and output module
- Adjustable quiescent current and power-down mode
- Suitable for CDMA and CDMA2000 1X systems

Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Vnits
Supply Voltage	Vc1, Vc2	6.0	V
Reference Voltage	Vref	1.5 to 4.0	V
RF Input Power[2]	Pin	+7	dBm
Load VSWR	VSWR	6:1	
Case Operating Temperature	Tc	-30 to +85	°C
Storage Temperature	Tstg	-55 to +150	°C

Electrical Characteristics[3]

Parameter	Min	Typ	Max	Unit
Frequency Range	824		849	MHz
Gain (Pout=+28 dBm)		30		dB
Gain AMPS (Pout=+31.5dBm)		30		dB
Analog Output Power	31.5			dBm
Power-Added Efficiency				
CDMA (Pout =+28 dBm)	30	35		%
Analog (Pout =+31.5 dBm)	44	50		%
ACPR1[5]		-52	-46	dBc
ACPR2[5]		-58	-55	dBc
Rx-Band Noise Power (All Power Levels)		-135		dBm/Hz

Parameter	Min	Typ	Max	Unit
Noise Figure		3		dB
Input VSWR (50Ω)		1.5:1	2.5:1	---
Output VSWR (50Ω)		2.5:1		---
Stability (All spurious)[4,7]			-60	dBc
Harmonics (Po ≤ 28 dBm)[7] 2fo, 3fo, 4fo			-30	dBc
Quiescent Current		80	100	mA
Power Shutdown Current[6]		2	10	uA
Vcc	3.0	3.5	4.0	Volts
Vref	2.0	3.0	3.2	Volts
Iref		16		mA

Notes:

1. No permanent damage with only one parameter set at extreme limit and other parameters typical.
2. Typical RF input powers for CDMA (-3 dBm) and AMPS mode (+2 dBm) operation.
3. All parameters to be met at Ta = +25°C, Vcc = +3.5V, Vref=3.0V and load VSWR ≤ 1.2:1.
4. Load VSWR ≤ 6:1 all phase angles.
5. CDMA Waveform measured using the ratio of the average power within the 1.23 MHz signal channel to the power within a 30 kHz resolution bandwidth, Pout=28 dBm. Offset is ± 885 KHz, ± 1.98 MHz.
6. No applied RF signal. Vcc=+3.5V nominal, Vref=+0.2V maximum.
7. Guaranteed by design.

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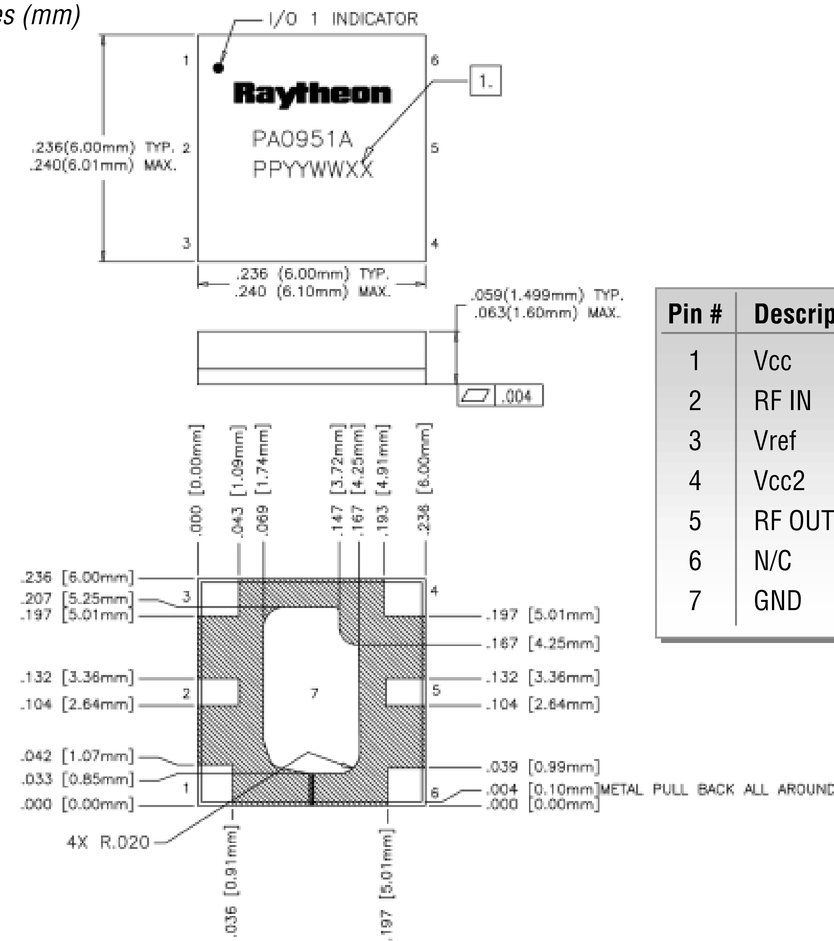
Figure 1
Package Outline and Pin Designations

Dimensions in inches (mm)



Pin #	Description
1	Vcc
2	RF IN
3	Vref
4	Vcc2
5	RF OUT
6	N/C
7	GND

Figure 2
Functional Block Diagram

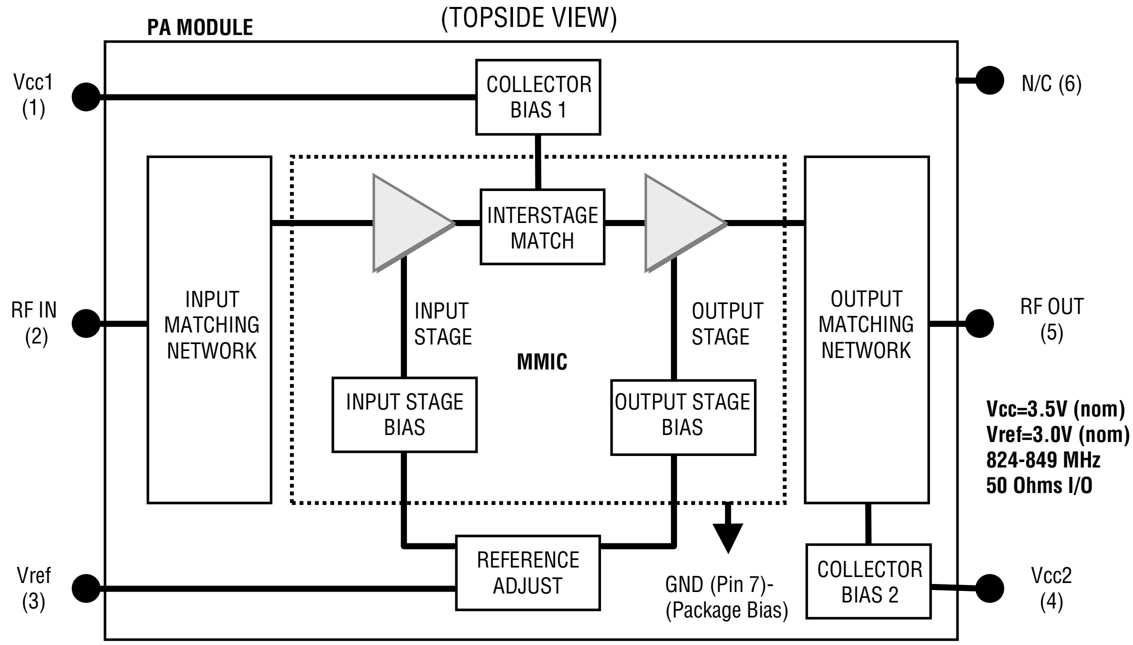


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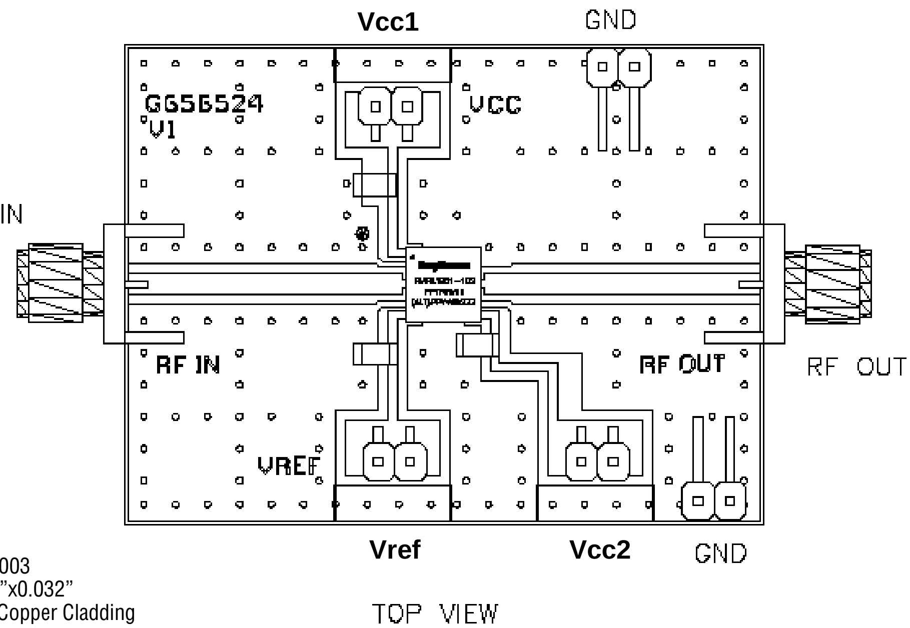
Figure 3
Evaluation Board Layout, Schematic, and Instructions

With device marking oriented right side up, RF IN is on the left and RF OUT is on the right.

Vcc= +3.5V nominal. Vref=+ 3.0V nominal to obtain Iccq= 80 mA. Operation at lower or higher quiescent currents can be achieved by decreasing or increasing Vref voltage relative to +3.0V.

First ground the PCB (GND terminal) and apply +3.5V to the collector supply terminals (Vcc1, Vcc2). Next apply +3.0V to the reference supply (Vref terminal). Quiescent collector current with no RF applied will be about 80 mA. Reference supply current with or without RF applied will be about 15 mA. When turning amplifier off, reverse power supply sequence.

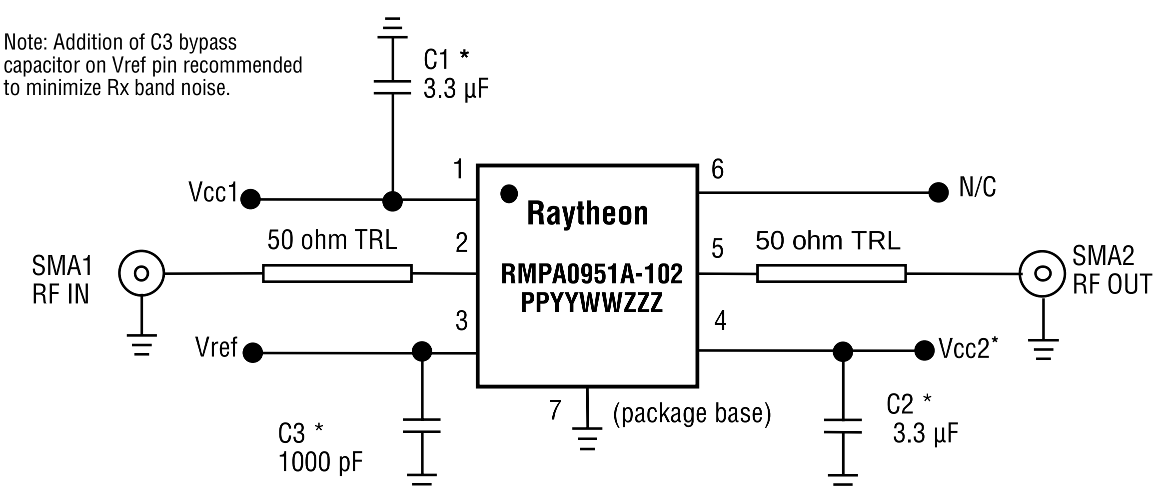
Apply -20 dBm RF input power at Cellular frequency (824-849 MHz). After making any initial small signal measurements at this drive level, input power may be increased up to a maximum of +7 dBm for large signal, analog (AMPS) or digital CDMA measurements. Do not exceed +7 dBm input power.



PCB Specifications:
Material: Rogers RO4003
Dimensions: 2.0"x1.5"x0.032"
Metallization: 1/2 oz Copper Cladding

PCB Schematic

Note: Addition of C3 bypass capacitor on Vref pin recommended to minimize Rx band noise.



* Minimum bypass capacitance recommended for best linearity/low-noise performance.

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Application Information

- **Precautions to Avoid Permanent Device Damage:**
  - **Cleanliness:** Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC & ground contact areas.
  - **Device Cleaning:** Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
  - **Static Sensitivity:** Follow ESD precautions to protect against ESD damage:
    - A properly grounded static-dissipative surface on which to place devices.
    - Static-dissipative floor or mat.
    - A properly grounded conductive wrist strap for each person to wear while handling devices.
  - **General Handling:** Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, & ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
  - **Device Storage:** Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.
- **Device Usage:** Raytheon recommends the following procedures prior to assembly.
    - Dry-bake devices at 125°C for 24 hours minimum. Note: The shipping trays cannot withstand 125°C baking temperature.
    - Assemble the dry-baked devices within 7 days of removal from the oven.
    - During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
    - If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure must be repeated.
- **Solder Materials & Temperature Profile:** Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.
  - **Reflow Profile**
    - Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A typical heating rate is 1- 2°C/sec.
    - Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 120-150 seconds at 150°C.
    - Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 10 seconds. Maximum soldering temperatures should be in the range 215-220°C, with a maximum limit of 225°C.
    - Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. Figure 1 indicates the recommended soldering profile.
- **Solder Joint Characteristics:** Proper operation of this device depends on a reliable void-free attachment of the heatsink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.
- **Rework Considerations:** Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should not be subjected to more than 225°C and reflow solder in the molten state for more than 5 seconds. No more than 2 rework operations should be performed.

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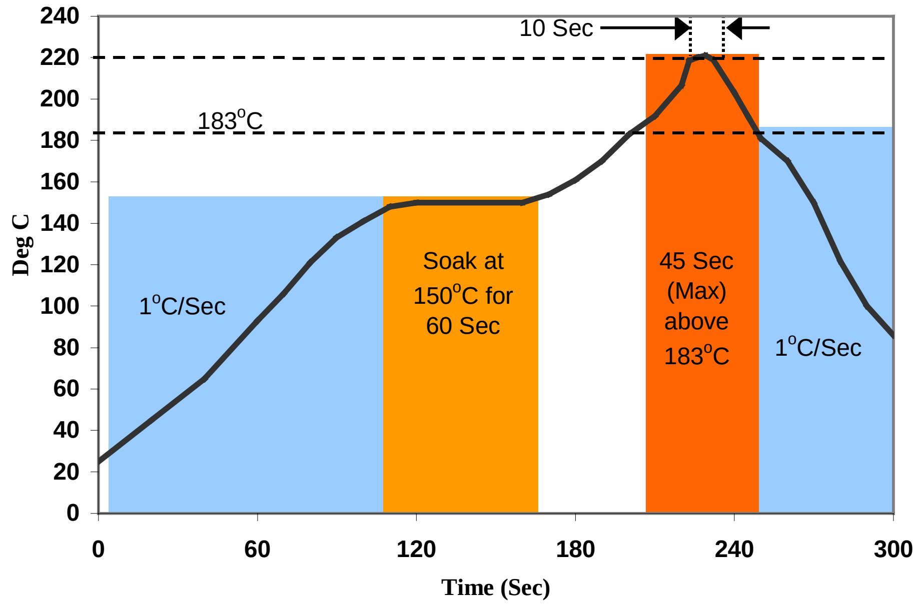
Figure 4
Recommended Solder Reflow Profile



Performance Data

Measured performance for typical production amplifiers is represented in the figures below. Key characteristics such as gain, efficiency, output power and linearity are shown for both AMPS and CDMA operation.

Figure 5

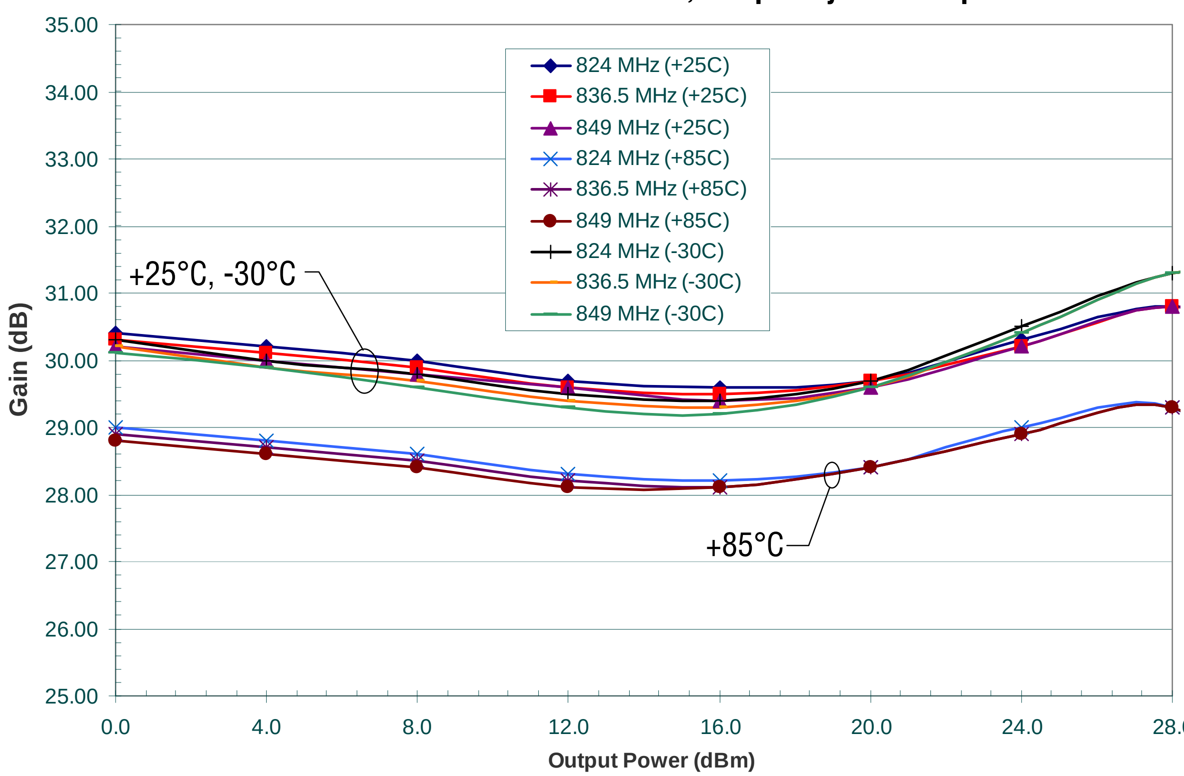


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Figure 6

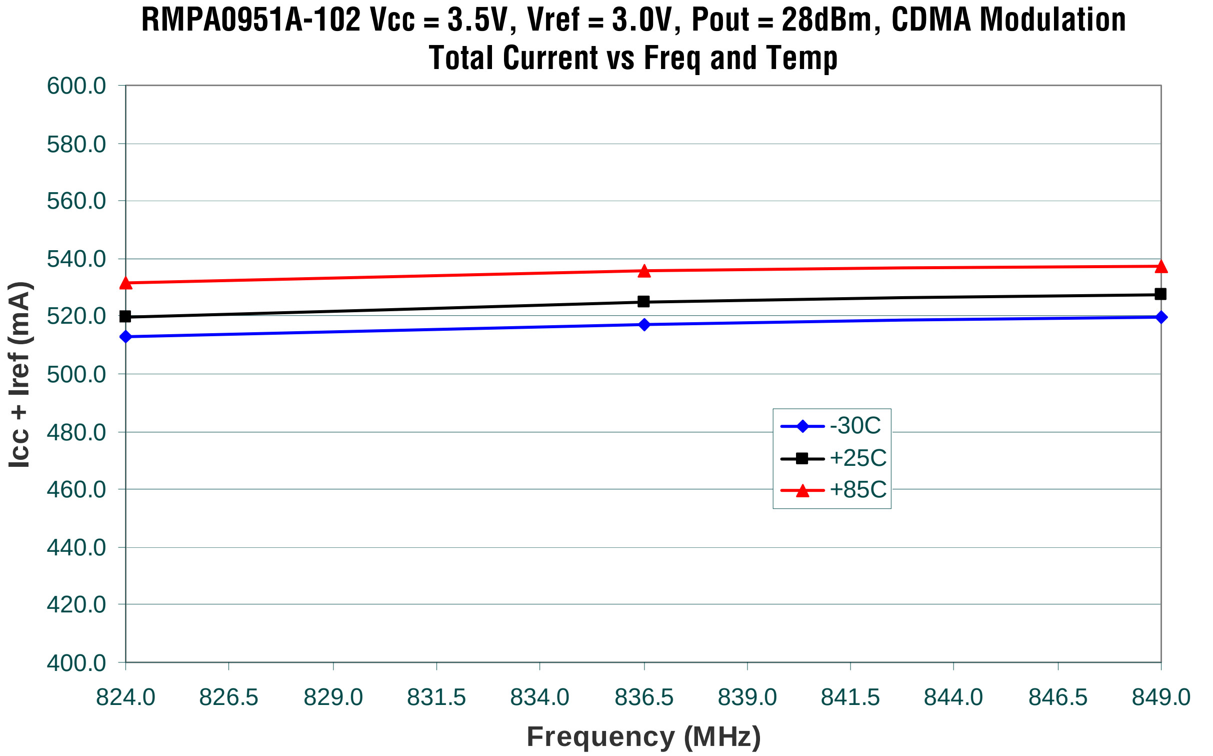

Figure 7

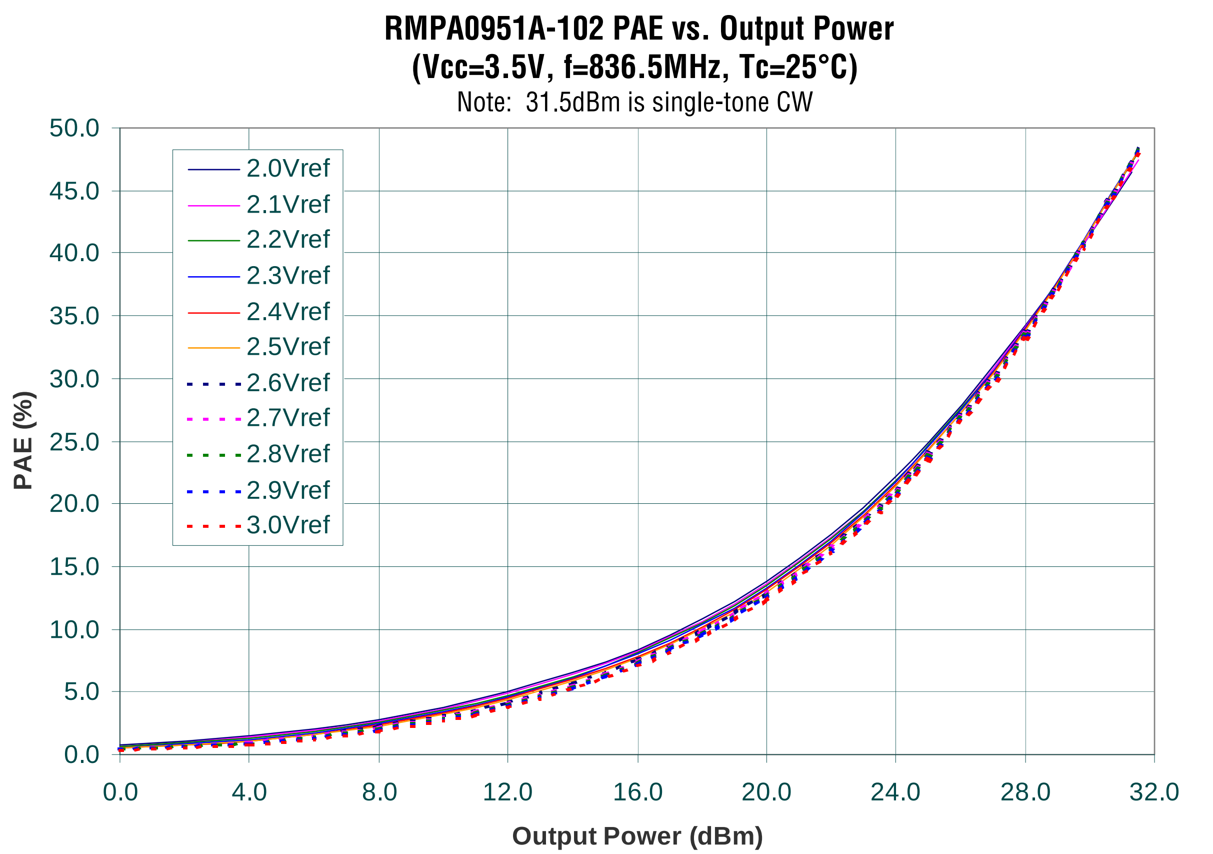

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Figure 8

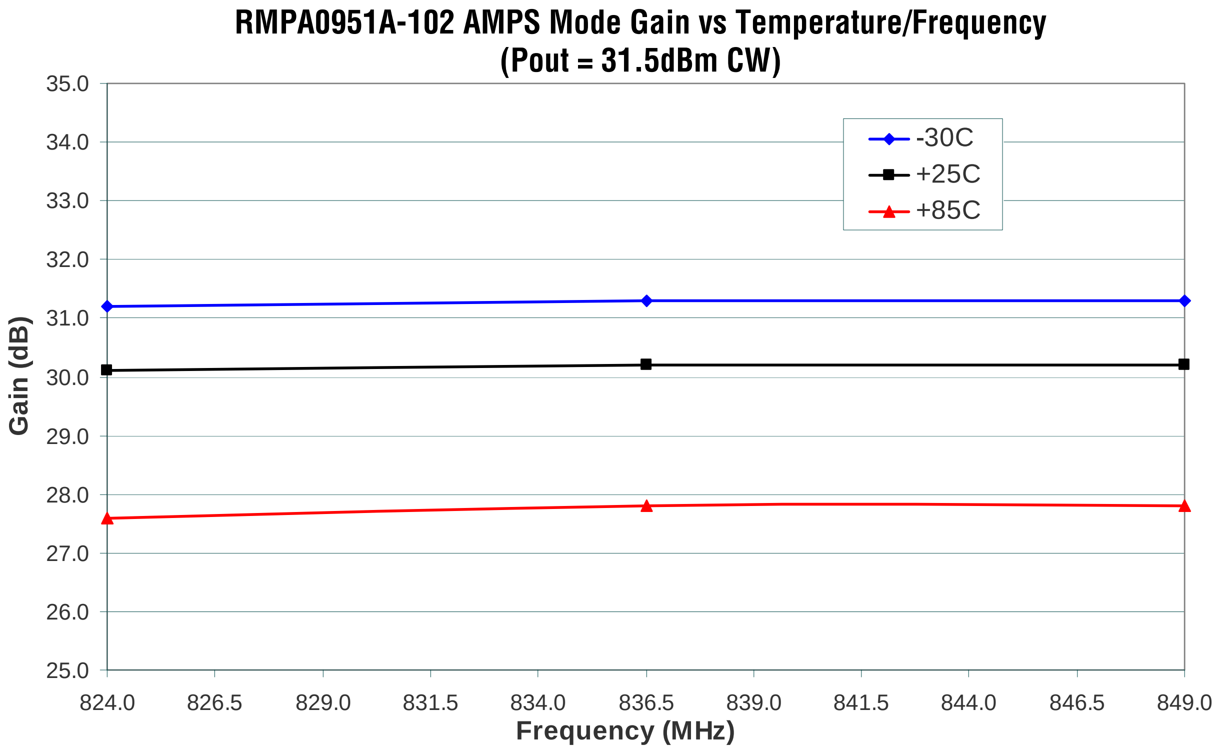

Figure 9

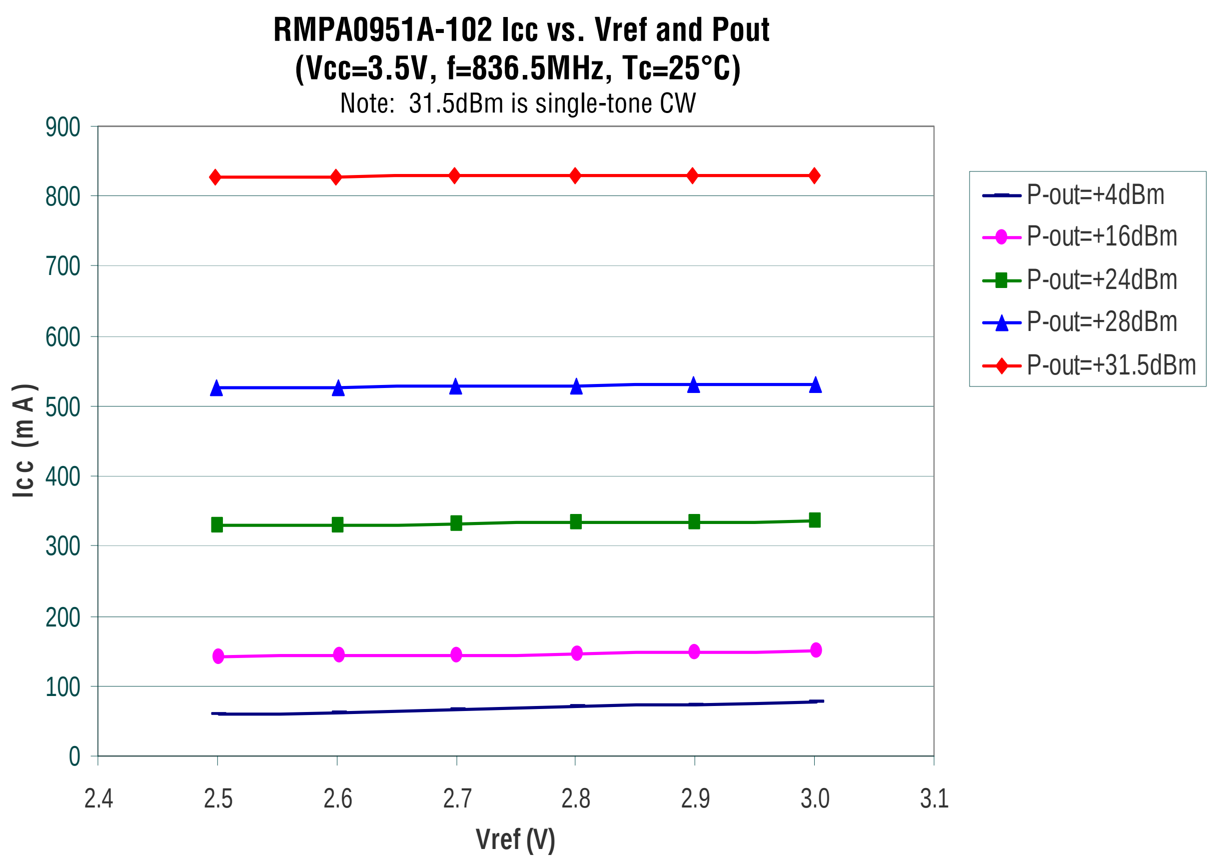

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Figure 10

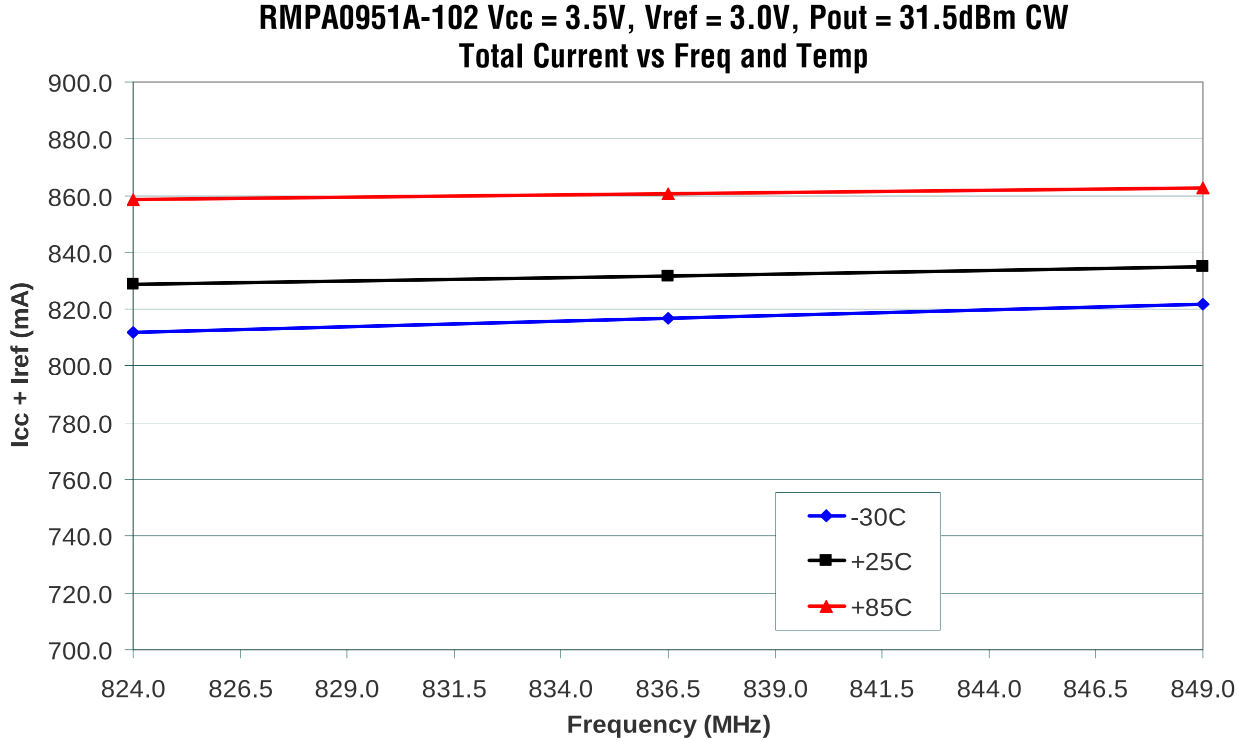

Figure 11

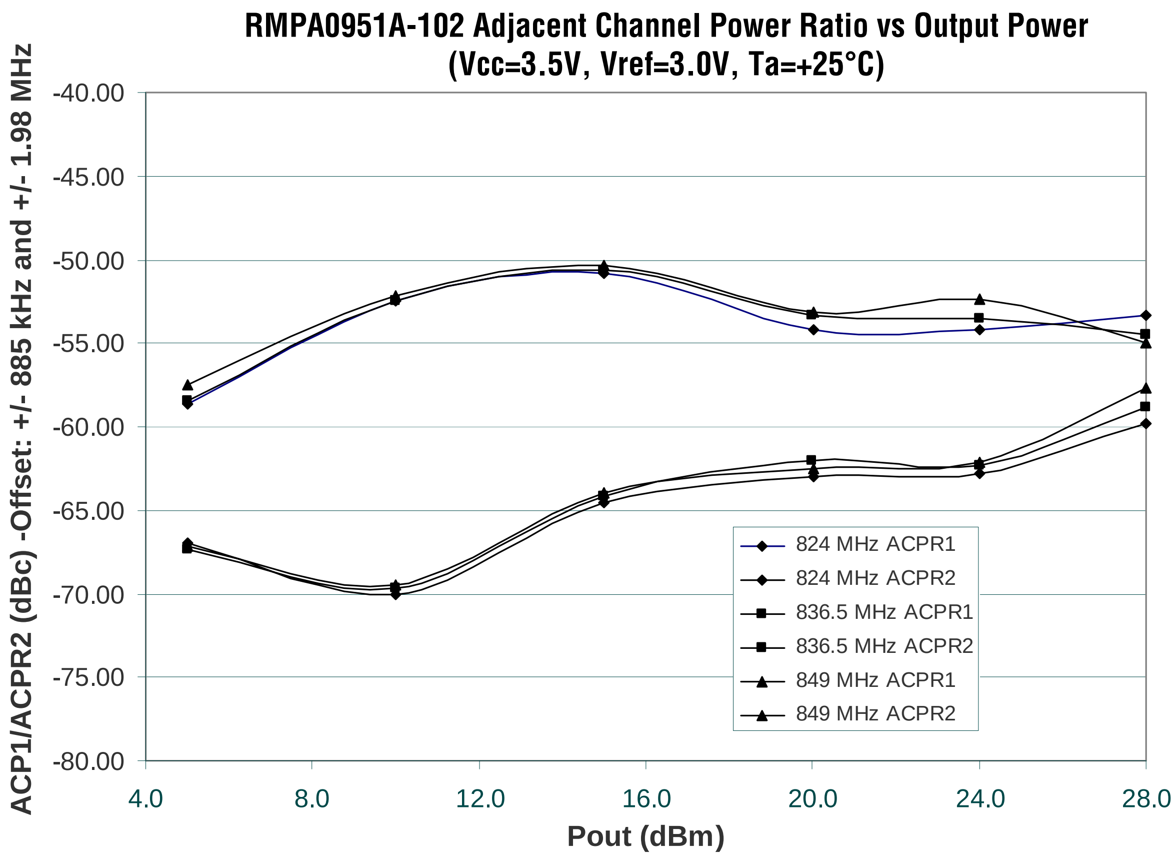

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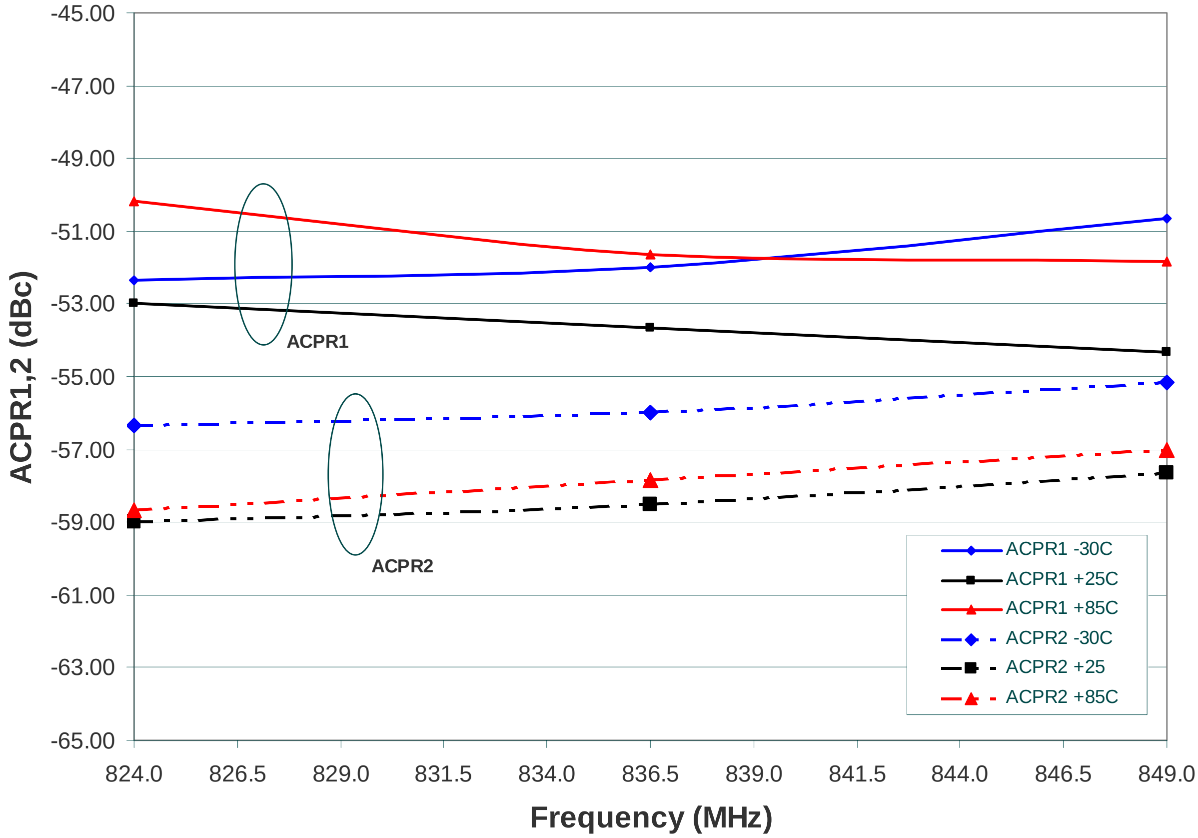
Figure 12

RMPA0951A-102
Vcc = 3.5V, Vref = 3.0V Pout = 28dBm,
CDMA Modulation ACPR1 @ 885kHz,
ACPR2 @ 1.98MHz vs Frequency and Temperature



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DC Power Management for Reduced-Power Operating Modes

Many Cellular/PCS handsets can benefit from gain control and DC power management to optimize transmitter performance while operating at backed-off output power levels. Oftentimes, cellular systems will operate at 10-20 dB back-off from maximum-rated linear power and peak power-added efficiency. The ability to reduce current consumption under these conditions, without sacrificing linearity, is critical to extending battery life in next-generation mobile phones.

The RMPA0951A-102 PA offers the ability to lower quiescent current by more than 60 percent and small-signal gain by 10-12 dB using a single control voltage (Vref). Even with the amplifier biased for lowest current consumption, high linearity is maintained over the full operating temperature range and at output power levels up to +16 dBm. Bias and gain control through Vref provides complete flexibility for the handset designer, allowing the user to define the operation by either an analog (continuously-variable) or digital (discrete-step) voltage input. As an example, reducing the Vref voltage from 3.0V (nominal) to 2.2V can lower PA current consumption by more than 20 percent at an output power of +12 dBm.

The following charts demonstrate analog and digital control techniques for minimizing DC power consumption at reduced RF output power levels. Figures 14 through 17 characterize analog control over a reference voltage (Vref) range of 1.8V to 3.0V. Using analog bias control, quiescent current is reduced to less than 30 mA and small-signal gain is reduced by 12 dB at Vref=1.8V. Operating current at +12 dBm is also reduced by 20 percent (25 mA) at Vref=2.2V and by more than 50 percent (50 mA) at the lowest reference voltage (Vref=1.8V) compared with fixed-bias operation at Vref=3.0V. In all cases, DC current savings is achieved while fully complying with IS-95 linearity requirements.

Figures 18 through 22 feature digital control performance using three discrete voltage levels (3.0V, 2.2V, 1.8V) to optimize linear PA performance over three output power ranges (< +4 dBm, +4 dBm to +16 dBm, >+16 dBm). Alternate output power ranges can be selected depending on the power-probability use in the cellular system.

Figure 13
Cellular PAM-Digital Control Mode

Parameter	Min	Typical	Max	Units	Conditions
Low-Power Range			+8	dBm	Vref=1.8 V typ.
Current		50		mA	
Gain		24		dB	
Linearity		-50		dBc	
Mid-Power Range	+8	+12	+16	dBm	Vref=2.2 V typ.
Current		120		mA	
Gain		28.5		dB	
Linearity		-50		dBc	
High-Power Range	+16		+28	dBm	Vref=3.0 V typ.
Current		540		mA	Pout=+28 dBm
Gain		32.5		dB	
Linearity		-38		dBc	

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Figure 14

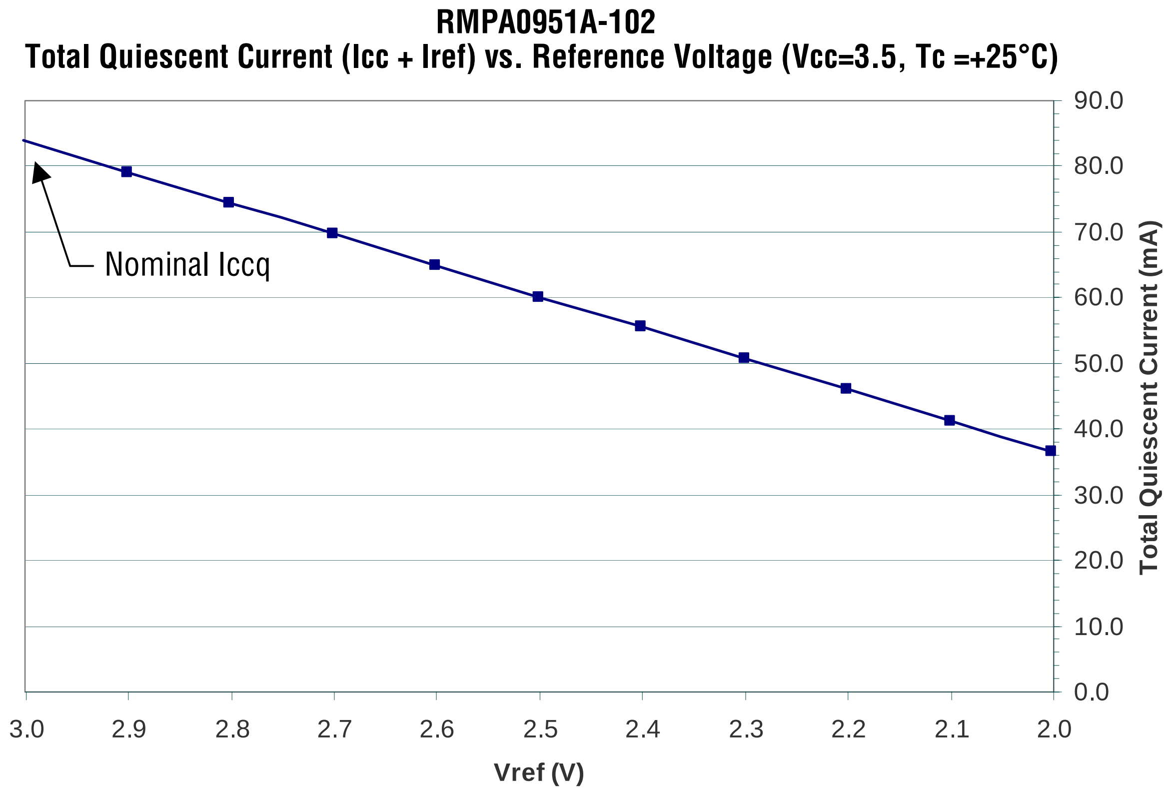

Figure 15

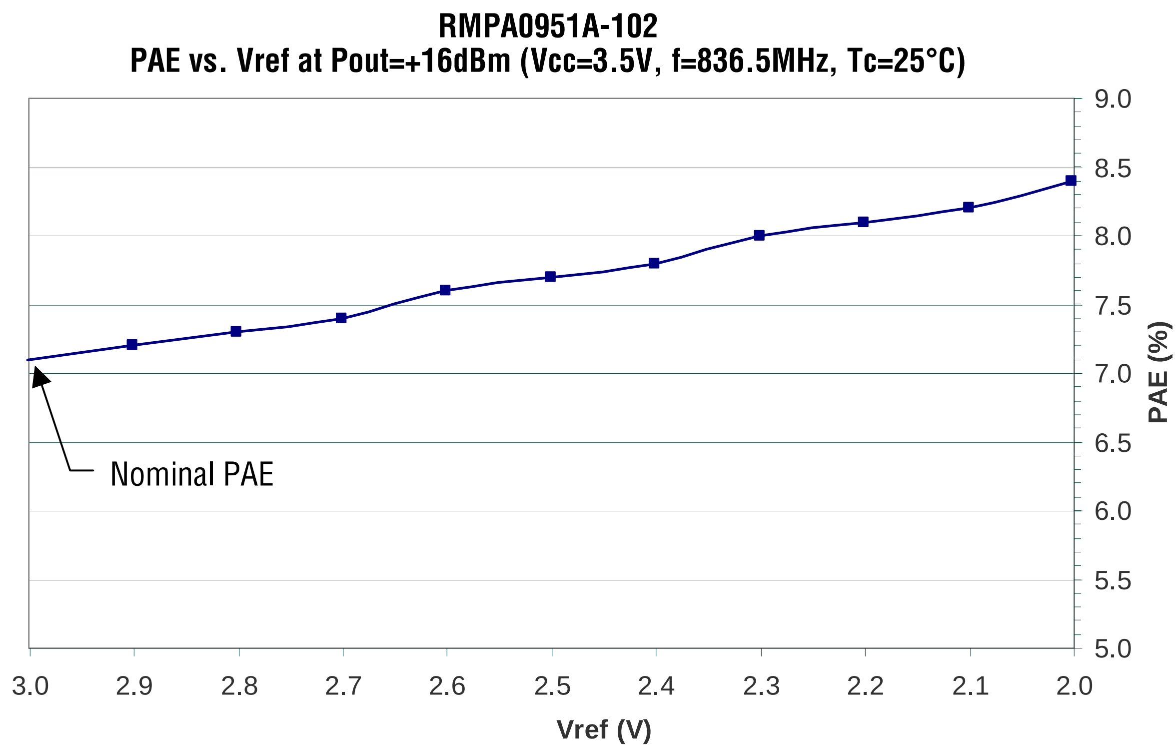

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Figure 16

RMPA0951A-102 Small-Signal Gain vs. Reference Voltage (Vcc=3.5V, f=836.5MHz, Pout=0 dBm, Tc=25°C)

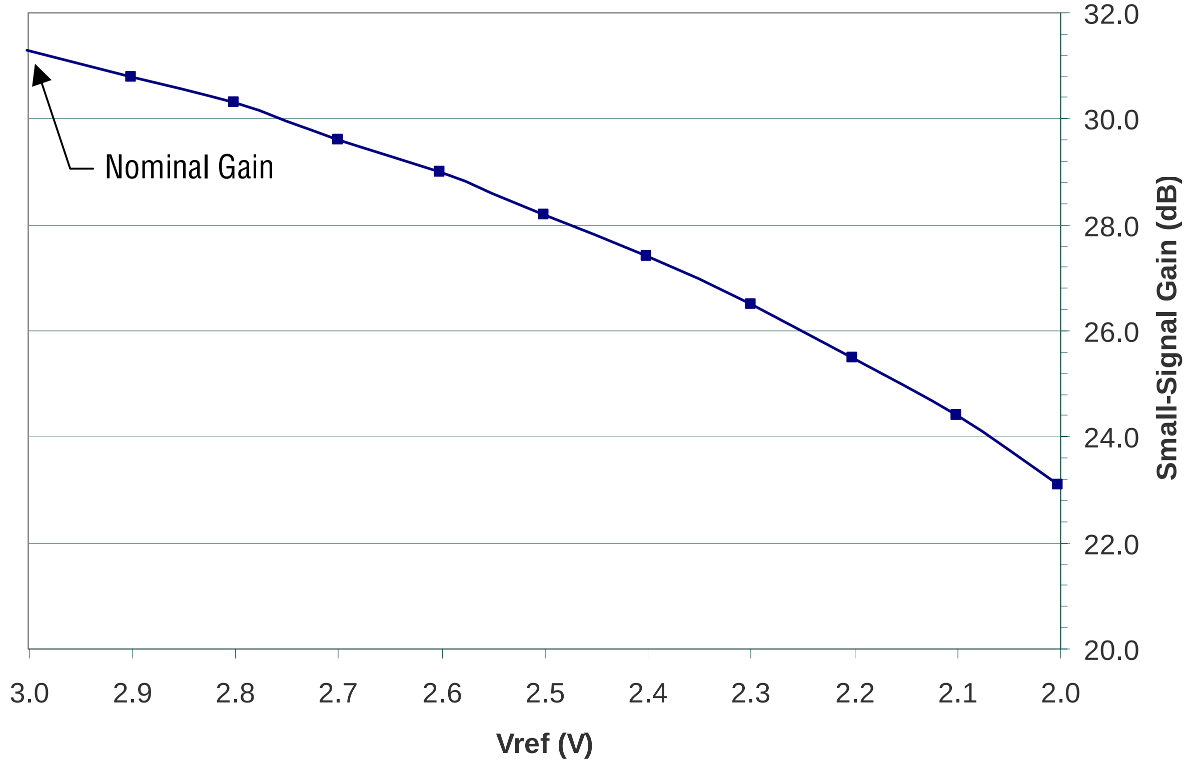

Figure 17

RMPA0951A-102 Total Current (Icc + Iref) vs. Output Power and Vref (Vcc=3.5V, f=836.5 MHz, Tc=25°C)

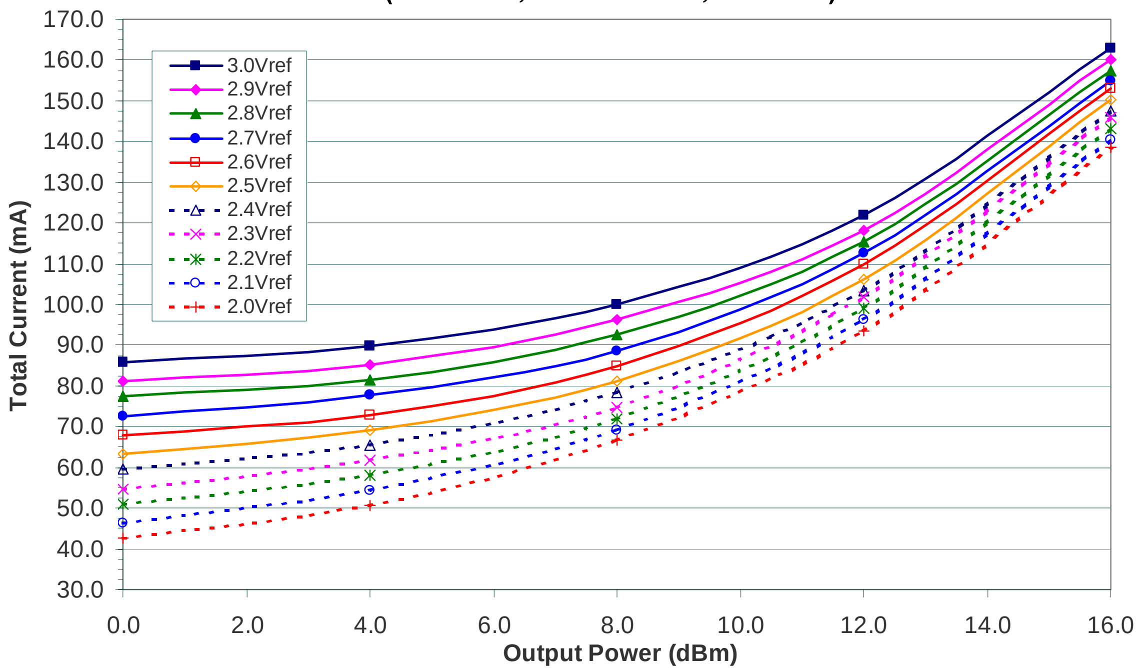

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Figure 18

RMPA0951A-102 Total Current (Icc + Iref) vs Reference Voltage and Temperature (Vcc=3.5V, f=836.5MHz, Pout=0 dBm)

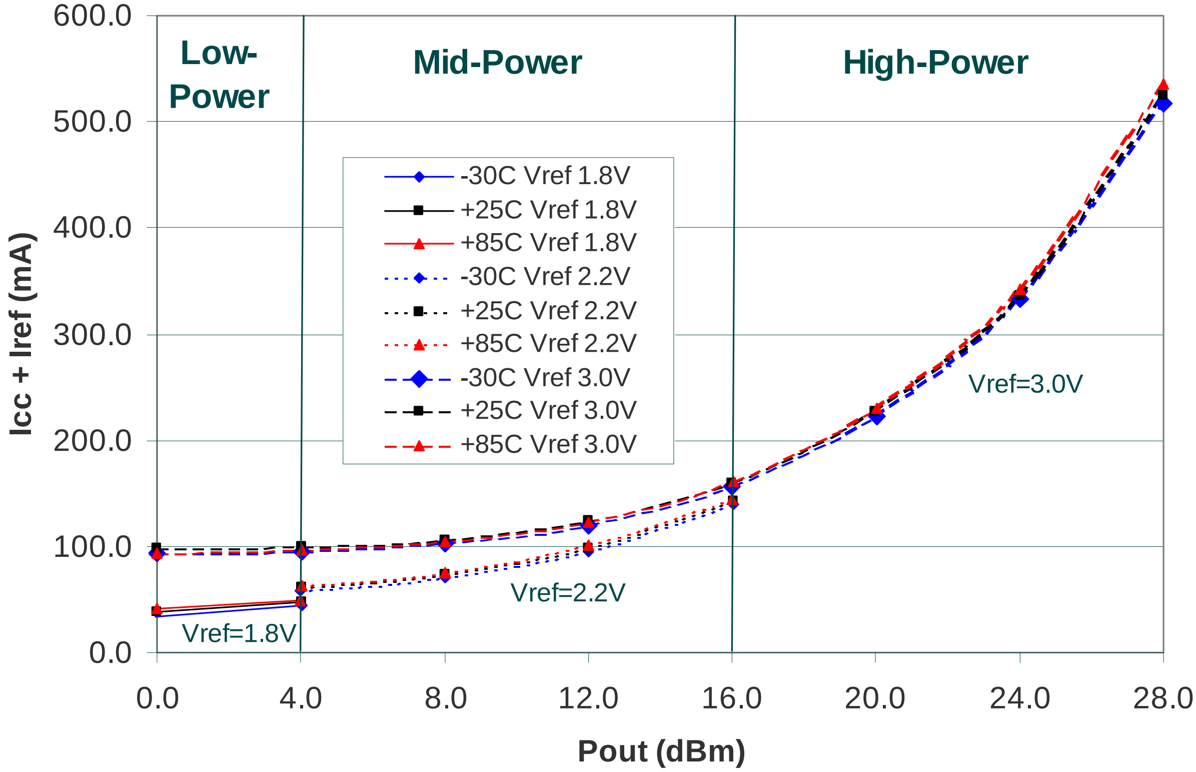

Figure 19

RMPA0951A-102 Freq = 836.5 MHz, Vcc = 3.5V Total Current (Icc + Iref) vs Pout and Temp (Digital Control)

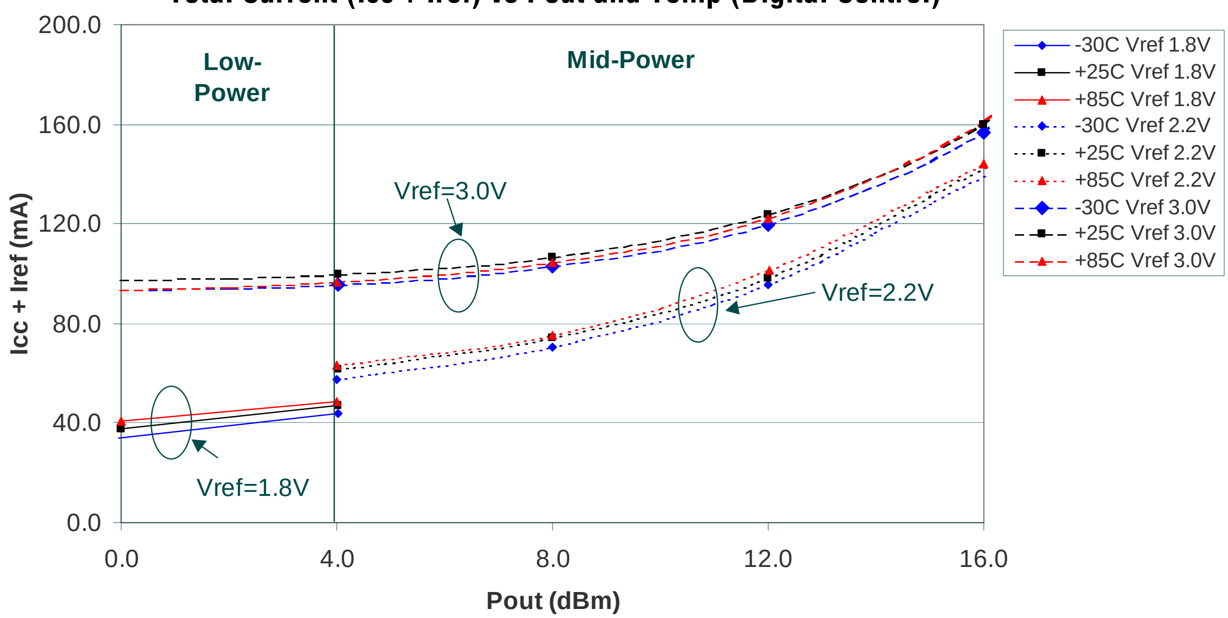

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Figure 20

RMPA0951A-102
Freq = 836.5 MHz, Vcc = 3.5V Gain vs Pout and Temp (Digital Control)

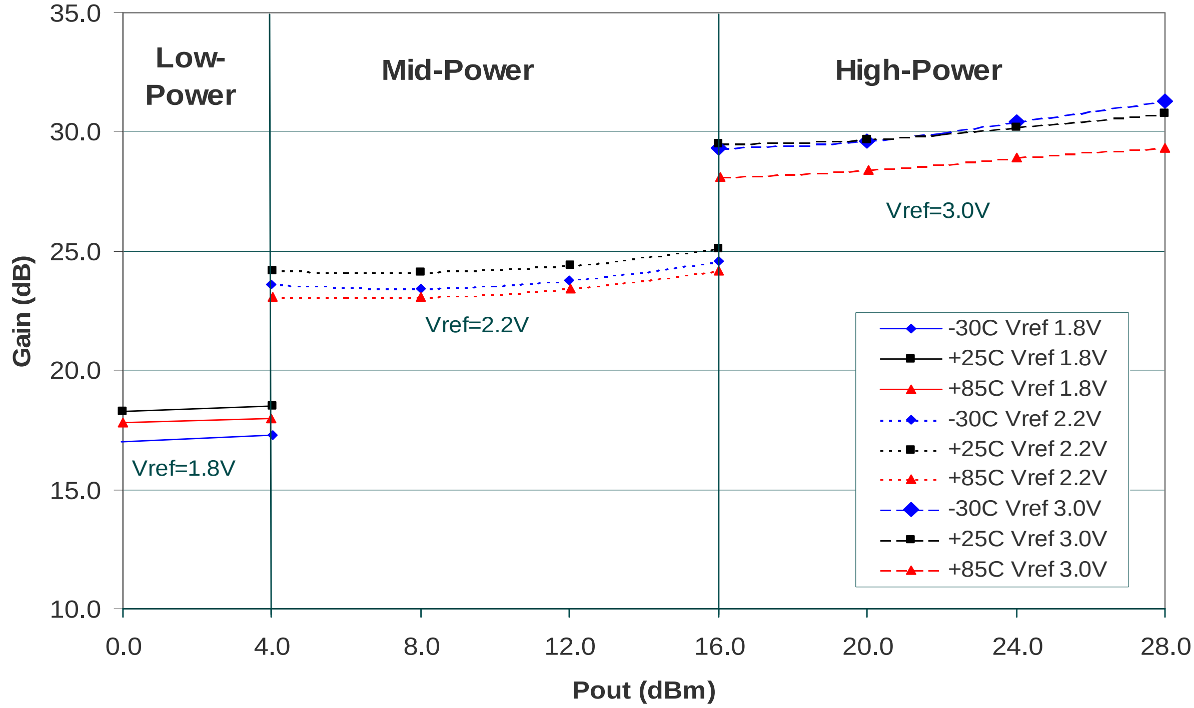

Figure 21

RMPA0951A-102
Freq = 836.5 MHz, Vcc = 3.5V ACPR1 vs Pout and Temp (Digital Control)

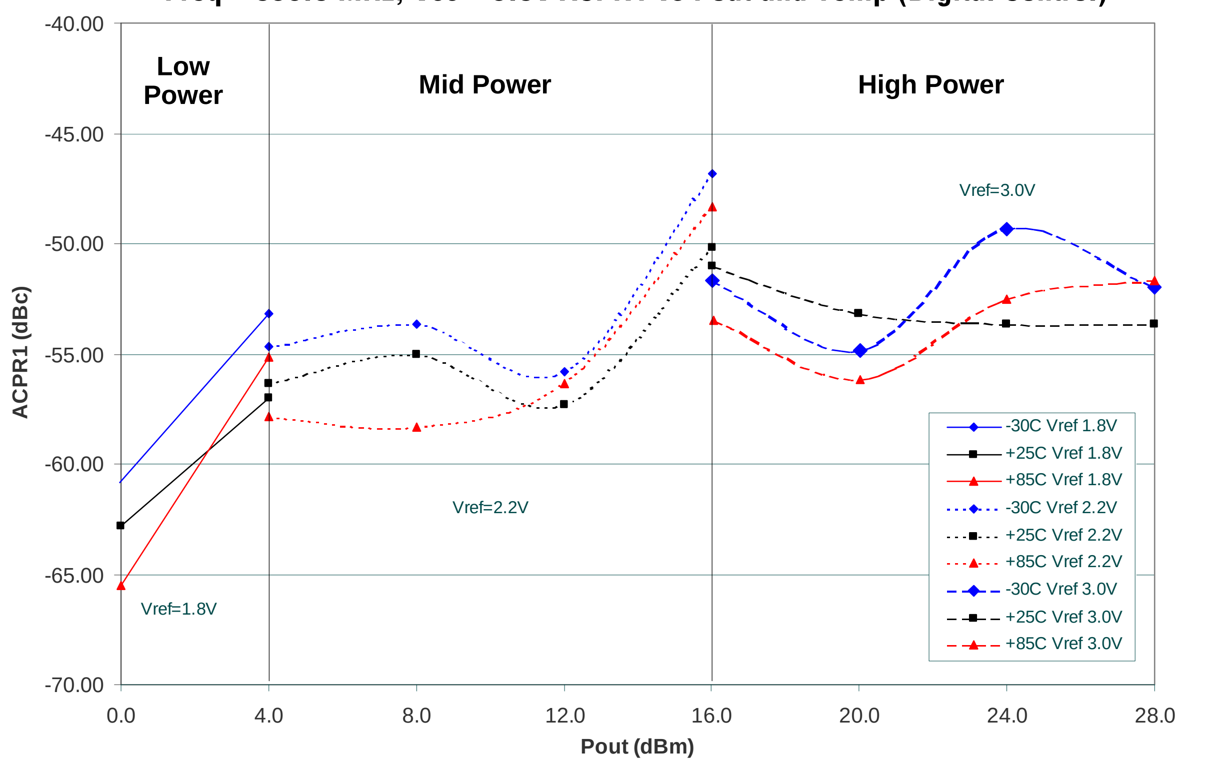

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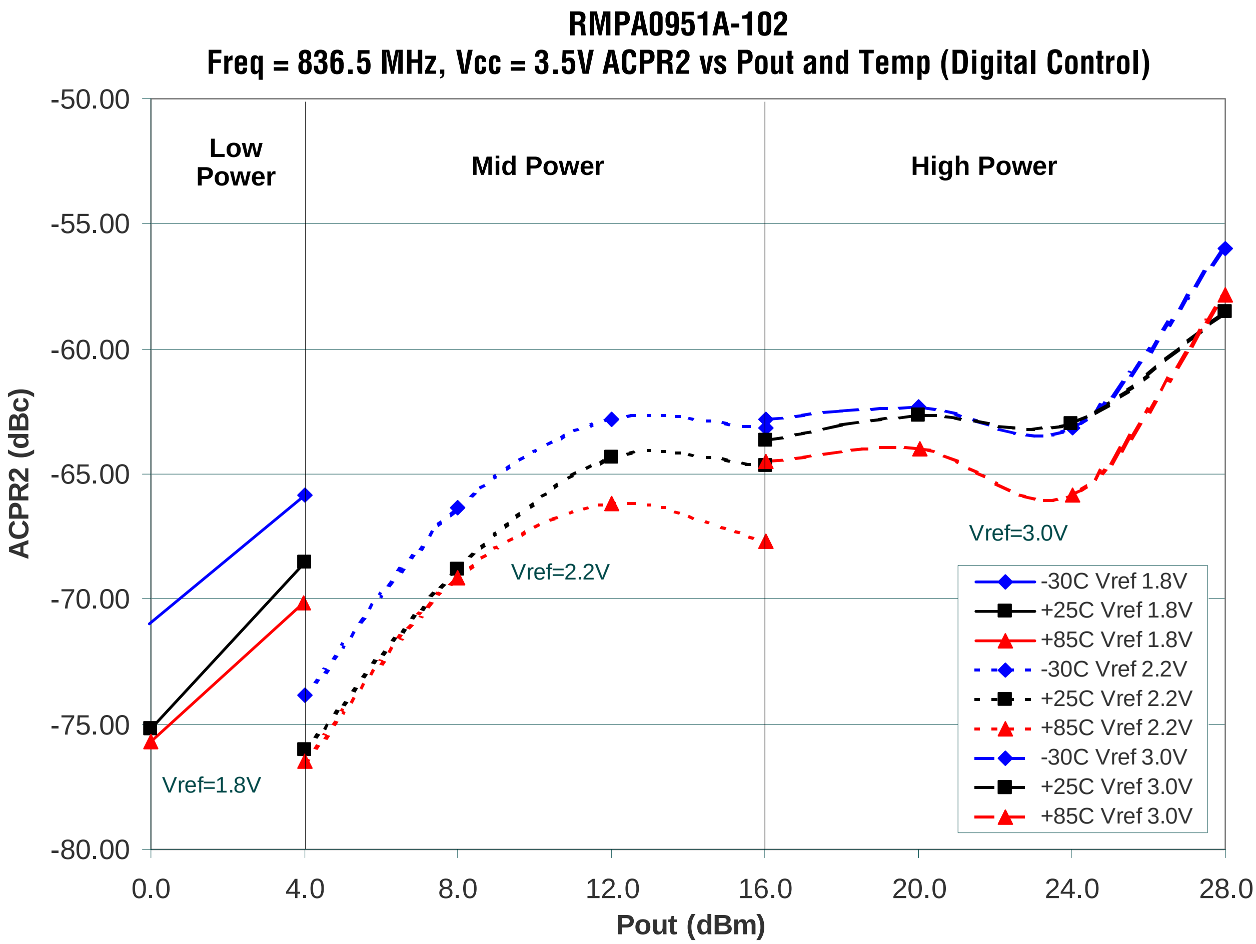
Figure 22



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