To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HAT2085R

Silicon N Channel MOS FET
High Speed Power Switching

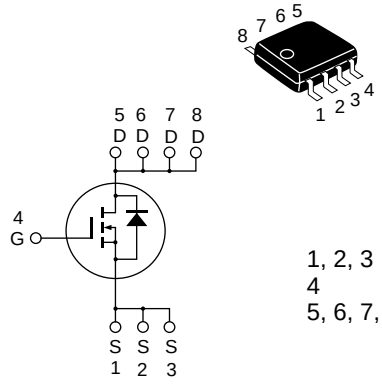
ADE-208-1232 (Z)
Target Specification 1st. Edition
Dec. 2000

Features

- Low on-resistance
- Low drive current
- High density mounting

Outline

SOP–8



1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	200	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	(2)	A
Drain peak current	$I_{D(pulse)}$ Note1	(16)	A
Body-drain diode reverse drain current	I_{DR}	(2)	A
Channel dissipation	Pch Note2	2.5	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW≤ 10s

Electrical Characteristics (Ta = 25°C)

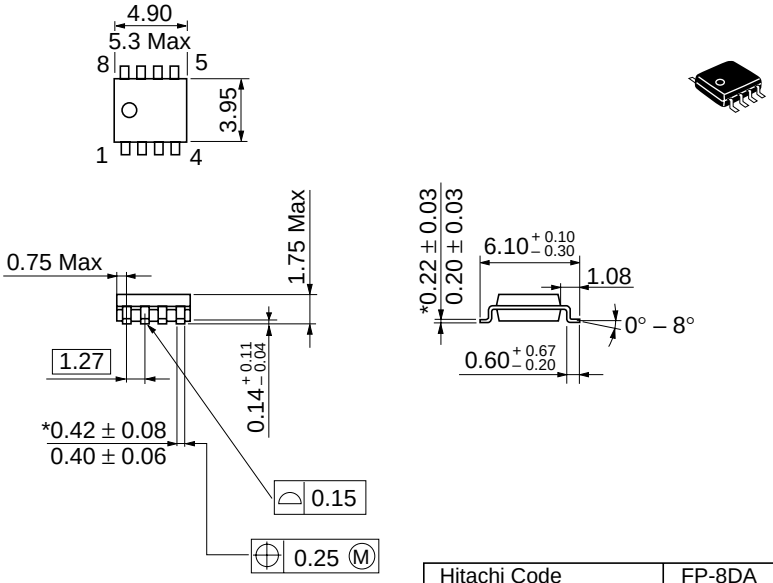
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	I_D = 10mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	µA	V_{GS} = ±30V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	1	µA	V_{DS} = 200 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	(3.0)	—	(4.5)	V	I_D = 1mA, V_{DS} = 10V
Static drain to source on state resistance	$R_{DS(on)}$	—	(0.49)	(0.64)	Ω	I_D = 1A, V_{GS} = 10V Note3
Forward transfer admittance	$\|y_{fs}\|$	(1.2)	(2.0)	—	S	I_D = 1A, V_{DS} = 10V Note3
Input capacitance	Ciss	—	(300)	—	pF	V_{DS} = 25V
Output capacitance	Coss	—	(43)	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	(12)	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	(20)	—	ns	V_{DD} ≅ 100V, I_D = 1A
Rise time	t_r	—	(10)	—	ns	V_{GS} = 10V
Turn-off delay time	$t_{d(off)}$	—	(50)	—	ns	R_L = 100Ω
Fall time	t_f	—	(10)	—	ns	R_g = 10Ω
Total gate charge	Qg	—	(10)	—	nC	V_{DD} = 160V
Gate to source charge	Qgs	—	(2)	—	nC	V_{GS} = 10V
Gate to drain charge	Qgd	—	(5)	—	nC	I_D = 2A
Body–drain diode forward voltage	V_{DF}	—	(0.8)	(1.2)	V	I_F = 2A, V_{GS} = 0 Note3
Body–drain diode reverse recovery time	t_{rr}	—	(75)	—	ns	I_F = 2A, V_{GS} = 0 diF/ dt =100A/µs

Note: 3. Pulse test

Package Dimensions

As of January, 2001

Unit: mm



*Dimension including the plating thickness

Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.085 g

Cautions

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