

R1LP0408C-C Series

4M SRAM (512-kword $\times$ 8-bit)

REJ03C0077-0200Z

Rev. 2.00

May.26.2004

Description

The R1LP0408C-C is a 4-Mbit static RAM organized 512-kword $\times$ 8-bit. R1LP0408C-C Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). The R1LP0408C-C Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has packaged in 32-pin SOP, 32-pin TSOP II.

Features

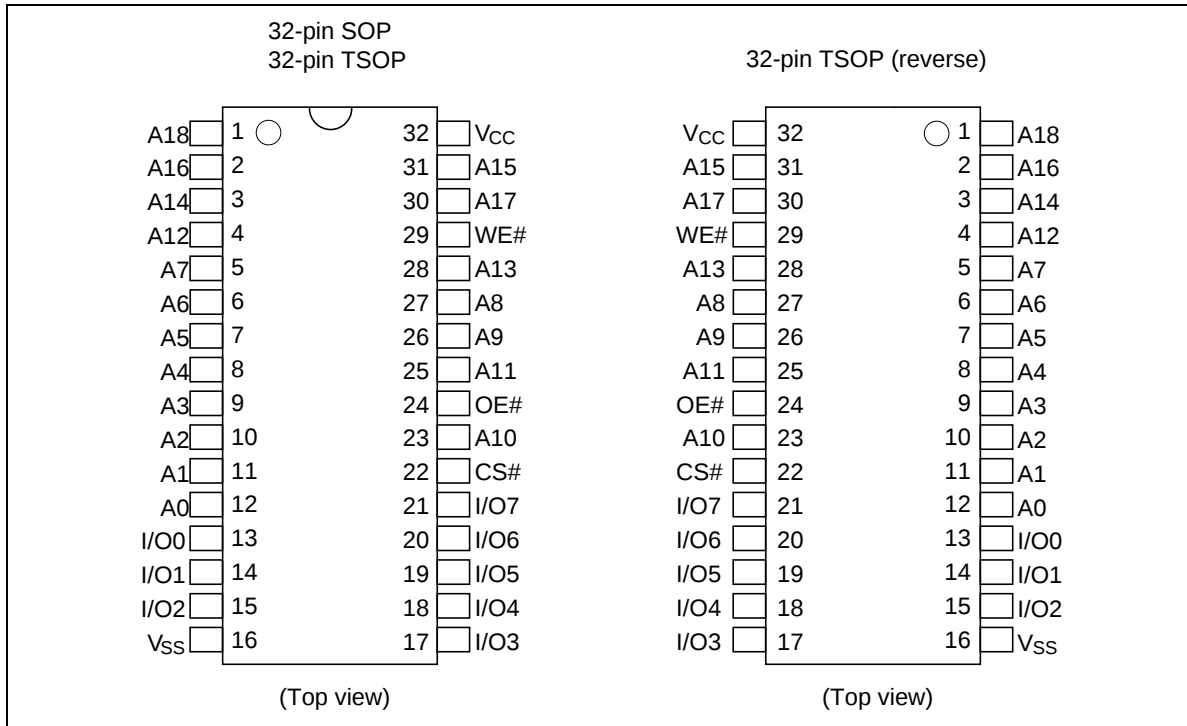
- Single 5 V supply: 5 V $\pm$ 10%
- Access time: 55/70 ns (max)
- Power dissipation:
 - Active: 10 mW/MHz (typ)
 - Standby: 4 μ W (typ)
- Completely static memory.
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
 - Three state output
- Directly TTL compatible.
 - All inputs and outputs
- Battery backup operation.
- Operating temperature: -20 to $+70^{\circ}\text{C}$

R1LP0408C-C Series

Ordering Information

Type No.	Access time	Package
R1LP0408CSP-5SC	55 ns	525-mil 32-pin plastic SOP (32P2M-A)
R1LP0408CSP-7LC	70 ns	
R1LP0408CSB-5SC	55 ns	400-mil 32-pin plastic TSOP II (32P3Y-H)
R1LP0408CSB-7LC	70 ns	
R1LP0408CSC-5SC	55 ns	400-mil 32-pin plastic TSOP II reverse (32P3Y-J)
R1LP0408CSC-7LC	70 ns	

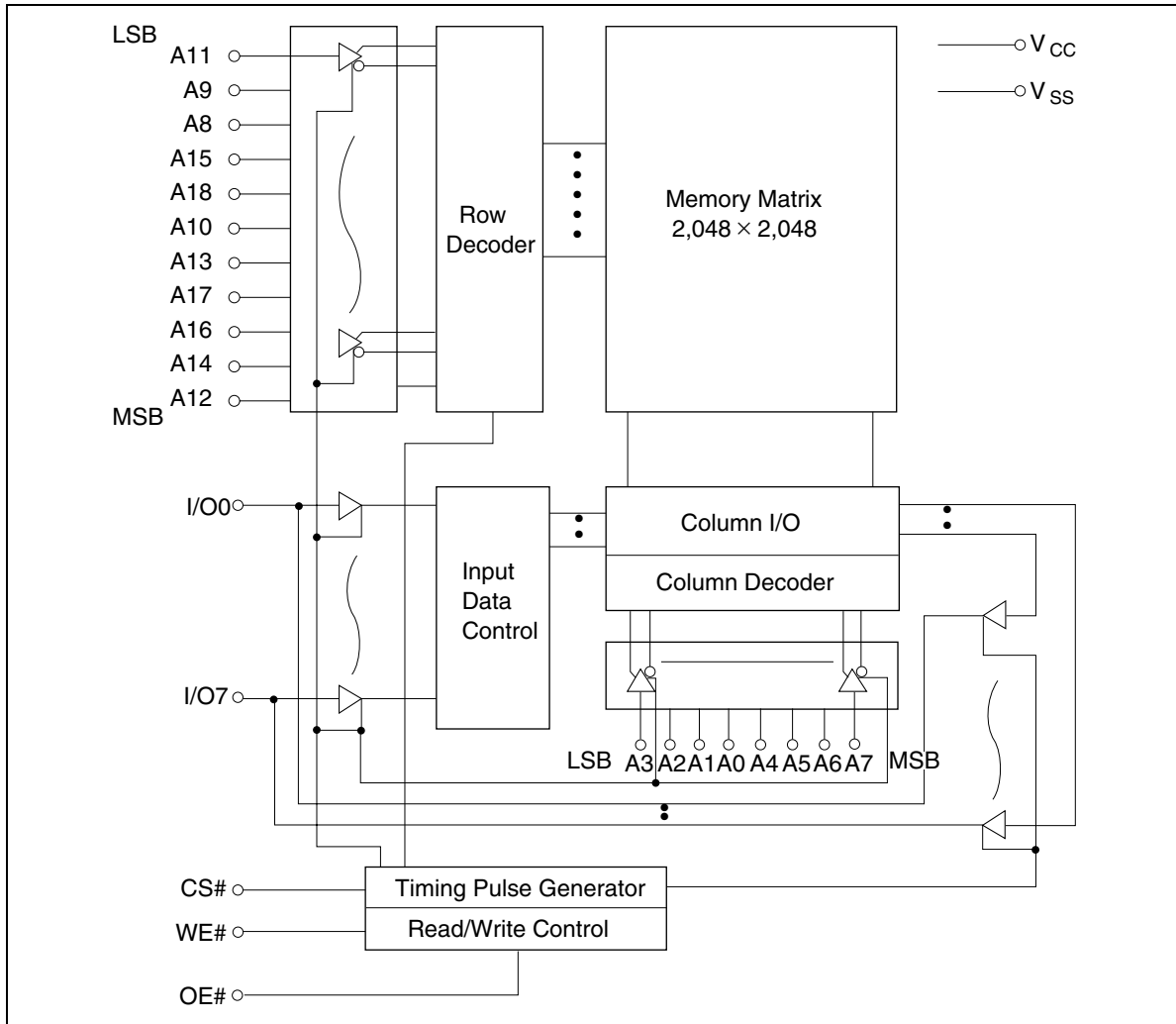
Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS# (CS)	Chip select
OE# (OE)	Output enable
WE# (WE)	Write enable
V _{CC}	Power supply
V _{SS}	Ground

Block Diagram



Operation Table

WE#	CS#	OE#	Mode	V _{CC} current	I/O0 to I/O7	Ref. cycle
×	H	×	Not selected	I _{SB} , I _{SB1}	High-Z	—
H	L	H	Output disable	I _{CC}	High-Z	—
H	L	L	Read	I _{CC}	Dout	Read cycle
L	L	H	Write	I _{CC}	Din	Write cycle (1)
L	L	L	Write	I _{CC}	Din	Write cycle (2)

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V _{SS}	V _{CC}	−0.5 to +7.0	V
Terminal voltage on any pin relative to V _{SS}	V _T	−0.5* ¹ to V _{CC} + 0.3* ²	V
Power dissipation	P _T	0.7	W
Operating temperature	T _{opr}	−20 to +70	°C
Storage temperature range	T _{stg}	−65 to +150	°C
Storage temperature range under bias	T _{bias}	−20 to +85	°C

Notes: 1. V_T min: −3.0 V for pulse half-width ≤ 30 ns.

2. Maximum voltage is +7.0 V.

DC Operating Conditions

(T_a = −20 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	−0.3* ¹	—	0.8	V

Note: 1. V_{IL} min: −3.0 V for pulse half-width ≤ 30 ns.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions		
Input leakage current	$ I_{Li} $	—	—	1	μA	$V_{in} = V_{SS}$ to V_{CC}		
Output leakage current	$ I_{Lo} $	—	—	1	μA	$CS\# = V_{IH}$ or $OE\# = V_{IH}$ or $WE\# = V_{IL}$ or $V_{I/O} = V_{SS}$ to V_{CC}		
Operating current	I_{CC}	—	1.5^{*1}	3	mA	$CS\# = V_{IL}$, Others = V_{IH}/V_{IL} , $I_{I/O} = 0$ mA		
Average operating current	I_{CC1}	—	8^{*1}	25	mA	Min. cycle, duty = 100%, $CS\# = V_{IL}$, Others = V_{IH}/V_{IL} , $I_{I/O} = 0$ mA		
	I_{CC2}	—	2^{*1}	5	mA	Cycle time = 1 μs , duty = 100%, $I_{I/O} = 0$ mA, $CS\# \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V		
Standby current	I_{SB}	—	0.1^{*1}	0.5	mA	$CS\# = V_{IH}$		
Standby current	−5SC	to +70°C	I_{SB1}	—	8	μA	$V_{in} \geq 0$ V, $CS\# \geq V_{CC} - 0.2$ V	
		to +40°C	I_{SB1}	—	1.0^{*2}	3		μA
		to +25°C	I_{SB1}	—	0.8^{*1}	3		μA
	−7LC	to +70°C	I_{SB1}	—	16	μA		
		to +40°C	I_{SB1}	—	1.0^{*2}	10		μA
		to +25°C	I_{SB1}	—	0.8^{*1}	10		μA
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.1$ mA		
Output high voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -1.0$ mA		
	V_{OH2}	2.6	—	—	V	$I_{OH} = -0.1$ mA		

Notes: 1. Typical values are at $V_{CC} = 5.0 \text{ V}$, $T_a = +25^\circ\text{C}$ and specified loading, and not guaranteed.

2. Typical values are at $V_{CC} = 5.0 \text{ V}$, $T_a = +40^\circ\text{C}$ and specified loading, and not guaranteed.

Capacitance

($T_a = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	8	pF	$V_{in} = 0 \text{ V}$	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0 \text{ V}$	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

(Ta = -20 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{IL} = 0.4 V, V_{IH} = 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C_L (50 pF) (R1LP0408C-5SC)
1 TTL Gate + C_L (100 pF) (R1LP0408C-7LC)
(Including scope and jig)

Read Cycle

		R1LP0408C-C					
		-5SC		-7LC			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t _{RC}	55	—	70	—	ns	
Address access time	t _{AA}	—	55	—	70	ns	
Chip select access time	t _{CO}	—	55	—	70	ns	
Output enable to output valid	t _{OE}	—	25	—	35	ns	
Chip select to output in low-Z	t _{LZ}	10	—	10	—	ns	2
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	ns	2
Chip deselect to output in high-Z	t _{HZ}	0	20	0	25	ns	1, 2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1, 2
Output hold from address change	t _{OH}	10	—	10	—	ns	

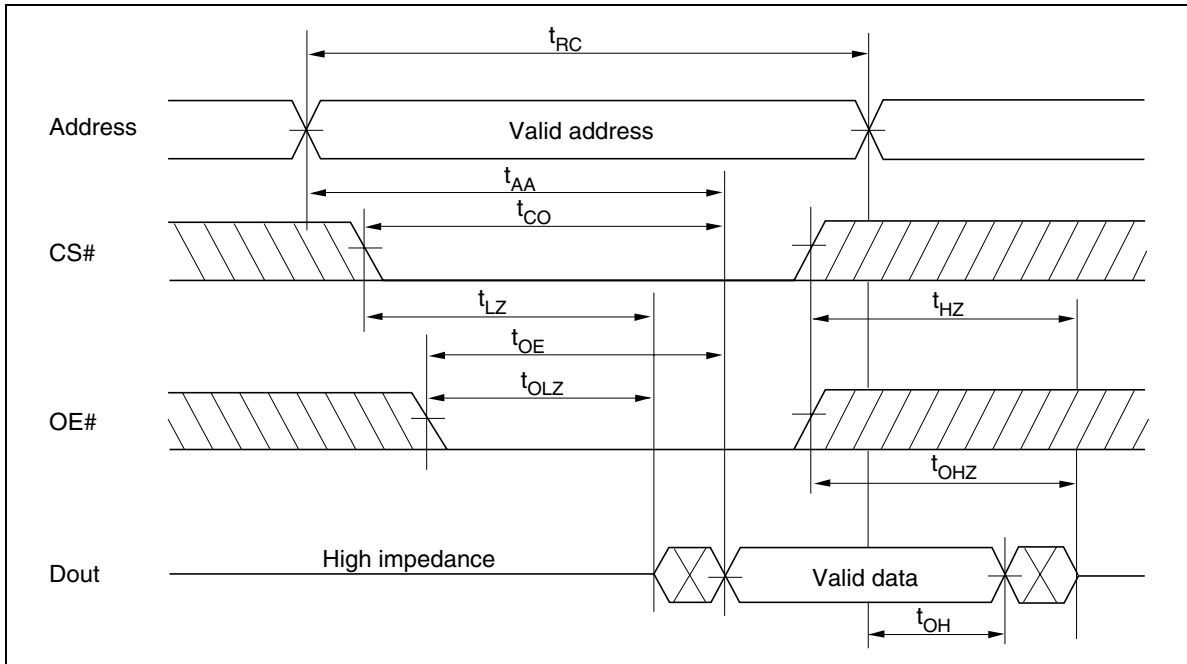
Write Cycle

		R1LP0408C-C					
		-5SC		-7LC			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	55	—	70	—	ns	
Chip selection to end of write	t _{CW}	50	—	60	—	ns	4
Address setup time	t _{AS}	0	—	0	—	ns	5
Address valid to end of write	t _{AW}	50	—	60	—	ns	
Write pulse width	t _{WP}	40	—	50	—	ns	3, 12
Write recovery time	t _{WR}	0	—	0	—	ns	6
Write to output in high-Z	t _{WHZ}	0	20	0	25	ns	1, 2, 7
Data to write time overlap	t _{DW}	25	—	30	—	ns	
Data hold from write time	t _{DH}	0	—	0	—	ns	
Output active from end of write	t _{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1, 2, 7

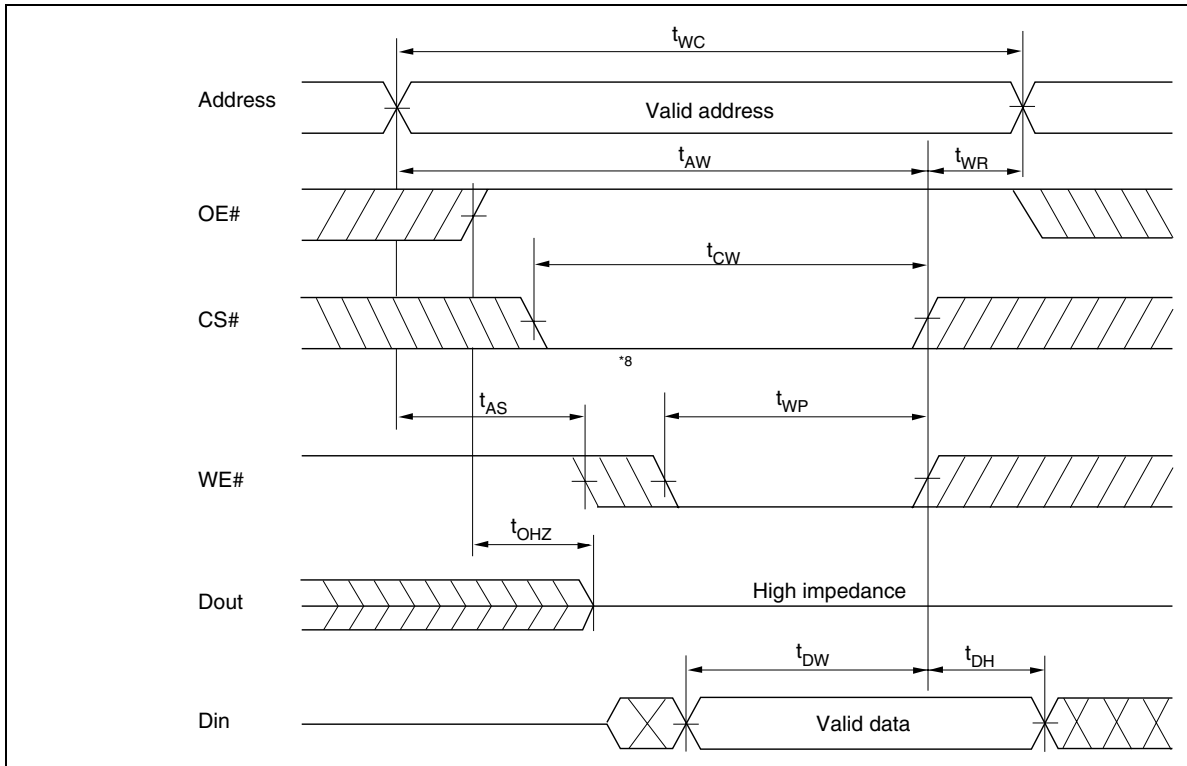
- Notes:
1. t_{HZ} , t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 2. This parameter is sampled and not 100% tested.
 3. A write occurs during the overlap (t_{WP}) of a low CS# and a low WE#. A write begins at the later transition of CS# going low or WE# going low. A write ends at the earlier transition of CS# going high or WE# going high. t_{WP} is measured from the beginning of write to the end of write.
 4. t_{CW} is measured from CS# going low to the end of write.
 5. t_{AS} is measured from the address valid to the beginning of write.
 6. t_{WR} is measured from the earlier of WE# or CS# going high to the end of write cycle.
 7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
 8. If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, the output remain in a high impedance state.
 9. Dout is the same phase of the write data of this write cycle.
 10. Dout is the read data of next address.
 11. If CS# is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
 12. In the write cycle with OE# low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

Timing Waveform

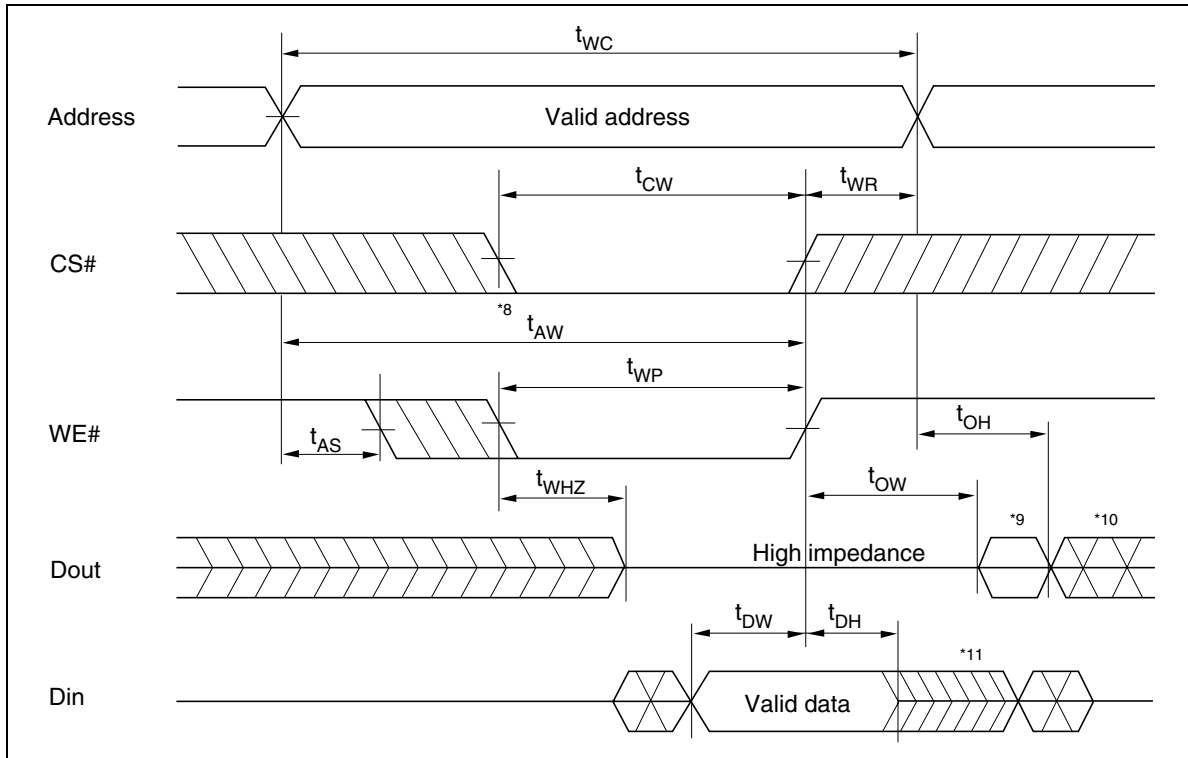
Read Timing Waveform ($WE\# = V_{IH}$)



Write Timing Waveform (1) (OE# Clock)



Write Timing Waveform (2) (OE# Low Fixed)



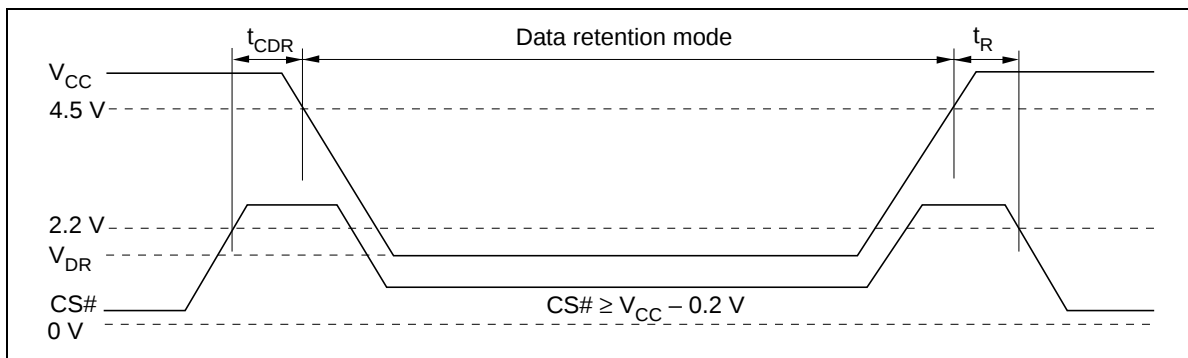
Low V_{CC} Data Retention Characteristics

($T_a = -20$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions* ³
V_{CC} for data retention	V_{DR}	2	—	—	V	$CS\# \geq V_{CC} - 0.2\text{ V}$, $V_{in} \geq 0\text{ V}$
Data retention current	-5SC	to $+70^\circ\text{C}$	I_{CCDR}	—	8	μA , $V_{CC} = 3.0\text{ V}$, $V_{in} \geq 0\text{ V}$
		to $+40^\circ\text{C}$	I_{CCDR}	—	1.0^{*2}	3 μA , $CS\# \geq V_{CC} - 0.2\text{ V}$
		to $+25^\circ\text{C}$	I_{CCDR}	—	0.8^{*1}	3 μA
	-7LC	to $+70^\circ\text{C}$	I_{CCDR}	—	16	μA
		to $+40^\circ\text{C}$	I_{CCDR}	—	1.0^{*2}	10 μA
		to $+25^\circ\text{C}$	I_{CCDR}	—	0.8^{*1}	10 μA
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}^{*4}	—	—	ns	

- Notes: 1. Typical values are at $V_{CC} = 3.0\text{ V}$, $T_a = +25^\circ\text{C}$ and specified loading, and not guaranteed.
2. Typical values are at $V_{CC} = 3.0\text{ V}$, $T_a = +40^\circ\text{C}$ and specified loading, and not guaranteed.
3. $CS\#$ controls address buffer, $WE\#$ buffer, $OE\#$ buffer, and Din buffer. In data retention mode, V_{in} levels (address, $WE\#$, $OE\#$, I/O) can be in the high impedance state.
4. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform ($CS\#$ Controlled)



Revision History

R1LP0408C-C Series Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
1.00	Aug.01.2003	—	Initial issue
2.00	May.26.2004	6	DC characteristics –5SC and –7LC items' description are divided.
		12	Low V_{CC} Data Retention Characteristics –5SC and –7LC items' description are divided.
		12	Low V_{CC} Data Retention Timing Waveform 2.4 V to 2.2 V

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH

Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.

7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.

FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001