

R1LV0416CBG-I Series

Wide Temperature Range Version
4M SRAM (256-kword × 16-bit)

REJ03C0259-0001
Preliminary
Rev.0.01
Jan.11.2005

Description

The R1LV0416CBG-I is a 4-Mbit static RAM organized 256-kword × 16-bit. The R1LV0416C-I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). The R1LV0416CBG-I Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has packaged in 48-pin CSP (0.75 mm ball pitch).

Features

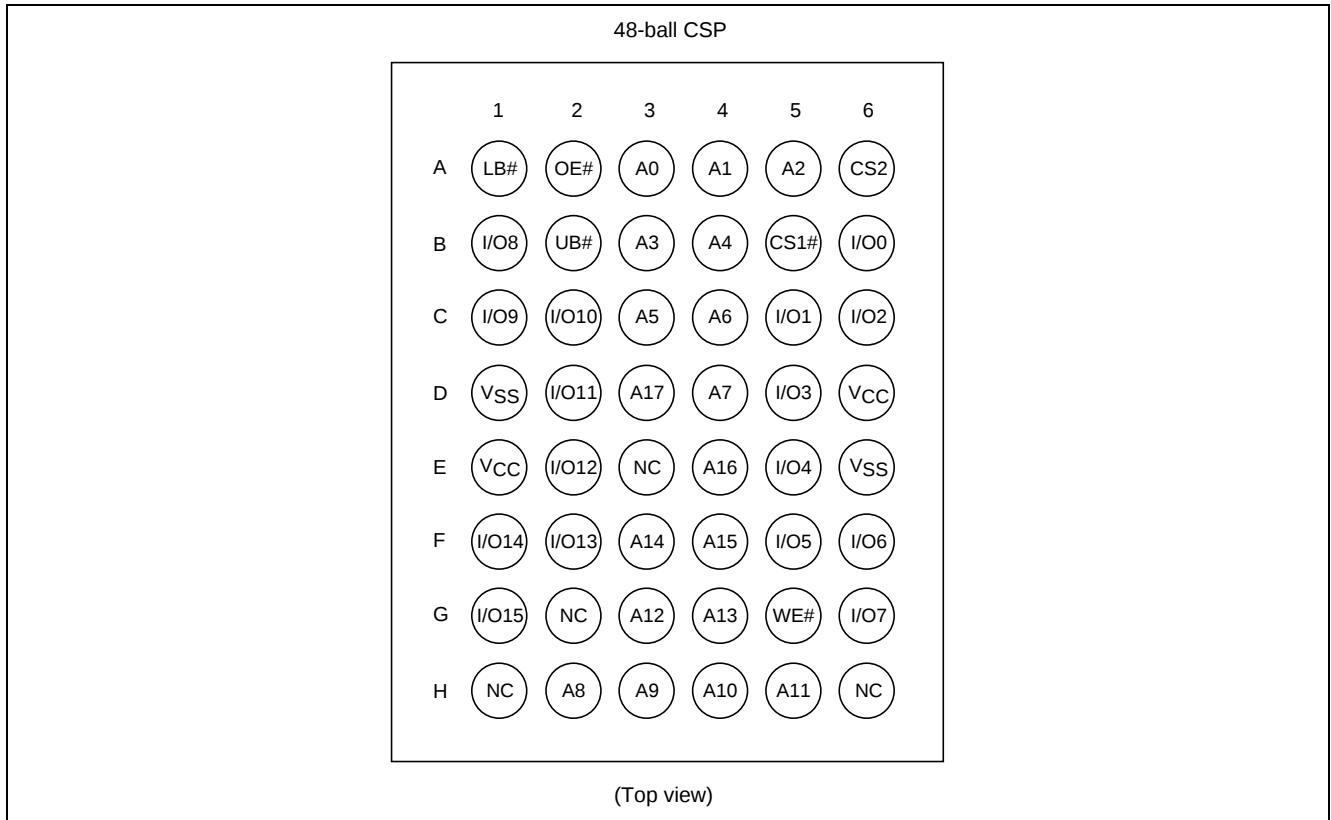
- Single 2.5 V and 3.0 V supply: 2.2 V to 3.6 V
- Fast access time: 55/70 ns (max)
- Power dissipation:
 - Active: 5.0 mW/MHz (typ) ($V_{CC} = 2.5$ V)
: 6.0 mW/MHz (typ) ($V_{CC} = 3.0$ V)
 - Standby: 1.25 μ W (typ) ($V_{CC} = 2.5$ V)
: 1.5 μ W (typ) ($V_{CC} = 3.0$ V)
- Completely static memory.
 - No clock or timing strobe required
- Access and cycle times are equal.
- Common data input and output.
 - Three state output
- Battery backup operation.
 - 2 chip selection for battery backup
- Temperature range: -40 to $+85^{\circ}\text{C}$

Ordering Information

Type No.	Access time	Package
R1LV0416CBG-5SI	55 ns	48-ball CSP with 0.75 mm ball pitch (48FHH)
R1LV0416CBG-7LI	70 ns	

Preliminary: The specifications of this device are subject to change without notice. Please contact your nearest Renesas Technology's Sales Dept. regarding specifications.

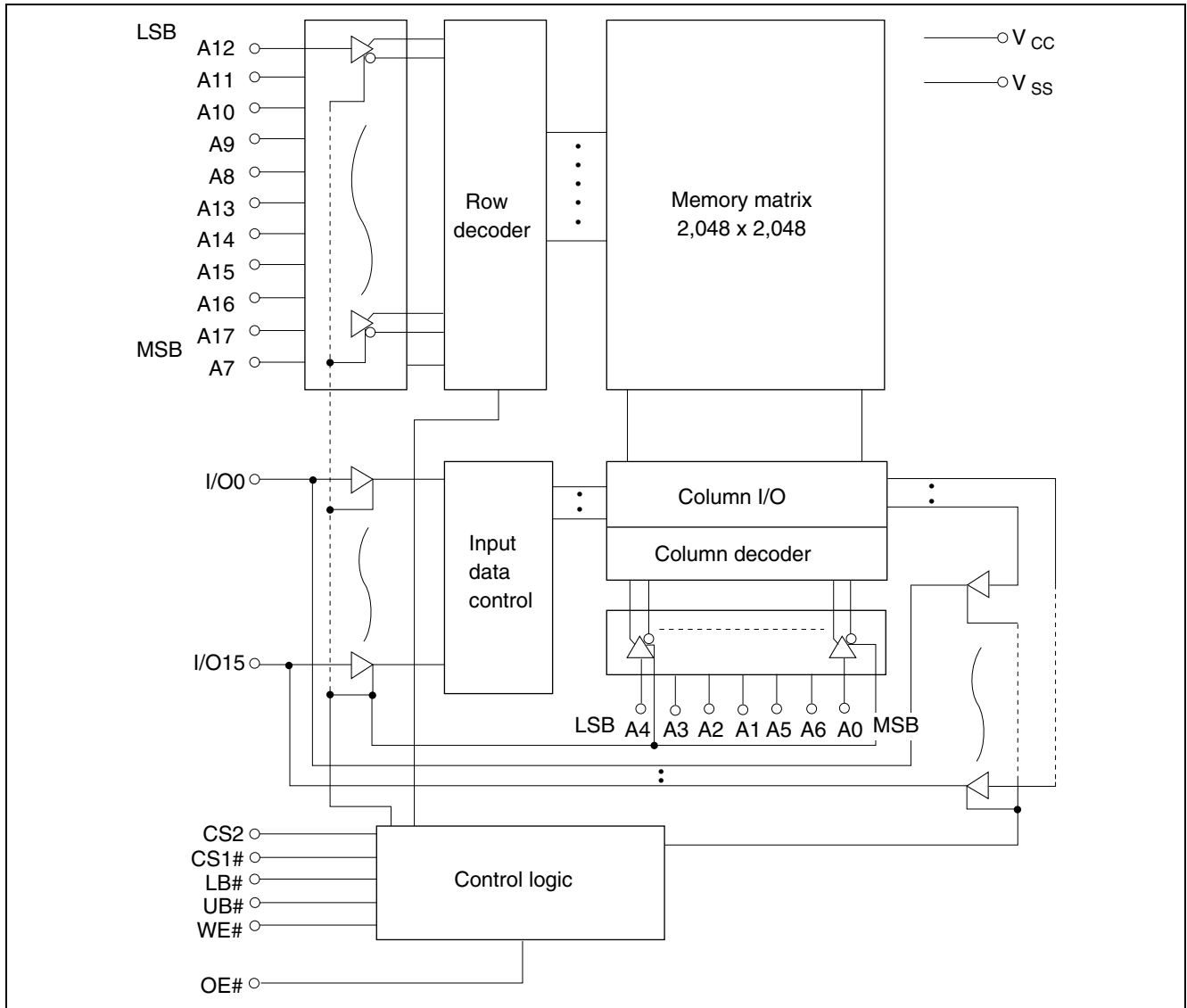
Pin Arrangement



Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
CS1# ($\overline{\text{CS1}}$)	Chip select 1
CS2	Chip select 2
WE# ($\overline{\text{WE}}$)	Write enable
OE# ($\overline{\text{OE}}$)	Output enable
LB# ($\overline{\text{LB}}$)	Lower byte select
UB# ($\overline{\text{UB}}$)	Upper byte select
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Block Diagram



Operation Table

CS1#	CS2	WE#	OE#	UB#	LB#	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	×	High-Z	High-Z	Standby
×	L	×	×	×	×	High-Z	High-Z	Standby
×	×	×	×	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	×	L	L	Din	Din	Write
L	H	L	×	H	L	Din	High-Z	Lower byte write
L	H	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	H	×	×	High-Z	High-Z	Output disable

Note: H: V_{IH} , L: V_{IL} , ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5* ¹ to $V_{CC} + 0.3$ * ²	V
Power dissipation	P_T	0.7	W
Operating temperature	T_{opr}	-40 to +85	°C
Storage temperature range	T_{stg}	-65 to +150	°C
Storage temperature range under bias	T_{bias}	-40 to +85	°C

Notes: 1. V_T min: -3.0 V for pulse half-width ≤ 30 ns.

2. Maximum voltage is +4.6 V.

DC Operating Conditions

($T_a = -40$ to +85°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply voltage		V_{CC}	2.2	2.5/3.0	3.6	V	
		V_{SS}	0	0	0	V	
Input high voltage	$V_{CC} = 2.2$ V to 2.7 V	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	
	$V_{CC} = 2.7$ V to 3.6 V	V_{IH}	2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	$V_{CC} = 2.2$ V to 2.7 V	V_{IL}	-0.2	—	0.4	V	1
	$V_{CC} = 2.7$ V to 3.6 V	V_{IL}	-0.3	—	0.6	V	1

Note: 1. V_{IL} min: -3.0 V for pulse half-width ≤ 30 ns.

DC Characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current			$ I_{LI} $	—	—	1	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current			$ I_{LO} $	—	—	1	μA	CS1# = V_{IH} or CS2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL} or LB# = UB# = V_{IH} , $V_{I/O} = V_{SS}$ to V_{CC}
Operating current			I_{CC}	—	5* ¹	20	mA	CS1# = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL} , $I_{I/O} = 0$ mA
Average operating current			I_{CC1}	—	8* ¹	25	mA	Min. cycle, duty = 100%, $I_{I/O} = 0$ mA, CS1# = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL}
			I_{CC2}	—	2* ¹	5	mA	Cycle time = 1 μs , duty = 100%, $I_{I/O} = 0$ mA, CS1# ≤ 0.2 V, CS2 $\geq V_{CC} - 0.2$ V $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby current			I_{SB}	—	0.1* ¹	0.3	mA	CS2 = V_{IL}
Standby current	-5SI	to +85°C	I_{SB1}	—	—	10	μA	$V_{in} \geq 0$ V (1) $0 \text{ V} \leq \text{CS2} \leq 0.2 \text{ V}$ or (2) CS1# $\geq V_{CC} - 0.2$ V, CS2 $\geq V_{CC} - 0.2$ V or (3) LB# = UB# $\geq V_{CC} - 0.2$ V, CS2 $\geq V_{CC} - 0.2$ V, CS1# ≤ 0.2 V
		to +70°C	I_{SB1}	—	—	8	μA	
		to +40°C	I_{SB1}	—	0.7* ²	3	μA	
		to +25°C	I_{SB1}	—	0.5* ¹	2.5	μA	
	-7LI	to +85°C	I_{SB1}	—	—	20	μA	
		to +70°C	I_{SB1}	—	—	16	μA	
		to +40°C	I_{SB1}	—	0.7* ²	10	μA	
		to +25°C	I_{SB1}	—	0.5* ¹	10	μA	
Output high voltage	$V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$		V_{OH}	2.0	—	—	V	$I_{OH} = -0.5 \text{ mA}$
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		V_{OH}	2.4	—	—	V	$I_{OH} = -1 \text{ mA}$
	$V_{CC} = 2.2 \text{ V to } 3.6 \text{ V}$		V_{OH2}	$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100 \mu\text{A}$
Output low voltage	$V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$		V_{OL}	—	—	0.4	V	$I_{OL} = 0.5 \text{ mA}$
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		V_{OL}	—	—	0.4	V	$I_{OL} = 2 \text{ mA}$
	$V_{CC} = 2.2 \text{ V to } 3.6 \text{ V}$		V_{OL2}	—	—	0.2	V	$I_{OL} = 100 \mu\text{A}$

Notes: 1. Typical values are at $V_{CC} = 3.0 \text{ V}$, $T_a = +25^\circ\text{C}$ and specified loading, and not guaranteed.

2. Typical values are at $V_{CC} = 3.0 \text{ V}$, $T_a = +40^\circ\text{C}$ and specified loading, and not guaranteed.

Capacitance

($T_a = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	8	pF	$V_{in} = 0 \text{ V}$	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0 \text{ V}$	1

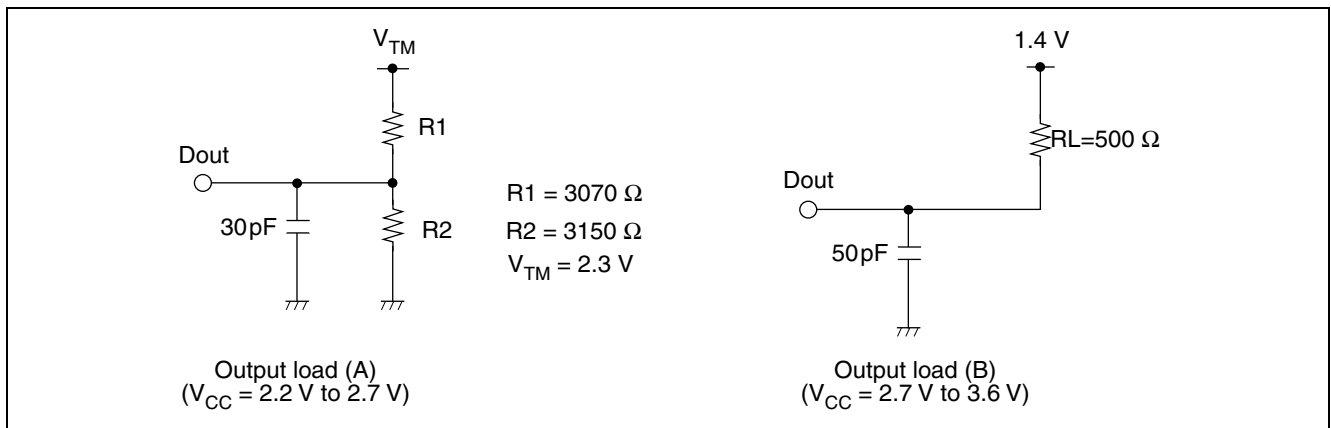
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

(Ta = -40 to +85°C, V_{CC} = 2.2 V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{IL} = 0.4 V, V_{IH} = 2.2 V (V_{CC} = 2.2 V to 2.7 V)
: V_{IL} = 0.4 V, V_{IH} = 2.4 V (V_{CC} = 2.7 V to 3.6 V)
- Input rise and fall time: 5 ns
- Input/output timing reference levels: 1.1 V (V_{CC} = 2.2 V to 2.7 V)
: 1.4 V (V_{CC} = 2.7 V to 3.6 V)
- Output load: See figures (Including scope and jig)



Read Cycle

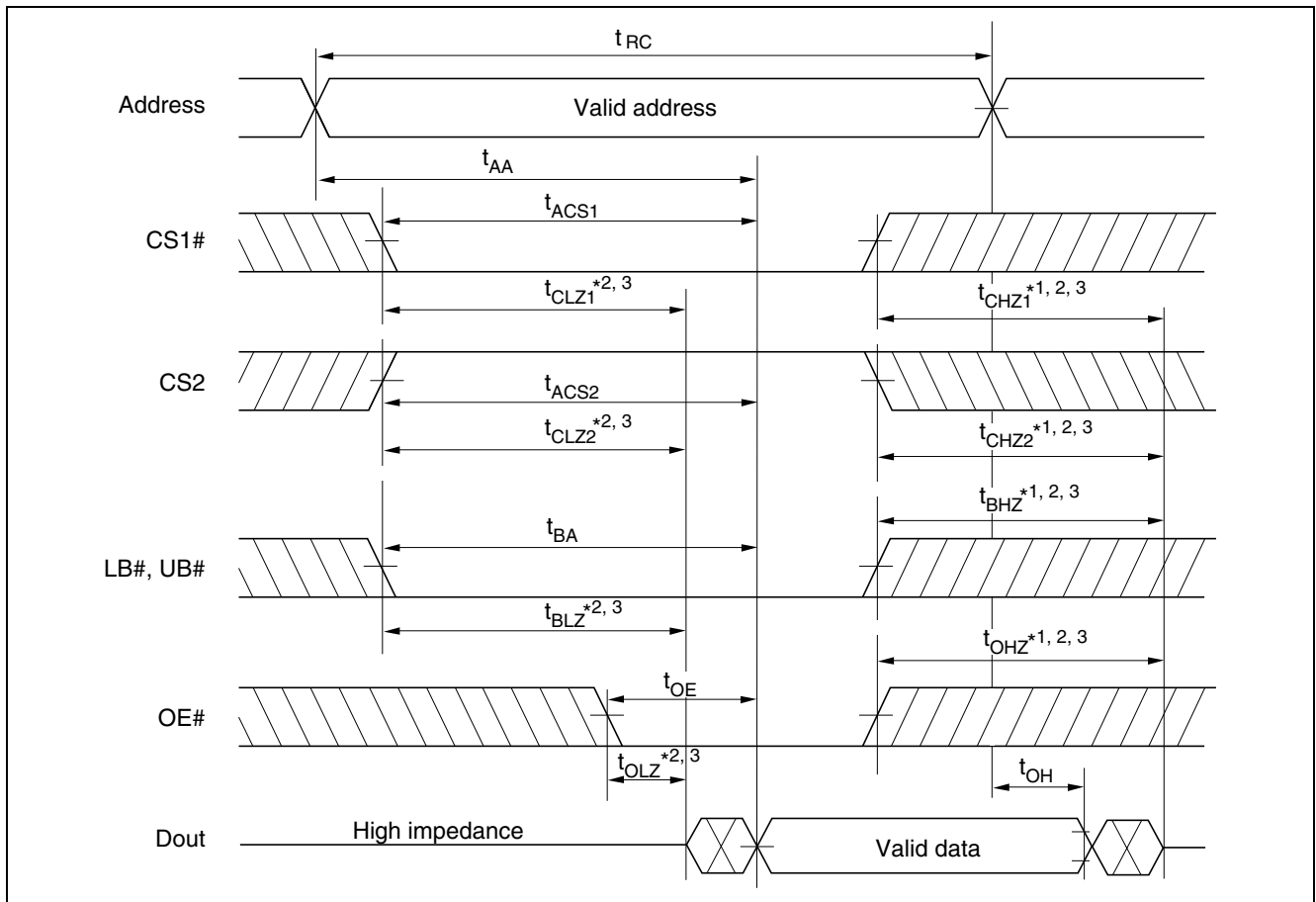
Parameter	Symbol	R1LV0416CBG-I				Unit	Notes
		-5SI		-7LI			
		Min	Max	Min	Max		
Read cycle time	t _{RC}	55	—	70	—	ns	
Address access time	t _{AA}	—	55	—	70	ns	
Chip select access time	t _{ACS1}	—	55	—	70	ns	
	t _{ACS2}	—	55	—	70	ns	
Output enable to output valid	t _{OE}	—	35	—	40	ns	
Output hold from address change	t _{OH}	10	—	10	—	ns	
LB#, UB# access time	t _{BA}	—	55	—	70	ns	
Chip select to output in low-Z	t _{CLZ1}	10	—	10	—	ns	2, 3
	t _{CLZ2}	10	—	10	—	ns	2, 3
LB#, UB# disable to low-Z	t _{BLZ}	5	—	5	—	ns	2, 3
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	t _{CHZ1}	0	20	0	25	ns	1, 2, 3
	t _{CHZ2}	0	20	0	25	ns	1, 2, 3
LB#, UB# disable to high-Z	t _{BHZ}	0	20	0	25	ns	1, 2, 3
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1, 2, 3

Write Cycle

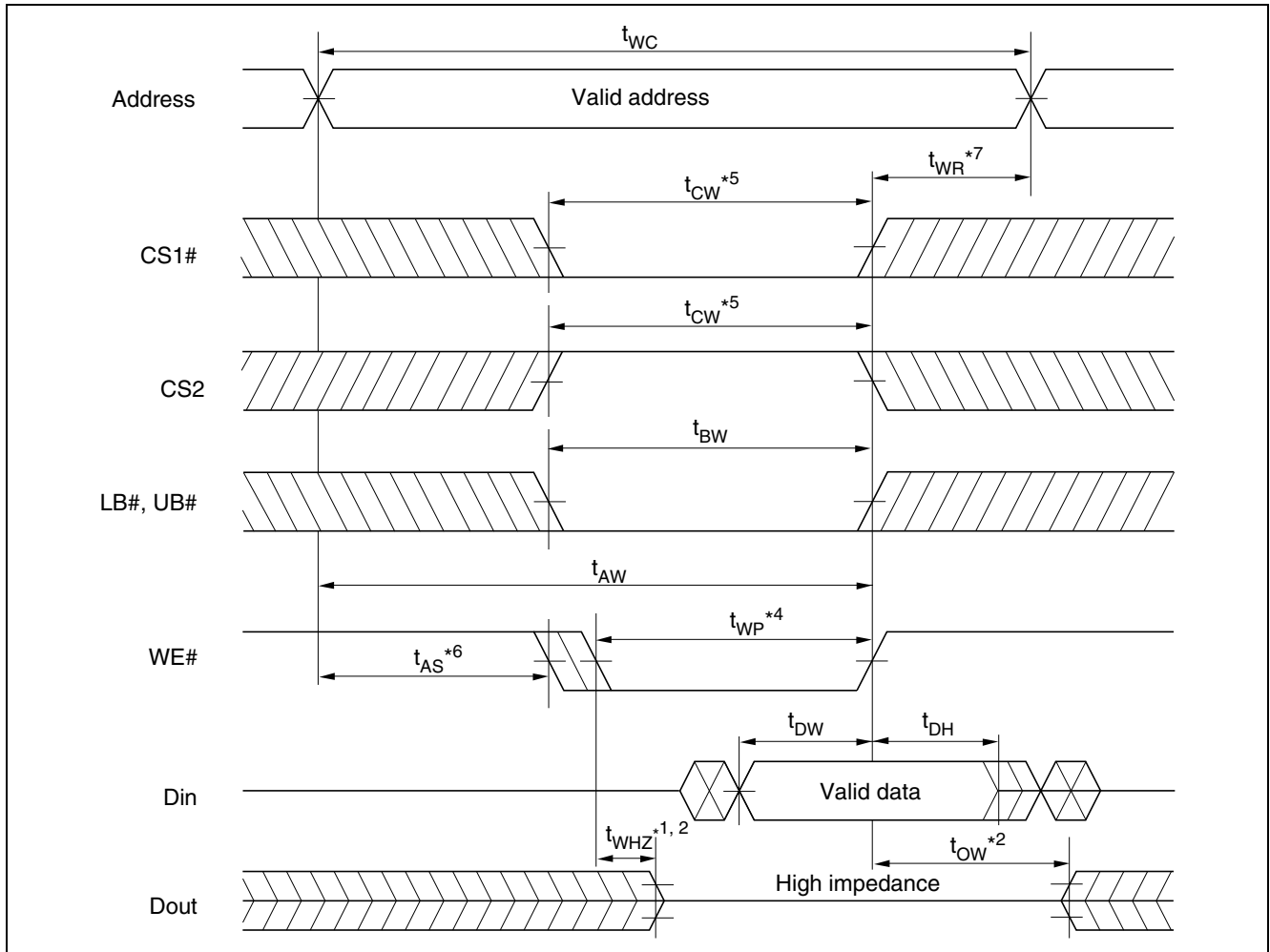
Parameter	Symbol	R1LV0416CBG-I				Unit	Notes
		-5SI		-7LI			
		Min	Max	Min	Max		
Write cycle time	t _{WC}	55	—	70	—	ns	
Address valid to end of write	t _{AW}	50	—	60	—	ns	
Chip selection to end of write	t _{CW}	50	—	60	—	ns	5
Write pulse width	t _{WP}	40	—	50	—	ns	4
LB#, UB# valid to end of write	t _{BW}	50	—	55	—	ns	
Address setup time	t _{AS}	0	—	0	—	ns	6
Write recovery time	t _{WR}	0	—	0	—	ns	7
Data to write time overlap	t _{DW}	25	—	30	—	ns	
Data hold from write time	t _{DH}	0	—	0	—	ns	
Output active from end of write	t _{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1, 2, 3
Write to output in high-Z	t _{WHZ}	0	20	0	25	ns	1, 2

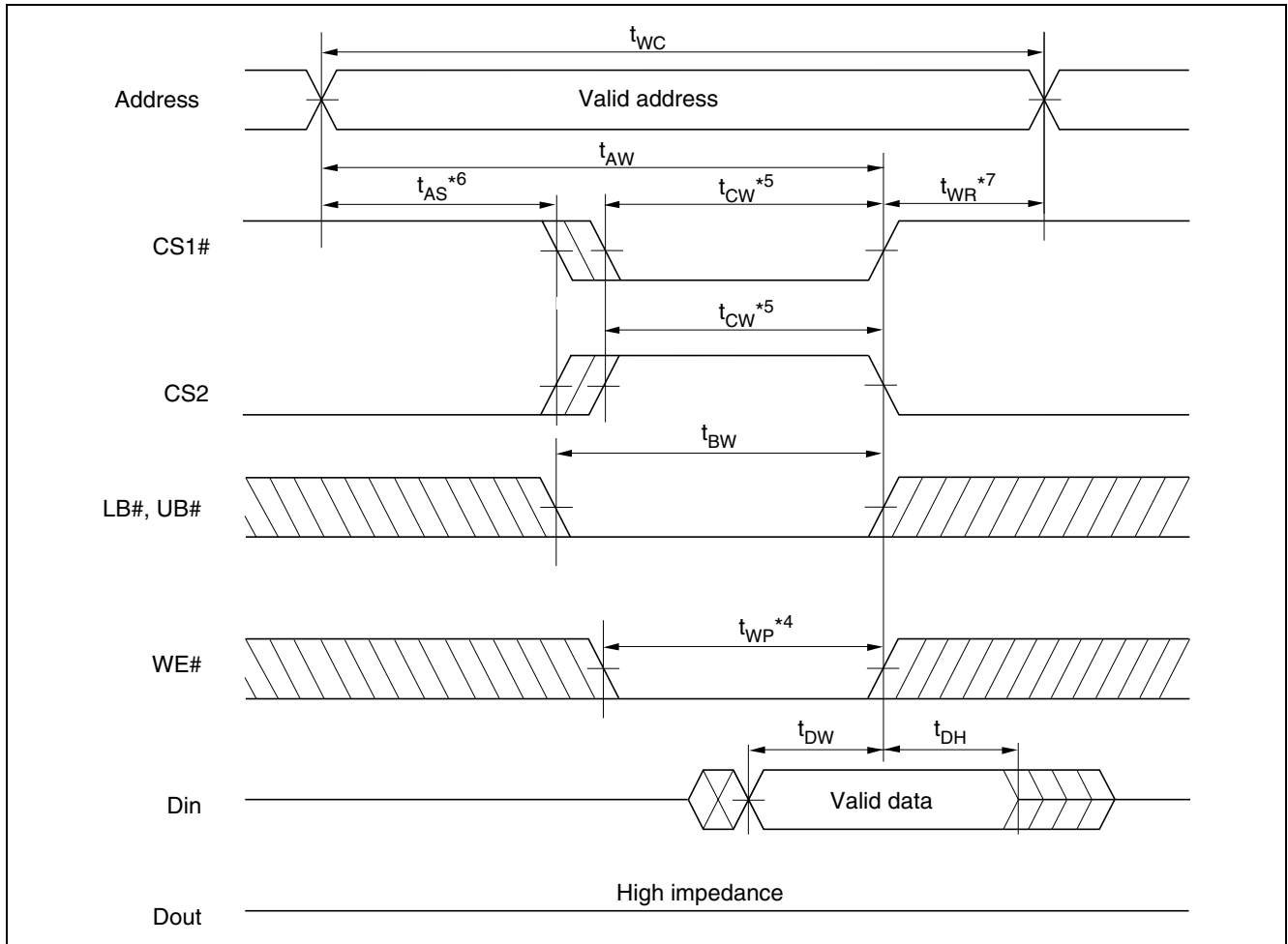
- Notes: 1. t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of CS1# going low or CS2 going high to the end of write.
6. t_{AS} is measured from the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

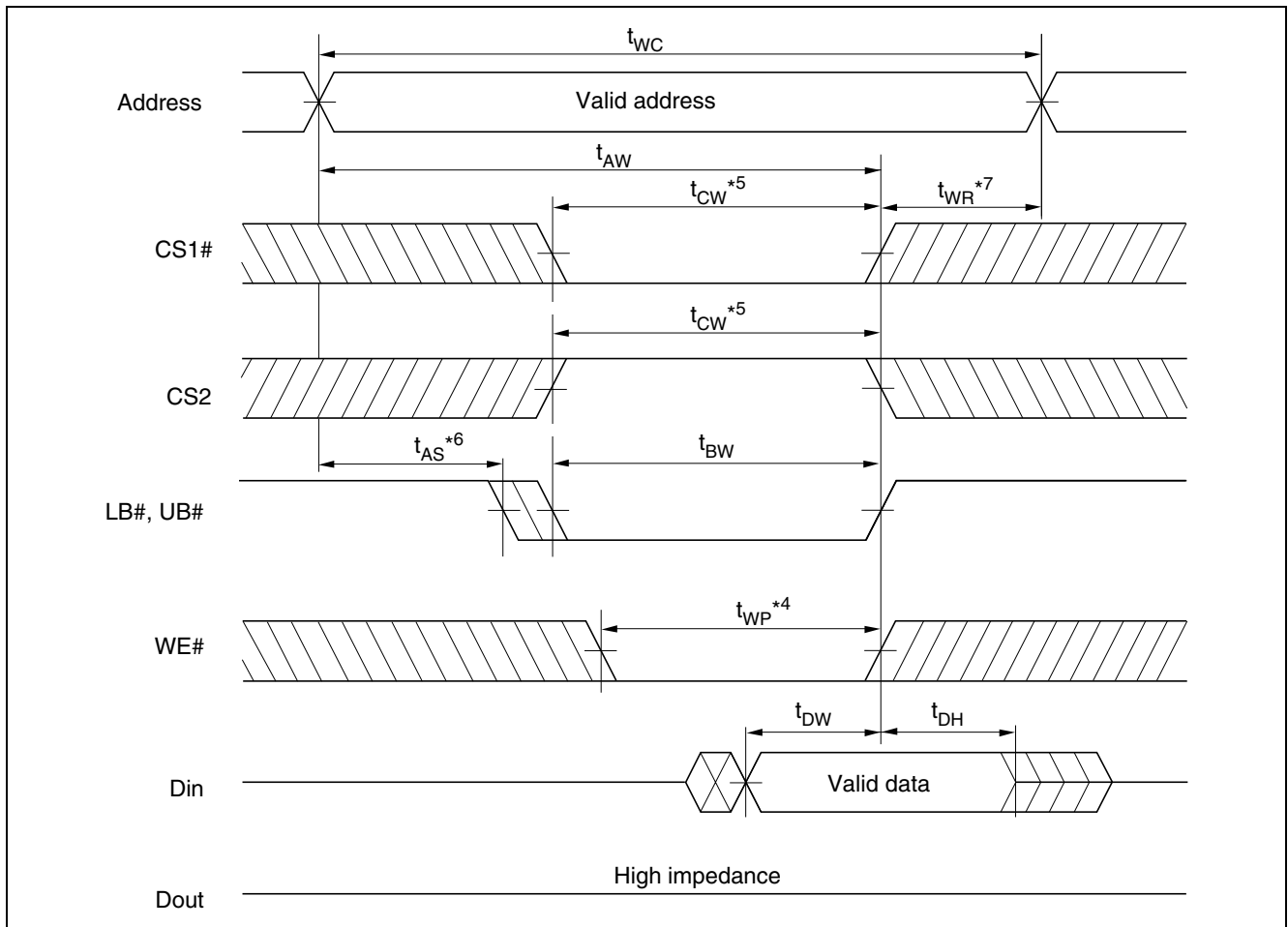
Timing Waveform

Read Timing Waveform ($WE\# = V_{IH}$)

Write Timing Waveform (1) (WE# Clock)



Write Timing Waveform (2) (CS# Clock, OE# = V_{IH})

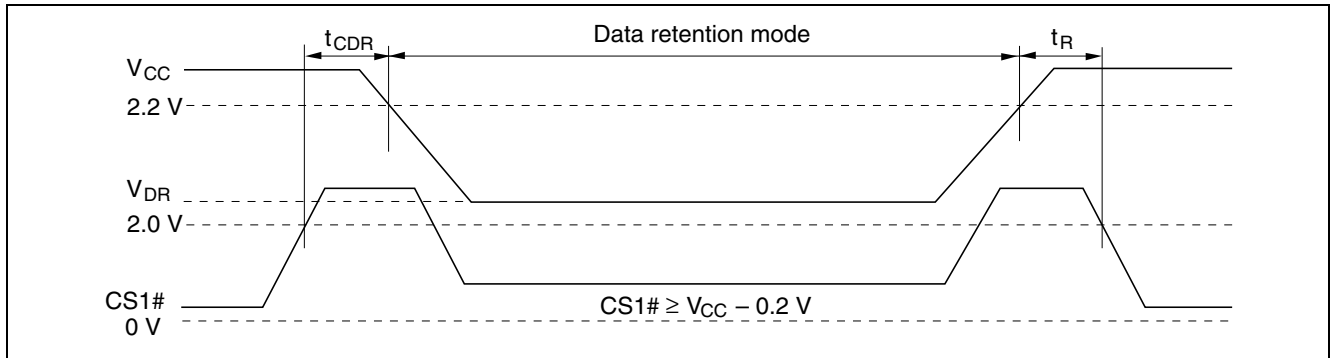
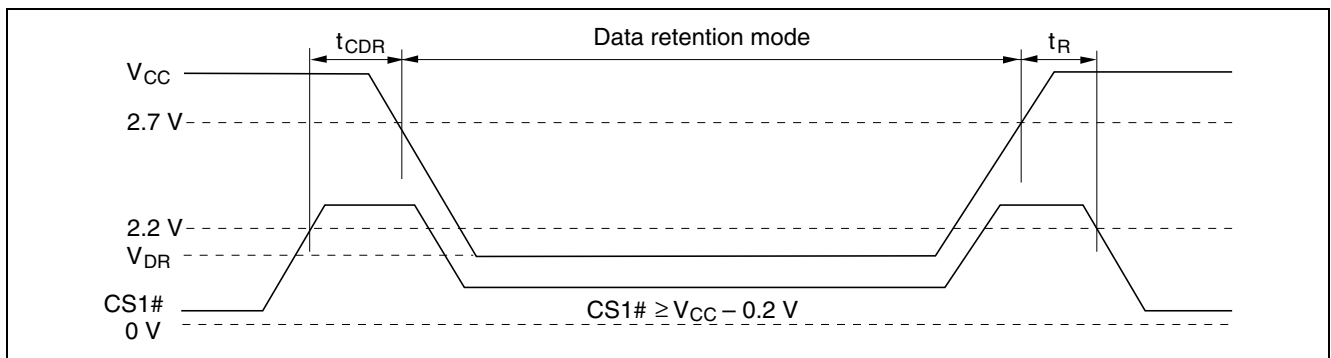
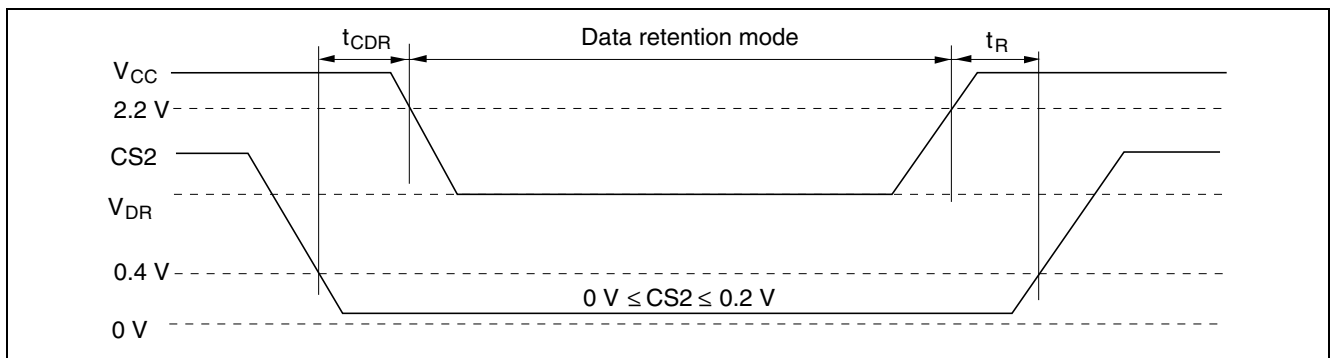
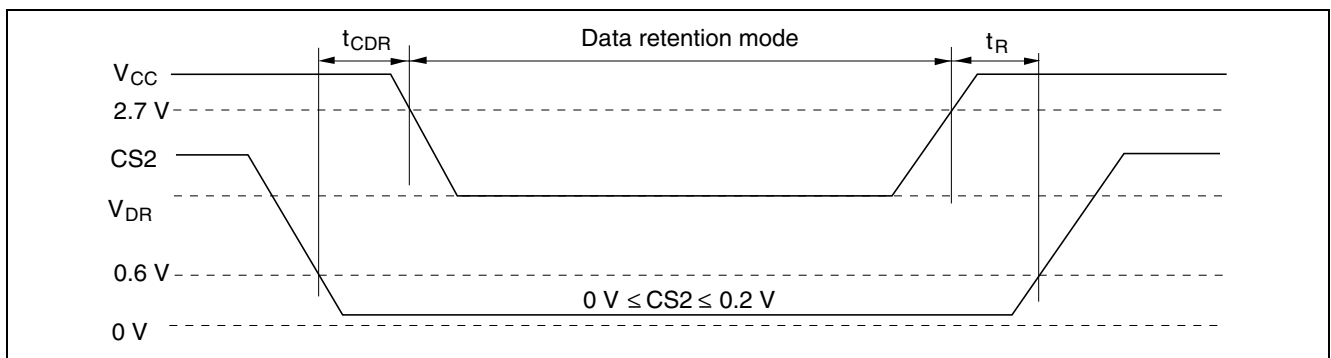
Write Timing Waveform (3) (LB#, UB# Clock, OE# = V_{IH})

Low V_{CC} Data Retention Characteristics

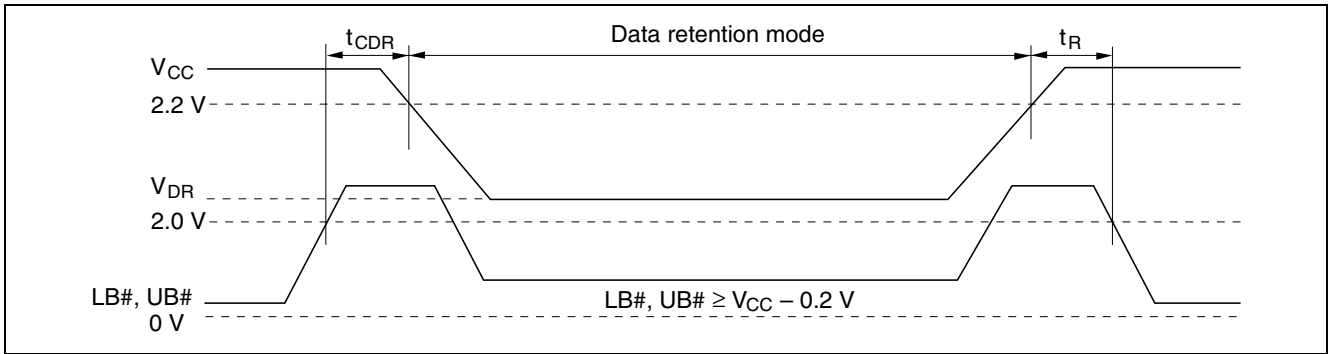
(Ta = -40 to +85°C)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions* ³
V _{CC} for data retention			V _{DR}	2.0	—	—	V	V _{in} ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V _{CC} − 0.2 V, CS1# ≥ V _{CC} − 0.2 V or (3) LB# = UB# ≥ V _{CC} − 0.2 V, CS2 ≥ V _{CC} − 0.2 V, CS1# ≤ 0.2 V
Data retention current	−5SI	to +85°C	I _{CCDR}	—	—	10	μA	V _{CC} = 3.0 V, V _{in} ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V _{CC} − 0.2 V, CS1# ≥ V _{CC} − 0.2 V or (3) LB# = UB# ≥ V _{CC} − 0.2 V, CS2 ≥ V _{CC} − 0.2 V, CS1# ≤ 0.2 V
		to +70°C	I _{CCDR}	—	—	8	μA	
		to +40°C	I _{CCDR}	—	0.7* ²	3	μA	
		to +25°C	I _{CCDR}	—	0.5* ¹	2.5	μA	
	−7LI	to +85°C	I _{CCDR}	—	—	20	μA	
		to +70°C	I _{CCDR}	—	—	16	μA	
		to +40°C	I _{CCDR}	—	0.7* ²	10	μA	
		to +25°C	I _{CCDR}	—	0.5* ¹	10	μA	
Chip deselect to data retention time			t _{CDR}	0	—	—	ns	See retention waveform
Operation recovery time			t _R	t _{RC} * ⁴	—	—	ns	

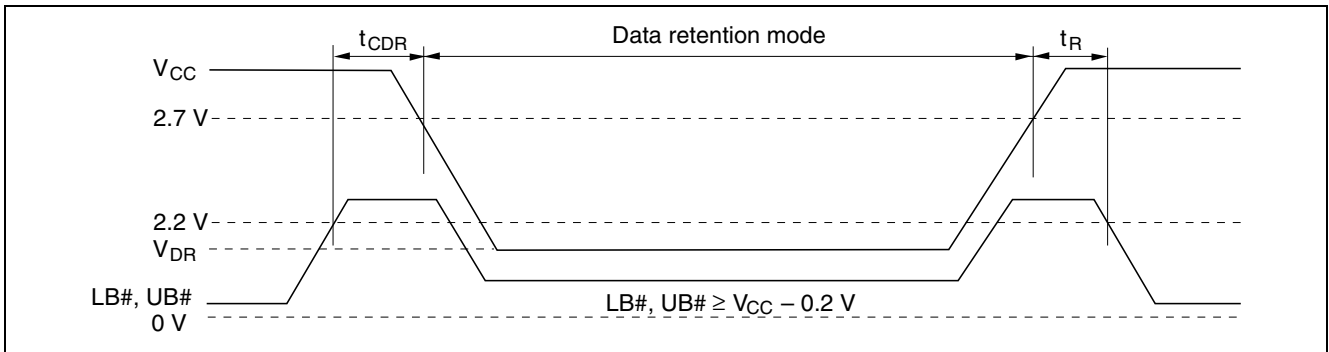
Notes: 1. Typical values are at $V_{CC} = 3.0V$, Ta = +25°C and specified loading, and not guaranteed.2. Typical values are at $V_{CC} = 3.0V$, Ta = +40°C and specified loading, and not guaranteed.3. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB#, UB# buffer and Din buffer. If CS2 controls data retention mode, V_{in} levels (address, WE#, OE#, CS1#, LB#, UB#, I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be $CS2 \geq V_{CC} - 0.2V$ or $0V \leq CS2 \leq 0.2V$. The other input levels (address, WE#, OE#, LB#, UB#, I/O) can be in the high impedance state.4. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform (1) (CS1# Controlled) ($V_{CC} = 2.2\text{ V}$ to 2.7 V)

Low V_{CC} Data Retention Timing Waveform (2) (CS1# Controlled) ($V_{CC} = 2.7\text{ V}$ to 3.6 V)

Low V_{CC} Data Retention Timing Waveform (3) (CS2 Controlled) ($V_{CC} = 2.2\text{ V}$ to 2.7 V)

Low V_{CC} Data Retention Timing Waveform (4) (CS2 Controlled) ($V_{CC} = 2.7\text{ V}$ to 3.6 V)


Low V_{CC} Data Retention Timing Waveform (5) (LB#, UB# Controlled) ($V_{CC} = 2.2\text{ V}$ to 2.7 V)



Low V_{CC} Data Retention Timing Waveform (6) (LB#, UB# Controlled) ($V_{CC} = 2.7\text{ V}$ to 3.6 V)



Revision History	R1LV0416CBG-I Series
-------------------------	-----------------------------

Rev.	Date	Contents of Modification	
		Page	Description
0.01	Jan.11.2005	—	Initial issue

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001