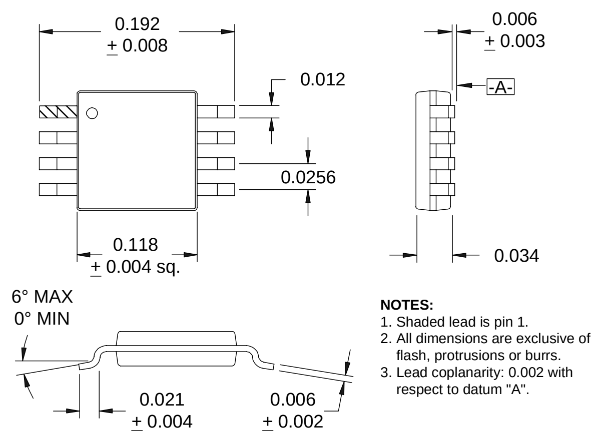
3V PCS DOWNCONVERTER

Typical Applications

- CDMA/TDMA/DCS1900 PCS Systems
- PHS 1500/WLAN 2400 Systems
- General Purpose Downconverter
- Micro-Cell PCS Base Stations
- Portable Battery-Powered Equipment

Product Description

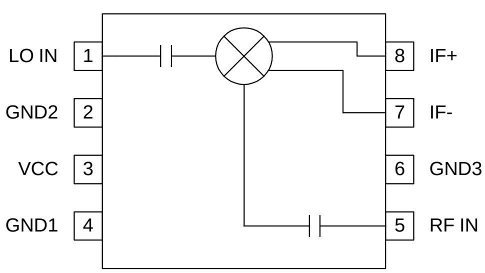
The RF2459 is a monolithic integrated downconverter for PCS, PHS, and WLAN applications. The IC contains all of the required components to implement the RF functions of the downconverter. It contains a double-balanced Gilbert cell mixer and a balanced IF output. The mixer's high third-order intercept point makes it ideal for digital cellular applications. The IC is designed to operate from a single 3V power supply.



Package Style: MSOP-8

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Extremely High Dynamic Range
- Single 3V Power Supply
- 1500MHz to 2500MHz Operation

Ordering Information

RF2459	3V PCS Downconverter
RF2459 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
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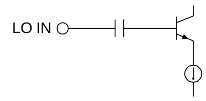
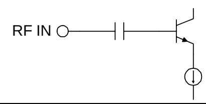
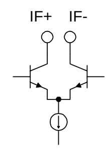
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

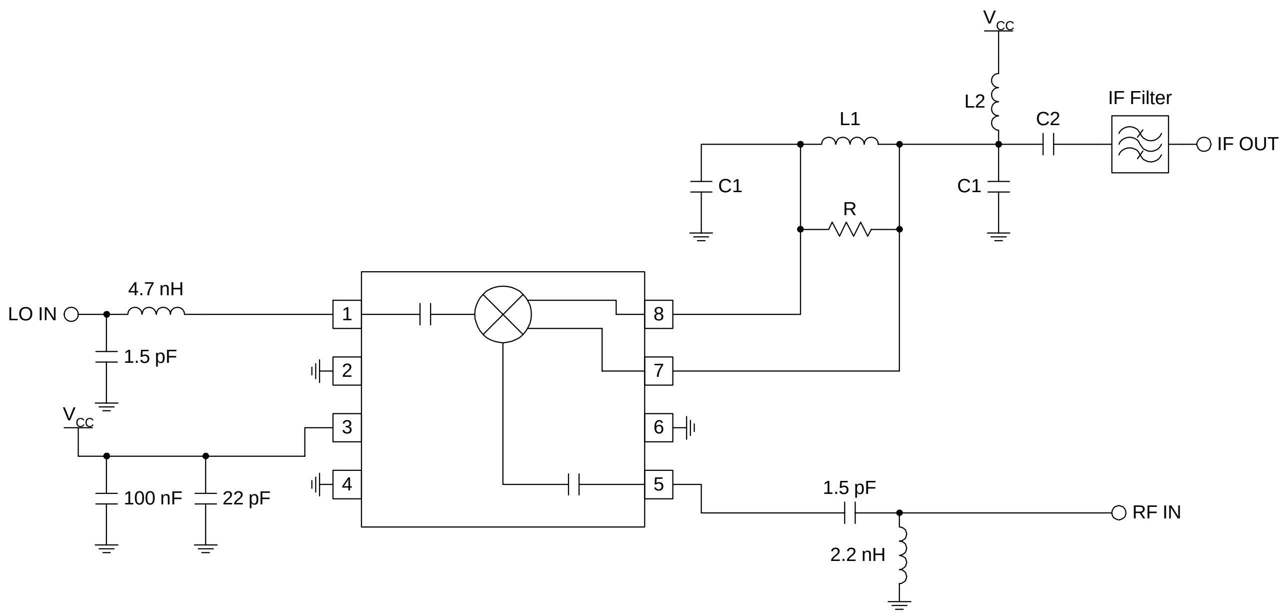
Parameter	Ratings	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, RF=1960MHz, LO=1750MHz@-2dBm
Usable RF Frequency Range	1500		2500	MHz	
Typical RF Frequency Range		1930 to 1990		MHz	
Usable LO Frequency Range	1200		2500	MHz	
Typical LO Frequency Range		1430 to 1990		MHz	
IF Frequency Range		DC to 500		MHz	
Noise Figure		14		dB	
Input VSWR		<2:1			Single-ended with external matching network.
Input IP3	+5.0	+7.0		dBm	
Gain	8	10		dB	
Output Impedance			1000	Ω	Single-ended with external matching network.
Input P1dB		-7.5		dBm	
LO Input					
LO Input Range		-5 to +3		dBm	
LO to RF (Mix In) Rejection		30		dB	
LO to IF		40		dB	
LO Input VSWR		<2:1			Single-ended with external matching network.
Power Supply					
Voltage	2.7	3.0	3.6	V	
Current Consumption		20	26	mA	

Pin	Function	Description	Interface Schematic
1	LO IN	Mixer LO single-ended input. The pin is internally DC blocked. External matching sets impedance.	
2	GND2	Ground for downconverter. Keep traces physically short and connect directly to ground plane for best performance.	
3	VCC	Supply voltage for downconverter. External RF bypassing is required. The trace length between the bypass caps and the pin should be minimized. Connect ground sides of caps directly to ground.	
4	GND1	Same as pin 2.	
5	RF IN	Mixer RF single-ended input. The pin is internally DC blocked. External matching sets input impedance.	
6	GND3	Same as pin 2.	
7	IF-	IF output pin. The output is balanced. A current combiner external network performs a differential to single-ended conversion and sets the output impedance. There must be a DC path from V_{CC} to this pin. this is normally achieved with the current combiner network. A DC blocking cap must be present if the IF filter input has a DC path to ground.	
8	IF+	Same as pin 7, except complementary output.	

Application Schematic



Output Interface Network

L1, C1 and R form a current combiner which performs a differential to single-ended conversion at the IF frequency and sets the output impedance. In most cases, the resonance frequency is independent of R and can be set according to the following equation:

$$f_{IF} = \frac{1}{2\pi\sqrt{\frac{L1}{2}(C1 + C_{EQ})}}$$

Where C_{EQ} is the equivalent stray capacitance and capacitance looking into pins 7 and 8. An average value to use for C_{EQ} is 2.5pF.

R can then be used to set the output impedance according to the following equation:

$$R = \left(\frac{1}{4 \cdot R_{OUT}} - \frac{1}{R_P}\right)^{-1}$$

where R_{OUT} is the desired output impedance and R_P is the parasitic equivalent parallel resistance of L1.

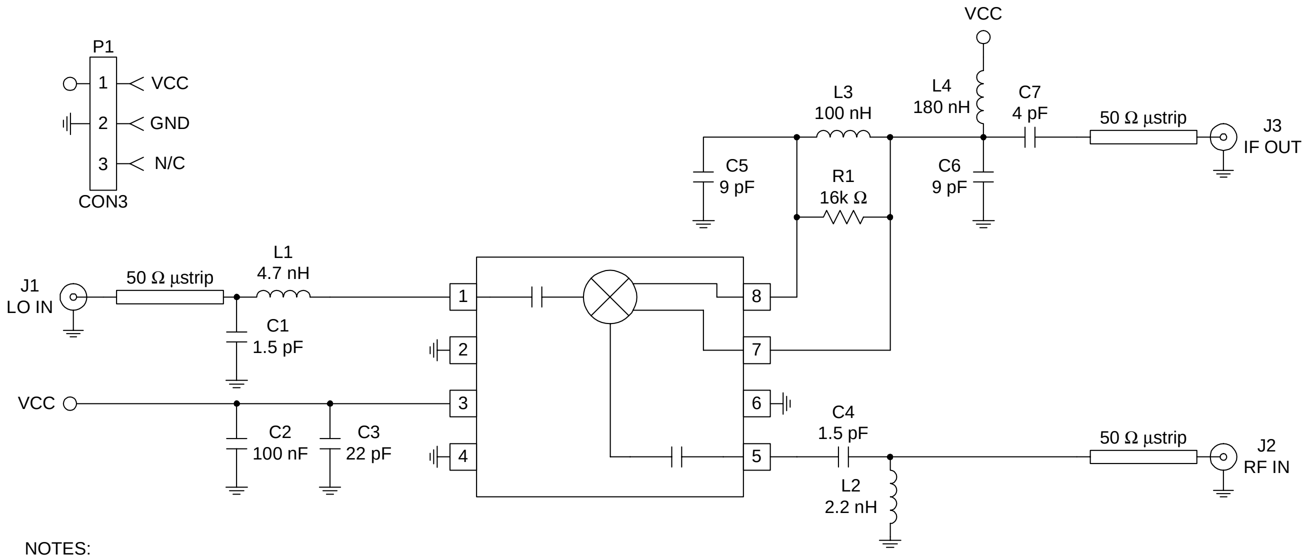
C1 should be chosen as high as possible, while maintaining an R_P of L1 that allows for the desired R_{OUT}.

L2 and C2 serve dual purposes. L2 serves as an output bias choke, and C2 serves as a series DC block.

In addition, L2 and C2 may be chosen to form an impedance matching network if the input impedance of the IF filter is not equal to ROUT. Otherwise, L2 is chosen to be large (suggested 8.2nH) and C2 is chosen to be large (suggested 22nF) if a DC path to ground is present in the IF filter, or omitted if the filter is DC blocked.

Evaluation Board Schematic
RF=1.959MHz, IF=210MHz

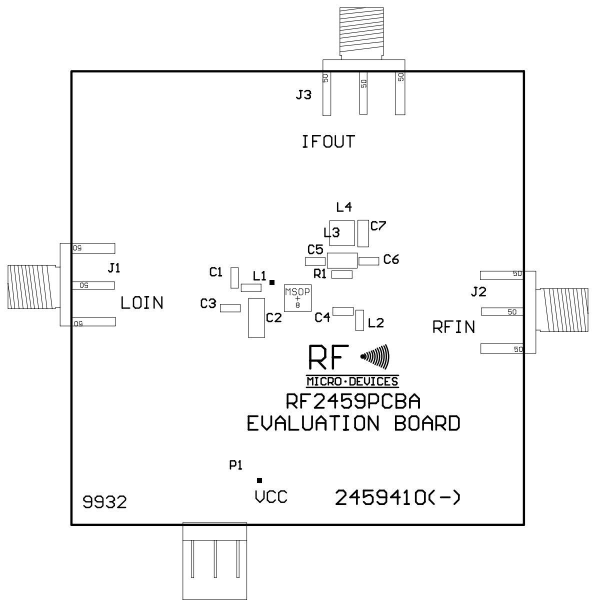
(Download Bill of Materials from www.rfmd.com.)

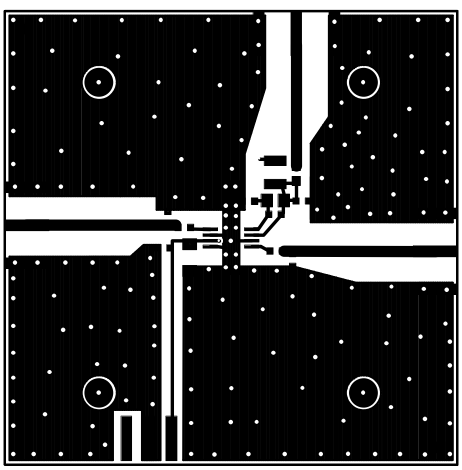


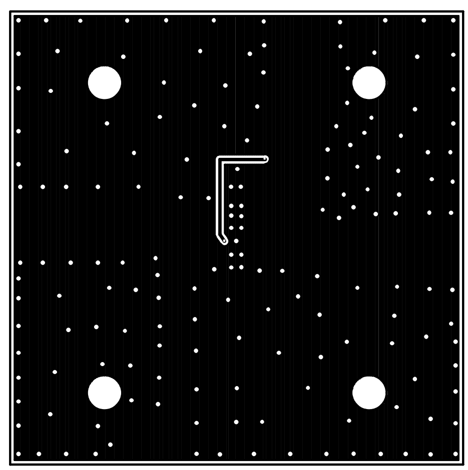
NOTES:
1) R1, L3, C5, and C6 are chosen to produce an output impedance, R_{OUT}, of 1000 Ω @ 210 MHz.
2) L4 and C7 are chosen to match the 1000 Ω output impedance to 50 Ω for testing purposes.

Evaluation Board Layout 900 MHz
Board Size 2.0" x 2.0"

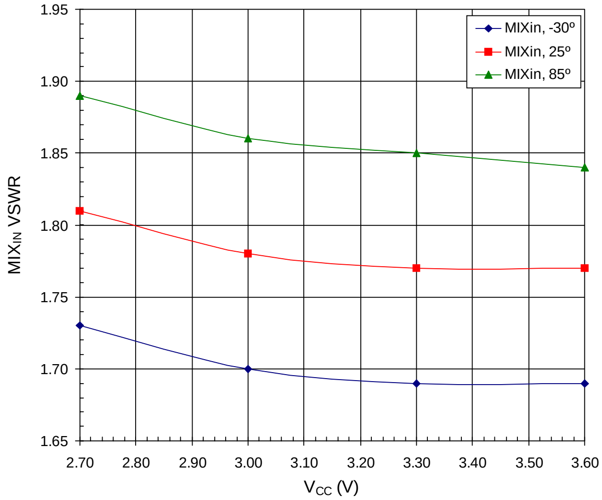
Board Thickness 0.031”, Board Material FR-4



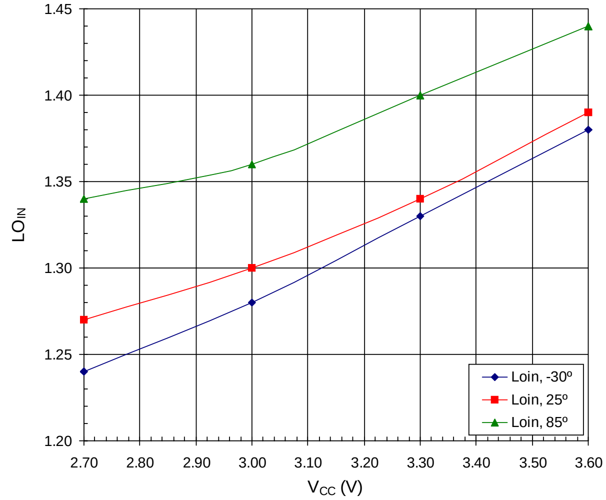




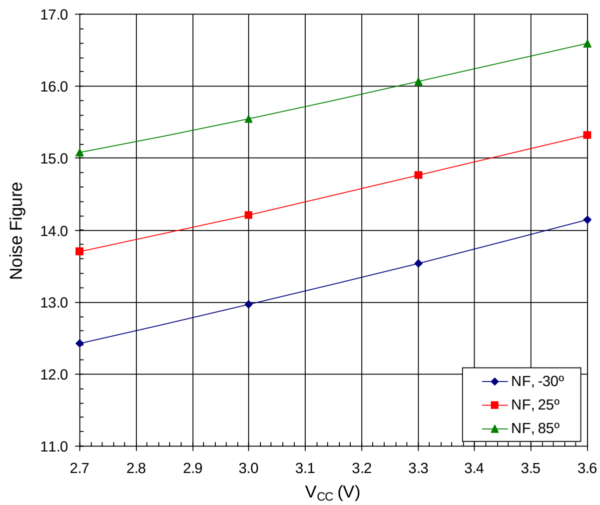
MIX_{IN} VSWR versus V_{CC}



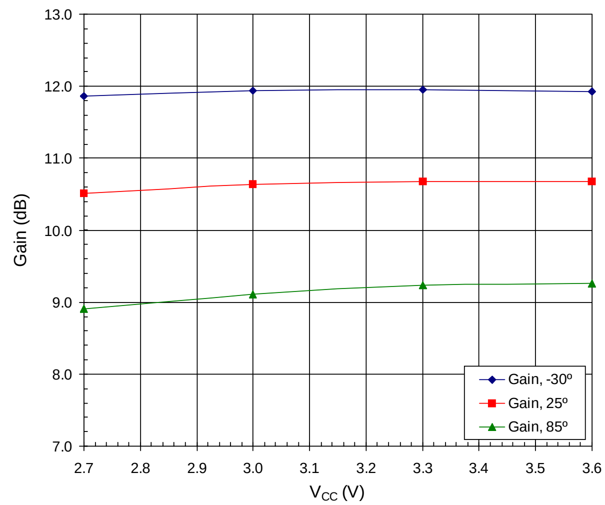
LO_{IN} VSWR versus V_{CC}



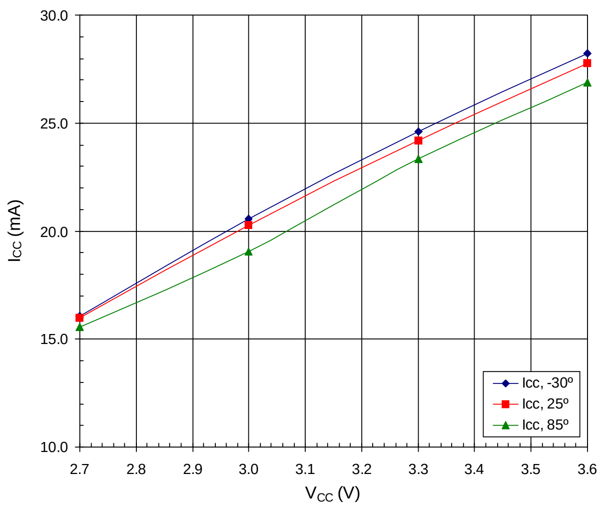
NF versus V_{CC}



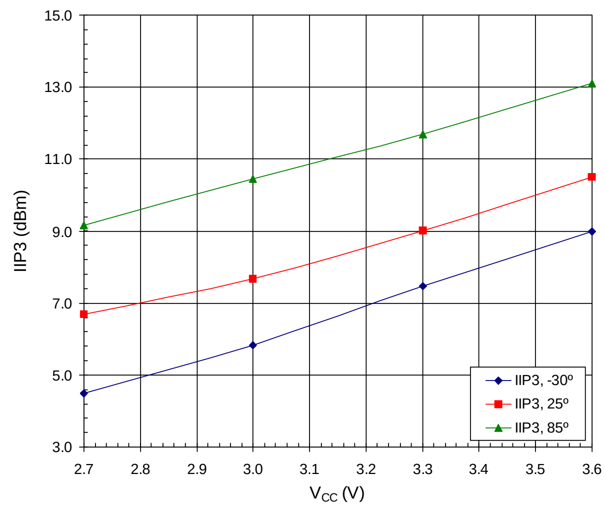
Gain versus V_{CC}

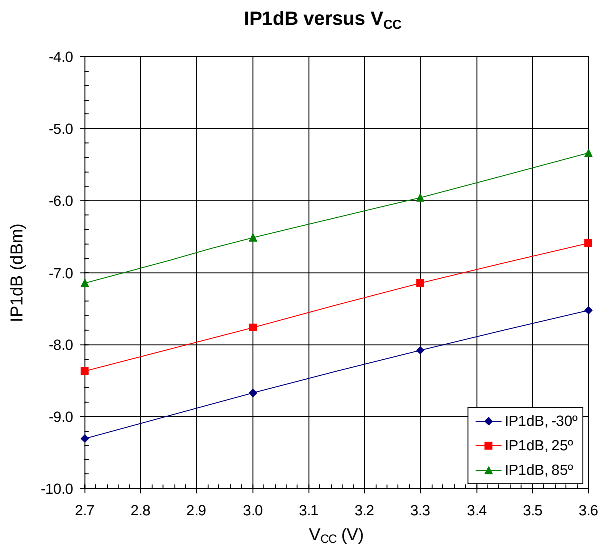


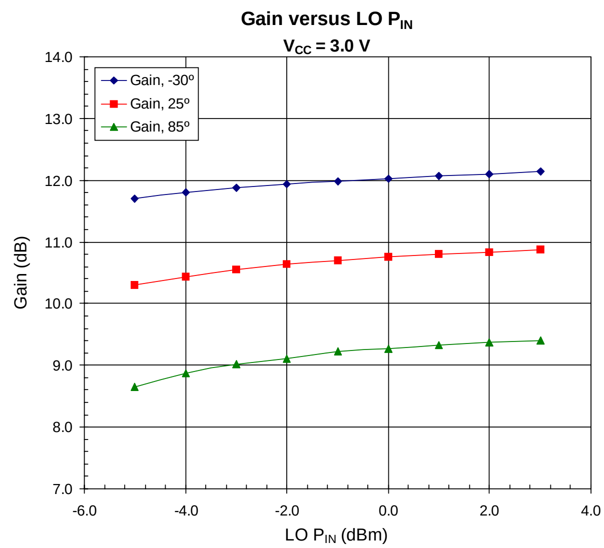
I_{CC} versus V_{CC}

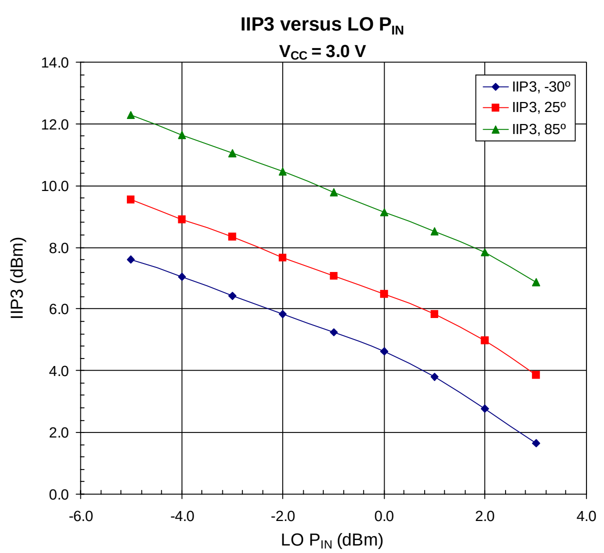


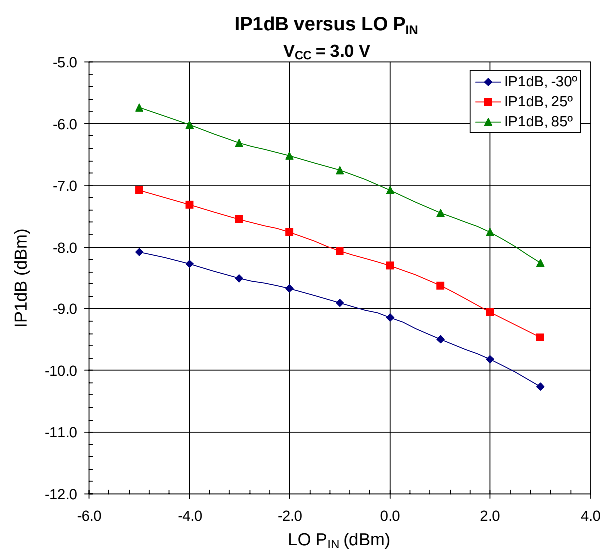
IIP3 versus V_{CC}




IP1dB versus VCC
IP1dB (dBm)
VCC (V)
IP1dB, -30º
IP1dB, 25º
IP1dB, 85º


Gain versus LO PIN
VCC = 3.0 V
Gain (dB)
LO PIN (dBm)
Gain, -30º
Gain, 25º
Gain, 85º


IIP3 versus LO PIN
VCC = 3.0 V
IIP3 (dBm)
LO PIN (dBm)
IIP3, -30º
IIP3, 25º
IIP3, 85º


IP1dB versus LO PIN
VCC = 3.0 V
IP1dB (dBm)
LO PIN (dBm)
IP1dB, -30º
IP1dB, 25º
IP1dB, 85º