

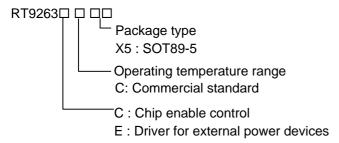
High Efficiency, Low Supply Current, Step-up DC/DC Converter

General Description

The RT9263 is a compact, high efficient, step-up DC/DC converter with an adaptive current mode PWM control loop, providing a stable and high efficient operation over a wide range of load currents. It operates in both continuous and discontinuous current modes in stable waveforms without external compensation.

The low start-up input voltage below 1V makes RT9263 suitable for 1 to 4 battery cell applications providing up to 400mA output current. The 550KHz high switching rate minimized the size of external components. Besides, the $17\mu A$ low quiescent current together with high efficiency maintains long battery lifetime.

Ordering Information



Marking Information

Part Number	Marking		
RT9263CCX5	СН		
RT9263ECX5	CJ		

Features

- 1.0V Low Start-up Input Voltage
- High Supply Capability to Deliver 3.3V 100mA with 1V Input Voltage
- 17µA Quiescent (Switch-off) Supply Current
- 90% Efficiency
- 550KHz Fixed Switching Rate
- Providing Flexibility for Using Internal and External Power Switches
- SOT89-5 Package

Applications

- PDA
- Portable Instrument
- DSC

Pin Configurations

Part Number	Pin Configurations		
RT9263CCX5 (Plastic SOT89-5)	5 - 4	TOP VIEW 1. CE 2. VDD 3. FB 4. LX 5. GND	
RT9263ECX5 (Plastic SOT89-5)	5 4	TOP VIEW 1. EXT 2. VDD 3. FB 4. LX 5. GND	

RT9263 Preliminary RICHT

Typical Application Circuit

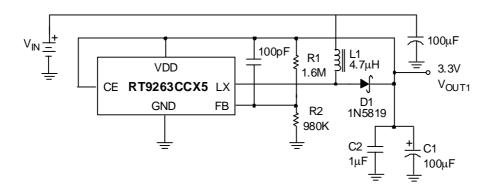


Fig. 1 RT9263CCX5 Typical Application for Portable Instruments below 400mA

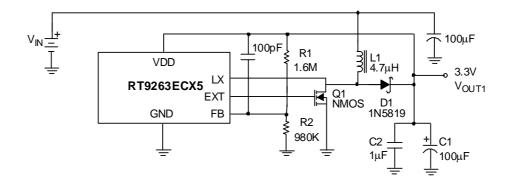


Fig. 2 0.4A ~ 1A Output Current Application

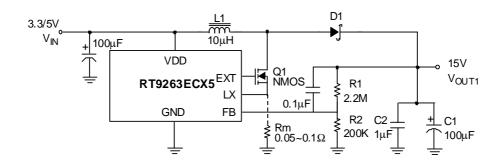


Fig. 3 High Voltage Application (Rm should be added when IL > 100mA)



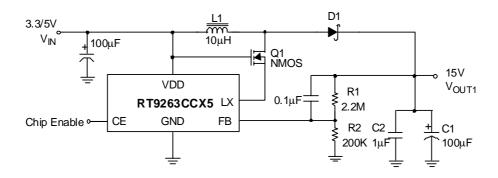
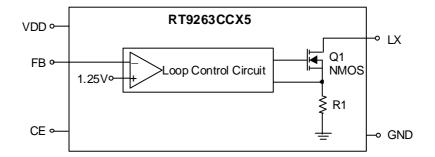
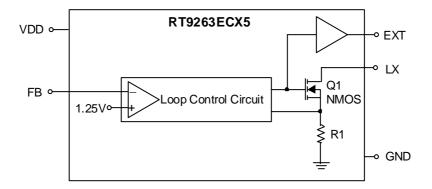


Fig.4 High Voltage Application with Shutdown Control

Function Block Diagram







Pin Description

Pin No.		Pin Name	B. E	
RT9263CCX5	RT9263ECX5		Pin Function	
	1	EXT	Output pin for driving external NMOS or NPN When driving an NPN, a resistor should be added for limiting base	
1		CE	Chip enable RT9263CCX5 gets into shutdown mode when CE pin set to low.	
2	2	VDD	Input positive power pin of RT9263	
3	3	FB	Feedback input pin Internal reference voltage for the error amplifier is 1.25V.	
4	4	LX	Pin for switching	
5	5	GND	Ground	

Absolute Maximum Ratings

Supply Voltage	0.3V to 7V
LX Pin Switch Voltage	-0.3V to (VDD + 0.8V)
Other I/O Pin Voltages	-0.3V to (VDD + 0.3V)
LX Pin Switch Current	2.5A
EXT Pin Driver Current	
 Power Dissipation, P_D @ T_A = 25°C 	
SOT89-5	0.5W
Package Thermal Resistance	
SOT89-5, θ _{JA}	300°C/W
Operating Junction Temperature	150°C
Storage Temperature Range	65°C ~ +150°C



Electrical Characteristics

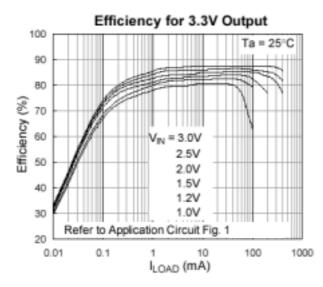
(V_{IN} = 1.5V, VDD set to 3.3V, Load Current = 0, T_A = 25°C, unless otherwise specified)

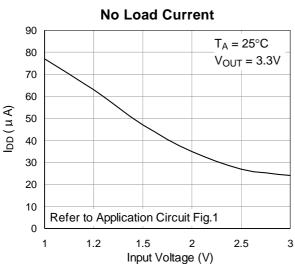
Parameter	Symbol	Test Conditions	Min	Тур	Max	Units
Start-UP Voltage	V _{ST}	I _L = 1mA		0.98	1.05	V
Operating VDD Range	V_{DD}	Start-up to I _{DD1} > 250μA	0.8		6.5	V
No Load Current I (V _{IN})	I _{NO LOAD}	$V_{IN} = 1.5V, V_{OUT} = 3.3V$		47		μΑ
Switch-off Current I (VDD)	I _{SWITCH OFF}	V _{IN} = 6V		17		μΑ
Shutdown Current I (V _{IN})	I _{OFF}	CE Pin = 0V, V _{IN} = 4.5V		0.1	1	μΑ
Feedback Reference Voltage	V_{REF}	Close Loop, VDD = 3.3V	1.225	1.25	1.275	V
Switching Rate	F _S	VDD = 3.3V		550		KHz
Maximum Duty	D _{MAX}	VDD = 3.3V		92		%
LX ON Resistance		VDD = 3.3V		0.25		Ω
Current Limit Setting	I _{LIMIT}	VDD = 3.3V		2		Α
EXT ON Resistance to VDD		VDD = 3.3V		40		Ω
EXT ON Resistance to GND		VDD = 3.3V		30		Ω
Line Regulation	ΔV_{LINE}	$V_{IN} = 1.5 \sim 2.5 V$, $I_L = 1 mA$		10		mV/V
Load Regulation	ΔV_{LOAD}	$V_{IN} = 2.5V$, $I_L = 1 \sim 100$ mA		0.25		mV/mA
CE Pin Trip Level		VDD = 3.3V	0.2	0.8	1.4	V
Temperature Stability for FB, LFB, LBI	T _S	Guaranteed by Design		50		ppm/∘C
Thermal Shutdown	T _{SD}	Guaranteed by Design		165		°C
Thermal Shutdown Hysterises	ΔT_{SD}	Guaranteed by Design		10		°C

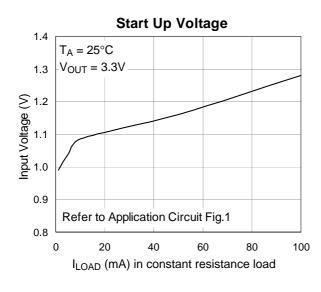
^{*} Note: The CE pin shall be tied to VDD pin and inhibit to act the ON/OFF state whenever the VDD pin voltage may reach to 5.5V or above.

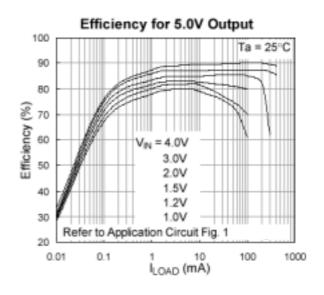


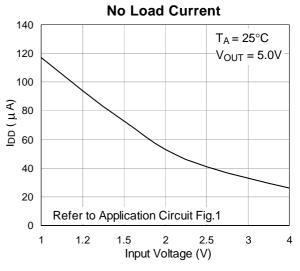
Typical Operating Charateristics

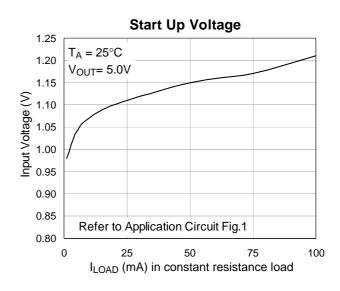














Application Note

Output Voltage Setting

Referring to application circuits Fig.1 to Fig.4, the output voltage of the switching regulator (V_{OUT1}) can be set with Eq.1.

$$V_{OUT1} = (1 + \frac{R1}{R2}) \times 1.25 V$$
 Eq. 1

Feedback Loop Design

Referring to application circuits Fig.1 to Fig.4, The selection of R1 and R2 based on the trade-off between quiescent current consumption and interference immunity is stated below:

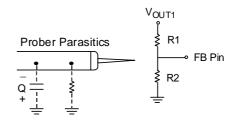
- Follow Eq.1
- Higher R reduces the quiescent current (Path current = 1.25V/R2), however resistors beyond 5MΩ are not recommended.
- Lower R gives better noise immunity, and is less sensitive to interference, layout parasitics, FB node leakage, and improper probing to FB pins.
- A proper value of feed forward capacitor parallel with R1 on Fig.1 to Fig.4 can improve the noise immunity of the feedback loops, especially in an improper layout. An empirical suggestion is around 100pF ~ 1 nF for feedback resistors of M Ω , and 10nF $\sim 0.1\mu$ F for feedback resistors of tens to hundreds K Ω .

For applications without standby or suspend modes, lower values of R1, and R2 are preferred. For applications concerning the current consumption in standby or suspend modes, the higher values of R1, and R2 are needed. Such "high impedance feedback loops" are sensitive to any interference, which require careful layout and avoid any interference, e.g. probing to FB pins.

PRECAUTION 1: Improper probing to FB pin will cause fluctuation at V_{OUT1} . It may damage RT9263 and system chips because V_{OUT1} may drastically rise to an over-rated level due to unexpected interference or parasitics being added to FB pin.

PRECAUTION 2: Disconnecting R1 or short circuit across R2 may also cause similar IC damage as described in precaution 1.

PRECAUTION 3: When large R values were used in feedback loops, any leakage in FB node may also cause V_{OUT1} voltage fluctuation, and IC damage. To be especially highlight here is when the air moisture frozen and re-melt on the circuit board may cause several μA leakage between IC or component pins. So, when large R values are used in feedback loops, post coating, or some other moisture-preventing processes are recommended.

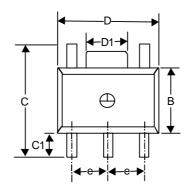


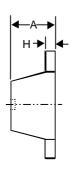
Layout Guide

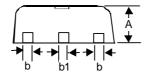
- A full GND plane without gap break.
- V_{OUT1} to GND noise bypass Short and wide connection for C2 to Pin2 and Pin5.
- V_{IN} to GND noise bypass Add a 100 μ F capacitor close to L1 inductor, when VIN is not an idea voltage source.
- Minimized FB node copper area and keep far away from noise sources.
- Minimized parasitic capacitance connecting to LX and EXT nodes, which may cause additional switching loss.



Package Information







Cymala al	Dimensions I	n Millimeters	Dimensions In Inches		
Symbol	Min	Max	Min	Max	
А	1.400	1.600	0.055	0.063	
b	0.360	0.520	0.014	0.020	
В	2.400	2.600	0.094	0.102	
b1	0.406	0.533	0.016	0.021	
С		4.250	-	0.167	
C1	0.800	-	0.031		
D	4.400	4.600	0.173	0.181	
D1		1.700		0.067	
е	1.400	1.600	0.055	0.063	
Н	0.380	0.430	0.014	0.017	

5-Lead SOT-89 Surface Mount





RICHTEK TECHNOLOGY CORP.

Headquarter 5F, No. 20, Taiyuen Street, Chupei City Hsinchu, Taiwan, R.O.C. Tel: (8863)5526789 Fax: (8863)5526611

RICHTEK TECHNOLOGY CORP.

Taipei Office (Marketing)
8F-1, No. 137, Lane 235, Paochiao Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)89191466 Fax: (8862)89191465
Email: marketing@richtek.com