

16M-Bit (2Mx8 /1Mx16) CMOS MASK ROM

FEATURES

- Switchable organization
2,097,152 x 8(byte mode)
1,048,576 x 16(word mode)
- Fast access time
Random Access
100ns(Max.) : CL=50pF
120ns(Max.) : CL=100pF
- Supply voltage : single +5V
- Current consumption
Operating : 50mA(Max.)
Standby : 50µA(Max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Package
-. K3N5C1000E-TC : 44-TSOP2-400

GENERAL DESCRIPTION

The K3N5C1000E-TC is a fully static mask programmable ROM fabricated using silicon gate CMOS process technology, and is organized either as 2,097,152x8 bit(byte mode) or as 1,048,576x16 bit(word mode) depending on BHE voltage level.(See mode selection table)

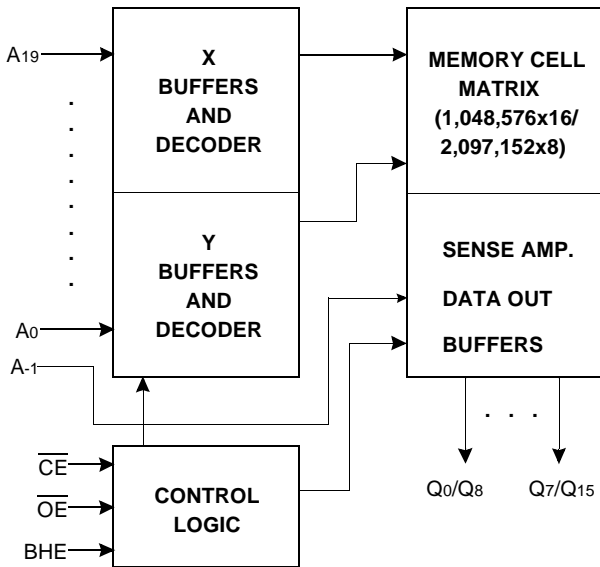
This device operates with a 5V single power supply, and all inputs and outputs are TTL compatible.

Because of its asynchronous operation, it requires no external clock assuring extremely easy operation.

It is suitable for use in program memory of microprocessor, and data memory, character generator.

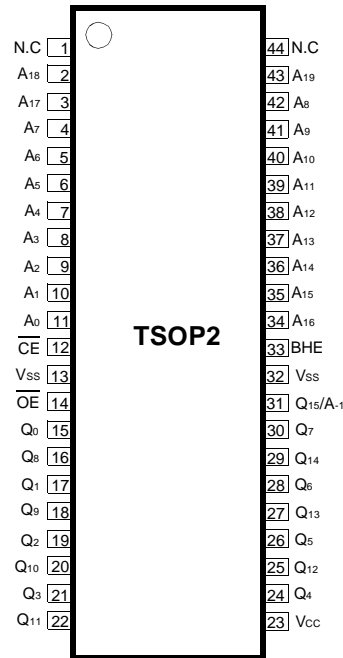
The K3N5C1000E-TC is packaged in a 44-TSOP2.

FUNCTIONAL BLOCK DIAGRAM



Pin Name	Pin Function
A0 - A19	Address Inputs
Q0 - Q14	Data Outputs
Q15 /A-1	Output 15(Word mode)/ LSB Address(Byte mode)
BHE	Word/Byte selection
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

PIN CONFIGURATION



K3N5C1000E-TC

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V _{IN}	-0.3 to +7.0	V
Temperature Under Bias	T _{BIAS}	-10 to +85	°C
Storage Temperature	T _{Stg}	-55 to +150	°C

NOTE : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(Voltage reference to Vss, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Supply Voltage	V _{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I _{CC}	Cycle=5MHz, all outputs open CE=OE=V _{IL} , V _{IN} =0.6V to 2.4V (AC Test Condition)	-	50	mA
Standby Current(TTL)	I _{SB1}	CE=V _{IH} , all outputs open	-	1	mA
Standby Current(CMOS)	I _{SB2}	CE=V _{CC} , all outputs open	-	50	μA
Input Leakage Current	I _{LI}	V _{IN} =0 to V _{CC}	-	10	μA
Output Leakage Current	I _{LO}	V _{OUT} =0 to V _{CC}	-	10	μA
Input High Voltage, All Inputs	V _{IH}		2.2	V _{CC} +0.3	V
Input Low Voltage, All Inputs	V _{IL}		-0.3	0.8	V
Output High Voltage Level	V _{OH}	I _{OH} = -400μA	2.4	-	V
Output Low Voltage Level	V _{OL}	I _{OL} = 2.1mA	-	0.4	V

NOTE : Minimum DC Voltage(V_{IL}) is -0.3V an input pins. During transitions, this level may undershoot to -2.0V for periods <20ns.
Maximum DC voltage on input pins(V_{IH}) is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.

MODE SELECTION

CE	OE	BHE	Q _{15/A-1}	Mode	Data	Power
H	X	X	X	Standby	High-Z	Standby
L	H	X	X	Operating	High-Z	Active
L	L	H	Output	Operating	Q ₀ ~Q ₁₅ : Dout	Active
		L	Input	Operating	Q ₀ ~Q ₇ : Dout Q ₈ ~Q ₁₄ : Hi-Z	Active

CAPACITANCE(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	Min	Max	Unit
Output Capacitance	C _{OUT}	V _{OUT} =0V	-	12	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	12	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

K3N5C1000E-TC

CMOS MASK ROM

AC CHARACTERISTICS ($T_A=0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

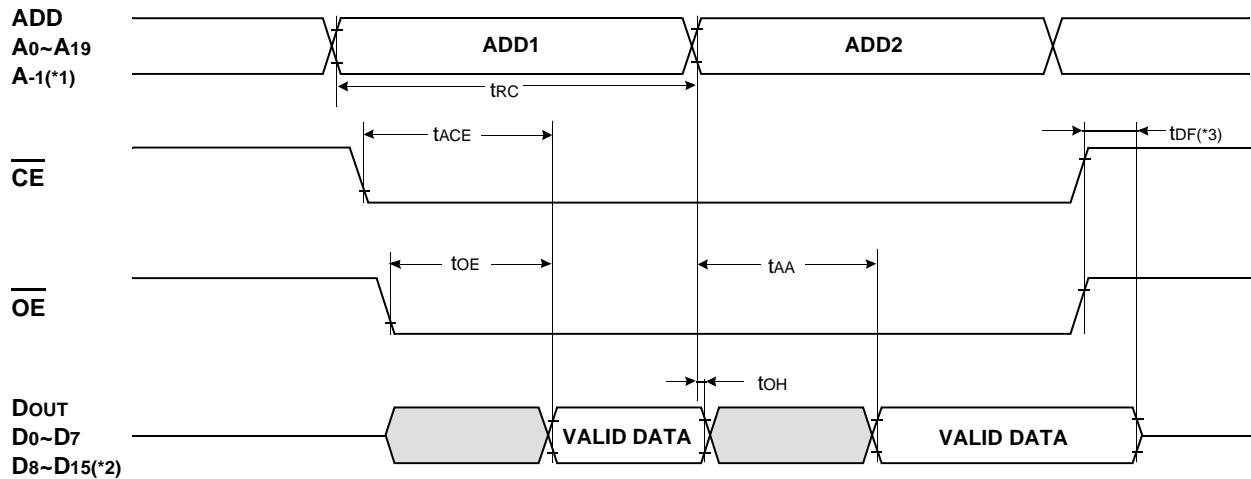
Item	Value
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	10ns
Input and Output timing Levels	0.8V and 2.0V
Output Loads	1 TTL Gate and $C_L=50\text{pF}$ or 100pF

READ CYCLE

Item	Symbol	K3N5C1000E-TC10 ($C_L=50\text{pF}$)		K3N5C1000E-TC12 ($C_L=100\text{pF}$)		K3N5C1000E-TC15 ($C_L=100\text{pF}$)		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	100		120		150		ns
Chip Enable Access Time	t _{ACE}		100		120		150	ns
Address Access Time	t _{AA}		100		120		150	ns
Output Enable Access Time	t _{OE}		50		60		70	ns
Output or Chip Disable to Output High-Z	t _{DF}		20		20		30	ns
Output Hold from Address Change	t _{OH}	0		0		0		ns

TIMING DIAGRAM

READ



NOTES :

*1. Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})

*2. Word Mode only. (BHE = V_{IH})

*3. t_{DF} is defined as the time at which the outputs achieve the open circuit condition and is not referenced to V_{OH} or V_{OL} level.