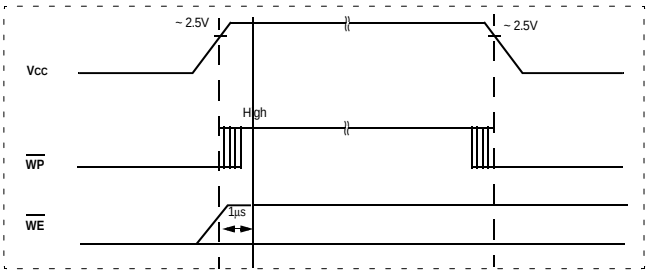
Document Title

SmartMedia™ Card

Revision History

Revision No	History	Draft Date	Remark
0.0	Initial issue	July 17th 2000	Advanced Information
0.1	1. Explain how pointer operation works in detail. 2. Updated operation for tRST timing - If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.	Nov. 20th 2000	Preliminary
0.2	1. Renamed the 17th pin from Vcc to LVD(Low Voltage Detect) -The LVD is used to electrically detect the proper supply voltage. By connecting this pin to Vss through a pull-down resister, it is possible to distinguish 3.3V product from 5V product. When 3.3V is applied as Vcc to pins 12 and 22, a 'High' level can be detected on the system side if the device is a 3.3V product, and 'Low' level for 5V product.	Mar. 2th 2001	Final
0.3	1.Powerup sequence is added Recovery time of minimum 1µs is required before internal circuit gets ready for any command sequences  2. AC parameter tCLR(CLE to $\overline{RE}$ Delay, min 50ns) is added. 3. AC parameter tAR1 value : 100ns --> 20ns	Sep. 7th 2001	

Note : For more detailed features and specifications including FAQ, please refer to Samsung's Flash web site.
http://www.samsung.com/Products/Semiconductor/Flash/TechnicalInfo/datasheets.htm

Revision History

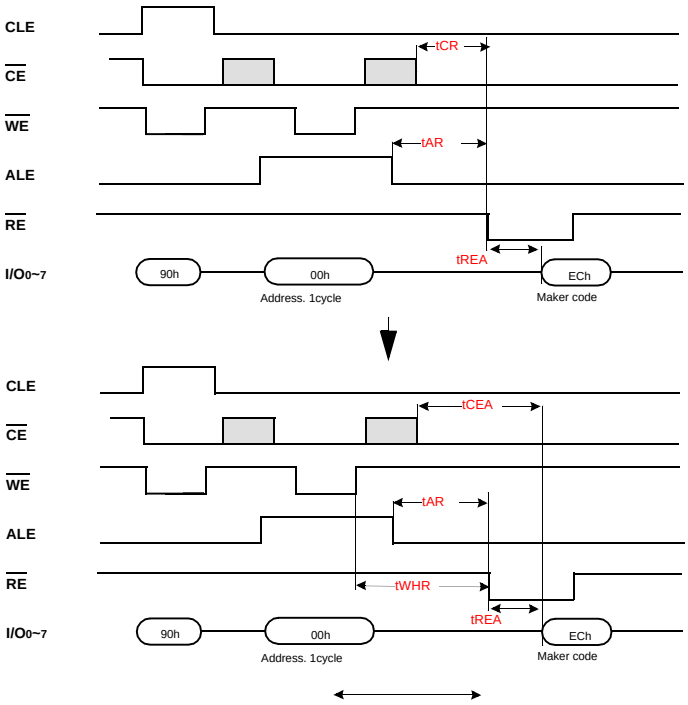
Revision No	History	Draft Date	Remark
0.4	1. Unified access timing parameter definition for multiple operating modes - Changed AC characteristics (Before)	Sep. 7th 2001	Final

Parameter	Symbol	Min	Max	Unit
ALE to $\overline{RE}$ Delay (ID read)	t_{AR1}	100	-	ns
ALE to $\overline{RE}$ Delay (Read cycle)	t_{AR2}	100	-	
$\overline{RE}$ Low to Status Output	t_{RSTO}	-	35	
$\overline{CE}$ Low to Status Output	t_{CSTO}	-	45	
$\overline{RE}$ access time(Read ID)	t_{READID}	-	35	

- AC characteristics (After)

. Deleted t_{RSTO}, t_{CSTO} and t_{READID} / Added t_{CLR}, t_{CEA}

Parameter	Symbol	Min	Max	Unit
ALE to $\overline{RE}$ Delay (ID read)	t_{AR1}	50	-	ns
ALE to $\overline{RE}$ Delay (Read cycle)	t_{AR2}	50	-	
CLE to $\overline{RE}$ Delay	t_{CLR}	10		
$\overline{CE}$ Access Time	t_{CEA}	-	45	



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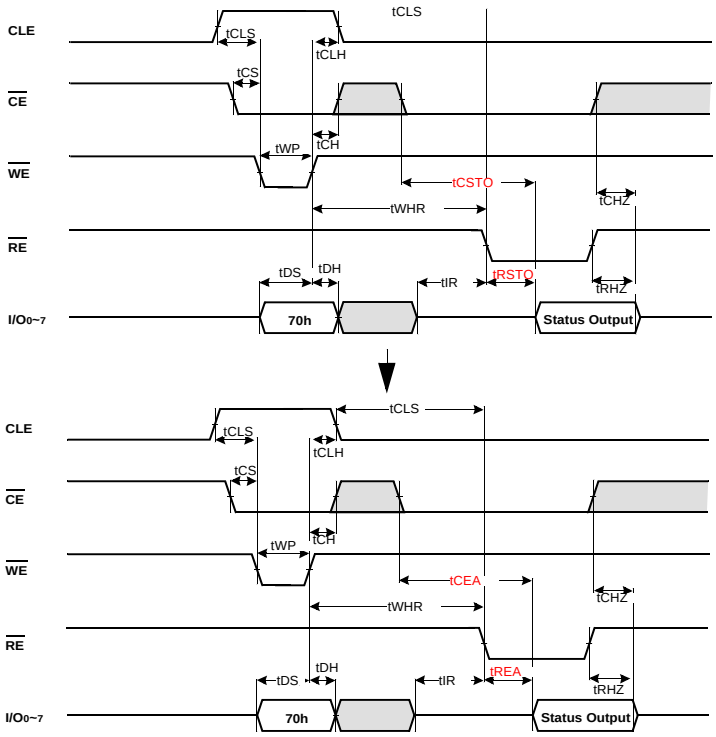


0.5	1. Eliminated the duplicated AC parameter. - AC characteristics (Before) . Replaced t_{AR1},t_{AR2} with t_{AR}	Feb. 9th 2002	Final

Parameter	Symbol	Min	Max	Unit
ALE to $\overline{RE}$ Delay (ID read)	t_{AR1}	50	-	ns
ALE to $\overline{RE}$ Delay (Read cycle)	t_{AR2}	50	-	
CLE to $\overline{RE}$ Delay	t_{CLR}	10		
$\overline{CE}$ Access Time	t_{CEA}	-	45	

- AC characteristics (After)

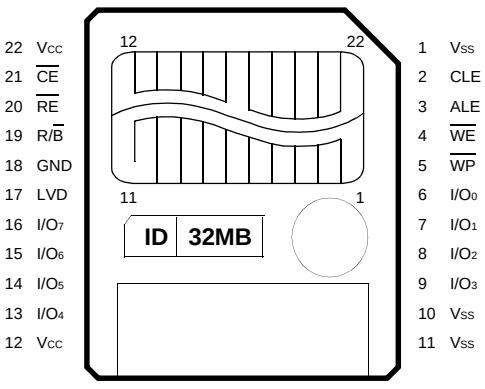
Parameter	Symbol	Min	Max	Unit
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10		
$\overline{CE}$ Access Time	t_{CEA}	-	45	

SmartMedia™ Card

FEATURES

•Single 2.7V~3.6V Supply
•Organization
- Memory Cell Array :
8MB(K9S6408V0X) : (8M + 256K)bit x 8bit
16MB(K9S2808V0X) : (16M + 512K)bit x 8bit
32MB(K9S5608V0X) : (32M + 1,024K)bit x 8bit
- Data Register : (512 + 16)bit x8bit
•Automatic Program and Erase
- Page Program : (512 + 16)Byte
- Block Erase
32MB, 16MB(K9S56/2808V0X) : (16K + 512)Byte
8MB (K9S6408V0X) : (8K + 256)Byte
•528-Byte Page Read Operation
- Random Access : 10µs(Max.)
* K9S6408V0B/A : 7µs(Max.)
* K9S6408V0C : 10µs(Max.)
- Serial Page Access : 50ns(Min.)
•Fast Write Cycle Time
- Program Time : 200µs(Typ.)
- Block Erase Time : 2ms(Typ.)
•Command/Address/Data Multiplexed I/O Port
•Hardware Data Protection
- Program/Erase Lockout During Power Transitions
•Reliable CMOS Floating-Gate Technology
- Endurance : 100K Program/Erase Cycles
* K9S6408V0X : 1Million Program/Erase Cycles
- Data Retention : 10 years
•Command Register Operation
•22pad SmartMedia™(SSFDC)
•Unique ID for Copyright Protection

SmartMedia™ CARD(SSFDC)



22 PAD SmartMedia™

GENERAL DESCRIPTION

Using Nand flash memory, SmartMedia provides the most cost-effective solution for the solid state mass storage market. A program operation is implemented by the single page of 528 bytes in typical 200µs and an erase operation is done by the single block of 16K bytes (K9S6408V0X: 8K bytes) in typical 2ms. Data in a page can be read out at 50ns cycle time per byte. The I/O pins serve as ports for address and data inputs/outputs as well as command inputs. The on-chip writing controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the SmartMeida′s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. (*Endurance varies according to its density. please refer to Features). SmartMedia is an optimum solution for data storage applications such as solid state file storage, digital voice recorder, digital still camera and other portable applications requiring non-volatility.

PIN DESCRIPTION

Device	Unique ID Support
K9S2808V0X K9S5608V0X K9S6408V0C	O
K9S6408V0A/M	X

PIN DESCRIPTION

Pin Name	Pin Function
I/O0 ~ I/O7	Data Input/Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
LVD	Low Voltage Detect
GND	Ground
R/$\overline{B}$	Ready/Busy output
VCC	Power
VSS	Ground
N.C	No Connection

NOTE : Connect all VCC and VSS pins of each device to common power supply outputs and do not leave VCC or VSS disconnected. The pin 17(LVD) is used to detect 5V or 3.3V product electrically. Please, refer to the SmartMedia Application note for detail.

Figure 1. FUNCTIONAL BLOCK DIAGRAM

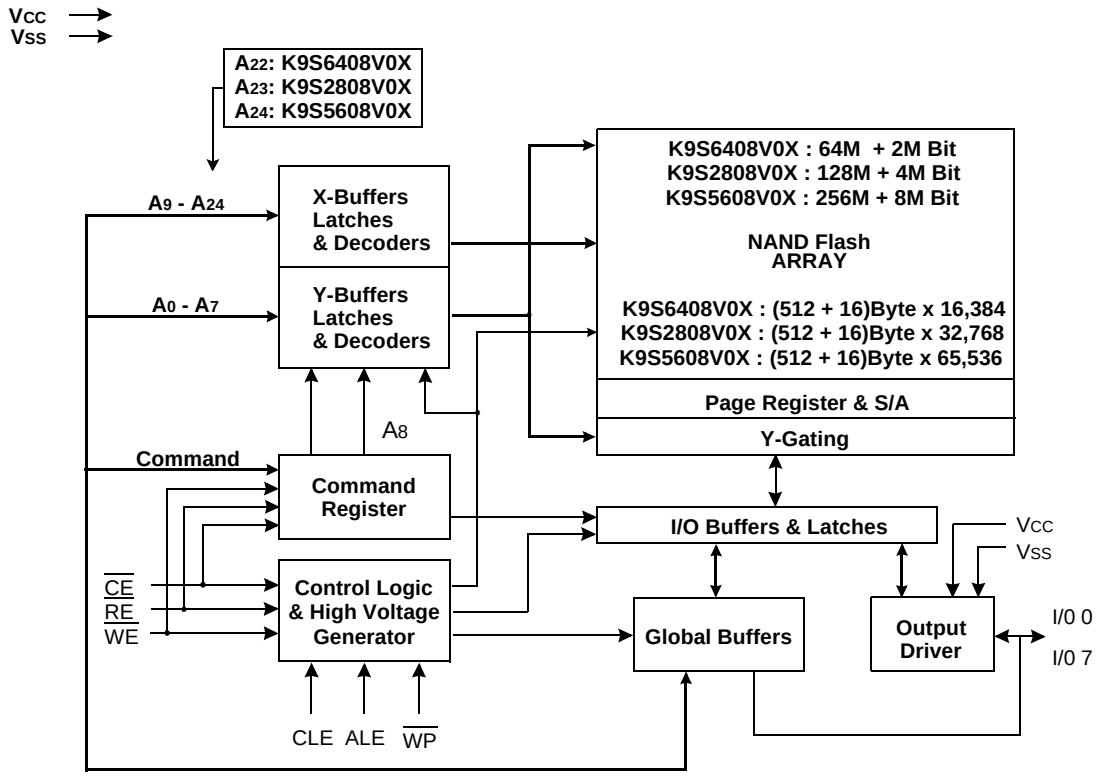
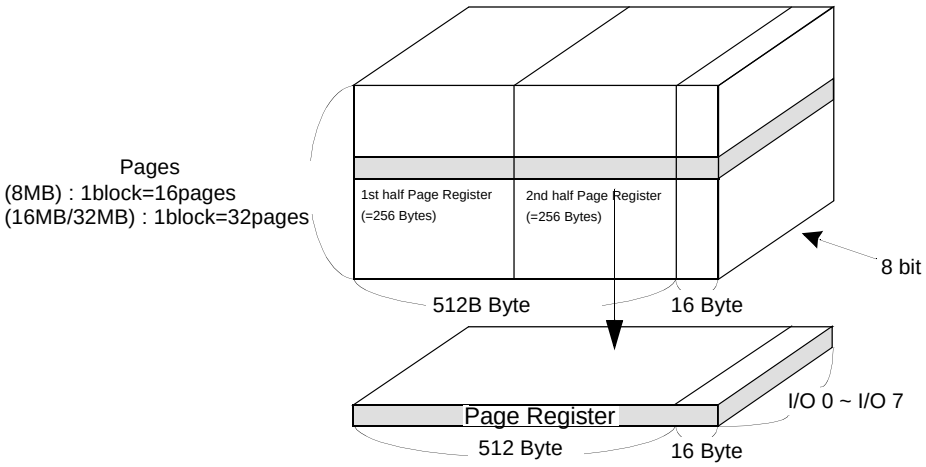


Figure 2. ARRAY ORGANIZATION



ARRAY ORGANIZATION

	1 Page	1 Block	1 Device
K9S6408V0X	528 Byte	528 Bytes x 16 Pages	528 Byte x 16Pages x 1024 Blocks
K9S2808V0X	528Byte	528Bytes x 32 Pages	528Byte x 32Pages x 1024 Blocks
K9S5608V0X	528 Byte	528 Byte x 32 Pages	528Bytes x 32Pages x 2048 Blocks

NOTE : Column Address : Starting Address of the Register.

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	**Column Address**
2nd Cycle	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	**Row Address (Page Address)**
3rd Cycle	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	(A_{22})	(A_{23})	(A_{24})	

00h Command(Read) : Defines the starting address of the 1st half of the register.

01h Command(Read) : Defines the starting address of the 2nd half of the register.

A_{22}: K9S6408V0X should be designated up to A_{22}, addresse A_{23} to A_{24} must be set to "Low".

A_{23}: K9S2808V0X should be designated up to A_{23}, address A_{24} must be set to "Low".

A_{24}: K9S5608V0X should be designated up to A_{24}.

* A_8 is set to "Low" or "High" by the 00h or 01h Command.

* The device ignores any additional input of address cycles than reguired.

PRODUCT INTRODUCTION

The SmartMeida has the memory organization as following Table1. Spare sixteen columns are located from column address of 512 to 527. A 528-byte data register is connected to memory cell arrays and is accommodating data-transfer between the I/O buffers and memory cell arrays during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of the 32 pages formed by two 16 cell memory array. The array organization is shown in Figure 2. The program and the read operations are executed on a page basis, while the erase operation is executed on a block basis.

The SmartMedia has addresses multiplexed into 8 I/O's. This scheme dramatically reduces pin counts and allows system upgrade to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except for Block Erase and Page Program commands which require two cycles: one cycle for a setup and another for an execution. The physical space of the SmartMedia varies according to its density and from 8MB to 32MB SmartMedia require three cycles for byte-level addressing; column address, row address, in that order. Page Read and Page Program need the same three address cycles following the required command input. In Block Erase operation, however, only the two row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 2. defines the specific commands of the SmartMedia.

Table 1.MEMORY ORGANIZATION

	Memory Organization	Number of rows(Pages)	Number of columns
K9S6408V0X	66Mbit (69,206,016 bit)	16,384 rows	528 columns
K9S2808V0X	132Mbit (138,412,032 bit)	32,768 rows	528 columns
K9S5608V0X	264Mbit (276,824,064 bit)	65,536 rows	528 columns

Table 2. COMMAND SETS

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read 1	00h/01h(1)	-	
Read 2	50h	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Block Erase	60h	D0h	
Read Status	70h	-	O

NOTE: 1. The 00h command defines starting address of the 1st half of registers.The 01h command defines starting address of the 2nd half of registers. After data access on the 2nd half of register by the 01h command, address pointer is automatically moved to the 1st half register(00h) on the next cycle.

Caution : Any undefined command inputs are prohibited except for above command sets of Table2.

PIN DESCRIPTION

Command Latch Enable(CLE)

The CLE input controls the path activation for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.

Address Latch Enable(ALE)

The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.

Chip Enable($\overline{CE}$)

The $\overline{CE}$ input is the device selection control. When $\overline{CE}$ goes high during a read operation the device is returned to standby mode. However, when the device is in the busy state during program or erase, $\overline{CE}$ high is ignored and does not return the device to standby mode.

Write Enable($\overline{WE}$)

The $\overline{WE}$ input controls writing to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.

Read Enable($\overline{RE}$)

The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus.

I/O Port : I/O 0 ~ I/O 7

The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.

Write Protect($\overline{WP}$)

The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.

Ready/$\overline{Busy}$(R/$\overline{B}$)

The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.

Low Voltage Detect(LVD)

The LVD is used to detect the proper supply voltage electrically. By connecting this pin to Vss through a pull-down resister, it is possible to distinguish 3.3V product from 5V product. When 3.3V is applied as Vcc to pins 12 and 22, a 'High' level can be detected on the system side if the device is a 3.3V product, and 'Low' level for 5V product.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}	-0.6 to + 4.6	V
	V_{CC}	-0.6 to + 4.6	
Temperature Under Bias	T_{BIAS}	-10 to +65	°C
Storage Temperature	T_{STG}	-20 to +65	°C

NOTE :
1. Minimum DC voltage is -0.3V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, T_A=0 to 55°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Sequential Read	I_{CC1}	tRC=50ns, $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	10	20	mA
	Program	I_{CC2}	-	-	10	20	
	Erase	I_{CC3}	-	-	10	20	
Stand-by Current(TTL)		I_{SB1}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	1	
Stand-by Current(CMOS)		I_{SB2}	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}	-	10	50	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to 3.6V	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to 3.6V	-	-	±10	
Input High Voltage, All inputs		V_{IH}	-	2.0	-	V_{CC}+0.3	V
Input Low Voltage, All inputs		V_{IL}	-	-0.3	-	0.8	
Output High Voltage Level		V_{OH}	I_{OH}=-400µA	2.4	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=2.1mA	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	mA

VALID BLOCK

Parameter		Symbol	Min	Typ.	Max	Unit
Valid Block Number	K9S6408V0X	N_{VB}	1,014	1,020	1,024	Blocks
	K9S2808V0X		1,004	-	1,024	
	K9S5608V0X		2013	-	2048	

NOTE :
1. The K9SXX08V0X may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for an appropriate management of invalid blocks.
2. Per the specification of the physical format version 1.2 by SSFDC forum, minimum 1,000 vaild blocks are guaranteed for each 16MB memory space. (Refer to the attached technical notes)

AC TEST CONDITION

(T_A=0 to 55°C, V_{CC}=2.7V~3.6V unless otherwise noted)

Parameter	Value
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load (3.0V +/-10%)	1 TTL GATE and CL=50pF
Output Load (3.3V +/-10%)	1 TTL GATE and CL=100pF

CAPACITANCE(T_A=25°C, V_{CC}=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input(3clock)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input(3clock)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	sequential Read & Data Output	
X	X	L	X	X	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program/Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	500	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	2	cycles
	Spare Array				3	cycles
Block Erase Time		t_{BERS}	-	2	3	ms

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE setup Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
$\overline{CE}$ setup Time	t_{CS}	0	-	ns
$\overline{CE}$ Hold Time	t_{CH}	10	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	25(1)	-	ns
ALE setup Time	t_{ALS}	0	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	50	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	-	ns

NOTE : 1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	10	µs
CLE to $\overline{RE}$ Delay	t_{CLR}	10	-	ns
ALE to $\overline{RE}$ Delay	t_{AR}	10	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	30	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	50	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	35	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	15	30	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	20	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	-	ns
Last RE High to Busy (at sequential read)	t_{RB}	-	100	ns
$\overline{CE}$ High to Ready (in case of interception by $\overline{CE}$ at read)	t_{CRY}	-	50 +tr(R/$\overline{B}$)(1)	ns
$\overline{CE}$ High Hold Time(at the last serial read)(2)	t_{CEH}	100	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	-	ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	5/10/500(3)	µs

NOTE : 1. The time to Ready depends on the value of the pull-up resistor tied R/$\overline{B}$ pin.
2. To break the sequential read cycle, $\overline{CE}$ must be held high for longer time than tCEH.
3. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.

SmartMedia Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping.

Identifying Invalid Block(s)

SSFDC Forum specifies the logical format and physical format to ensure compatibility of SmartMedia. Samsung pre-formats SmartMedia in the Forum-compliant format prior to shipping. The physical format standard by SSFDC Forum specifies that invalid block information is written at the 6th byte of spare area in invalid blocks with two or more "0" bits, while valid blocks are erased(FFh). Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the original invalid block information is prohibited.

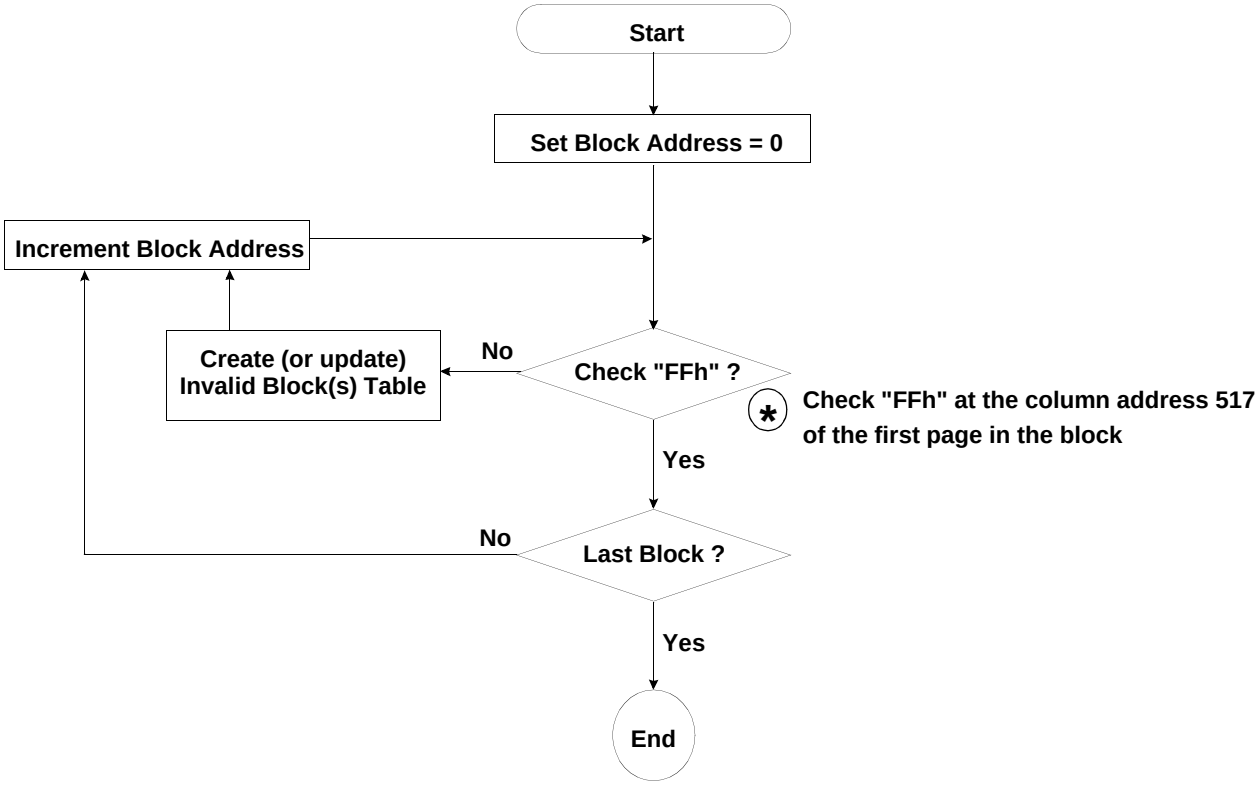


Figure 3. Flow chart to create invalid block table.

SmartMedia Technical Notes *(Continued)*

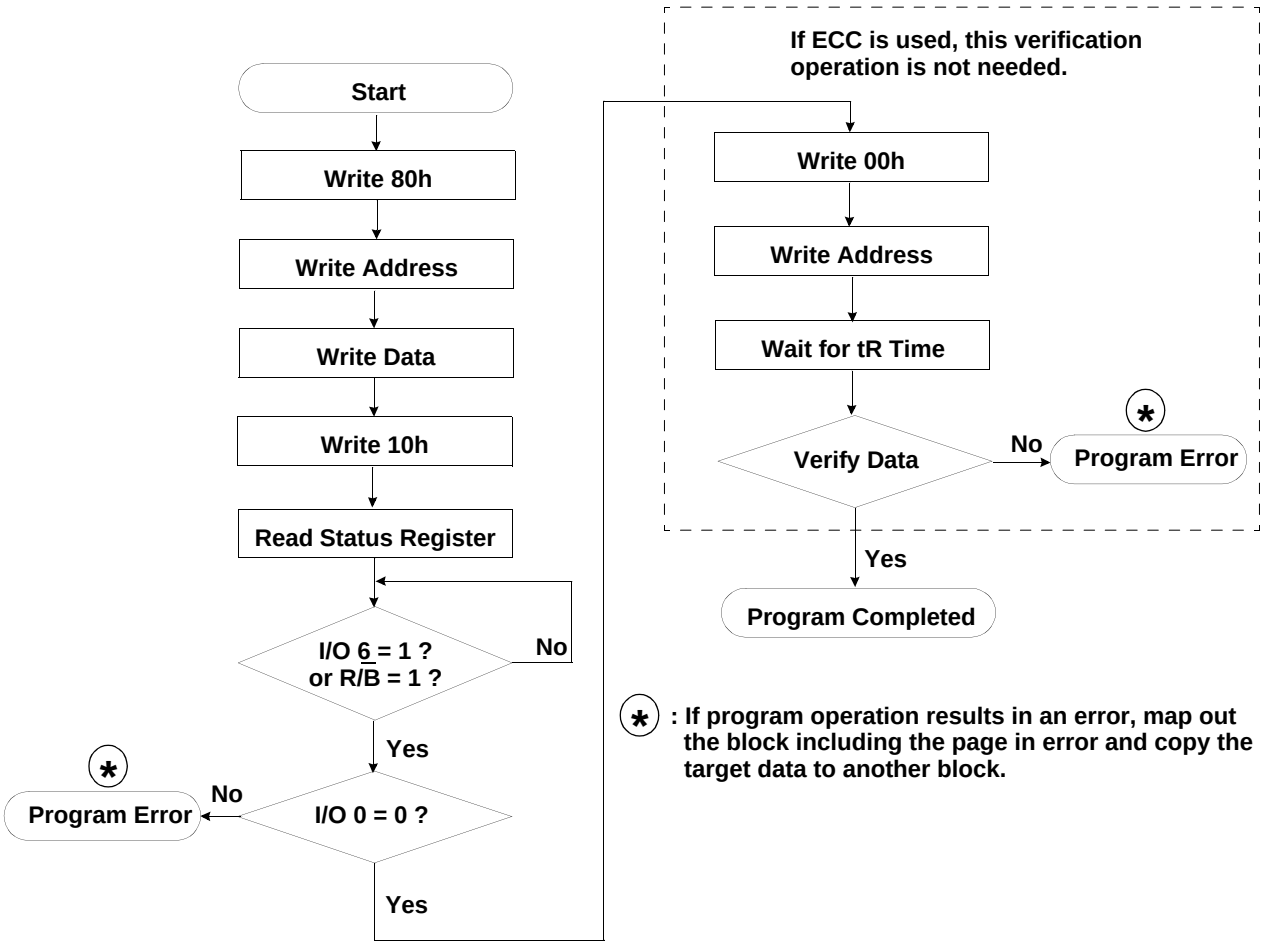
Error in write or read operation

Over its life time, the additional invalid blocks may be developed during its use. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status failure during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest data of the replaced block. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement or ECC Correction
Read	Single Bit Failure	Verify ECC -> ECC Correction

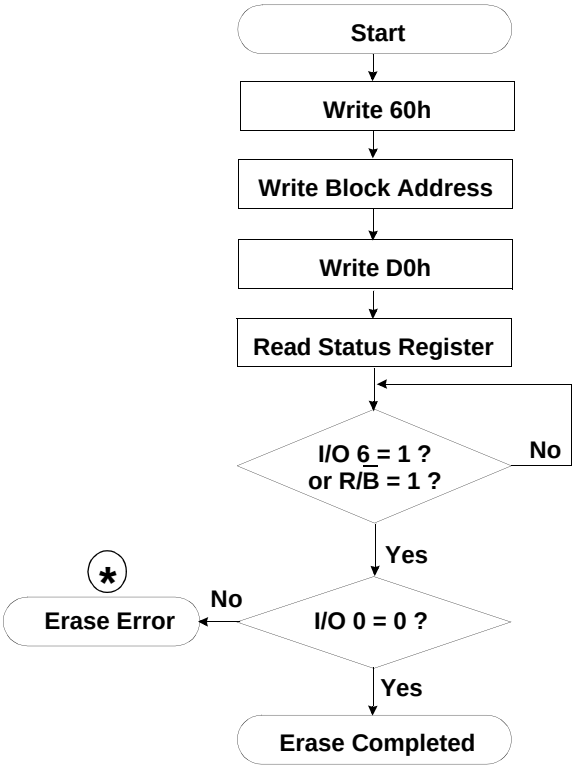
ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

Program Flow Chart

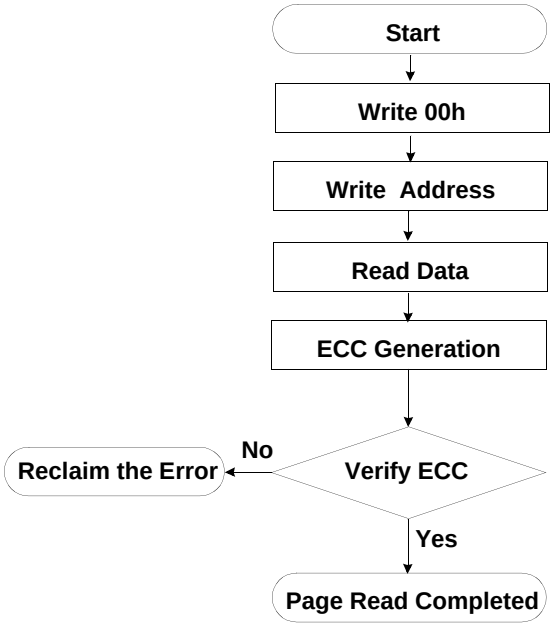


SmartMedia Technical Notes *(Continued)*

Erase Flow Chart

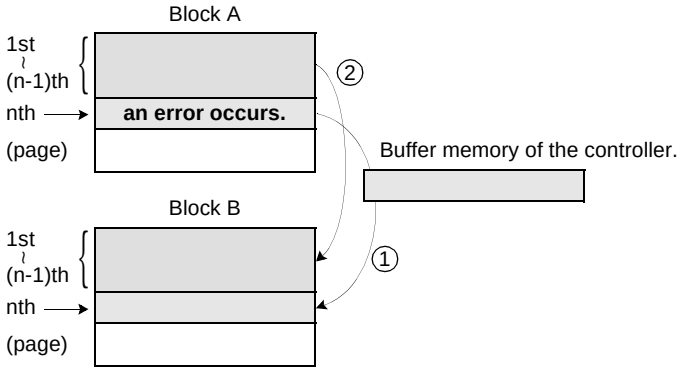


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement



* Step1
When an error happens in the nth page of the Block 'A' during the program operation.
* Step2
Copy the nth page data of the Block 'A' in the buffer memory to the nth page of another free block. (Block 'B')
* Step3
Then, copy the data in the 1st ~ (n-1)th page of the Block 'A' to the same location of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid Block' table or using other appropriate scheme.

Pointer Operation of the SmartMedia

Samsung NAND Flash has three address pointer commands as a substitute for the two most significant column addresses. '00h' command sets the pointer to 'A' area(0~255byte), '01h' command sets the pointer to 'B' area(256~511byte), and '50h' command sets the pointer to 'C' area(512~527byte). With these commands, the starting column address can be set to any of a whole page(0~527byte). '00h' or '50h' is sustained until another address pointer command is inputted. '01h' command, however, is effective only for one operation. After any operation of Read, Program, Erase, Reset, Power_Up is executed once with '01h' command, the address pointer returns to 'A' area by itself. To program data starting from 'A' or 'C' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary. To program data starting from 'B' area, '01h' command must be inputted right before '80h' command is written.

Destination of the pointer

Command	Pointer position	Area
00h	0 ~ 255 byte	1st half array(A)
01h	256 ~ 511 byte	2nd half array(B)
50h	512 ~ 527 byte	spare array(C)

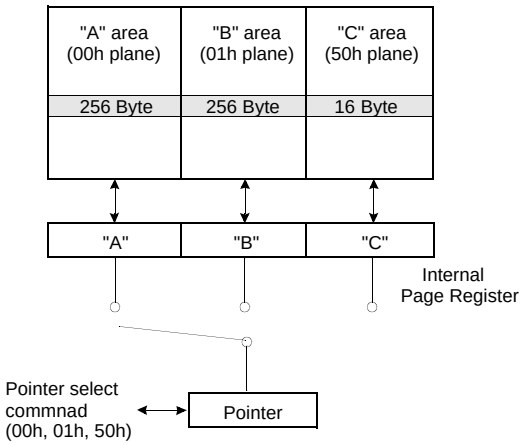
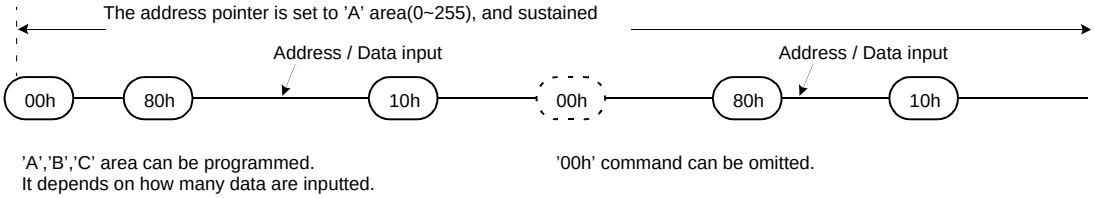


Figure 4. Block Diagram of Pointer Operation

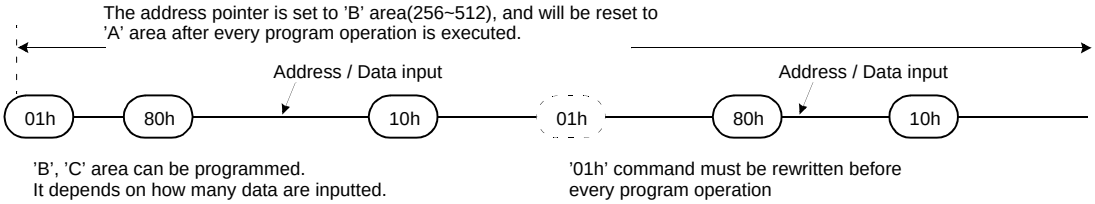
(1) Command input sequence for programming 'A' area



'A','B','C' area can be programmed.
It depends on how many data are inputted.

'00h' command can be omitted.

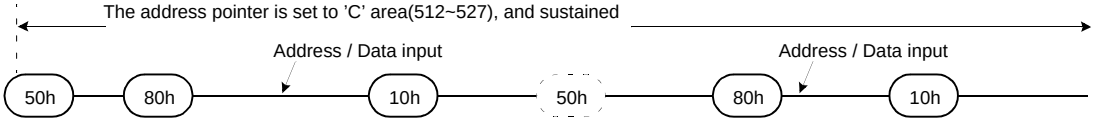
(2) Command input sequence for programming 'B' area



'B', 'C' area can be programmed.
It depends on how many data are inputted.

'01h' command must be rewritten before
every program operation

(3) Command input sequence for programming 'C' area



Only 'C' area can be programmed.

'50h' command can be omitted.

System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or sequential read as shown below. The internal 528byte page registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant savings in power consumption.

Figure 5. Program Operation with $\overline{CE}$ don't-care.

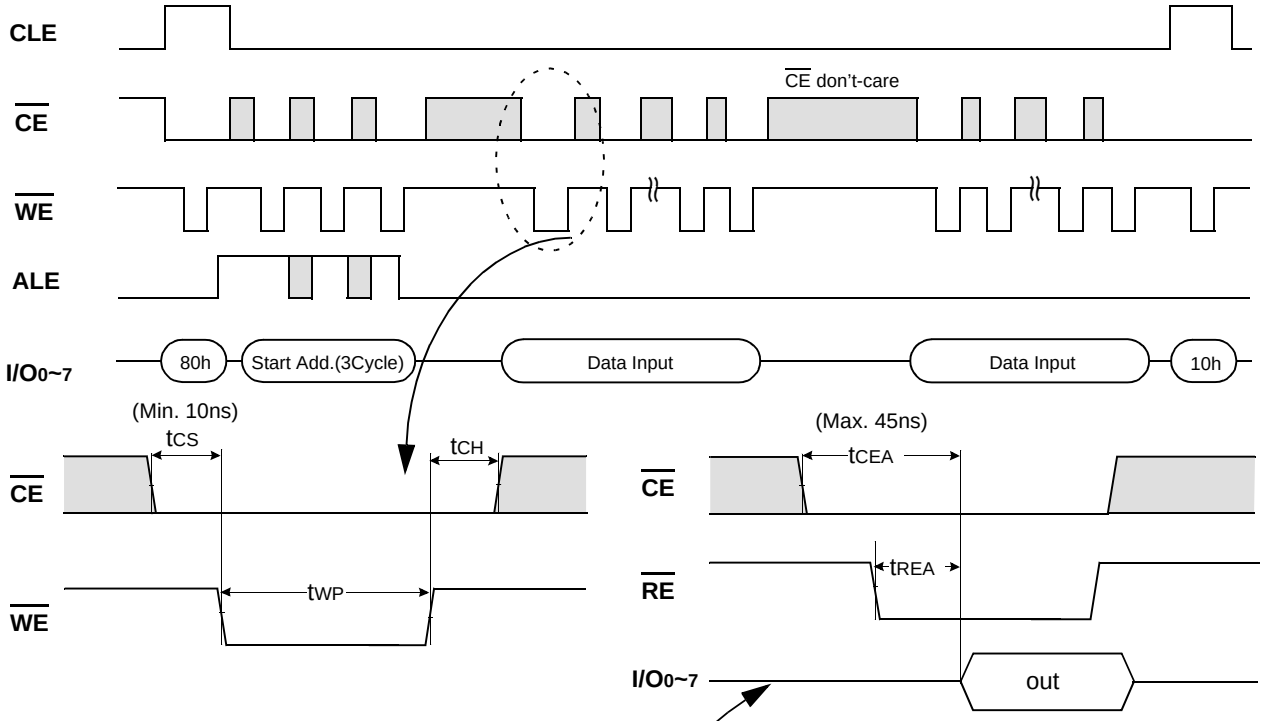
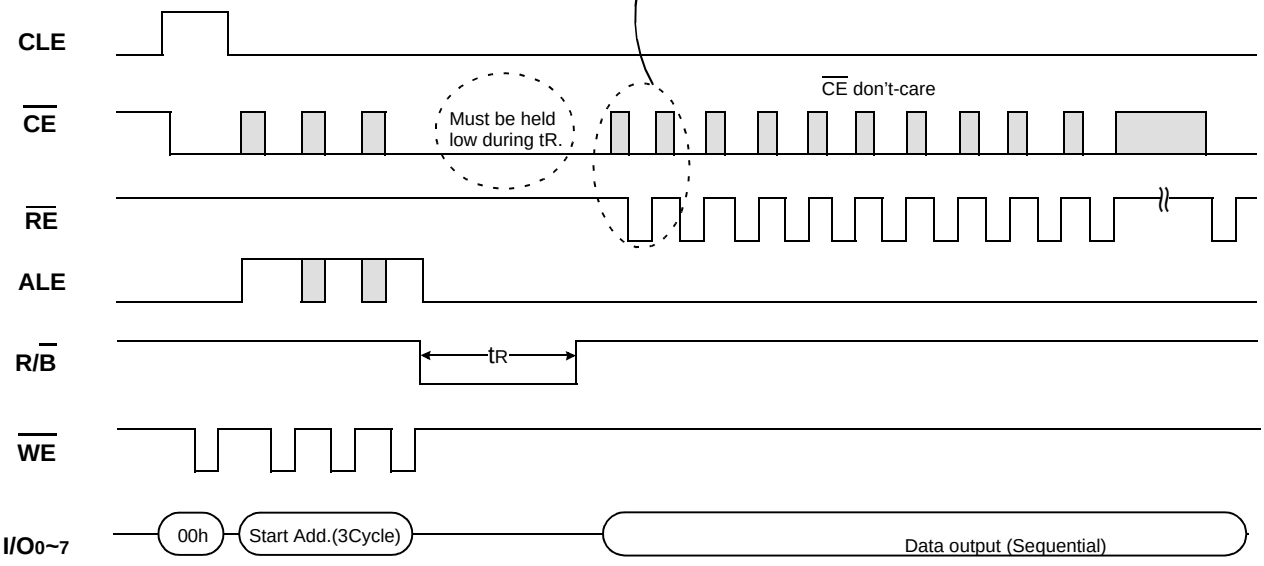
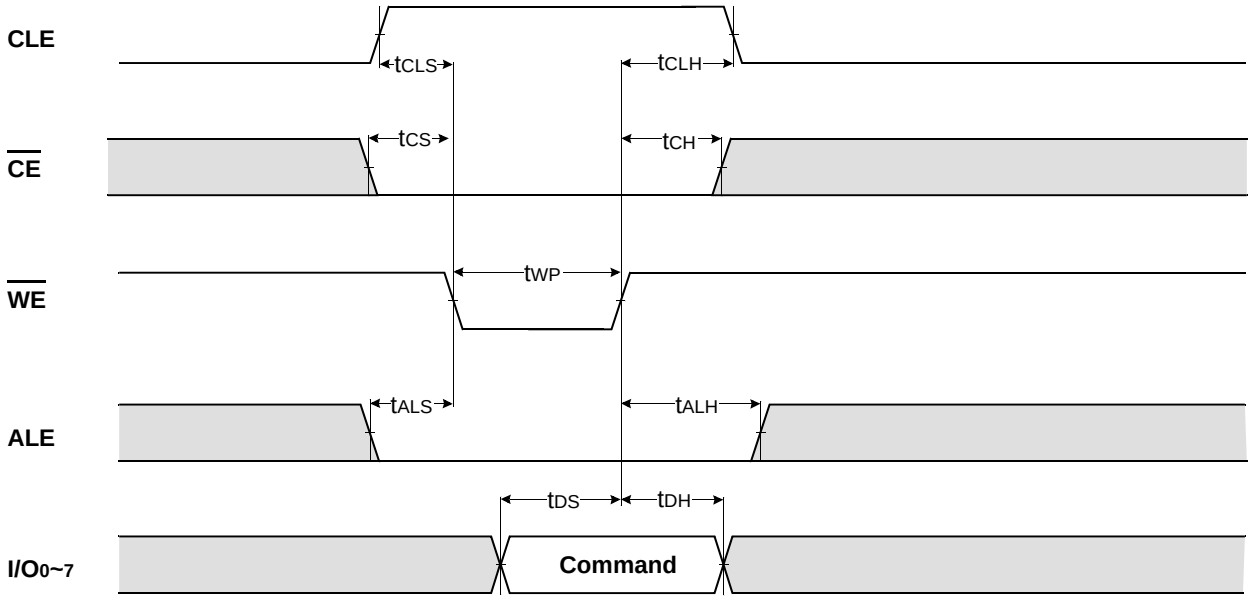


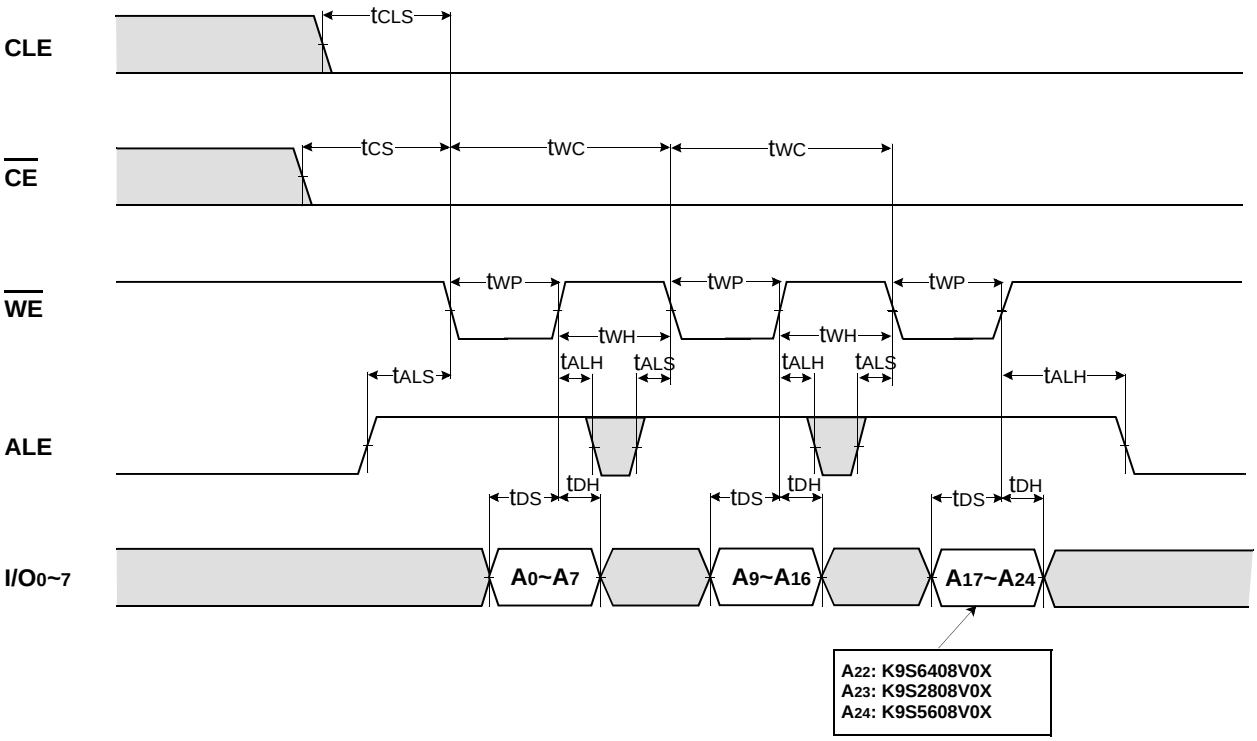
Figure 6. Read Operation with CE don't-care.



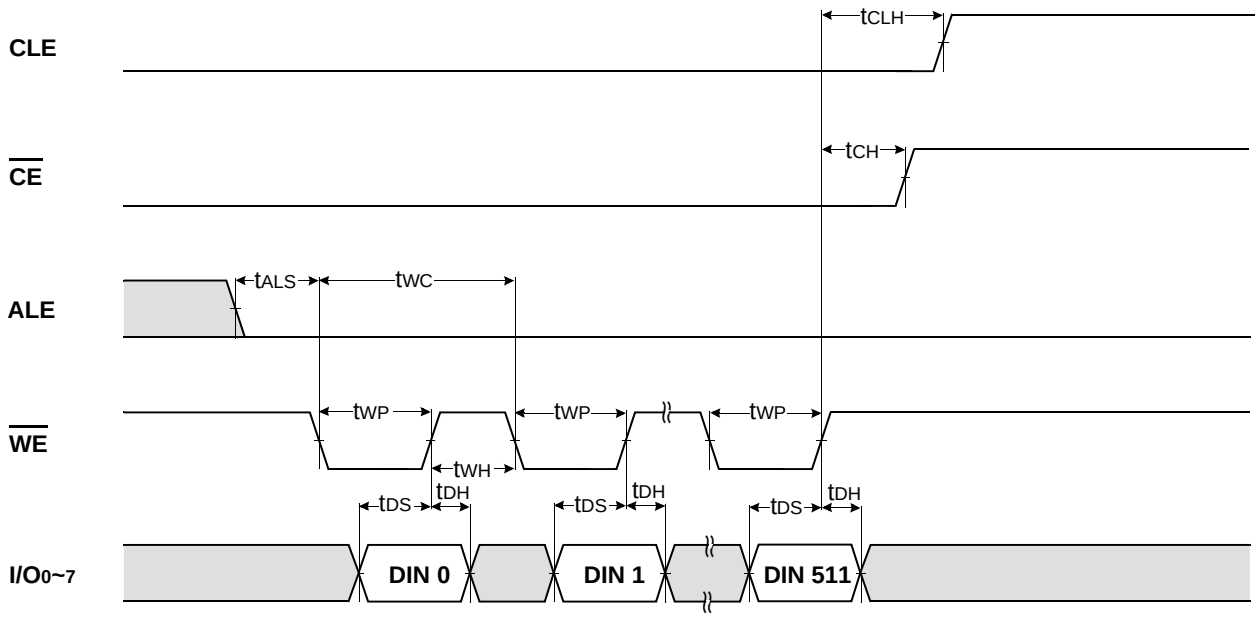
Command Latch Cycle



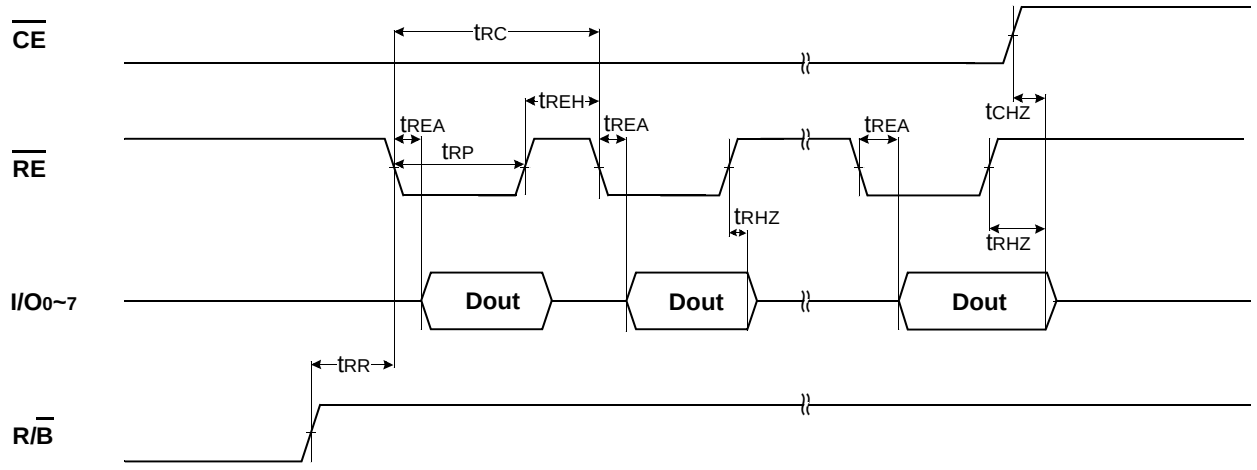
Address Latch Cycle



Input Data Latch Cycle

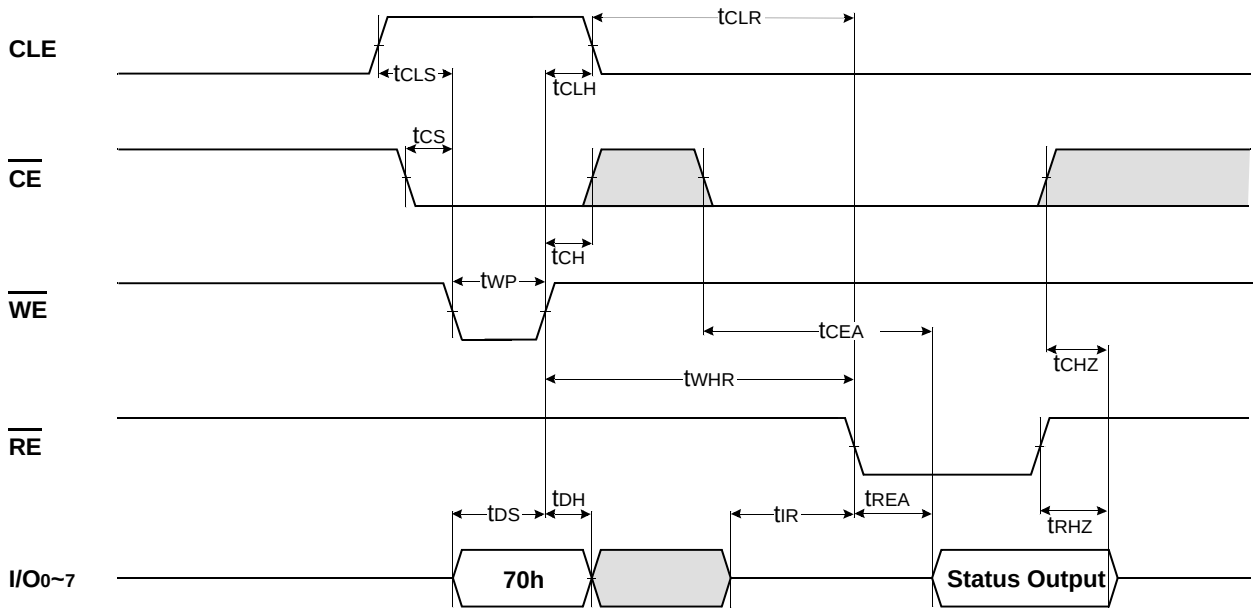


Serial Access Cycle after Read(CLE=L, $\overline{WE}$=H, ALE=L)

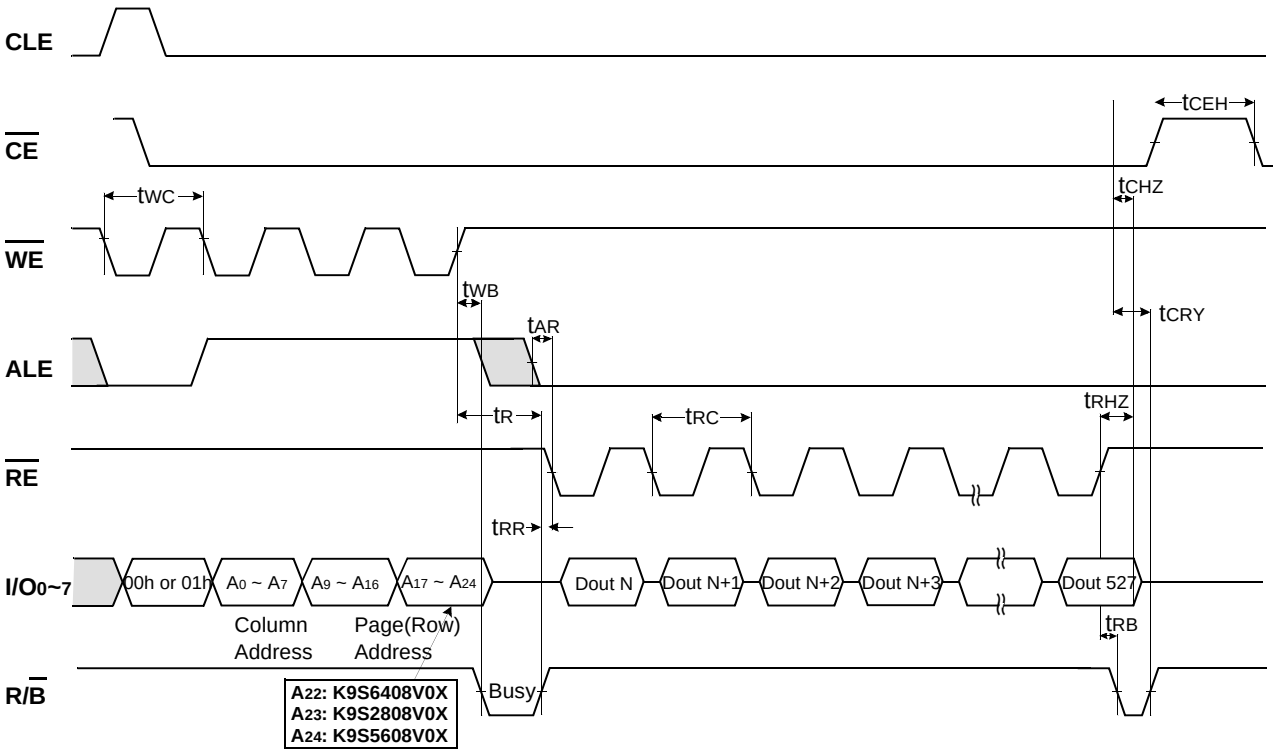


NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

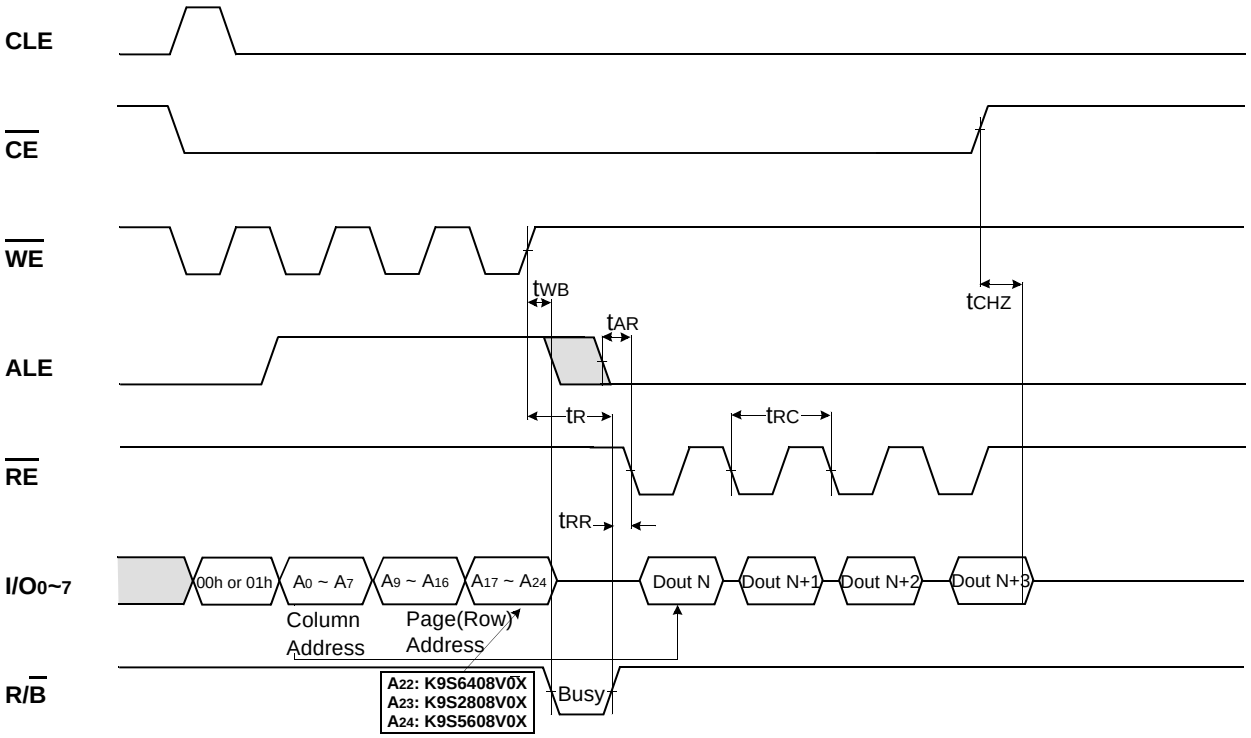
Status Read Cycle



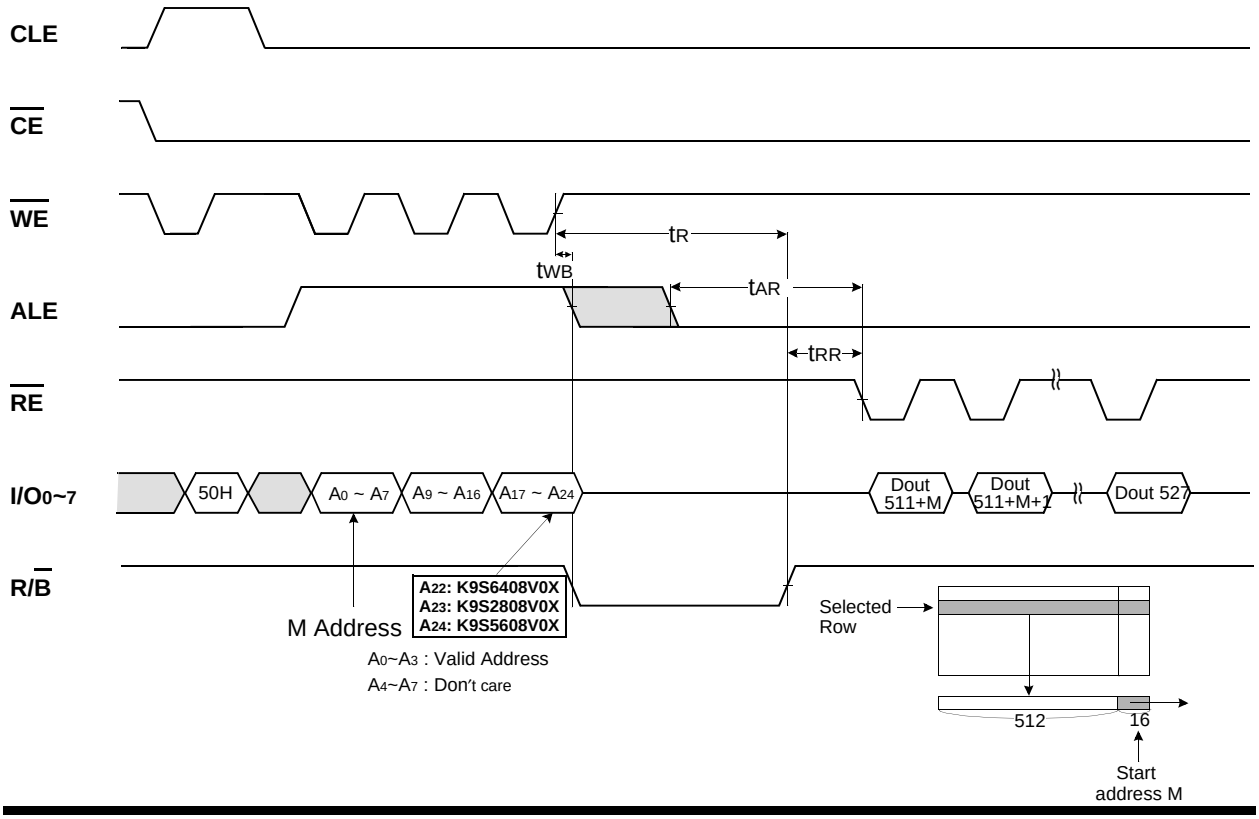
READ1 OPERATION(READ ONE PAGE)



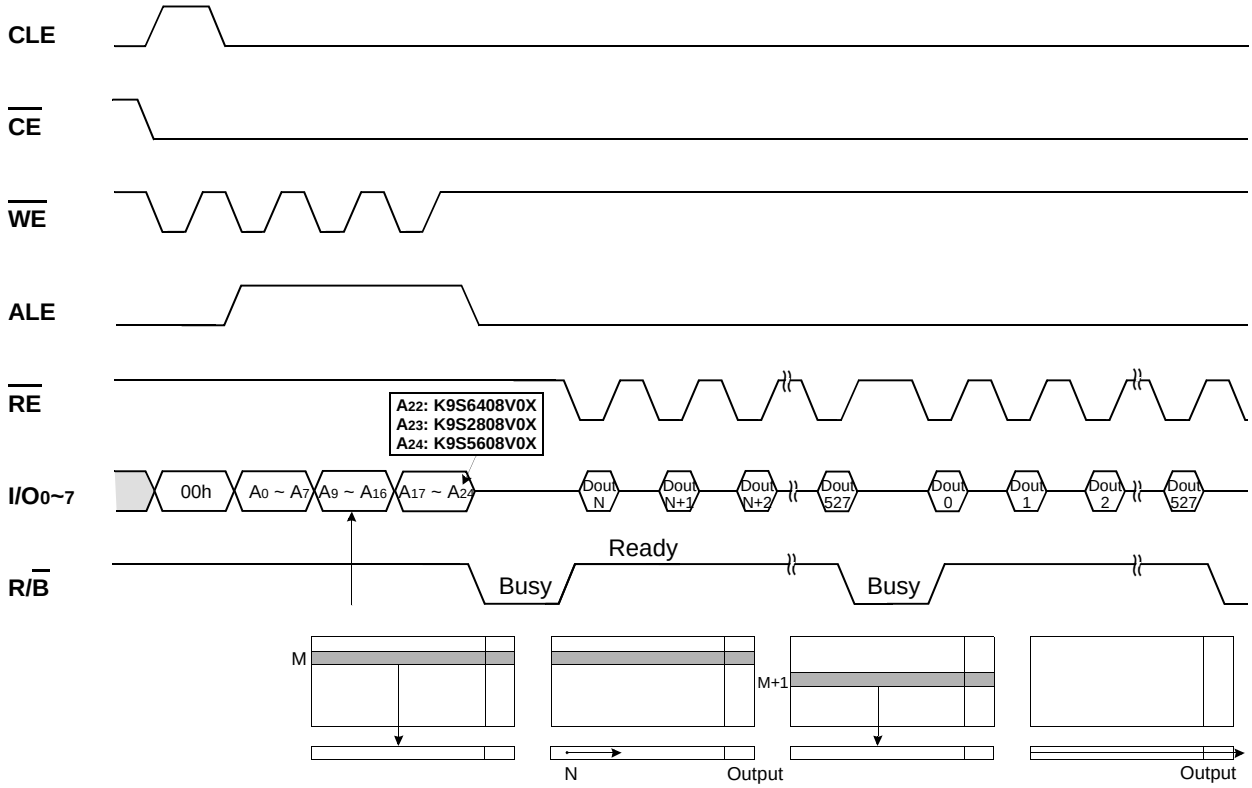
READ1 OPERATION(INTERCEPTED BY $\overline{CE}$)



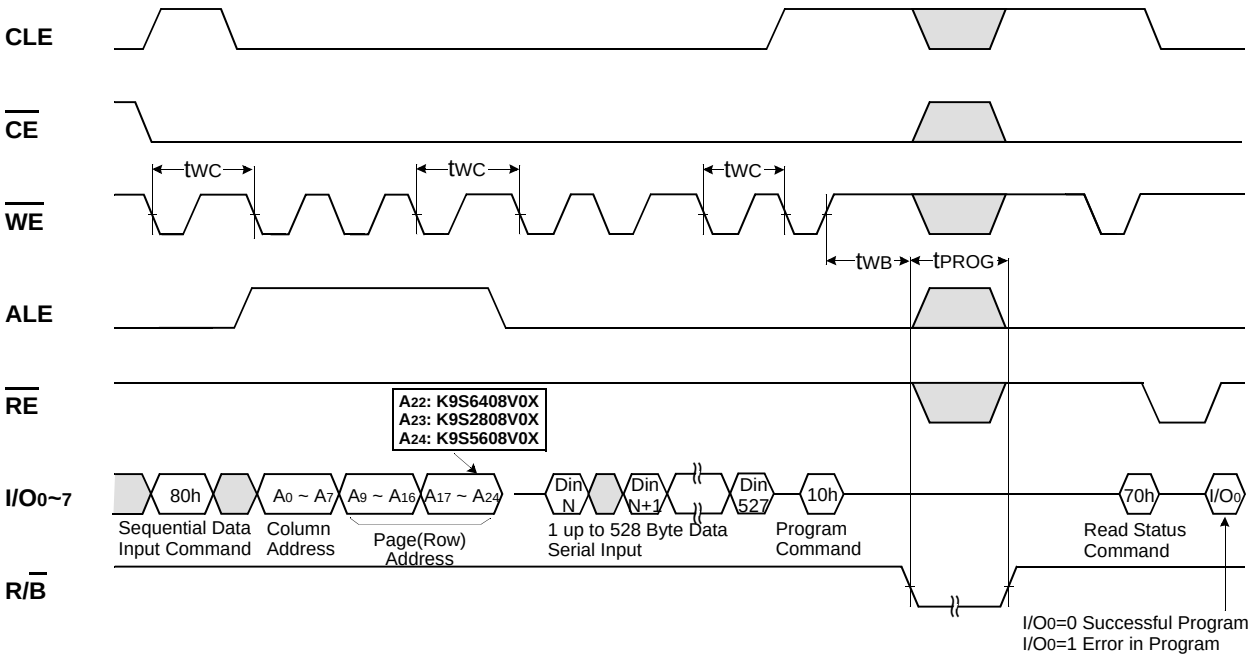
READ2 OPERATION(READ ONE PAGE)



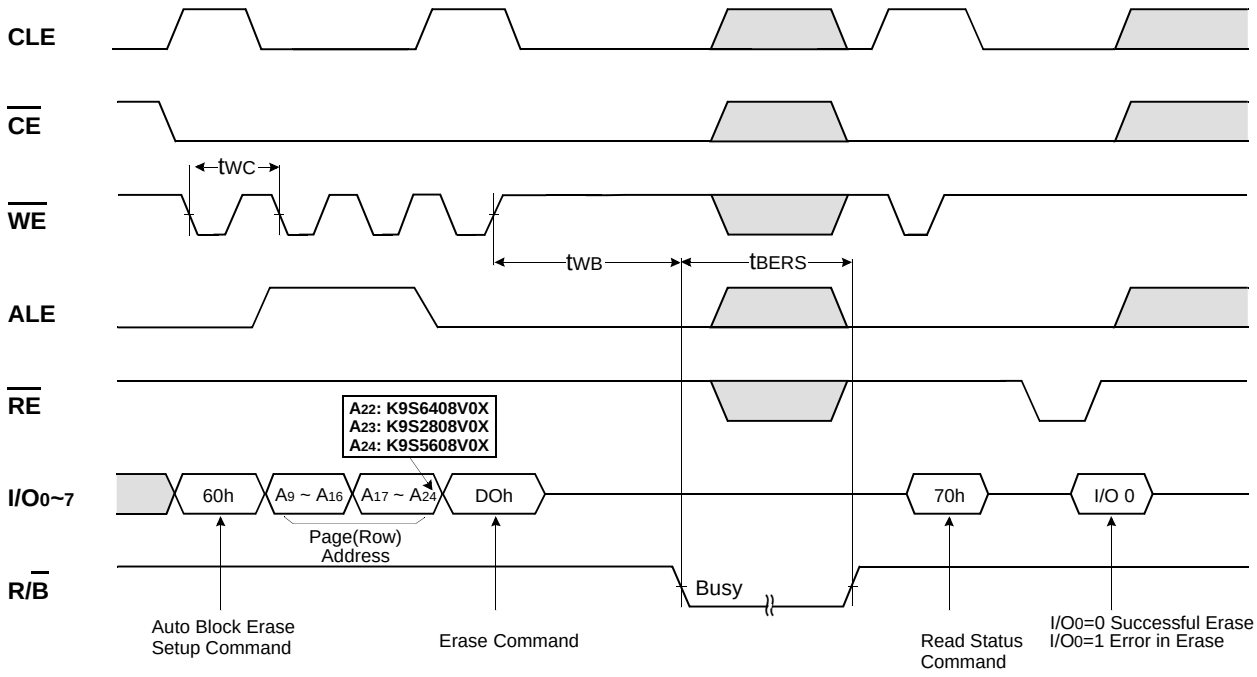
SEQUENTIAL ROW READ OPERATION (Within a block especially for 64Mb-Cdie and 128Mb Bdie)



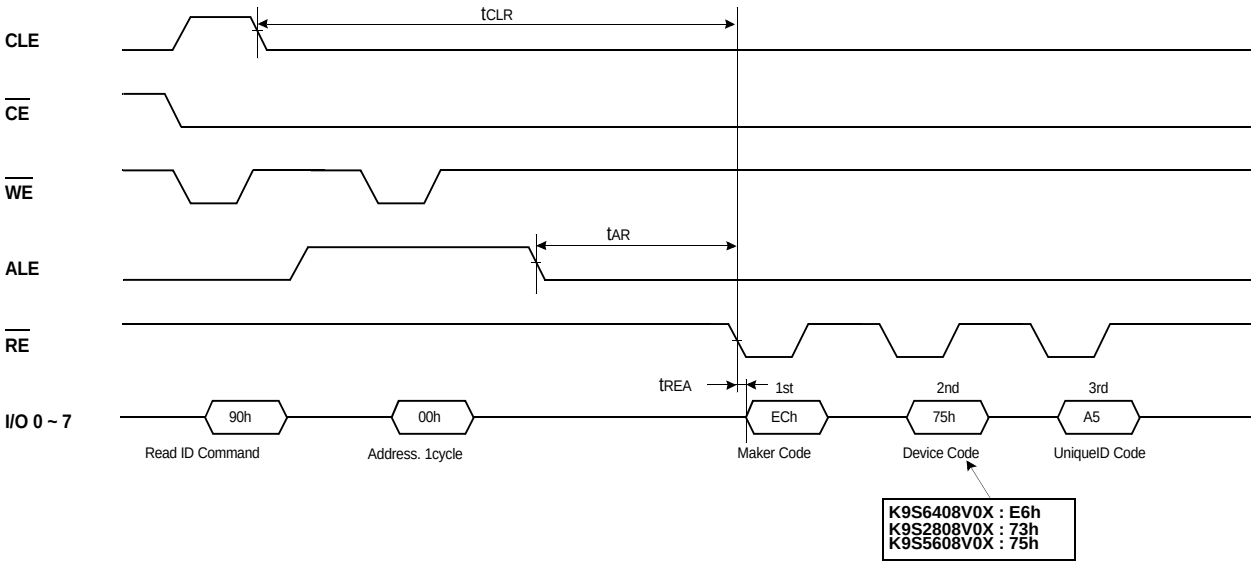
PAGE PROGRAM OPERATION



BLOCK ERASE OPERATION (ERASE ONE BLOCK)



MANUFACTURE & DEVICE ID READ OPERATION



NOTE :
The 3rd byte of device IDs represents whether there is Unigue ID or not. If A5h is read out, that means that the Smart Media has the Unigue ID.

ID Definition Table
90 ID : Access command = 90H

READ ID (1)	Value	Description
1st Byte	ECh	Maker Code
2nd Byte	*75h	Device Code
3rd Byte	A5h	Unique1D code

NOTE :
*Device Code : K9S6408V0X : E6h , K9S2808V0X : 73h , K9S5608V0X: 75h

DEVICE OPERATION

PAGE READ

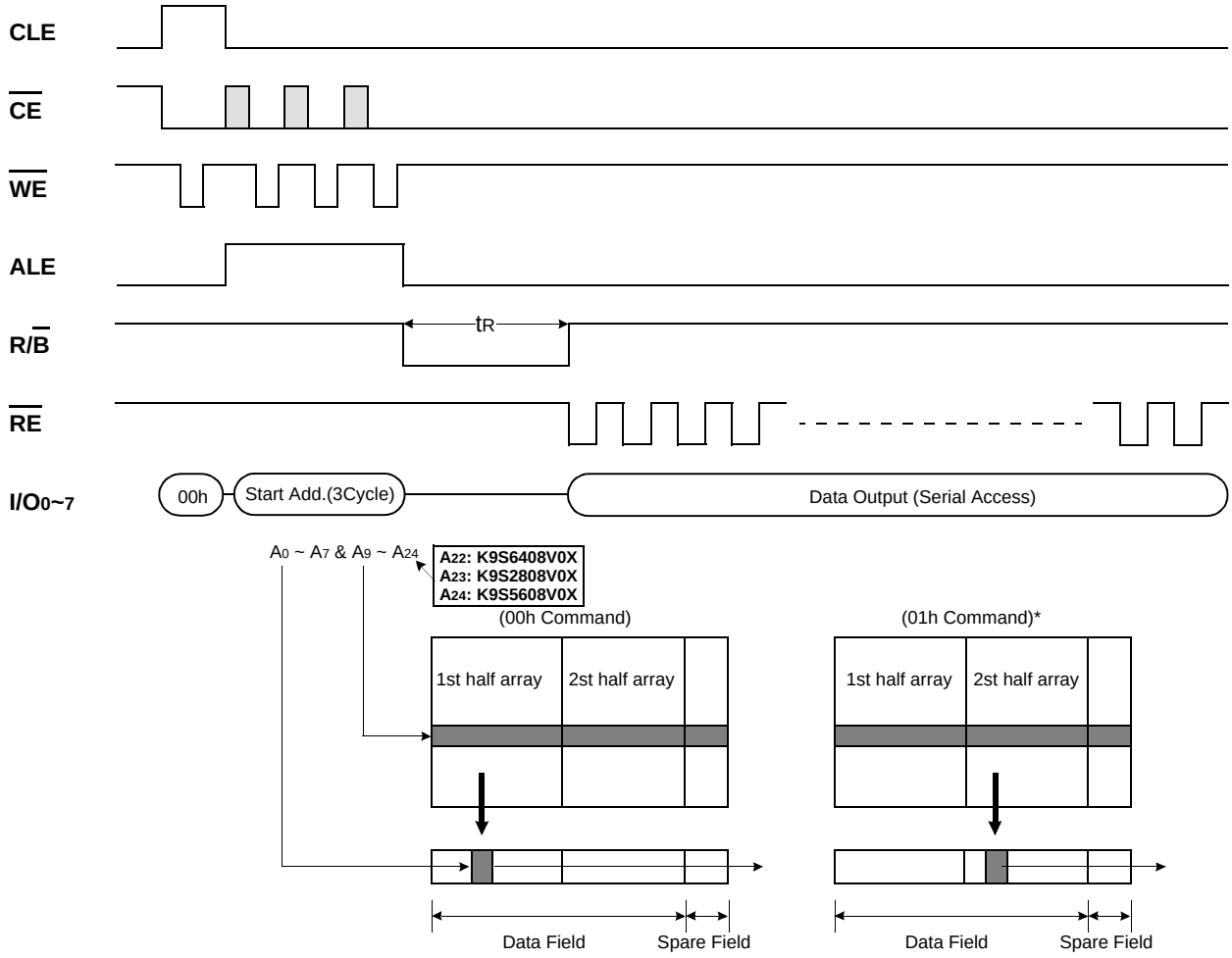
Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available : random read, sequential read and sequential row read.

The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 10µs(t_R). The system controller can detect the completion of this data transfer(tR) by monitoring the output of R/B pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by pulsing RE sequentially. High to low transitions of the RE clock output the data starting from the selected column address up to the last column address.

After the data of the last column address is clocked out, the next page is automatically selected for sequential row read.

Waiting 10µs again allows reading the selected page. The sequential row read operation is terminated by bringing CE high. The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read2 command. Addresses A_0 to A_3 set the starting address of the spare area while addresses A_4 to A_7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command(00h/01h) is needed to move the pointer back to the main area. Figures 7 through 10 show typical sequence and timings for each read operation.

Figure 7. Read1 Operation



* After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array (00h) at next cycle.

Figure 8. Read2 Operation

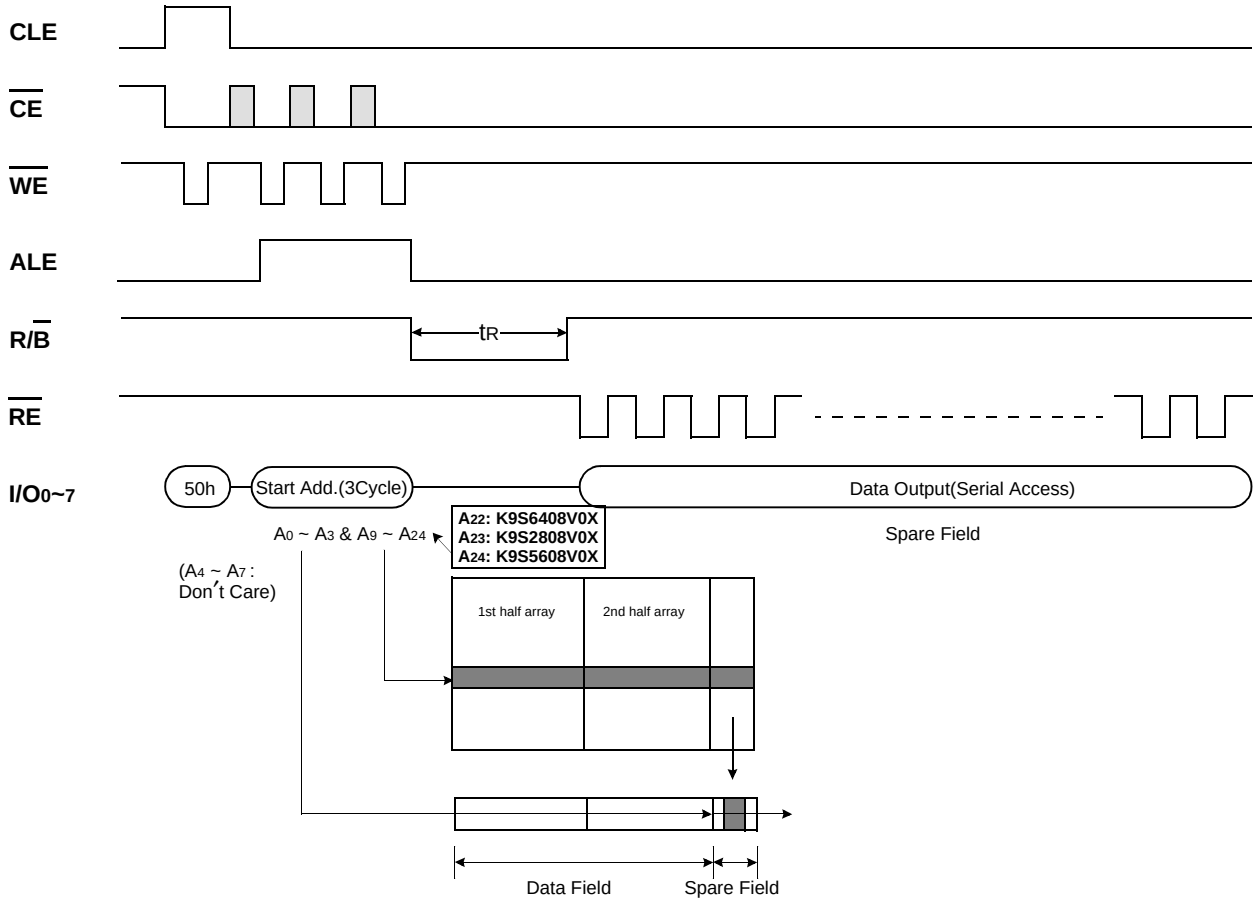
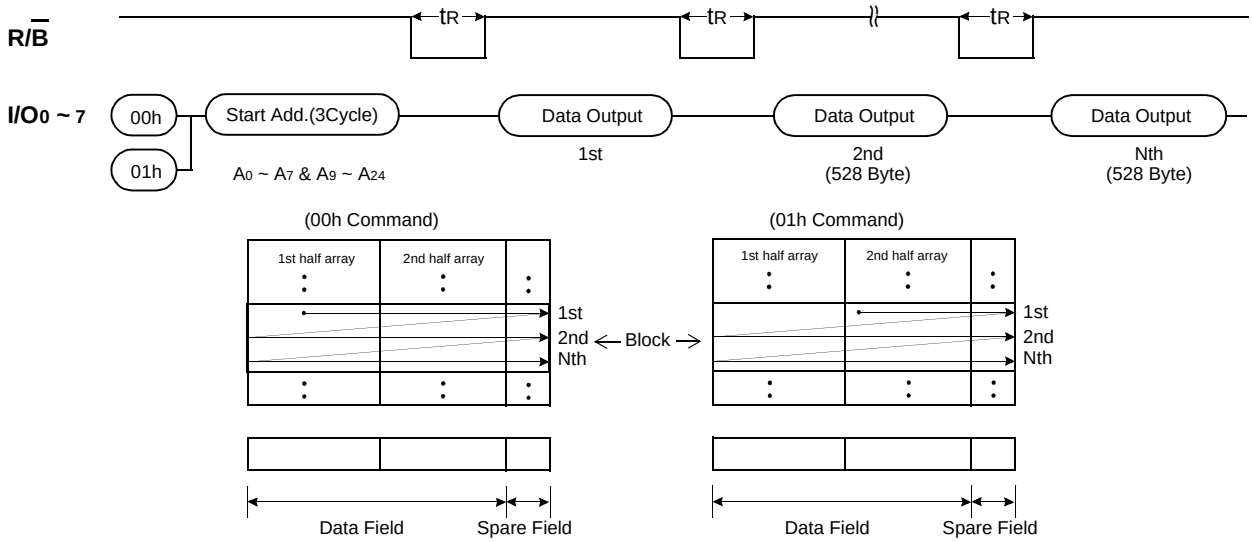
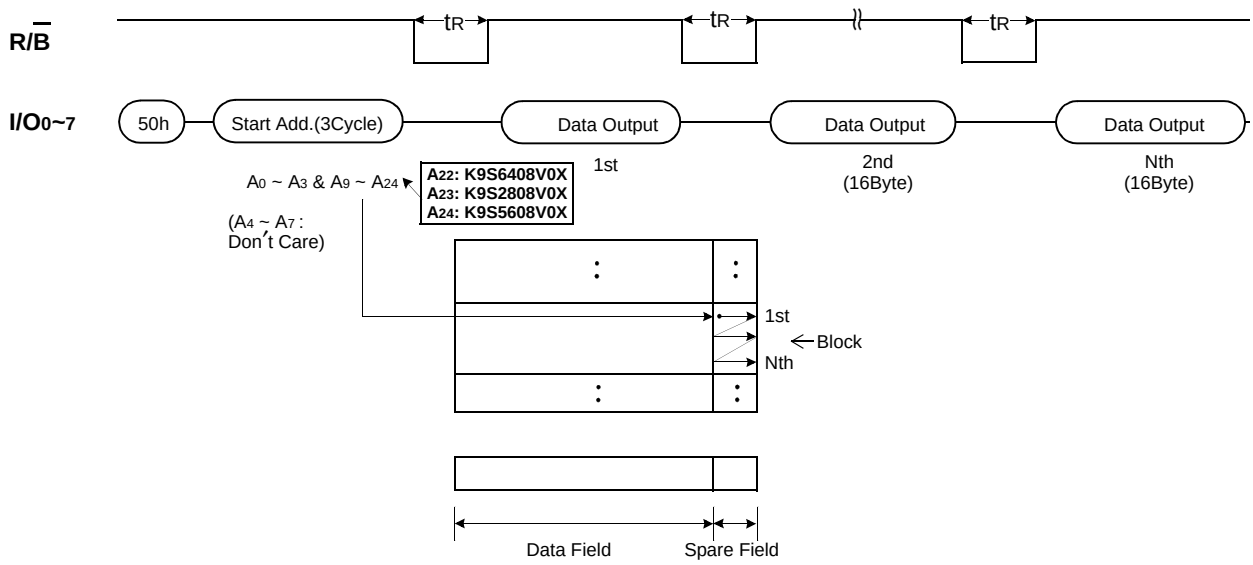


Figure 9. Sequential Row Read1 Operation



The Sequential Read 1 and Read 2 operations are allowed only within a block and after the last page of a block is readout, the sequential read operation must be terminated by bringing $\overline{CE}$ high. When the page address moves onto the next block, read command and address must be given.

Figure 10. Sequential Row Read2 Operation

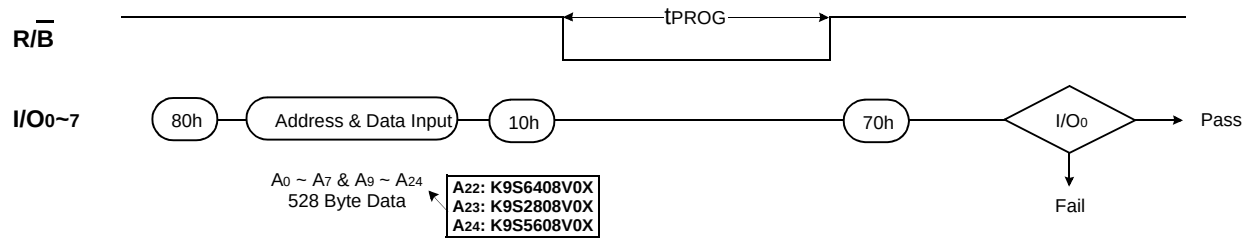


PAGE PROGRAM

The device is programmed basically on a page basis, however it does allow multiple partial page programing of a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation has the limit by its density. (See the Table of Program/Erase Characteristics) It is advisable not to program more often than recommend. It might cause failures due to disturbance when it exceeds its limits. The failure mode could be that data "1" of the erased cell might be changed into data"0"of the programmed cell.

The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from the 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes.The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the three cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded.The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write-controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is completed, the Write Status Bit(I/O 0) may be checked(Figure 11). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 11. Program & Read Status Operation

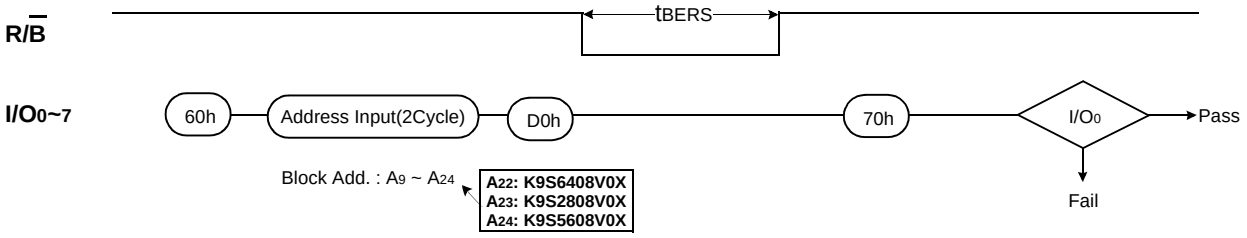


BLOCK ERASE

The Erase operation is done on a block(16K Byte) basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address A_{14} to (A_{22}: K9S6408V0X, A_{23}: K9S2808V0X, A_{24}: K9S5608V0X) is valid while A_9 to A_{13} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 12 details the sequence.

Figure 12. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to Table3 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read mode, a read command(00h or 50h) should be given before the sequential read cycle.

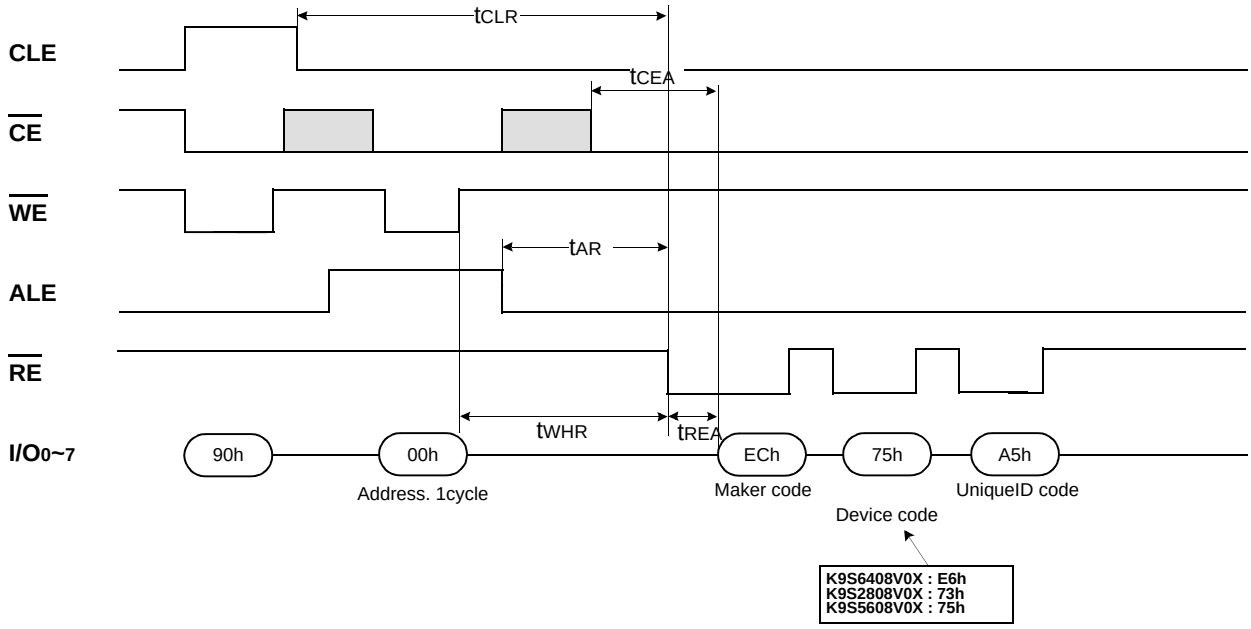
Read Status Register Definition

I/O #	Status	Definition
I/O 0	Program / Erase	"0" : Successful Program / Erase
		"1" : Error in Program / Erase
I/O 1	Reserved for Future Use	"0"
I/O 2		"0"
I/O 3		"0"
I/O 4		"0"
I/O 5		"0"
I/O 6	Device Operation	"0" : Busy "1" : Ready
I/O 7	Write Protect	"0" : Protected "1" : Not Protected

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Three read cycles sequentially output the manufacture code(ECH), the device code (K9S6408V0X : E6h , K9S2808V0X : 73h , K9S5608V0X: 75h), the UniqueID code(A5h) respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 13 shows the operation sequence.

Figure 13. Read ID Operation



RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to Table 4 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/B pin transitions to low for tRST after the Reset command is written. Reset command is not necessary for normal operation. Refer to Figure 14 below.

Figure 14. RESET Operation

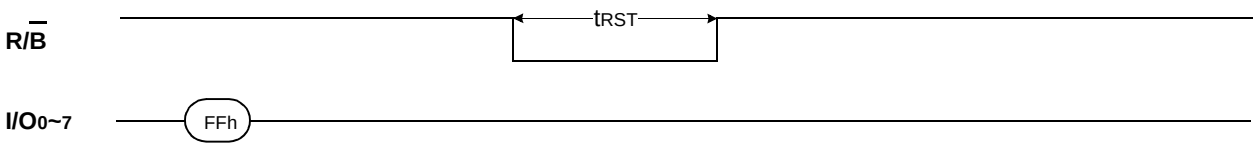


Table 4. Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

READY/BUSY

The device has a R/B output that provides a hardware method of indicating the completion of a page program, erase and random read operations. The R/B pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B outputs to be Or-tied. Because pull-up resistor value is related to tr(R/B) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Figure 15). Its value can be determined by the following guidance.

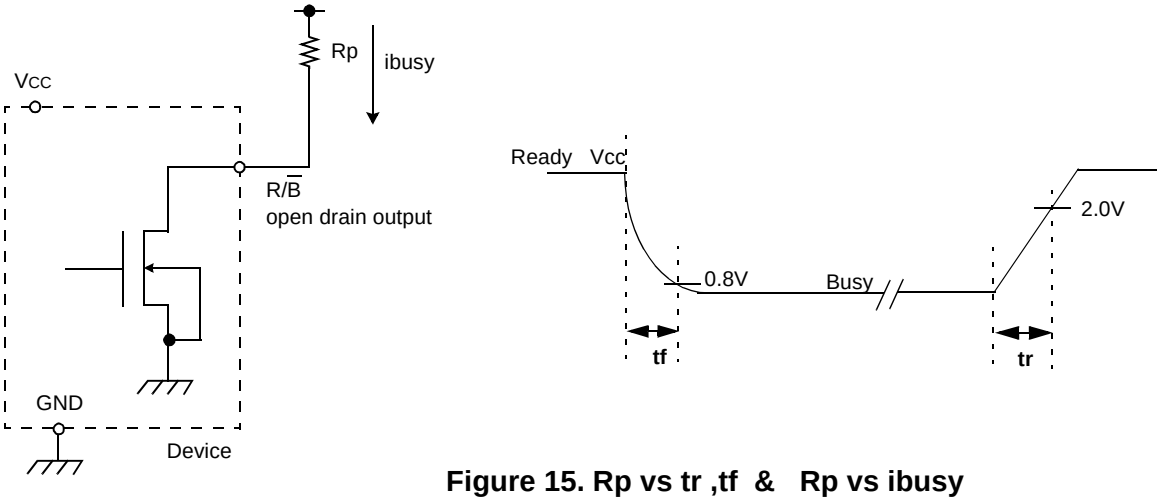
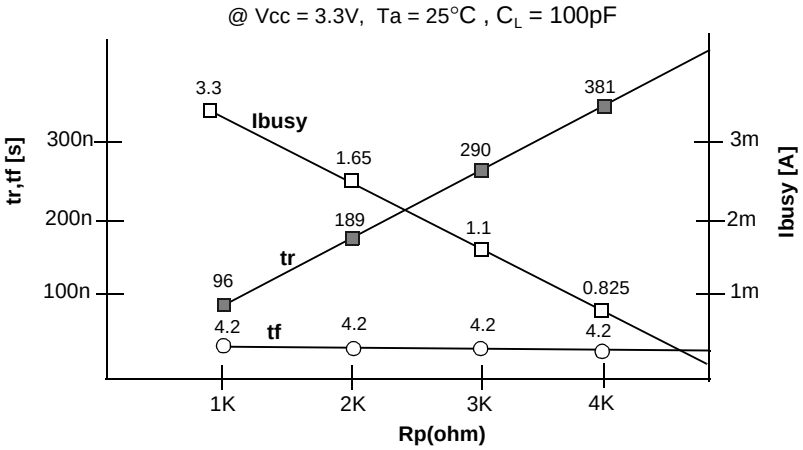


Figure 15. Rp vs tr ,tf & Rp vs ibusy



Rp value guidance

$$Rp(min) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

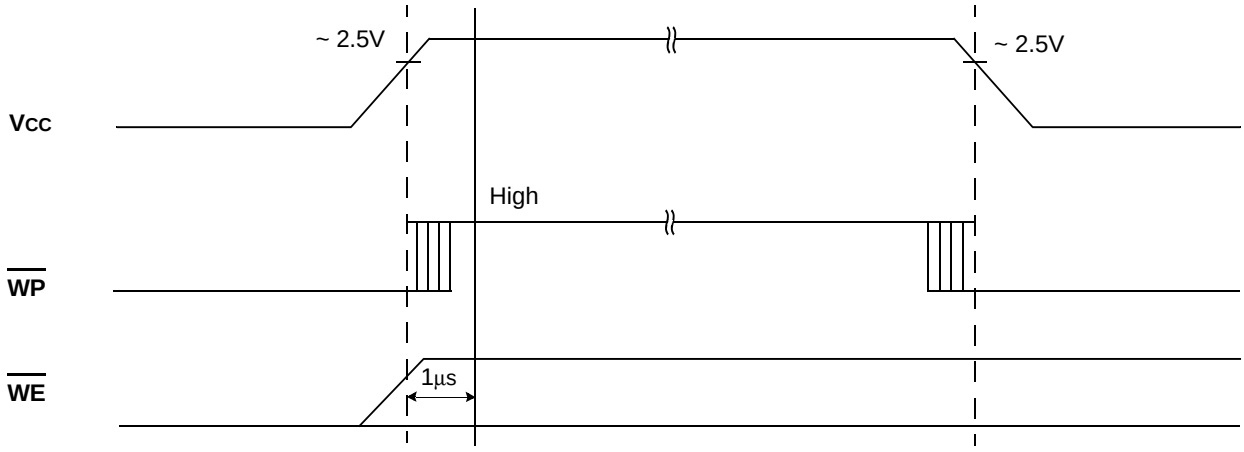
where I_L is the sum of the input currents of all devices tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr

Data Protection & Power up Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down as shown in Figure 16. The two step command sequence for program/erase provides additional software protection.

Figure 16. AC Waveforms for Power Transition



DIMENSIONS

Unit:mm

22 PAD SOLID STATE FLOPPY DISK CARD (3.3V)

SOLID STATE PRODUCT OUTLINE