OneNAND™MCP SPECIFICATION

NAND Density	Part No.	Vcc_core	Vcc_IO	PKG
256Mb NAND	T.B.D	1.8V(1.7V~1.95V)	1.8V(1.7V~1.95V)	T.B.D
	KEF00F0000CM-EG00	2.6V(2.4V~2.8V)	2.6V(2.4V~2.8V)	63FBGA(LF)
	KEF00F0000CM-SG00			63FBGA
512Mb NAND	KEC00C00CM-EGG0	1.8V(1.7V~1.95V)	1.8V(1.7V~1.95V)	63FBGA(LF)
	KEC00C00CM-SGG0			63FBGA
	T.B.D	2.6V(2.4V~2.8V)	2.6V(2.4V~2.8V)	T.B.D

Version: Ver. 0.0
Date: April 4, 2003

1. FEATURES

♦ Architecture

- Design Technology: 0.25µm
- Voltage Supply
  - Main: 1.8V device(1.7V~1.95V)
    2.6V device(2.4V~2.8V)
  - Host Interface & NAND Flash Interface: 1.8V device(1.7V~1.95V)
    2.6V device(2.4V~2.8V)
- Organization
  - Host Interface:16bit
- Internal BufferRAM
  - BootRAM at booting, Cache-like at normal operation

♦ Performance

- Host Interface type
  - Synchronous Random Read
    : Clock Frequency: up to 45MHz @30pF
  - Synchronous Burst Read
    : Clock Frequency: up to 45MHz @30pF
    : Burst Length: 4 words/ 8 words/ 16 words/ 32 words/ Continuous Linear Burst(2K words)
  - Asynchronous Random Read
  - Asynchronous Page Read: 4words
  - Asynchronous Random Write
- Programmable Read latency
- 2Bit EDC / 1Bit ECC
- Multiple Reset
  - Cold Reset / Warm Reset / Hot Reset
- Internal Bootloader
- Itelligent Data Protection
- Unique ID
  - Detail information can be obtained by contact with Samsung

♦ Software

- Handshaking Feature
- Interface Chip ID Read
  - Detailed chip information by additional controller ID register

♦ Packaging

- Package
  - 63ball, 9.5mm x 12mm x max 1.4mmt FBGA

2. GENERAL DESCRIPTION

OneNAND™ (MCP of NAND Flash Interface chip and NAND Flash) allows standard NAND Flash chips to interface with OneNAND™ bus without performance penalty. This device is 1.8V/2.6V operation and comprised of about 10,000 gates and 4KB internal BufferRAM.

This 4KB BufferRAM is used as bootRAM during cold reset, and is used as cache RAM after cold reset. The operating clock frequency is up to 45MHz. This device is X16 interface with Host and X8 interface with NAND Flash. (Notice, in this specification, address is expressed by the byte order)

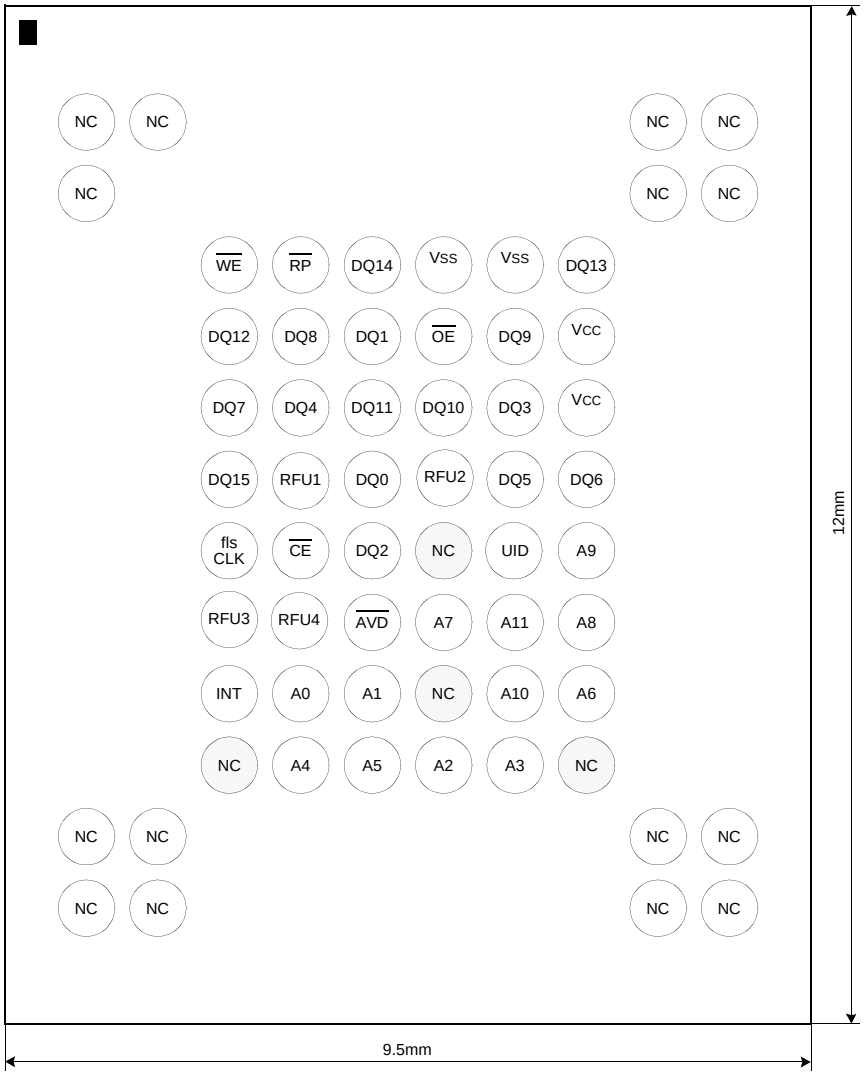
Also this device has the speed of ~40ns random access time. Actually, it is accessible with minimum 3clock latency(host-driven clock for synchronous read), but this device adopts the appropriate wait cycles by programmable read latency. OneNAND™ provides the multiple page read operation by assigming the number of pages to be read in the page counter register. The device is offered in the single type of package; 63ball, 9.5mm x 12mm x max 1.4mmt FBGA. The device includes one block sized OTP(One Time Programmable), which can be used to increase system security or to provide identification capabilities.

3. PIN DESCRIPTION

Pin Name	Type	Nameand Description
Host Interface		
A11~A0	I	**Address Inputs** - Inputs for addresses during read operation, which are for addressing BufferRAM & Register.
INT	O	**Interrupt** Notifyin Host when a command has completed. CMOS type driver output.
DQ15~DQ0	I/O	**Data Inputs/Outputs** - Inputs data during program and commands during all operations, outputs data during memory array/ register read cycles. Data pins float to high-impedance when the chip is deselected or outputs aredisabled.
CLK	I	**Clock** CLK synchronizes the device to the system bus frequency in synchronous read mode. The first rising edge of CLK in conjunction with AVD low latches address input.
$\overline{WE}$	I	**Write Enable** $\overline{WE}$ controls writes to the bufferRAM and registers. Datas are latched on the $\overline{WE}$ pulse's rising edge
$\overline{AVD}$	I	**Address Valid Detect** Indicates valid address presence on address inputs. During asynchronous read operation, all addresses are transparent during $\overline{AVD}$'s low, and during synchronous read operation, all addresses are latched on CLK's rising edge while $\overline{AVD}$ is held low for one clock cycle. >Low: for asynchronous mode, indicates valid address: for vurst mode, causes starting address to ve latched on rising edge on CLK >High: device ignores address inputs
$\overline{RP}$	I	**Reset Pin** When low, $\overline{RP}$ resets internal operation of OneNAND™. $\overline{RP}$ status is don't care during power-up and bootloading.
$\overline{CE}$	I	**Chip Enable** $\overline{CE}$-low activates internal controll logic, and $\overline{CE}$-high deselects the device, places it in standby state, and places A/DQ in Hi-Z
$\overline{OE}$	I	**Output Enable** $\overline{OE}$-low enables the device's output data buffers during a read cycle.
UID		**UID** The device is set to access Unique ID from NAND when this is high. This should be low in normal operation.
Power Supply		
V_{CC}		**Power**
V_{SS}-Core		**Ground**
etc		
RFU		**Reserved for future use** RFU1 reserved for A12. RFU2 is reserved for A15. RFU3 is reserved for A14. RFU4 is reserved for A13.
DNU		**Do Not Use** Leave it disconnected. These pins are used for testing.
NC		**No Connection** Lead is not internally connected.

NOTE:
Do not leave power supply(V_{CC}, V_{SS}) disconnected.

4. PIN CONFIGURATION

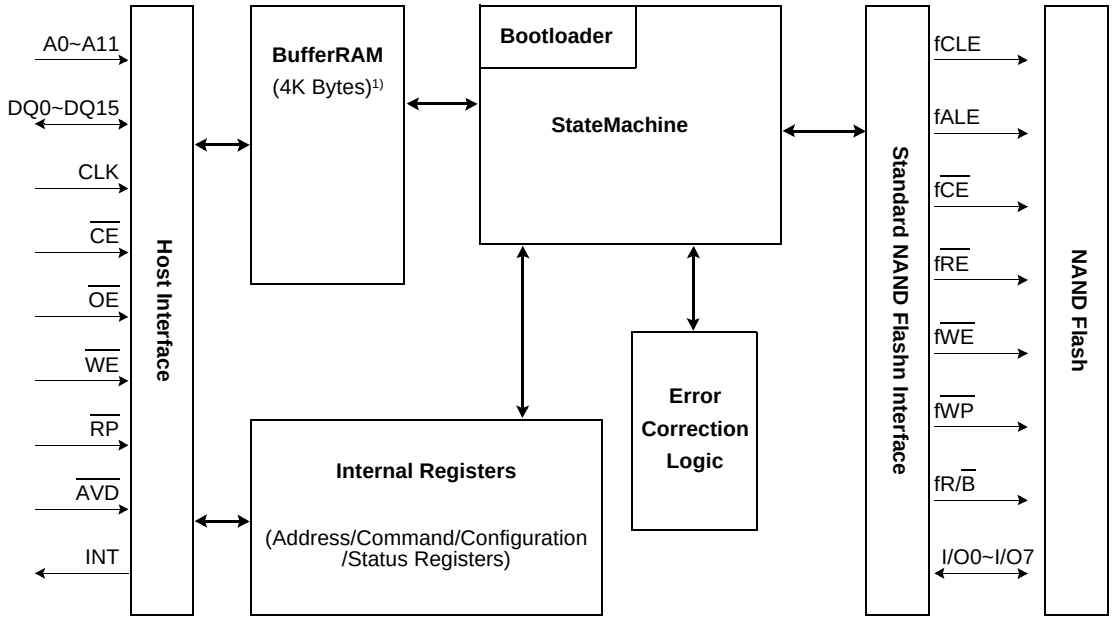


(TOP VIEW, Balls Facing Down)

63ball FBGA OneNAND™ Chip

9.5mm x 12mm x max. 1.4mmt, Ball Pitch: 0.8mm

5. BLOCK DIAGRAM For OneNAND™MCP



- Host interface
- 4KB BufferRAM
- Command and status registers
- State Machine (Bootloader is included)
- Error Correction Logic
- Standard NAND flash Interface
- NAND Flash

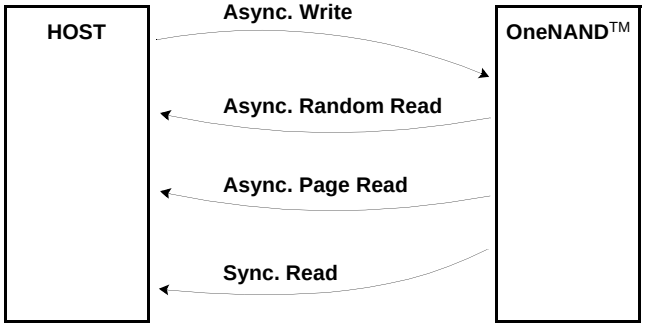
NOTE:
1) At cold reset, bootloader copies boot code(4K byte size) from NAND Flash BufferRAM.
and except cold reset host can use BufferRAM like cacheRAM.

6. ACCESS TIMINGS for OneNAND™ MCP

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0~15	DQ0~15	$\overline{RP}$	CLK	$\overline{AVD}$
Standby	H	X	X	X	High-Z	H	X	X
Warm Reset	X	X	X	X	High-Z	L	X	X
Asynchronous Write	L	H	L	Add. In	Data In	H	X	
Asynchronous Read	L	L	H	Add. In	Data Out	H	L	 or
Load Initial Burst Address	L	H	H	Add. In	X	H		
Burst Read	L	L	H	X	Burst Dout	H		 or
Terminate Burst Read Cycle	H	X	H	X	High-Z	H	X	X
Terminate Burst Read Cycle	X	X	X	X	High-Z	L	X	X
Terminate Current Burst Read Cycle and Srart New Burst Read Cycle		H	H	Add In	High-Z	H		

X=Don't Care

< BUS OPERATION >



< ACCESS TYPES >

Figure 1. Asynchronous Read Mode

* Please notice, t_{AES} is Address delay from $\overline{CE}$ & $\overline{AVD}$'s low, and t_{AES} should not be over 10ns.

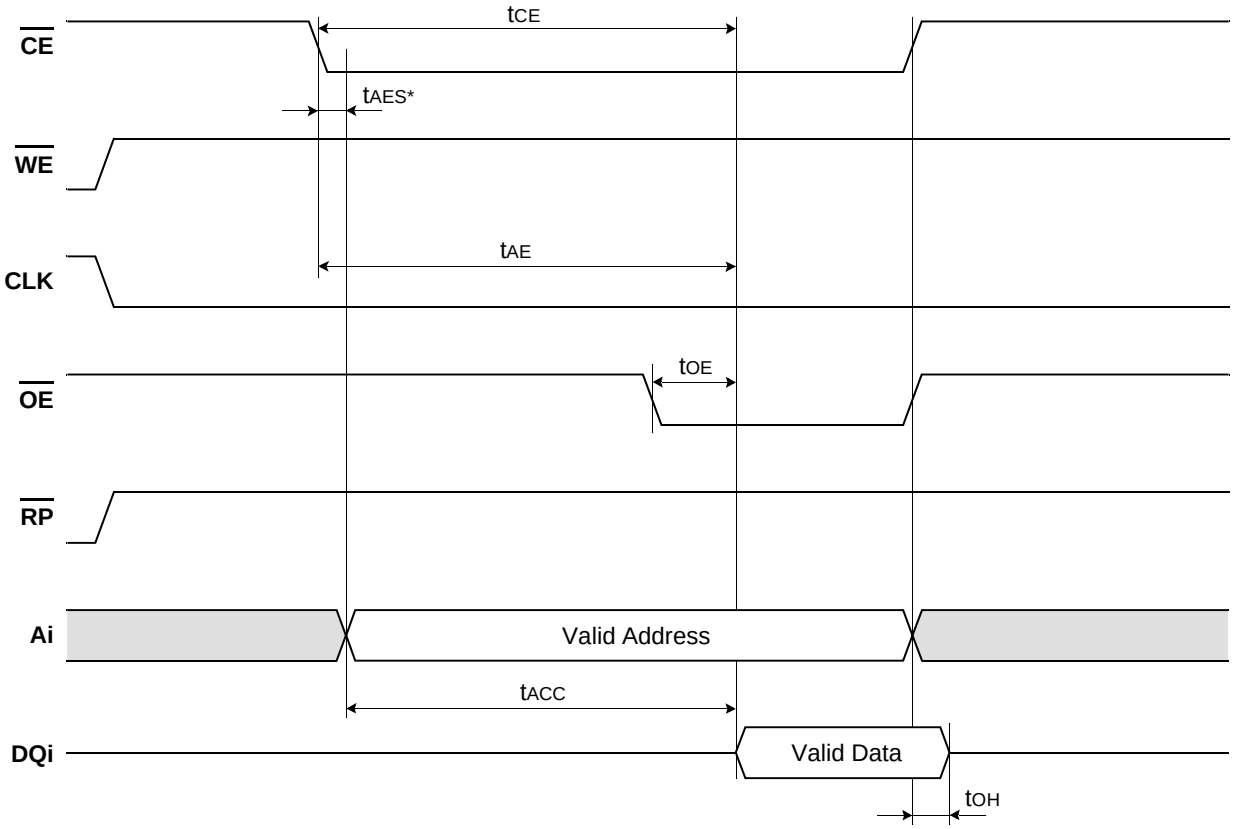


Figure 2. Latched Asynchronous Read Mode

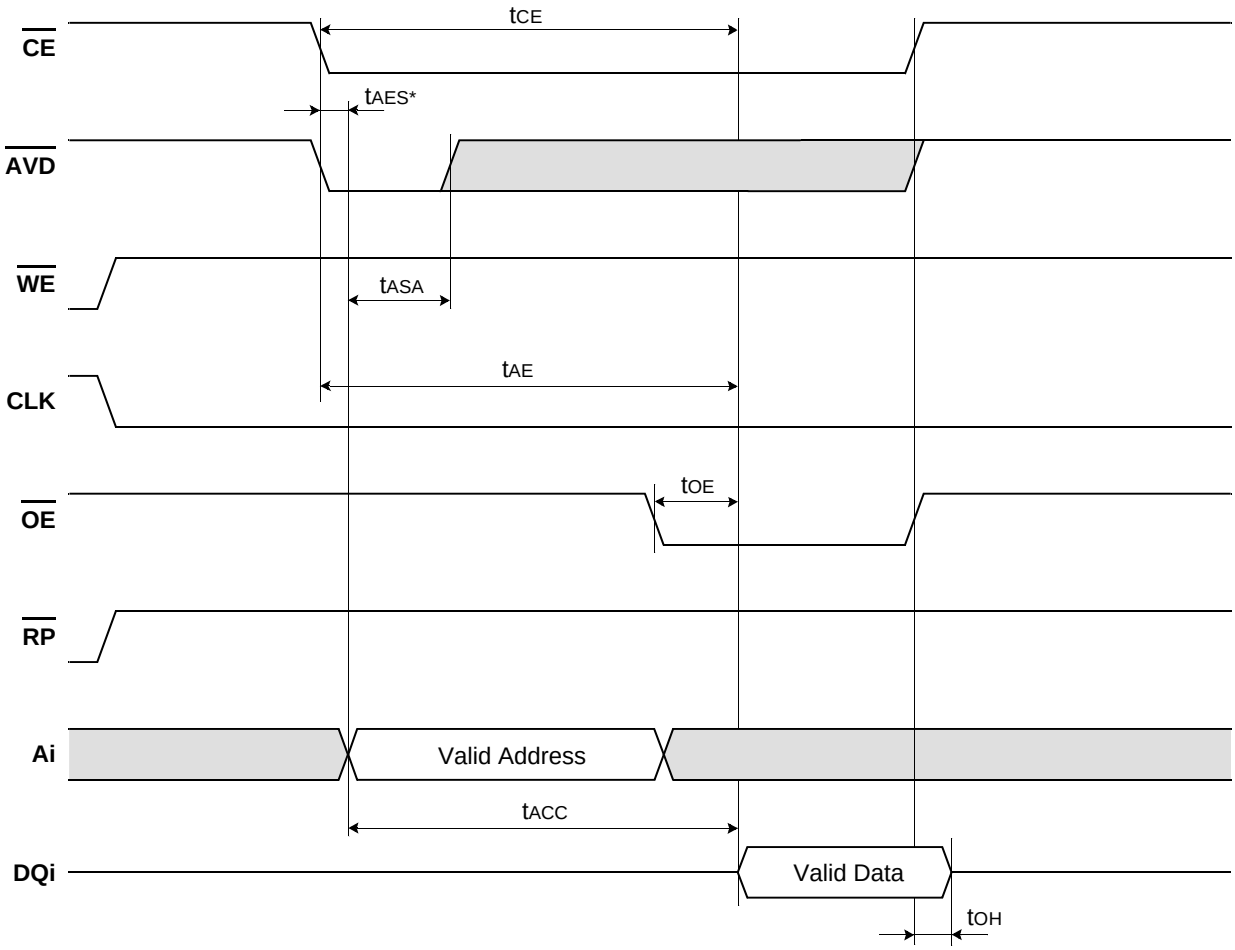


Figure 3. Asynchronous Page Read Mode

* Please notice, t_{AES} is Address delay from $\overline{CE}$ & $\overline{AVD}$'s low, and t_{AES} should not be over 10ns.

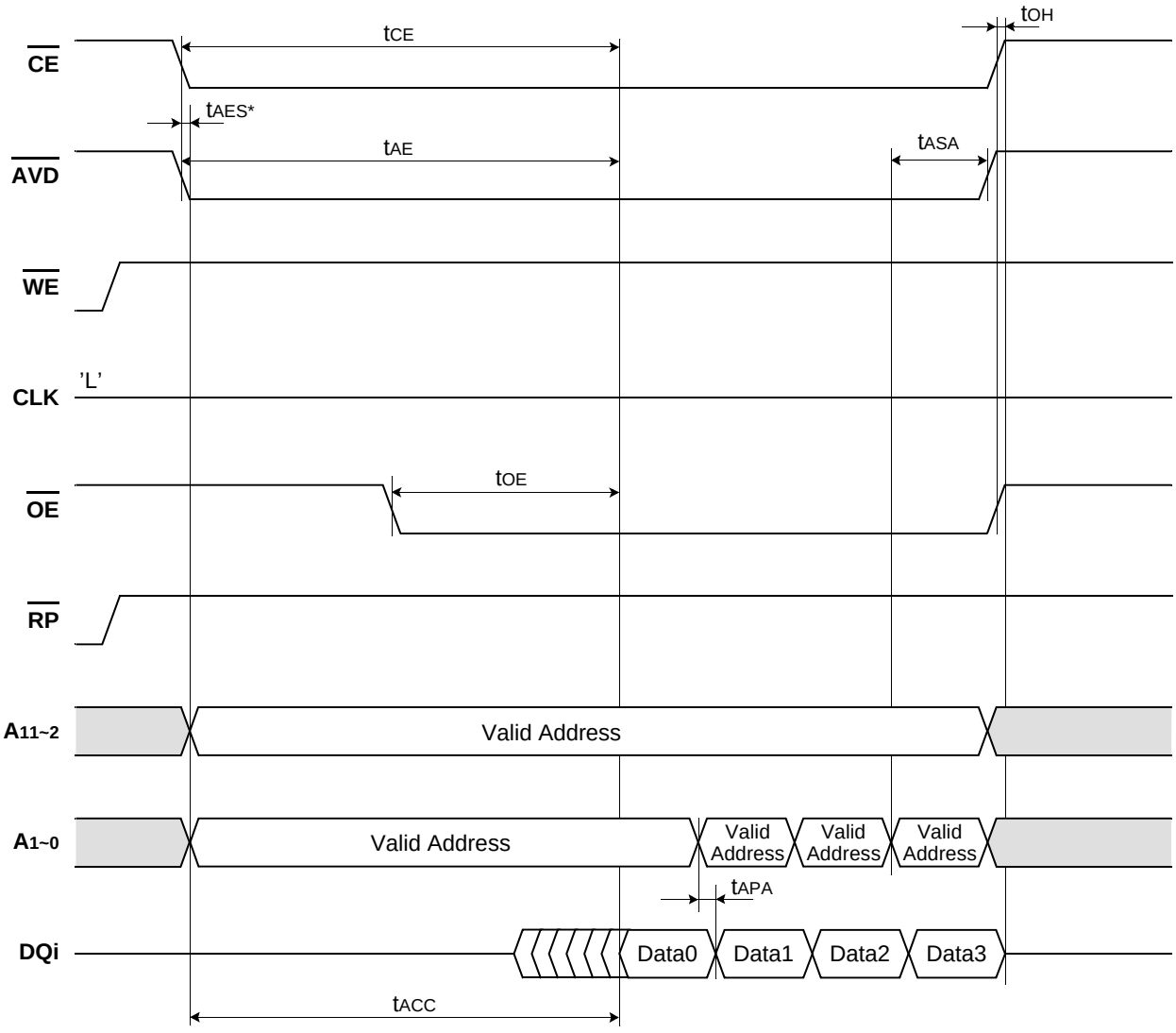


Figure 4. Synchronous Burst Read Mode

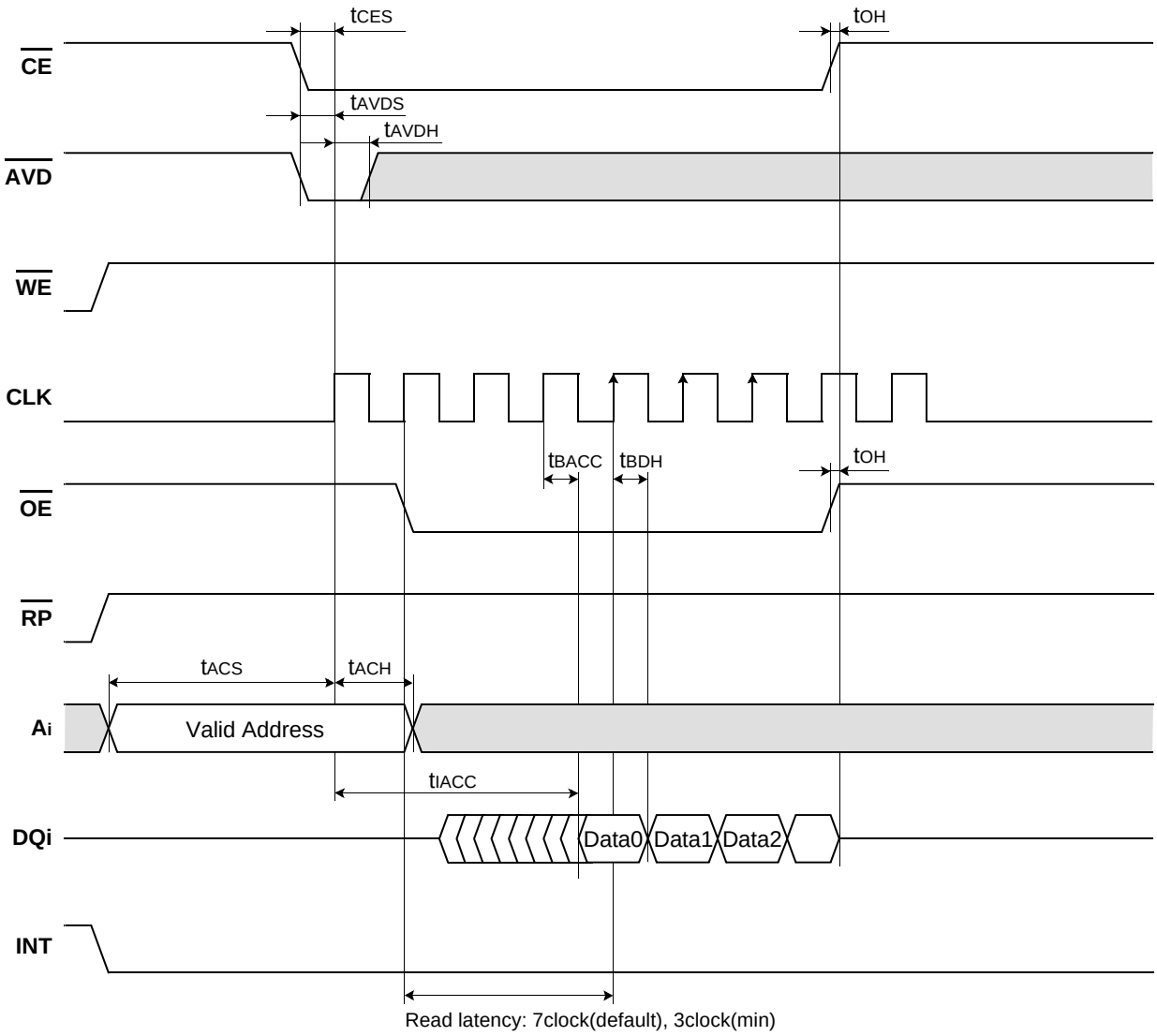


Figure 5. Asynchronous Write Mode(No $\overline{AVD}$ pin case)

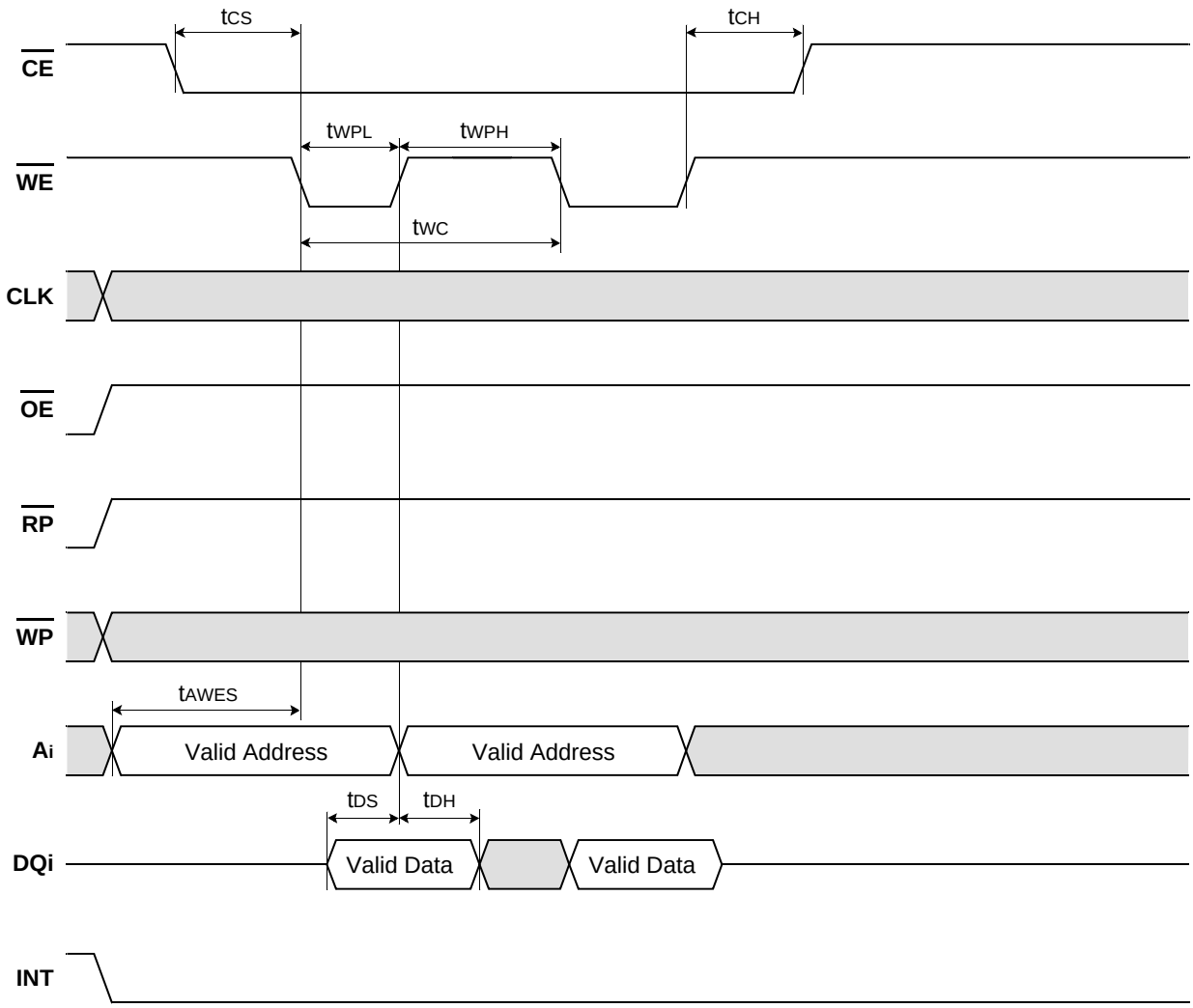
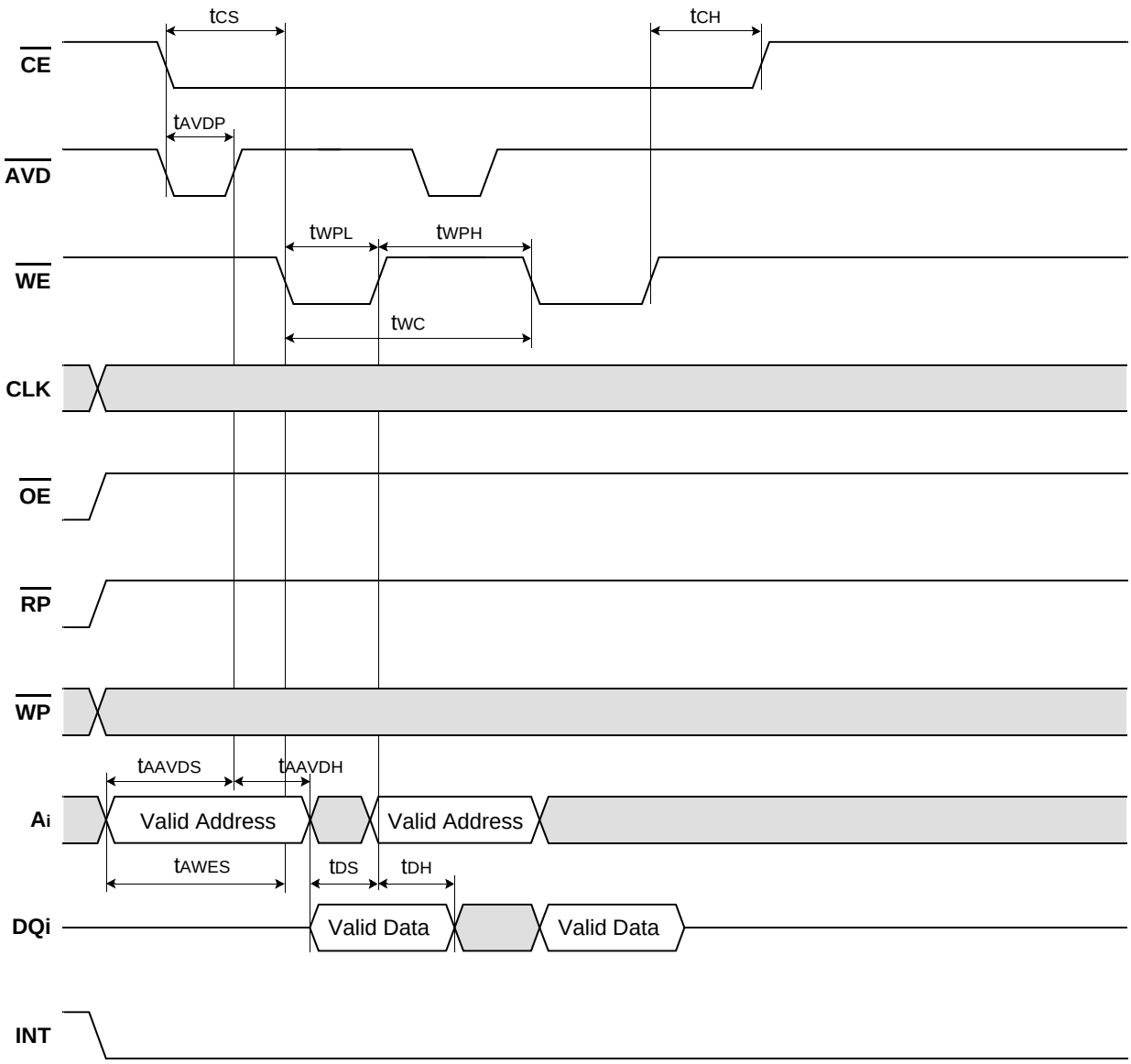


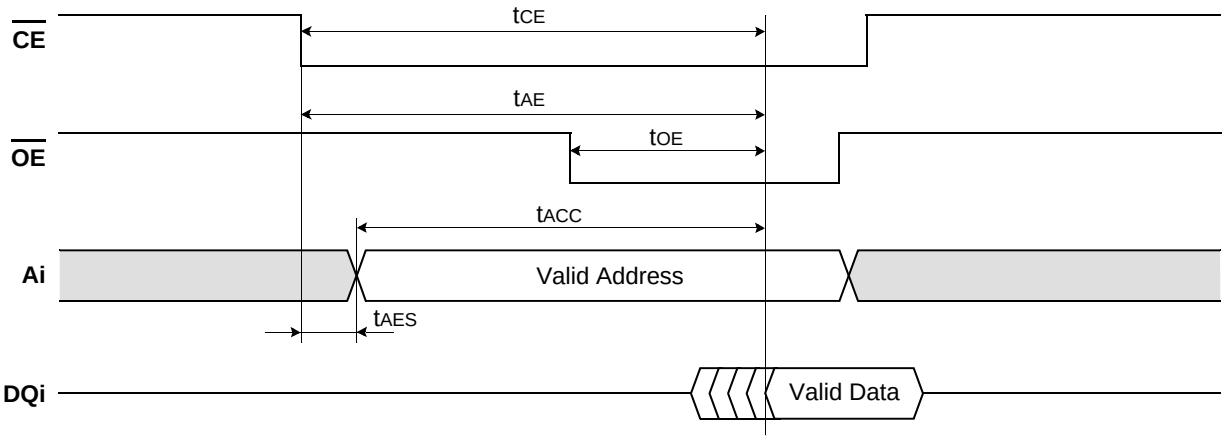
Figure 6. Latched Asynchronous Write Mode



Timing Diagram for OneNAND™

The read cycle is initiated by first applying address to the address bus. The address latch is transparent while $\overline{CE}$ is low. The random access time is measured from a stable address, falling edge of $\overline{CE}$. The clock should remain "0" during asynchronous access. Address access time(tACC) is equal to the delay from stable addresses to valid output data. The chip enable access time(tCE) is the delay from the stable addresses and stable $\overline{CE}$ to valid data at the outputs. The output enable access time(tOE) is the delay from the falling edge of $\overline{OE}$ to valid data at the output. $\overline{CE}$ must toggle in asynchromous read operation.

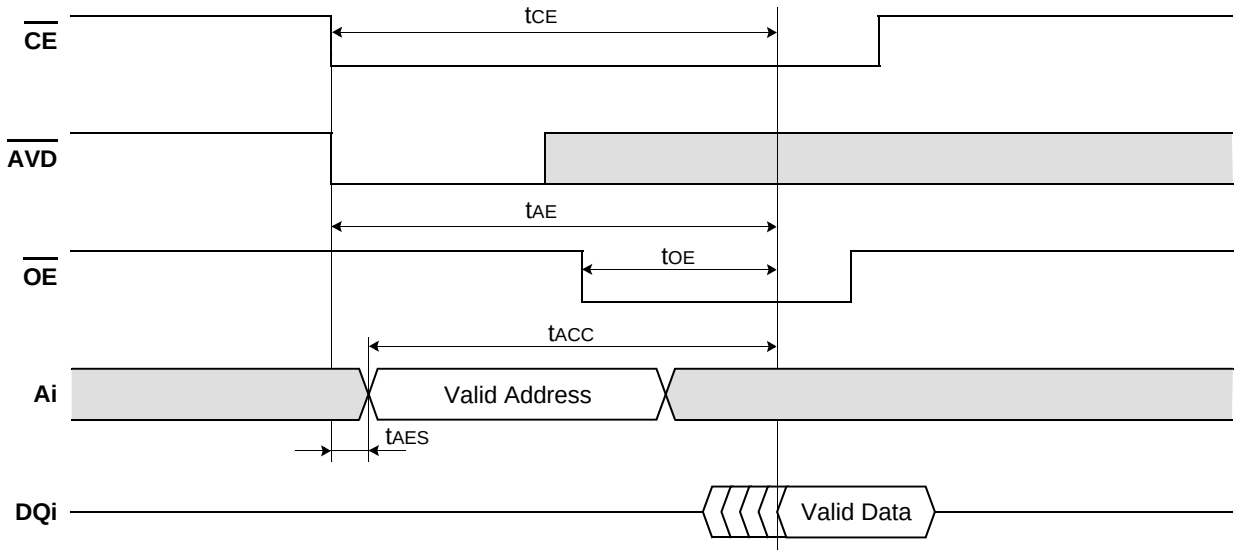
Figure 7. Asynchronous Read Mode



Lathced Asynchronous Read Operation

The read cycle is initiated by first applying address to the address bus. The address latch is transparent while $\overline{AVD}$ is low. The random access time is measured from a stable address, falling edge of $\overline{AVD}$ or falling edge of $\overline{CE}$ which ever occurs last. The clock should remain "0" during asynchronous access. Address access time(tACC) is equal to the delay from stable addresses to valid output data. The chip enable access time(tCE) is the delay from the stable addresses and stable $\overline{CE}$ to valid data at the outputs. The output enable access time(tOE) is the delay from the falling edge of $\overline{OE}$ to valid data at the output. $\overline{CE}$ and $\overline{AVD}$ must toggle in asynchromous read operation.

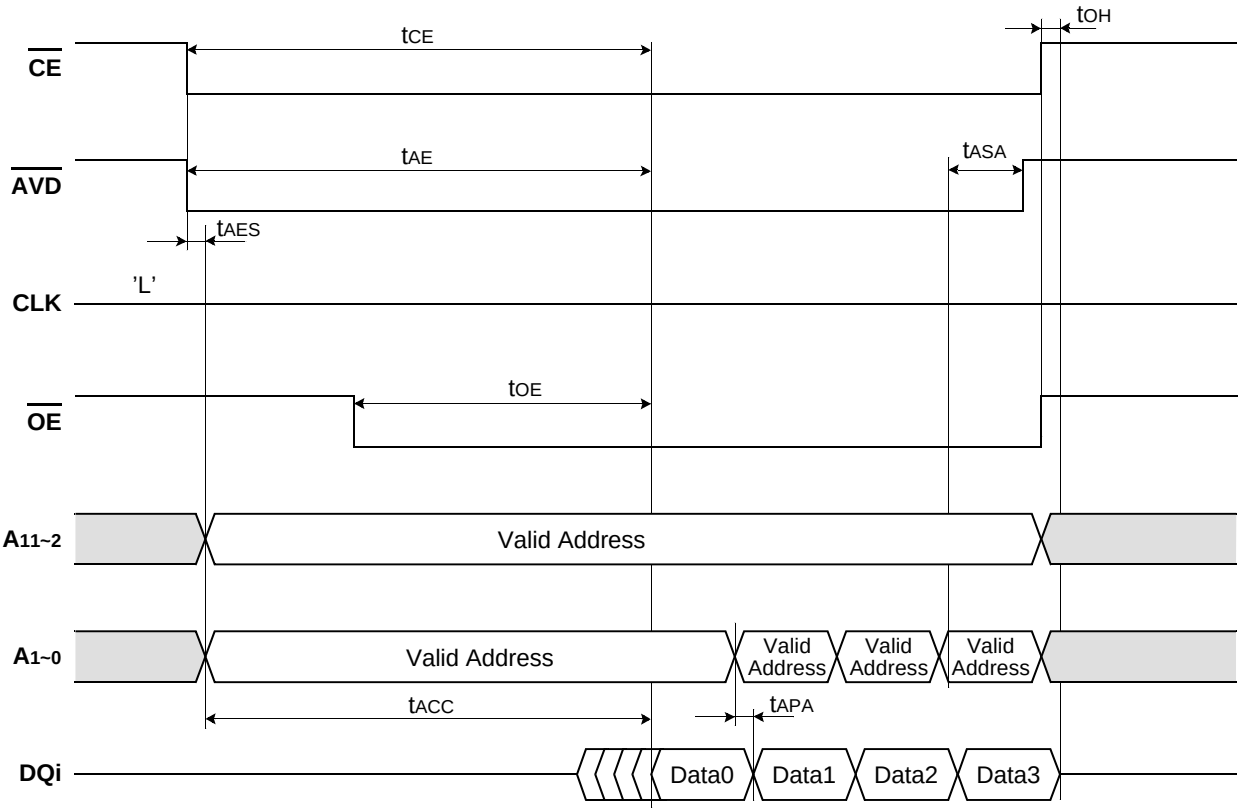
Figure 8. Asynchronous Read Mode



Asynchronous Page Read Operation

Asynchronous page read mode is the default state and provides a high data transfer rate for non clocked memory subsystems. The page size is four words, and A1~0 addresses one of the four words. The read cycle is initiated by first applying address to the address bus. The address latch is transparent while AVD is low. The address is latched by internal address latch circuit. The random access time is measured from a stable address, falling edge of AVD or falling edge of CE which ever occurs last. The clock should remain "1" during asynchronous access. Address access time(tACC) is equal to the delay from stable addresses to valid output data. The chip enable access time(tCE) is the delay from the stable addresses and stable CE to valid data at the outputs. The output enable access time(tOE) is the delay from the falling edge of OE to valid data at the output. CE and AVD must toggle in asynchromous read operation.

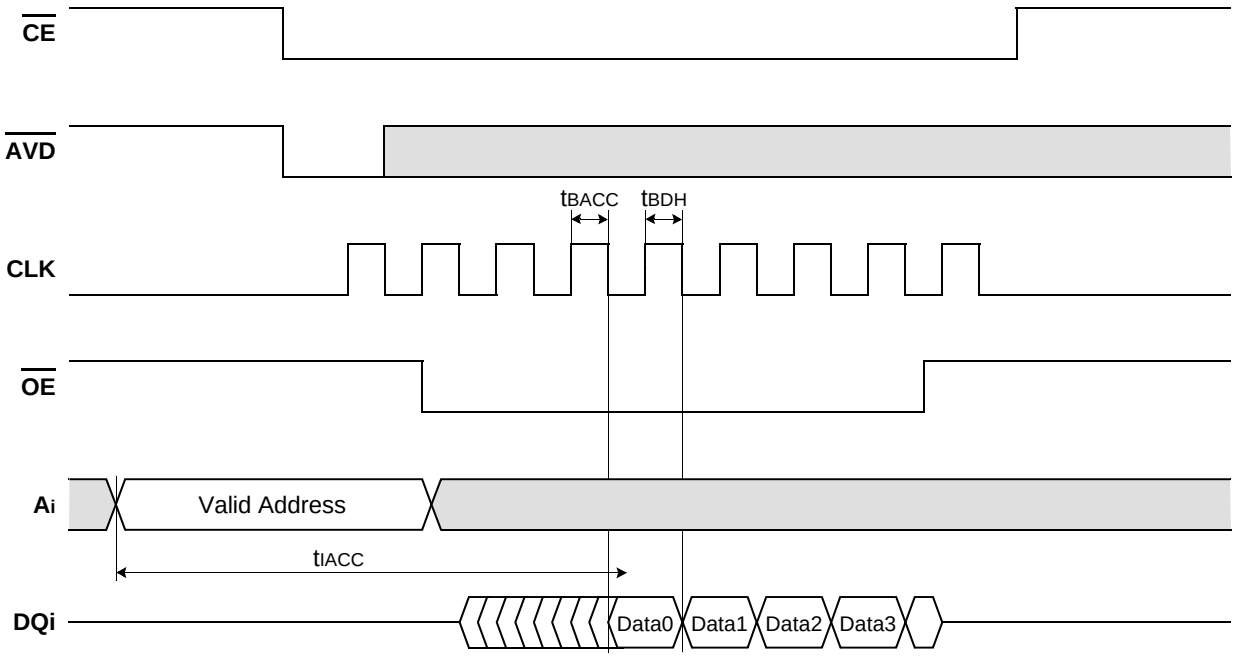
Figure 9. Asynchronous Page Read Mode



Synchronous Burst Read Operation

When the device is powered up, it defaults to asynchronous read operation. Burst mode is selected by System Configuration register bit 15. The burst mode is used to improve the data transfer between the memory and the system processor. The burst mode is used only for read operations. Burst length is available on 4words/ 8words/ 16words/ 32words/ Continuous length, and is set by BL of System configuration reguster. The Bus Controller in the system will insert required read latency to meet host random access time. The first access time in the burst is equal to the random access time. In the burst access, the address is latched at the rising edge of the clock pulse when AVD is low. The first data in the burst access is available after the random access time. The Bus Controller reads data at the first rising edge of the clock after read latency. There is no conflict between AVD's low and OE's low.
The output buffers need to settle before the first data is available. Due to this, the shortest random access is at least one clock cycles from the rising edge of the clock when AVD is low. This is defined as random access without any wait state. As the random access is allowed to be much longer than one clock cycles, the flash device has to support wait state insertion in order to synchronize the start of the burst access.

Figure 10. Synchronous Burst Read Mode(3clock read latency case)

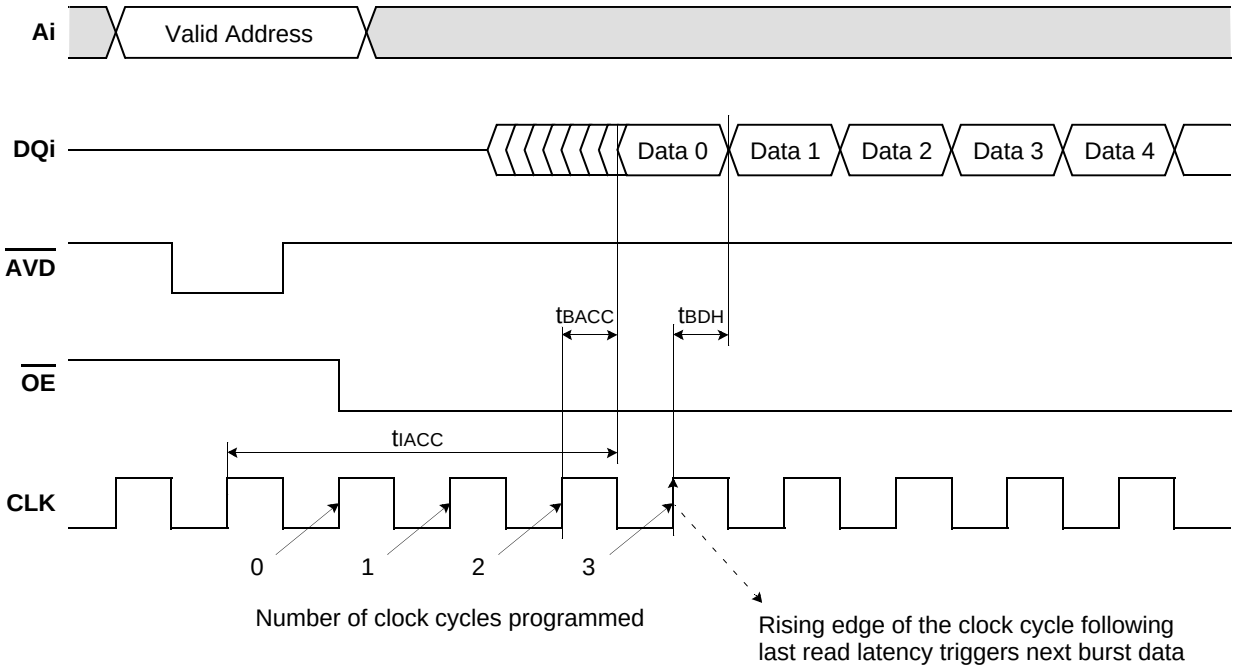


Programmable Read Latency

The programmable read latency value indicates to the device the number of additional clock cycles that must elapse after $\overline{AVD}$ is driven active before data will be available.

The number of read latency that should be programmed into the device is directly related to the clock frequency. Upon Power up, the device defaults to seven cycles. The total number of the read latency is programmable from zero to seven cycles. A hardware reset will set read latency to seven cycles after power-up. The minimum read latency for this device is three cycle assuming 40MHz system clock.

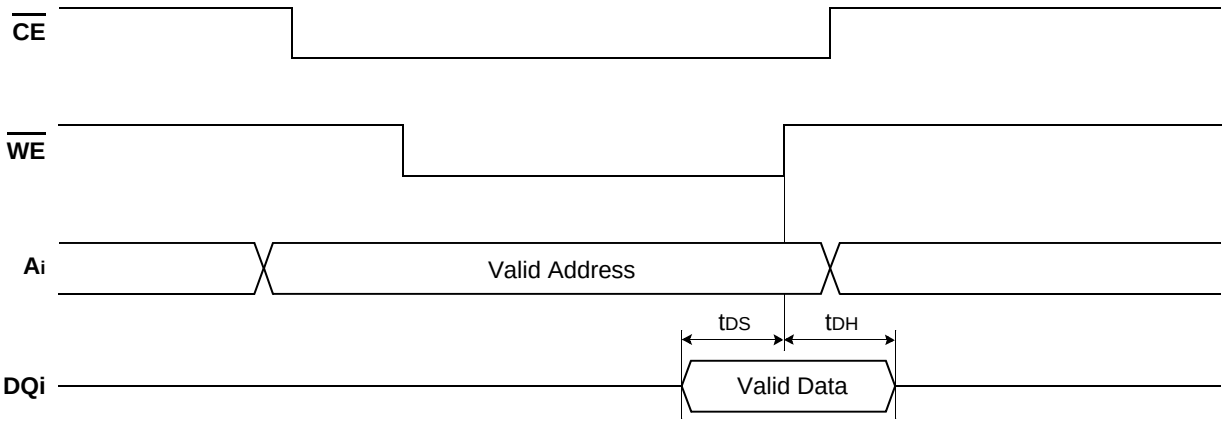
Figure 11. Example of 3clock Read Latency Insertion



Asynchronous Write Operation

Write is allowed only in the asynchronous mode. The address is latched at the rising edge of the $\overline{CE}$ signal. The random access time is measured from a stable address, falling edge of $\overline{CE}$. Write operations are asynchronous. Therefore, CLK is ignored during write operation. There is no conflict between $\overline{CE}$'s low and $\overline{OE}$'s low.

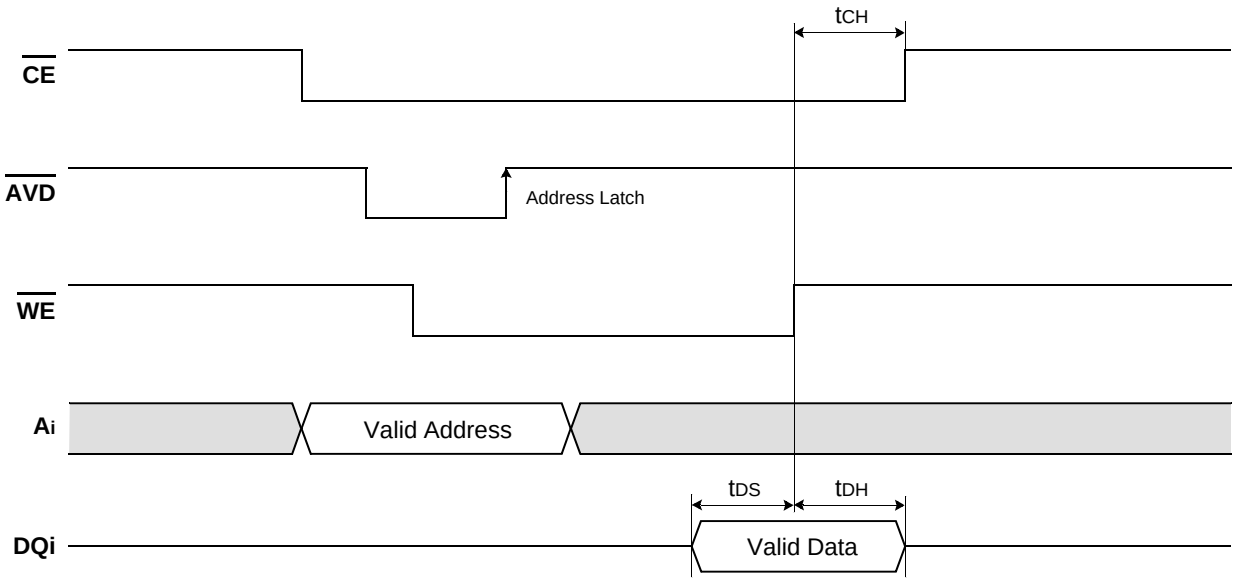
Figure 12 Asynchronous Write Mode



Latched Asynchronous Write Operation

At Latched Asynchronous Write operation, the address is latched at the rising edge of the $\overline{AVD}$ signal. Because Write operations are asynchronous operation, CLK is ignored during write operation. There is no conflict between $\overline{AVD}$'s low and $\overline{OE}$'s low.

Figure 13. Latched Asynchronous Write Mode



7. Electrical Specifications

7-1. Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	V_{CC}	3.6	V
	All other pins	V_{IN}	3.6	
Latch-up current		I_{latch}	±200	mA
Storage temperature		T_{STG}	-65 to 150	°C

NOTE:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Exposure to absolute maximum rating conditions for extended periods may affect reliability.

7-2 Recommended Operating Ratings

7-2-1. Supply Voltage(Voltage reference to GND)

Parameter	Symbol	1.8V Part			2.6V Part			Unit
		Min	Typ.	Max	Min	Typ.	Max	
Supply Voltage	V_{CC}	1.7	1.8	1.95	2.4	2.6	2.8	V
	V_{SS}	0	0	0	0	0	0	

7-2-2. Temperature

Parameter	Symbol	Rating	Unit
Commercial temperature	T_A(Commercial temp.)	0 to 70	°C
Industrial temperature	T_A(Industrial temp.)	-25 to 85	

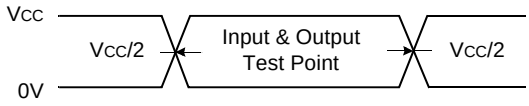
7-3. DC Characteristics

Parameter	Symbol	Test Condition	1.8V Part			2.6V Part			Unit
			Min	Typ.	Max	Min	Typ.	Max	
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc Vcc=Vcc(max)	-7	-	7	-10	-	10	uA
Output leakage current	I_{LO}	V_{OUT}=Vss to Vcc Vcc=Vcc(max)	-7	-	7	-10	-	10	
Standby current	I_{CCS}	$\overline{Vcc}$=$\overline{Vcc}$(max) CE=RP=V_{IH} INT=floating	-	22	85		22	85	
Active Async. Read Current	I_{CCR1}	V_{IN}=V_{IH} or V_{IL} $\overline{CE}$=V_{IL} $\overline{OE}$=V_{IH}	-	10	20		10	25	mA
Active Sync. Read Current	I_{CCR2}	$\overline{CE}$=V_{IL} $\overline{OE}$=V_{IH} Continuous Burst CLK=45Mhz	-	11	20		11	25	
Active Program Current	I_{CCW}	Program in Progress	-	12	20		12	25	
Active Erase Current	I_{CCE}	Erase in Progress	-	12	20		12	25	
Input High voltage	V_{IH}	-	Vcc -0.4	-	Vcc+ 0.4	Vcc- 0.4	-	Vcc+ 0.4	V
Input Low voltage	V_{IL}	-	-0.5	-	0.4	-0.5	-	0.4	
High level output voltage	V_{OH}	I_{OH}=-100uA Vcc=Vcc(min)	Vcc- 0.2	-	-	Vcc- 0.2	-	-	
Low level output voltage	V_{OL}	I_{OH}=-100uA Vcc=Vcc(min)	-	-	0.2	-	-	0.2	
Input capacitance[1)]	C_{IN}	Any input and Bi-directional buffers	-	-	10	-	-	10	pF
Output capacitance[1)]	C_{OUT}	Any output buffers	-	-	10	-	-	10	

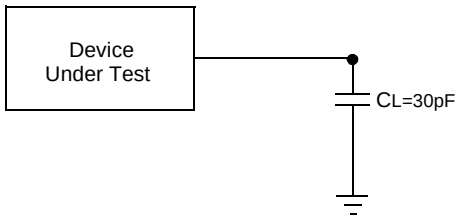
NOTE:
1. This value excludes package parasitic

7-4. AC Test Condition

Parameter	Value
Input Palse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load	CL=30pF



Input Pulse and Test Point



Output Load

7-5. AC Characteristics

Asynchronous Read AC Parameters

Parameter	Description	1.8V Part			2.6V Part			Unit
		Min	Typ.	Max	Min	Typ.	Max	
tCE	Access time from $\overline{CE}$ Low	-	-	55	-	-	55	ns
tOE	Output Enable to Output Valid	-	-	23	-	-	23	ns
tACC	Asynchronous Access Time	-	-	55	-	-	55	ns
tAE	Random Access $\overline{AVD}$-Data Valid	-	-	55	-	-	55	ns
tOH	Output hold from $\overline{CE}$ or $\overline{OE}$ change, whichever occurs first	0		4	0		4	ns
tAPA	Page address access time			40			40	ns
tASA	Address setup to $\overline{AVD}$ high	7		-	7		-	ns
tAES	$\overline{CE}$ & $\overline{AVD}$ setup to Valid Address	-	-	10	-	-	10	ns
tCA	$\overline{CE}$ setup to $\overline{AVD}$ falling edge	0	-	-	0	-	-	ns

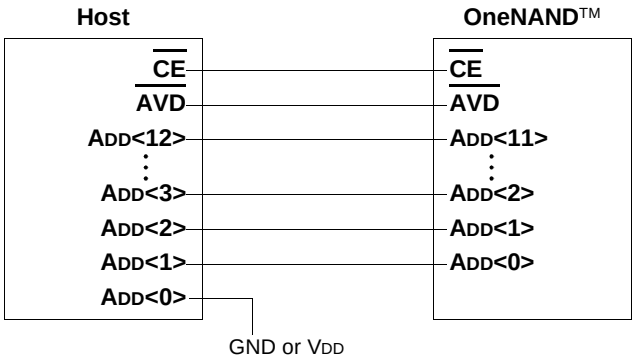
Asynchronous Read AC Parameters

Parameter	Description	1.8V Part			2.6V Part			Unit
		Min	Typ.	Max	Min	Typ.	Max	
tCES	$\overline{CE}$ setup time to CLK	5	-	-	5	-	-	ns
tIACC	Initial Access Time @45Mhz	-	-	85.6		-	84.6	ns
tBACC	Burst Access Time Valid clock to output delay	-	-	19		-	17	ns
tBDH	Data hold time from next clock cycle	4		-	4	-	-	ns
tAVDS	$\overline{AVD}$ setup time to CLK	5		-	5	-	-	ns
tAVDH	$\overline{AVD}$ hold time to CLK	7		-	8	-	-	ns
tACS	Address setup time to CLK	5		-	5	-	-	ns
tACH	Address hold time to CLK	7		-	7	-	-	ns
tOH	Output hold from $\overline{CE}$ or $\overline{OE}$ change, whichever occurs first	4		-	4	-	-	ns
tOE	Output Enable ot Output Valid		23			23		ns
tCLKH	FlsCLK high time	10			10			ns
tCLKL	FlsCLK low time	10			10			ns
tCA	$\overline{CE}$ setup to $\overline{AVD}$ falling edge	0	-	-	0	-	-	ns

Write AC Parameters

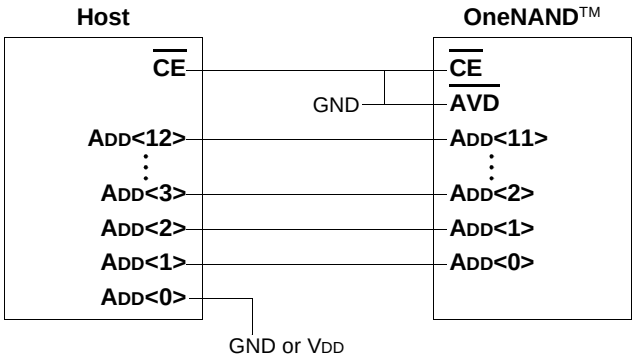
Parameter	Description	1.8V Part			2.6V Part			Unit
		Min	Typ.	Max	Min	Typ.	Max	
tAVDP	$\overline{AVD}$ Low time	12		-	12		-	ns
tAAVDS	Asynchronous Address setup time	7		-	7		-	ns
tAWES	Asynchronous Address setup to new low	5			5			
tAAVDH	Asynchronous Address hold time	7		-	7		-	ns
tDS	Data Setup Time	5		-	5		-	ns
tDH	Data Hold Time	4		-	4		-	ns
tWC	Write Cycle Time	80		-	80		-	ns
tWPL	Write Pulse Width Low	20			20		-	ns
tWPH	Write Pulse Width High	50			50		-	ns
tCS	$\overline{CE}$ setup time	0	-		0	-	-	ns
tCH	$\overline{CE}$ Hold Time	4			4		-	ns
tAWES	Address setup to $\overline{WE}$ low	5			5			ns
tVLWH	$\overline{AVD}$ rising edge to $\overline{WE}$ rising edge	10			10			ns

***$\overline{\text{AVD}}$ connected case**



> If host uses byte-order typed address, ADD<0> can be used as byte/word selection pin.

***$\overline{\text{AVD}}$ disconnected case**



> If host uses byte-order typed address, ADD<0> can be used as byte/word selection pin.
> In $\overline{\text{AVD}}$ disconnected case, $\overline{\text{AVD}}$ can be tied to $\overline{\text{CE}}$ or GND.