1M x 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- **Performance range:**

	tRAC	tCAC	tRC	tHPC
KM416V1004A-6/A-L6/A-F6	60ns	17ns	110ns	24ns
KM416V1004A-7/A-L7/A-F7	70ns	20ns	130ns	29ns
KM416V1004A-8/A-L8/A-F8	80ns	20ns	150ns	34ns

- **Extended Data Out Mode (Fast Page Mode with Extended Data Out)**
- **2 $\overline{CAS}$ Byte/Word Read/Write operation**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +3.3V±0.3V power supply**
- **Refresh Cycle**
  - **4096 cycle/64ms (Normal)**
  - **4096 cycle/128ms (L-version)**
  - **4096 cycle/128ms (F-version)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

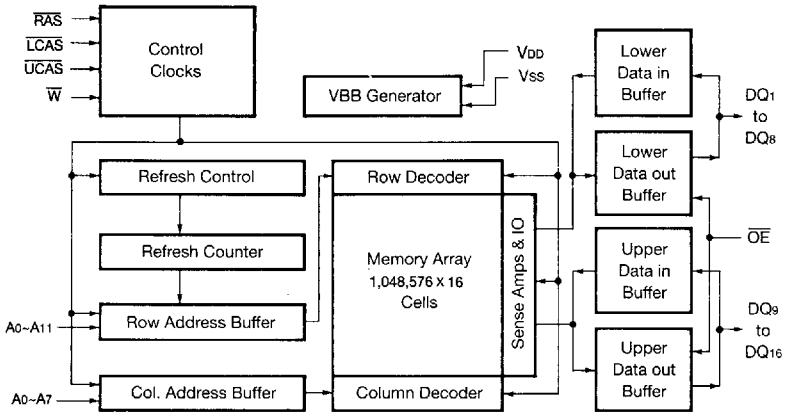
GENERAL DESCRIPTION

The Samsung KM416V1004A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416V1004A/A-L/A-F features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All inputs and outputs are fully TTL compatible.

The KM416V1004A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

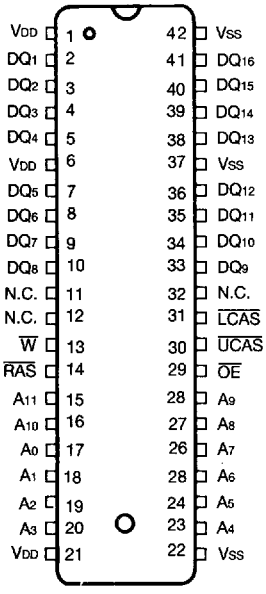
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

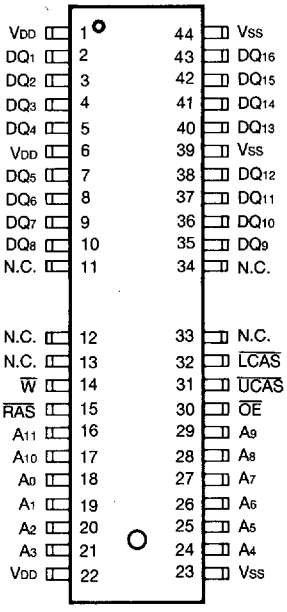
PIN CONFIGURATION (Top Views)

• KM416V1004AJ



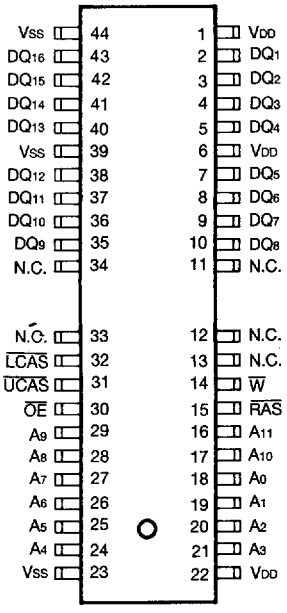
(SOJ)

• KM416V1004AT



(TSOP(II)-Forword)

• KM416V1004AR



(TSOP(II)-Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-16	Data In/Out
VSS	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
VDD	Power(+3.3V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to 4.6	V
Storage Temperature	T_{stg}	-55 to+150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.1	—	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{RC}=min.)	KM416V1004A-6/A-L6/A-F6	I_{CC1}	-	90	mA
	KM416V1004A-7/A-L7/A-F7			80	mA
	KM416V1004A-8/A-L8/A-F8			70	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})	KM416V1004A	I_{CC2}	-	2	mA
	KM416V1004AL			1	mA
	KM416V1004ALL			1	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM416V1004A-6/A-L6/A-F6	I_{CC3}	-	90	mA
	KM416V1004A-7/A-L7/A-F7			80	mA
	KM416V1004A-8/A-L8/A-F8			70	mA
EDO Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address Cycling @t_{PC}=min.)	KM416V1004A-6/A-L6/A-F6	I_{CC4}	-	110	mA
	KM416V1004A-7/A-L7/A-F7			100	mA
	KM416V1004A-8/A-L8/A-F8			90	mA
Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{DD}-0.2V)	KM416V1004A	I_{CC5}	-	1	mA
	KM416V1004AL			300	μA
	KM416V1004ALL			200	μA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ Cycling @t_{RC}=min.)	KM416V1004A-6/A-L6/A-F6	I_{CC6}	-	90	mA
	KM416V1004A-7/A-L7/A-F7			80	mA
	KM416V1004A-8/A-L8/A-F8			70	mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V_{IH})=V_{DD}-0.2V, Input Low Voltage(V_{IL})=0.2V $\overline{UCAS}$, $\overline{LCAS}$=0.2V D_{IN}=Don't Care, t_{RC}=31.25μs (L-Version) t_{RAS}=t_{RAS} min~300ns	KM416V1004A-L	I_{CC7}	-	450	μA

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DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V $\overline{W}$=$\overline{OE}$=A_0-A_{11}=V_{DD}-0.2V or 0.2V DQ_1-DQ_{16}=V_{DD}-0.2V or 0.2V or Open	KM416V1004A-F	I_{CCS}	-	250	μA
Input Leakage Current (Any input 0≤V_{IN}≤V_{DD}+0.3V, all other pins not under test=0 V)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{DD})		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-2mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once while one Hyper page mode cycle time t_{HPC}.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0~$_{11}$)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{W}$, $\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ_1~DQ_{16})	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{DD}=3.3V±0.3V, See notes 1,2)

(Test condition : V_{IH}/V_{IL}=2.1V/0.8V, V_{OH}/V_{OL}=2.0V/0.8V, Output Loading C_L=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	3,4,11
Access time from $\overline{CAS}$	t_{CAC}		17		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	17		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10,000	15	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	4

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	15
Column address hold time	tCAH	10		15		15		ns	15
Column address hold time referenced to $\overline{RAS}$	tAR	45		55		60		ns	6
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{RAS}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	10		15		20		ns	18
Data-in set-up time	tDS	0		0		0		ns	10,21
Data-in hold time	tDH	10		15		15		ns	10,21
Data-in hold time referenced to $\overline{RAS}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	40		50		50		ns	8,17
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{W}$ delay time	tAWD	55		60		65		ns	8
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	60		65		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	19
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	20
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		30		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	15		20		20		ns	
$\overline{OE}$ access time	tOEA		15		20		20	ns	
$\overline{OE}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	tOEZ	3	15	3	20	3	20	ns	7
$\overline{OE}$ command hold time	tOEH	15		20		20		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Hyper Page mode cycle time	tHPC	24		29		34		ns	12
Hyper Page mode read-modify-write cycle time	tHPRWC	76		81		91		ns	12
$\overline{CAS}$ precharge time (Hyper page mode)	tCP	10		10		10		ns	16
$\overline{RAS}$ pulse width (Hyper Page mode)	tRASP	60		70		80		ns	
$\overline{RAS}$ hold time from CAS precharge	tRHCP	35		40		45		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from $\overline{W}$	tWEZ	3	15	3	20	3	20	ns	7
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width	tWPE	5		5		5		ns	
$\overline{W}$ to data delay	tWED	15		20		20		ns	
$\overline{RAS}$ pulse width (F-ver)	tRASS	100		100		100		μs	13
$\overline{RAS}$ precharge time (F-ver)	tRPS	110		130		150		ns	13
$\overline{CAS}$ hlod time (F-ver)	tCHS	-50		-50		-50		ns	13

KM416V1004A/A-L/A-F Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1~DQ8	DQ9~DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL Loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. $t_{ASC} \geq t_{CP}$ min, Assume t_T=2.0ns.
13. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (F-version)
14. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
16. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
17. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
19. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
20. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.
21. t_{DS}, t_{DH} is independetly specified for lower byte D_{in} (1~8), upper byte $D_{in(9\sim16)}$

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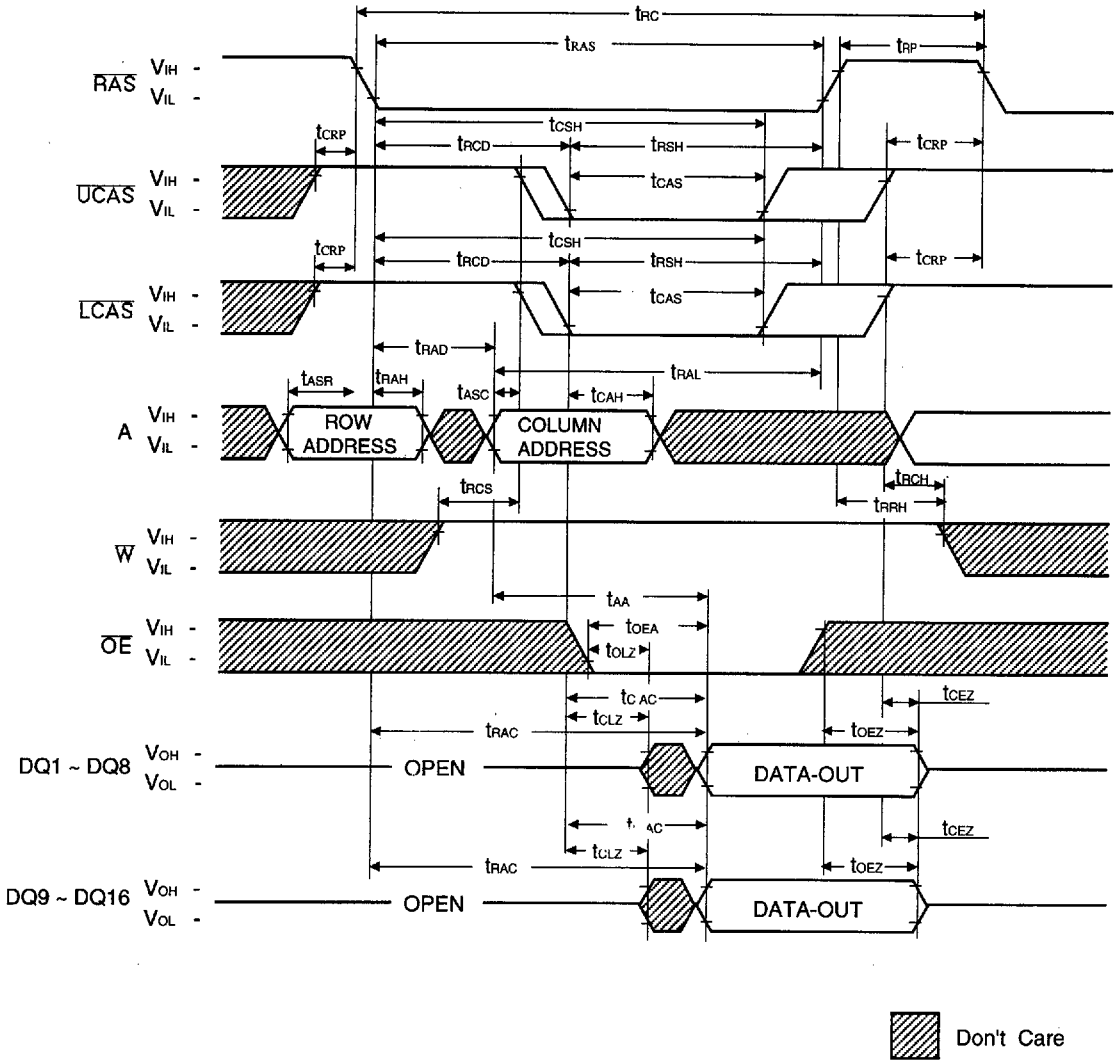
TIMING DIAGRAM

WORD READ CYCLE

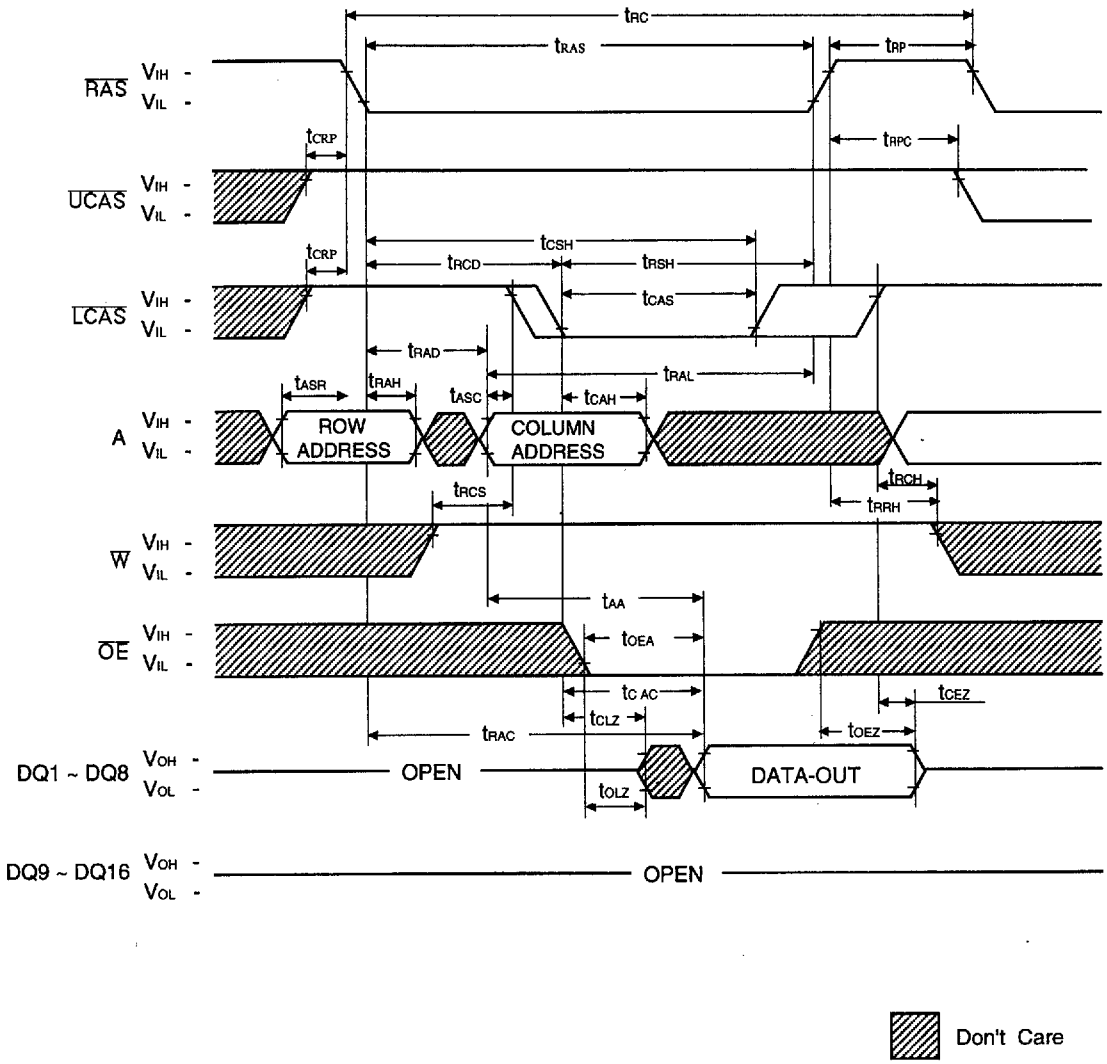
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

LOWER BYTE READ CYCLE

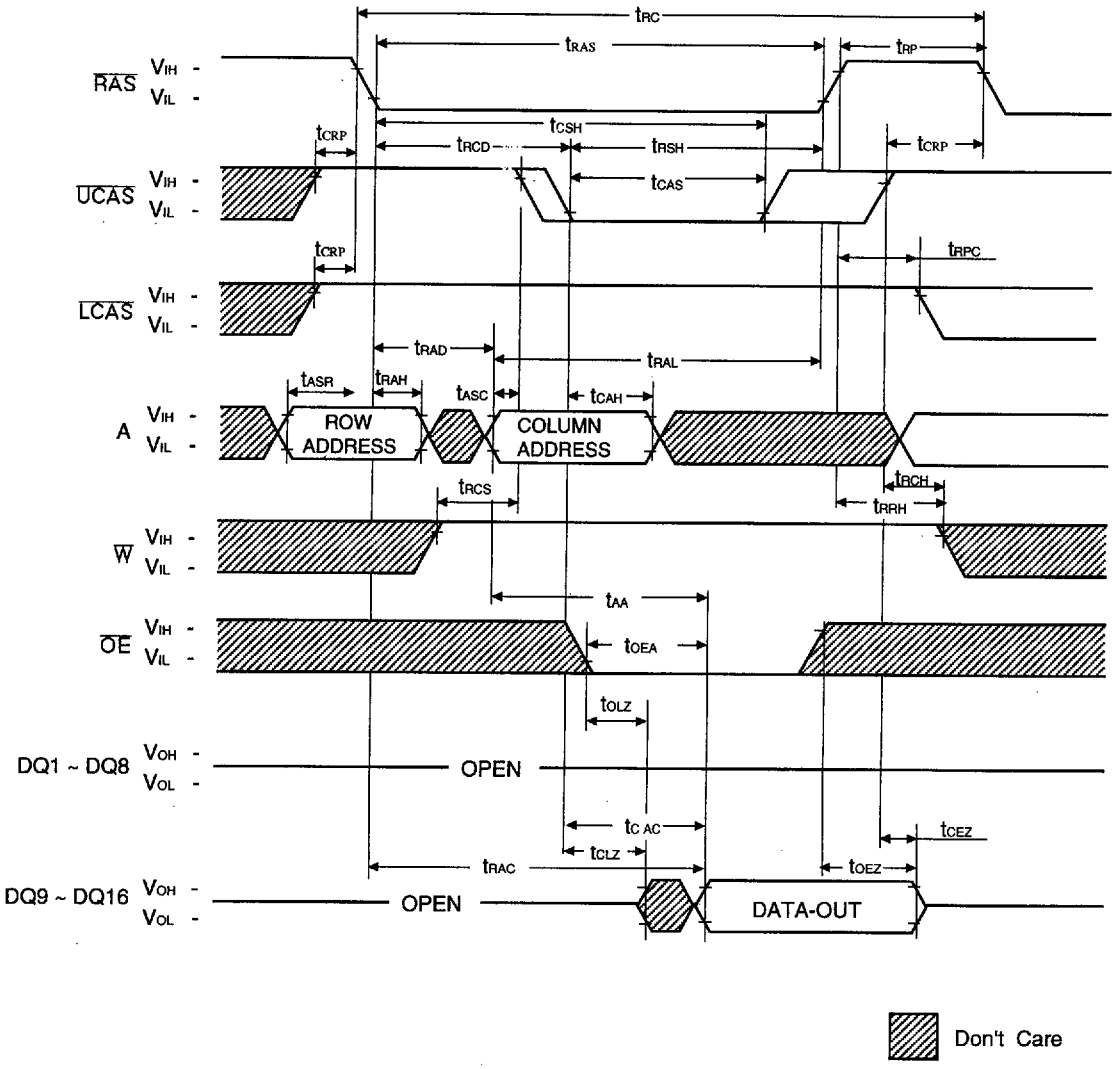
NOTE : D_{IN} = OPEN



TIMING DIAGRAM

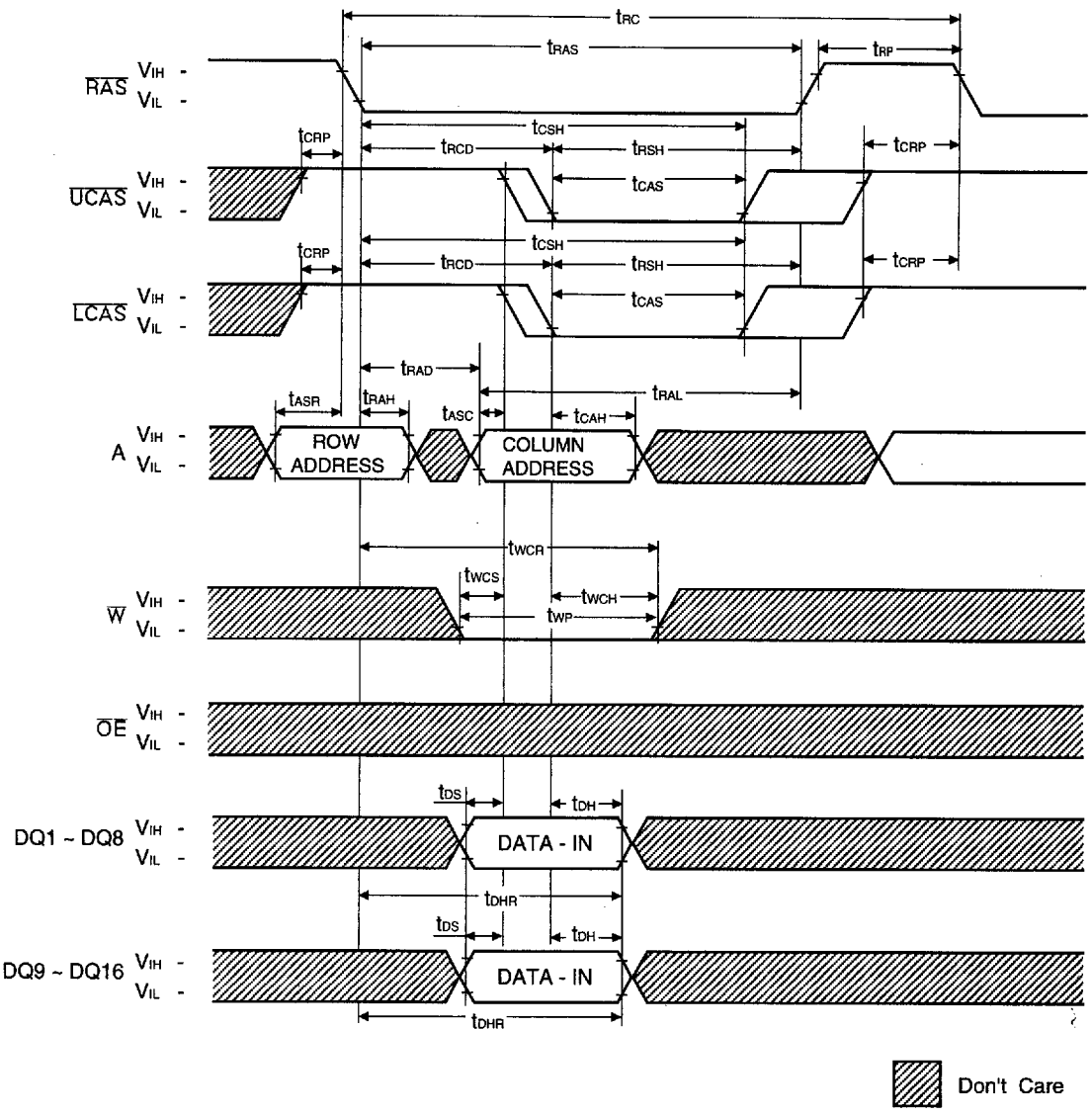
UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



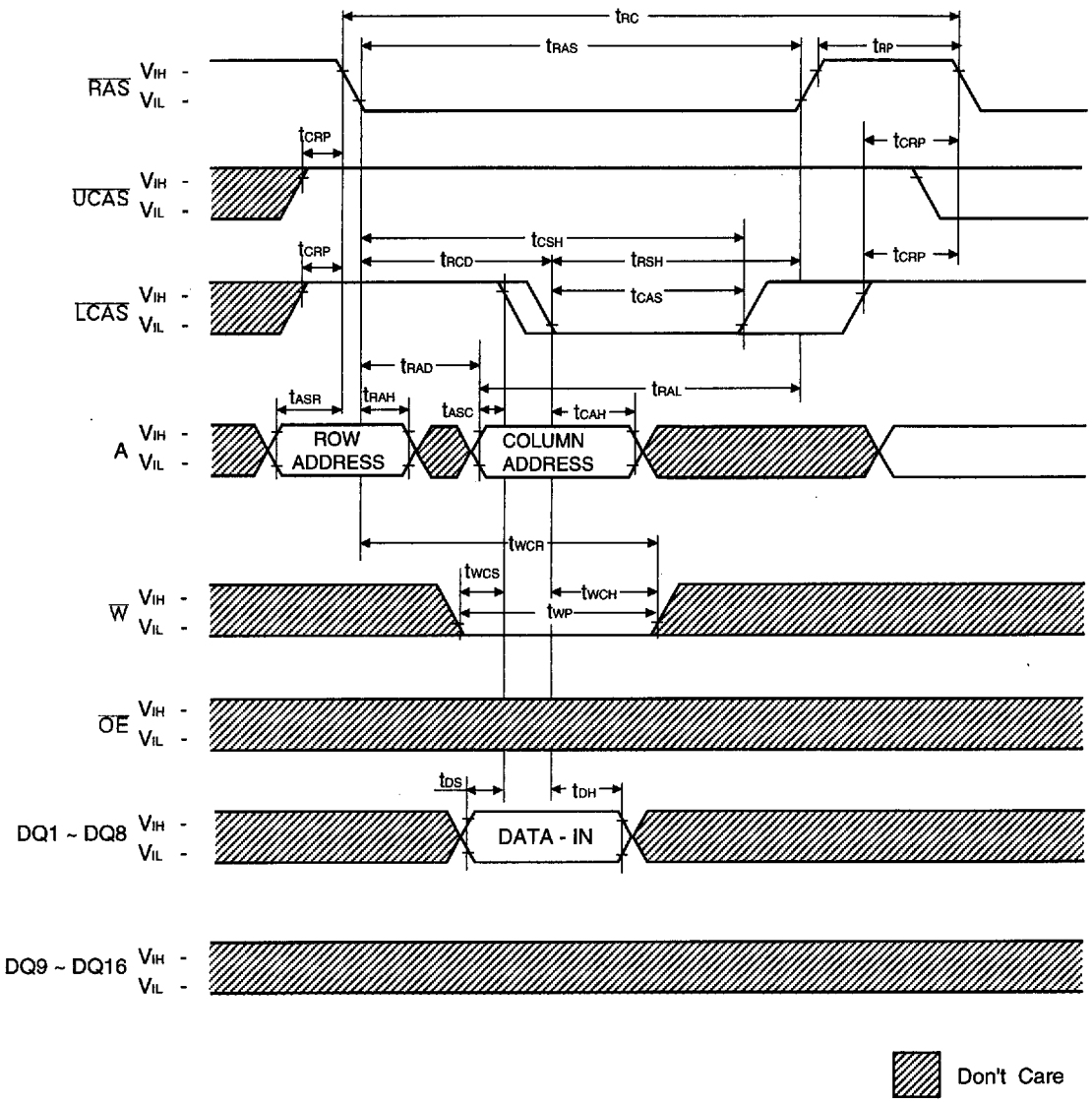
WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



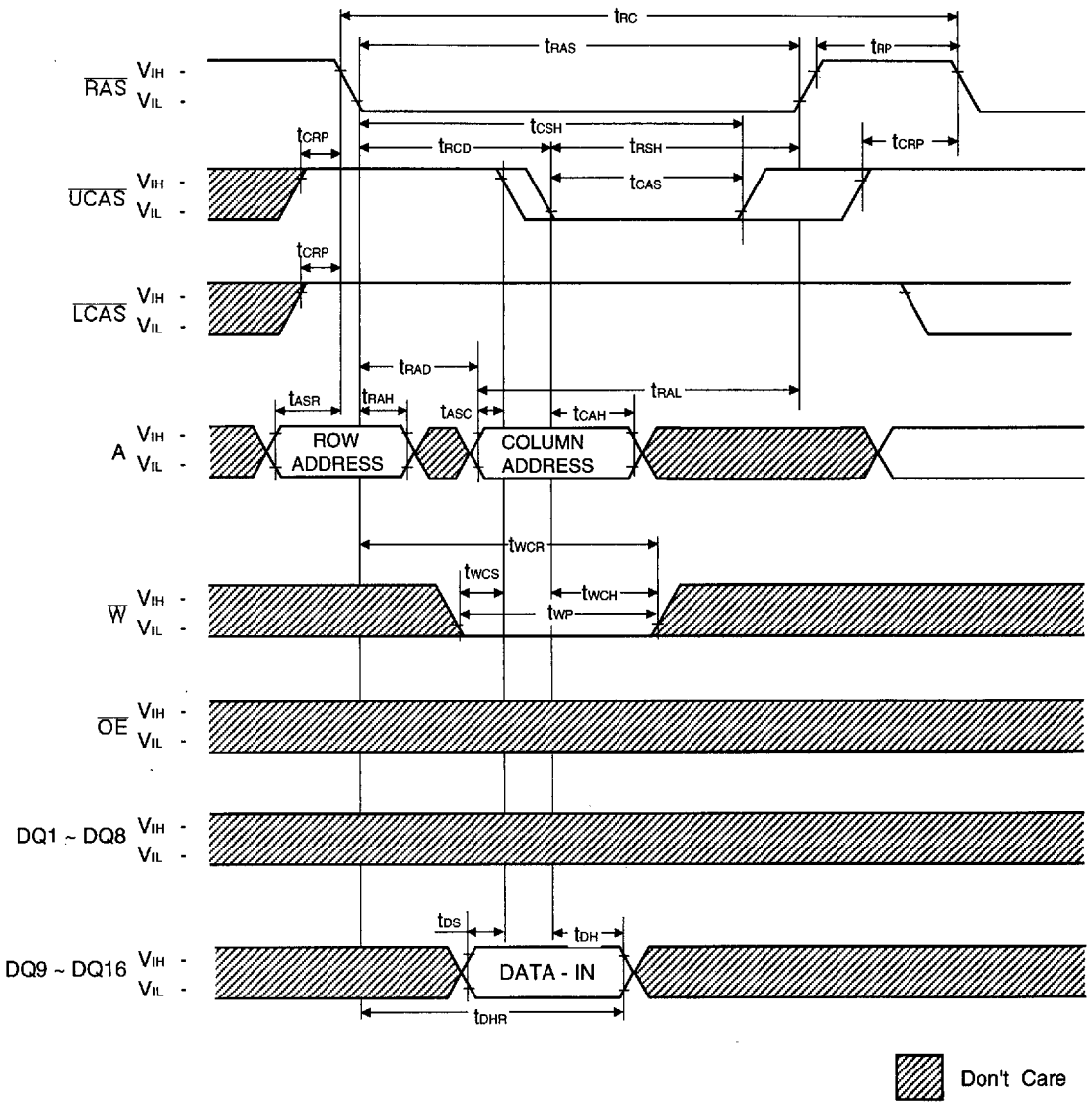
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



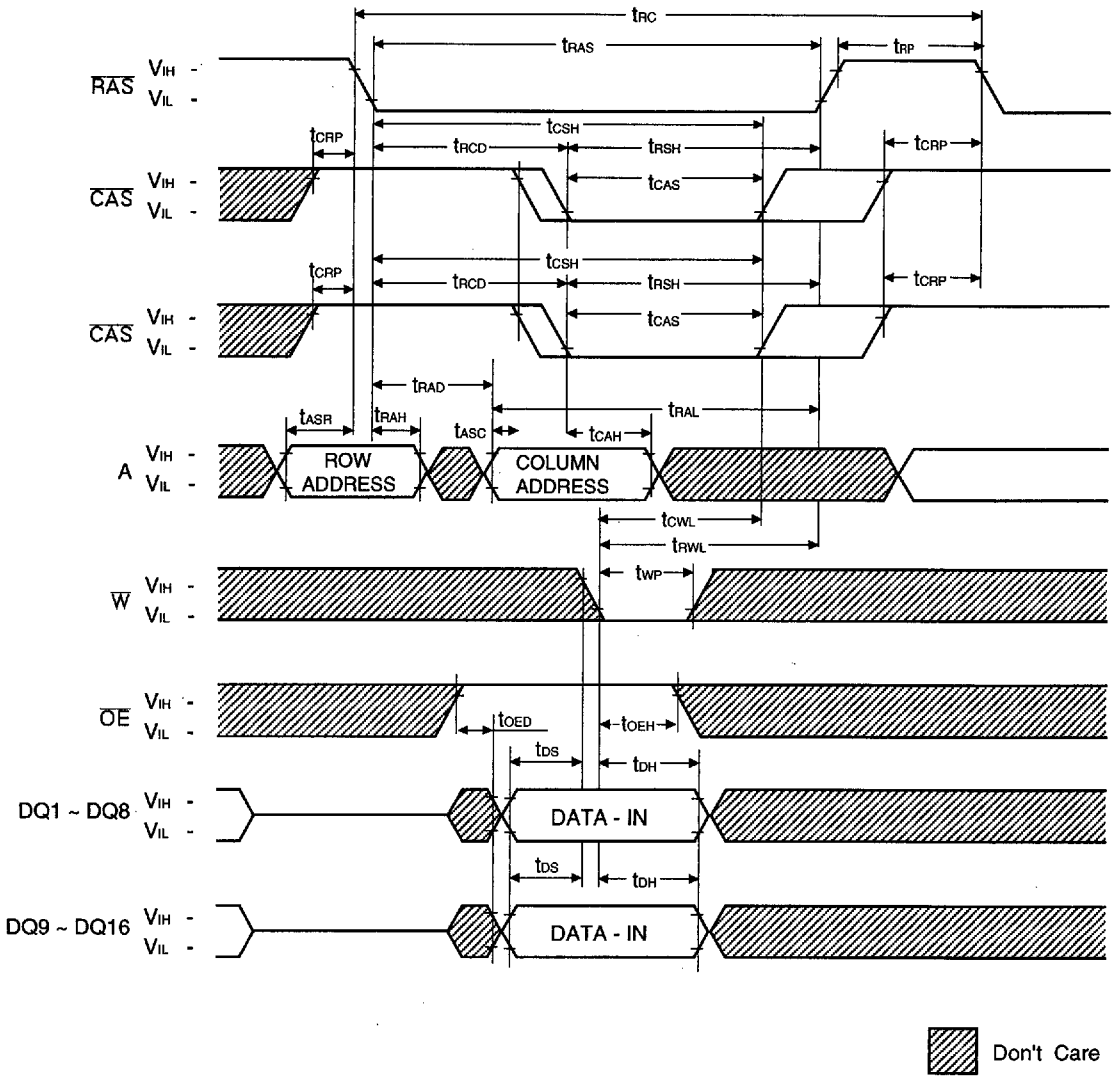
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



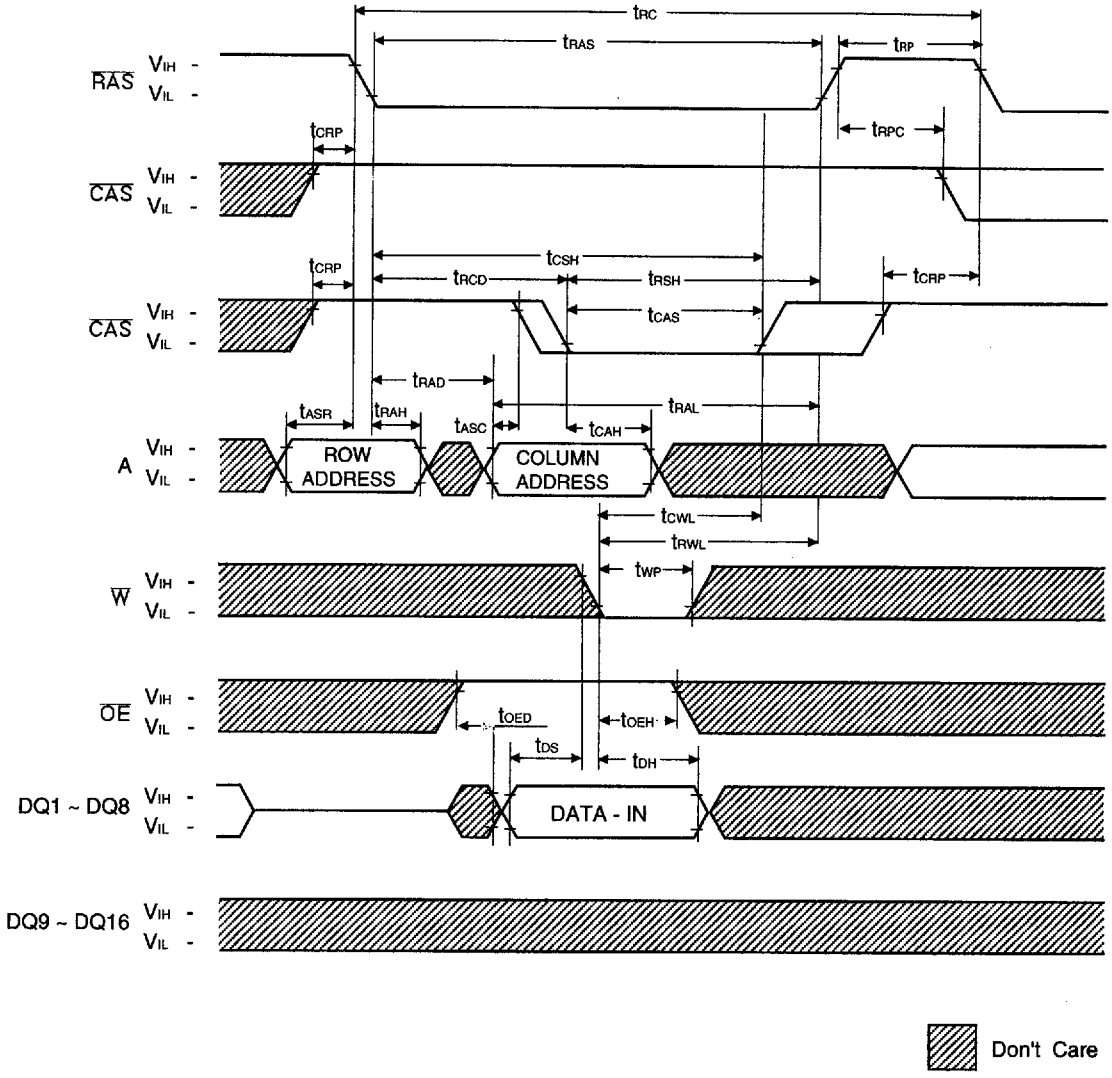
WORD WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



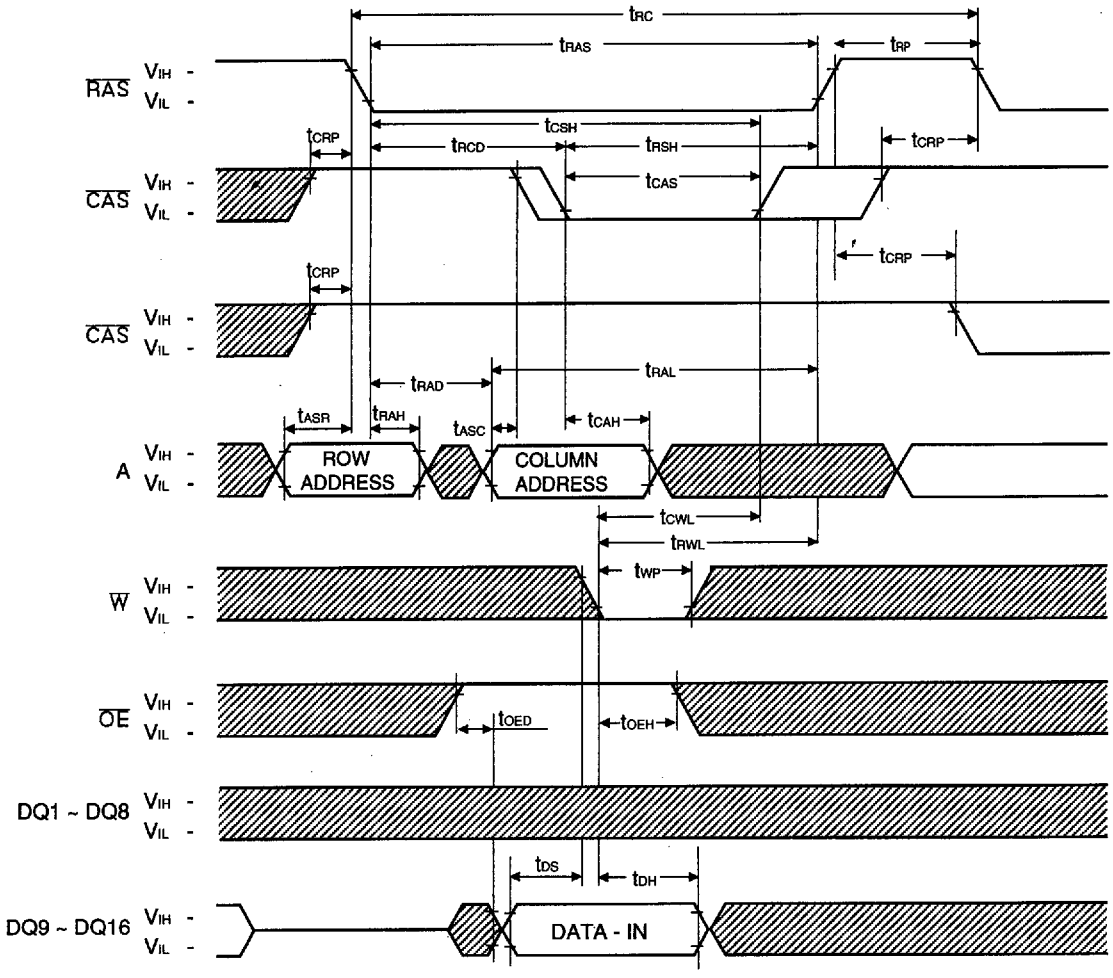
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

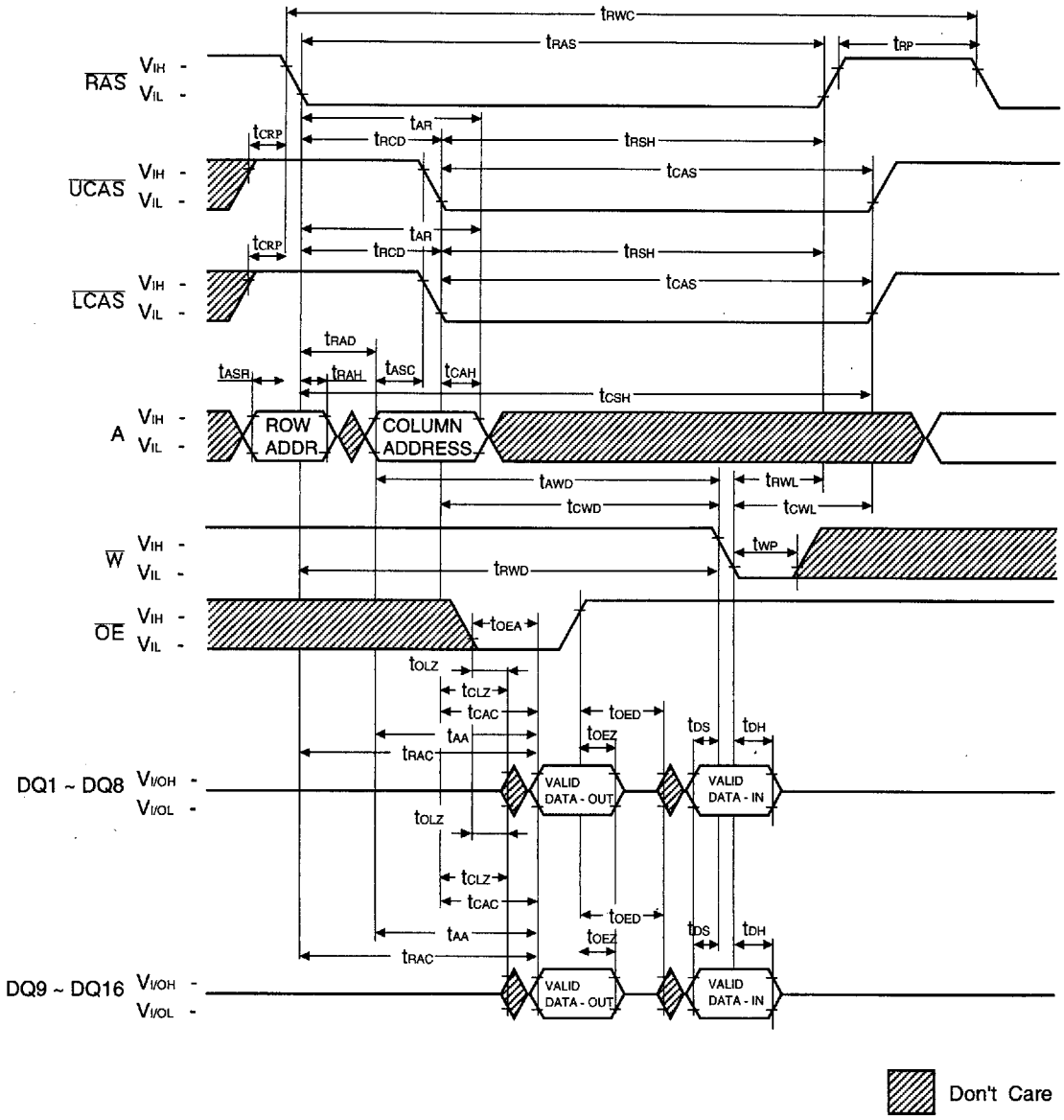


UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

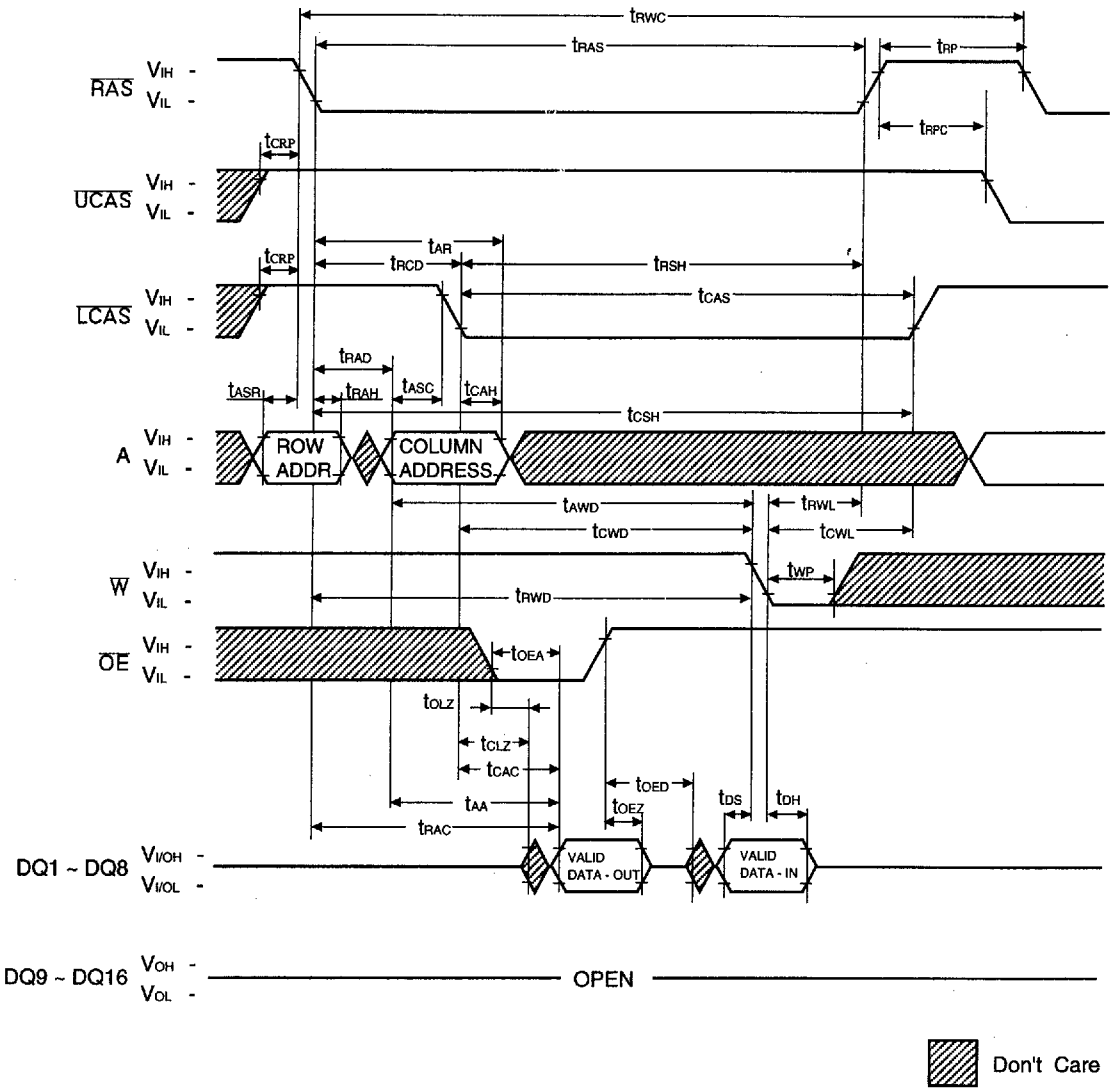
NOTE : D_{OUT} = OPEN



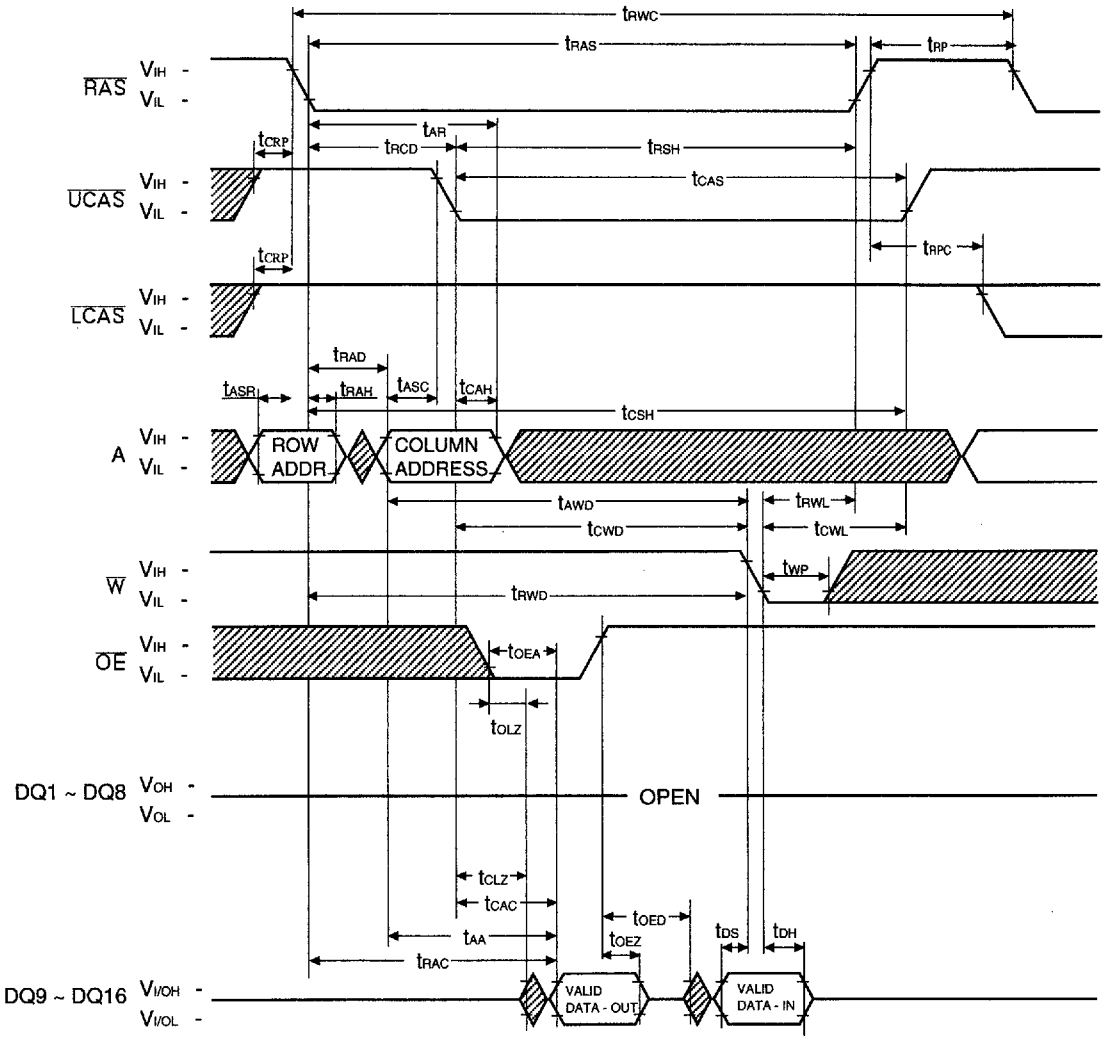
WORD READ - MODIFY - WRITE CYCLE



LOWER-BYTE READ - MODIFY - WRITE CYCLE

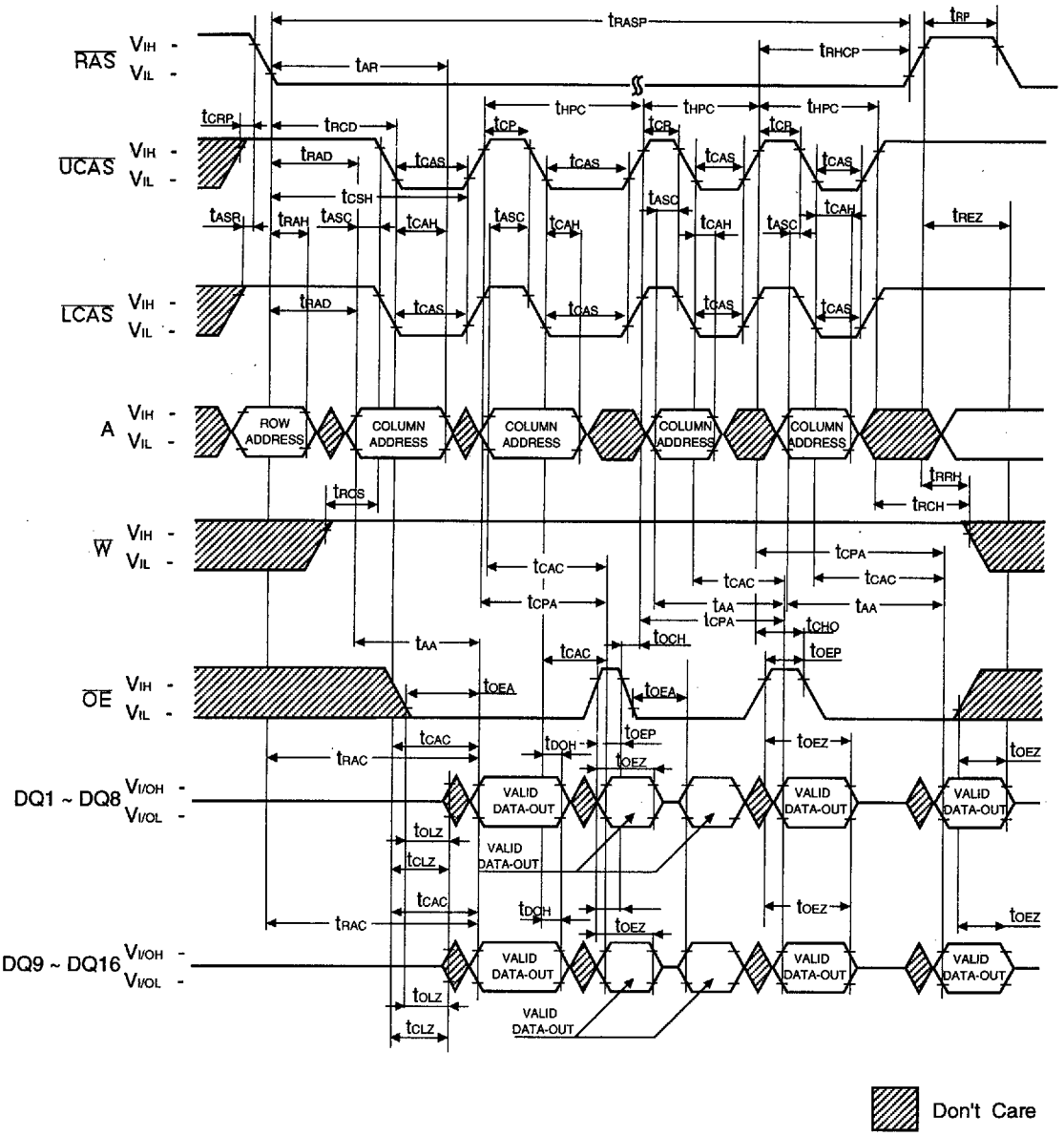


UPPER-BYTE READ - MODIFY - WRITE CYCLE

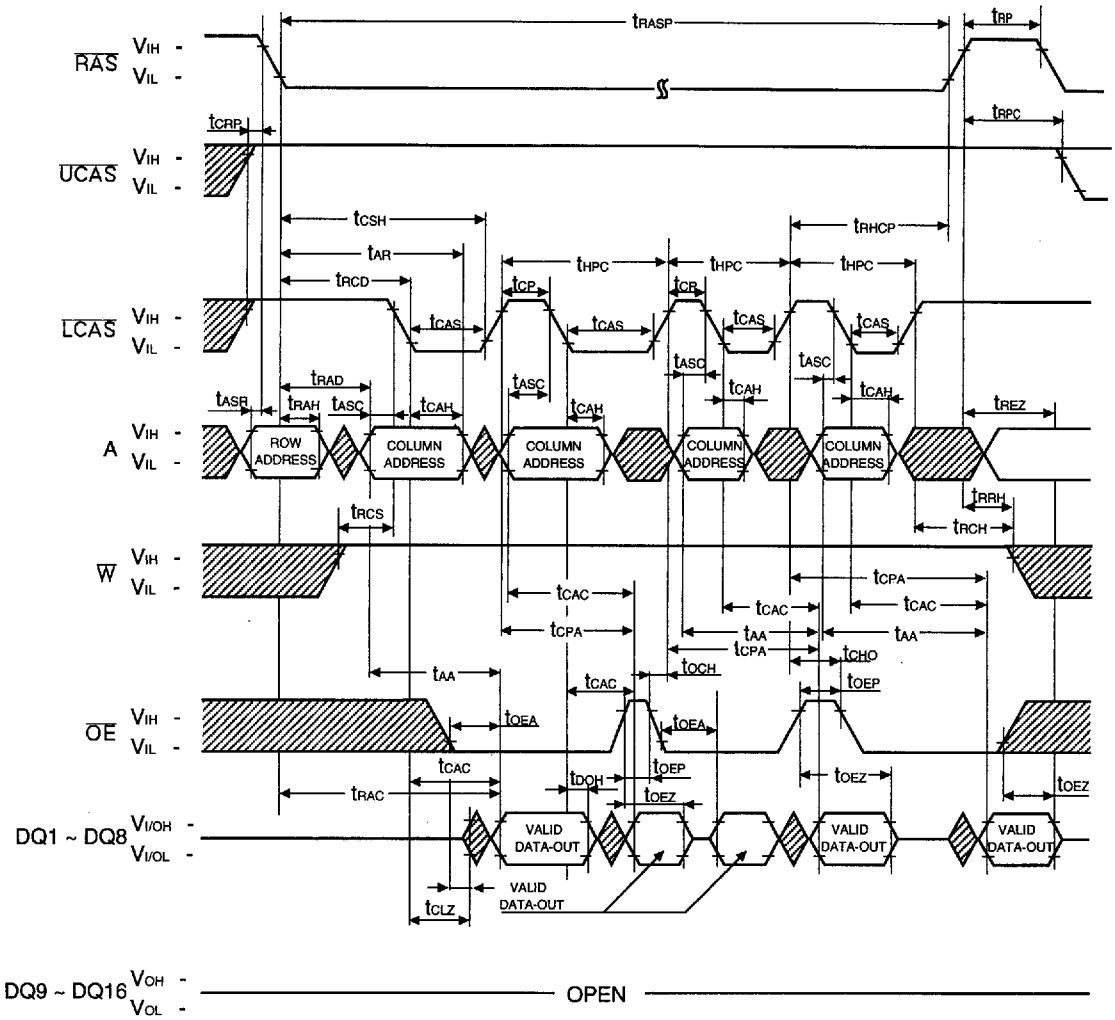


6

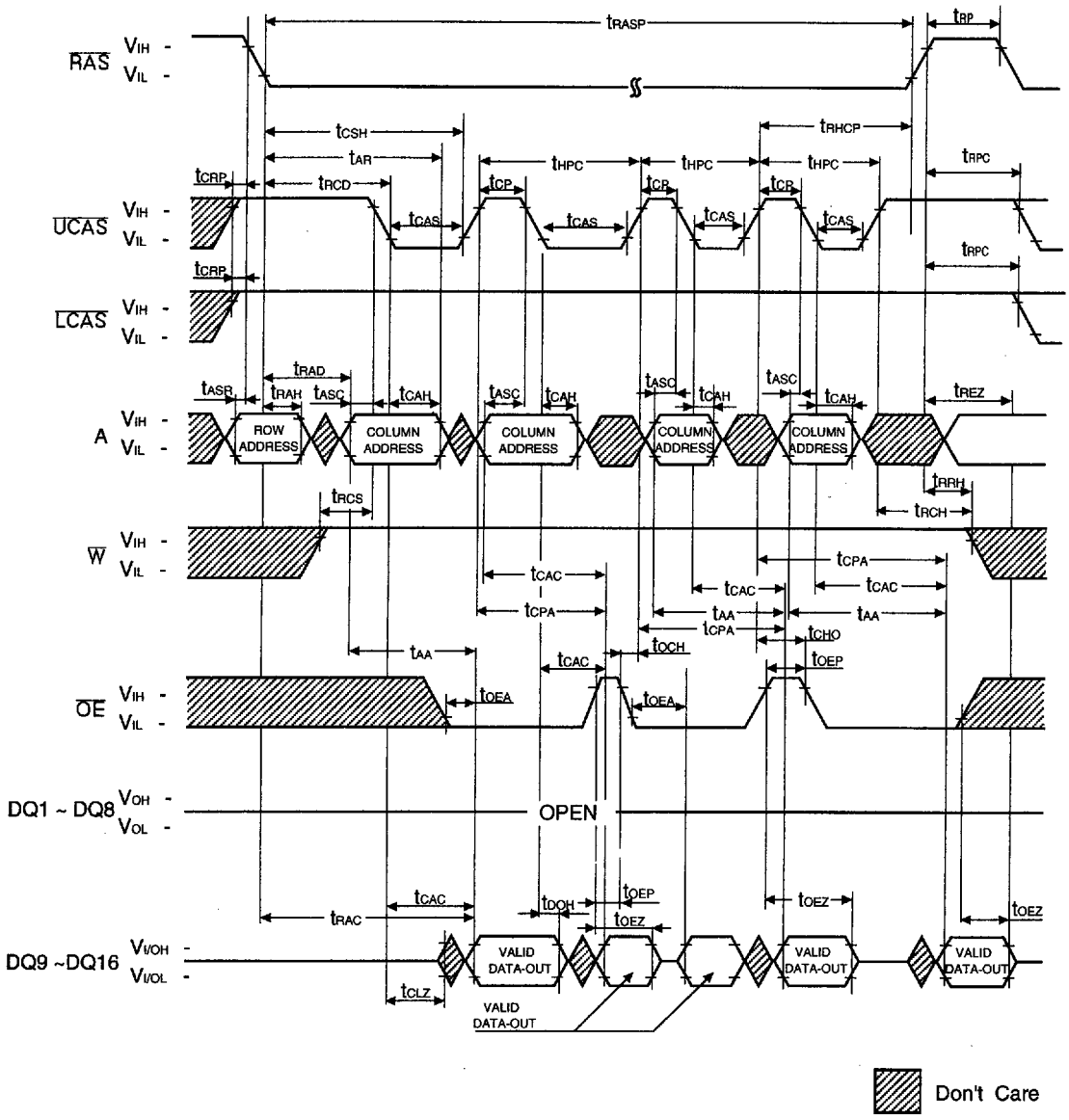
HYPER PAGE MODE WORD READ CYCLE



HYPER PAGE MODE LOWER BYTE READ CYCLE

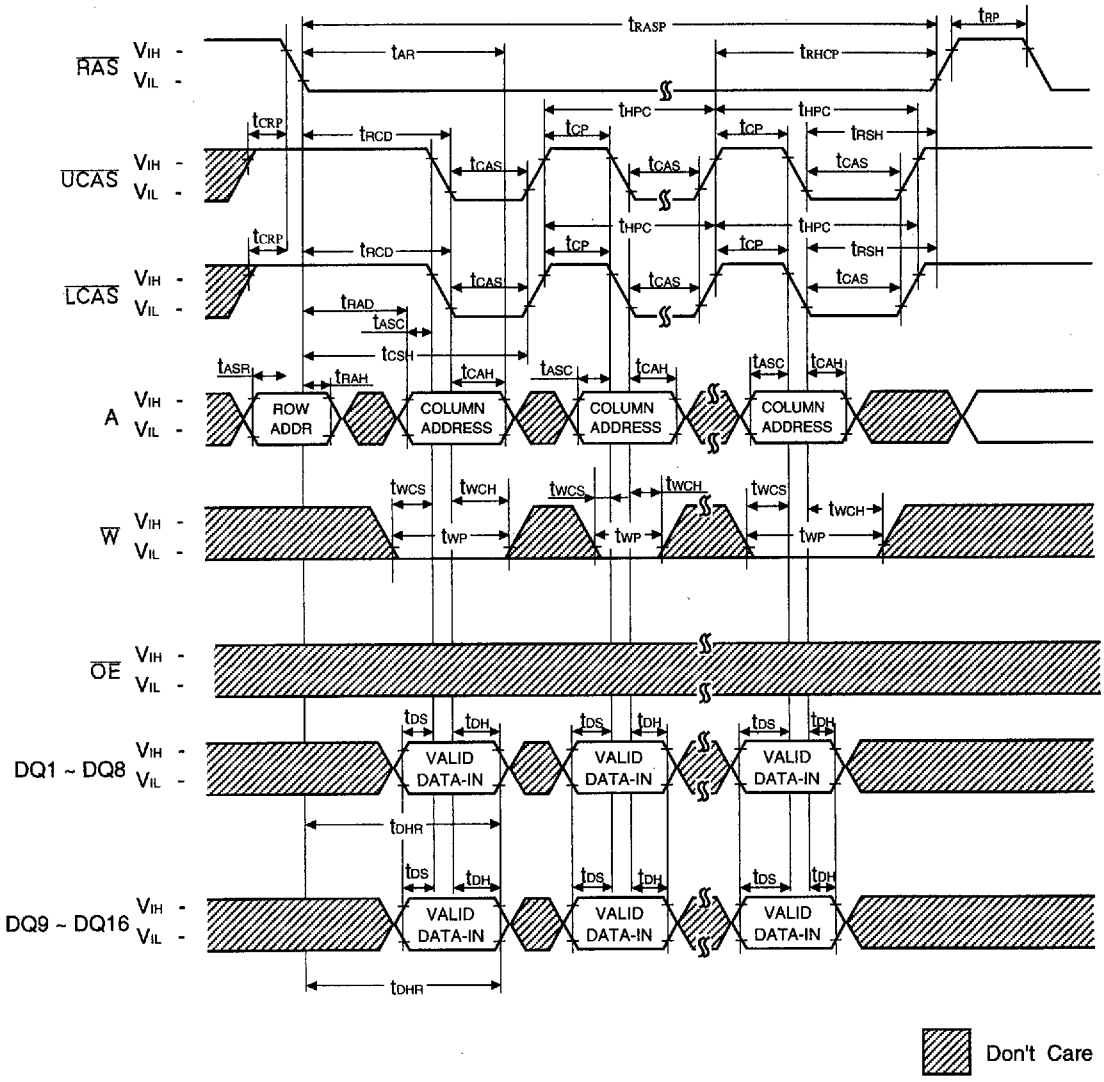


HYPER PAGE MODE UPPER BYTE READ CYCLE



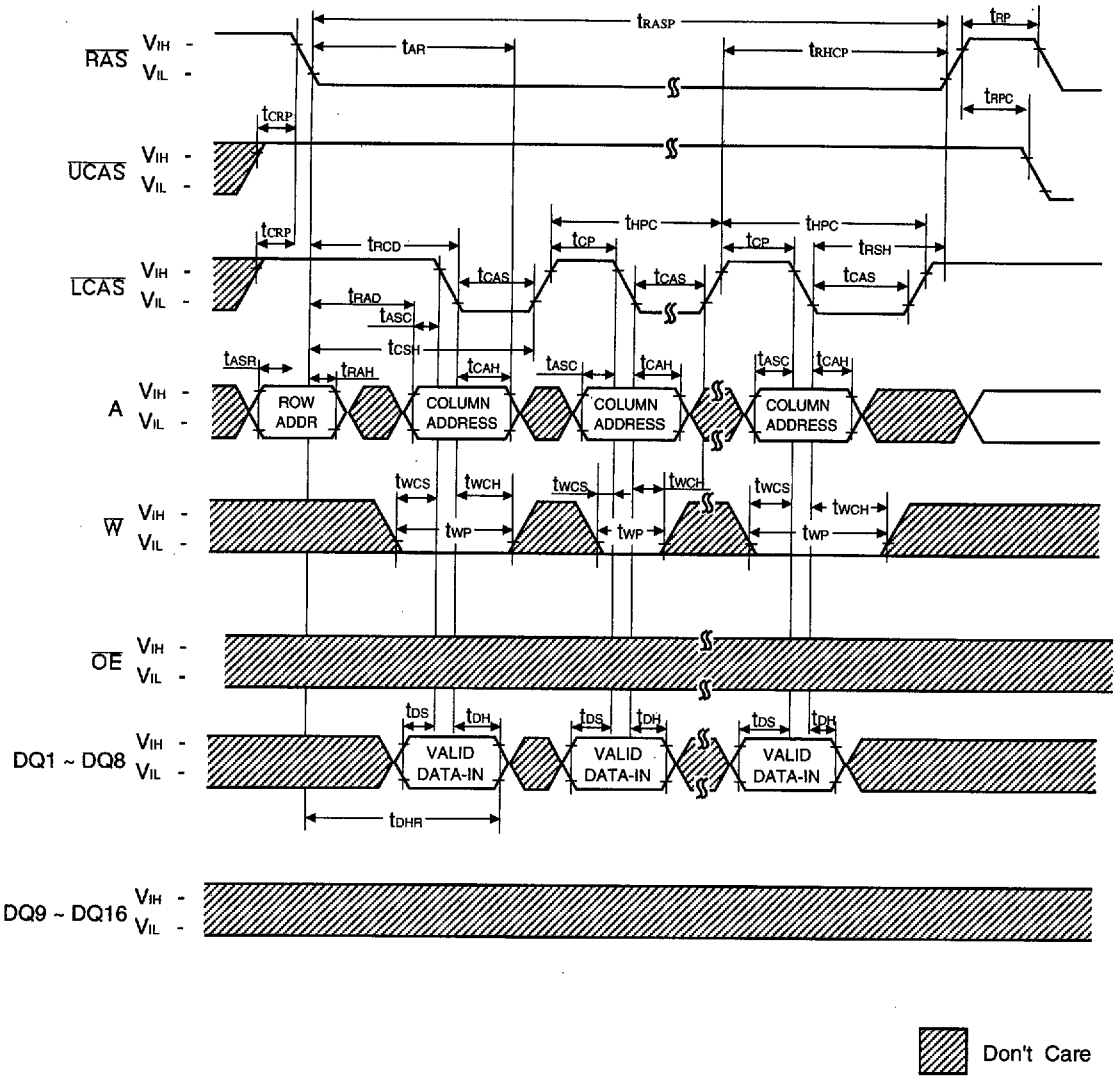
HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



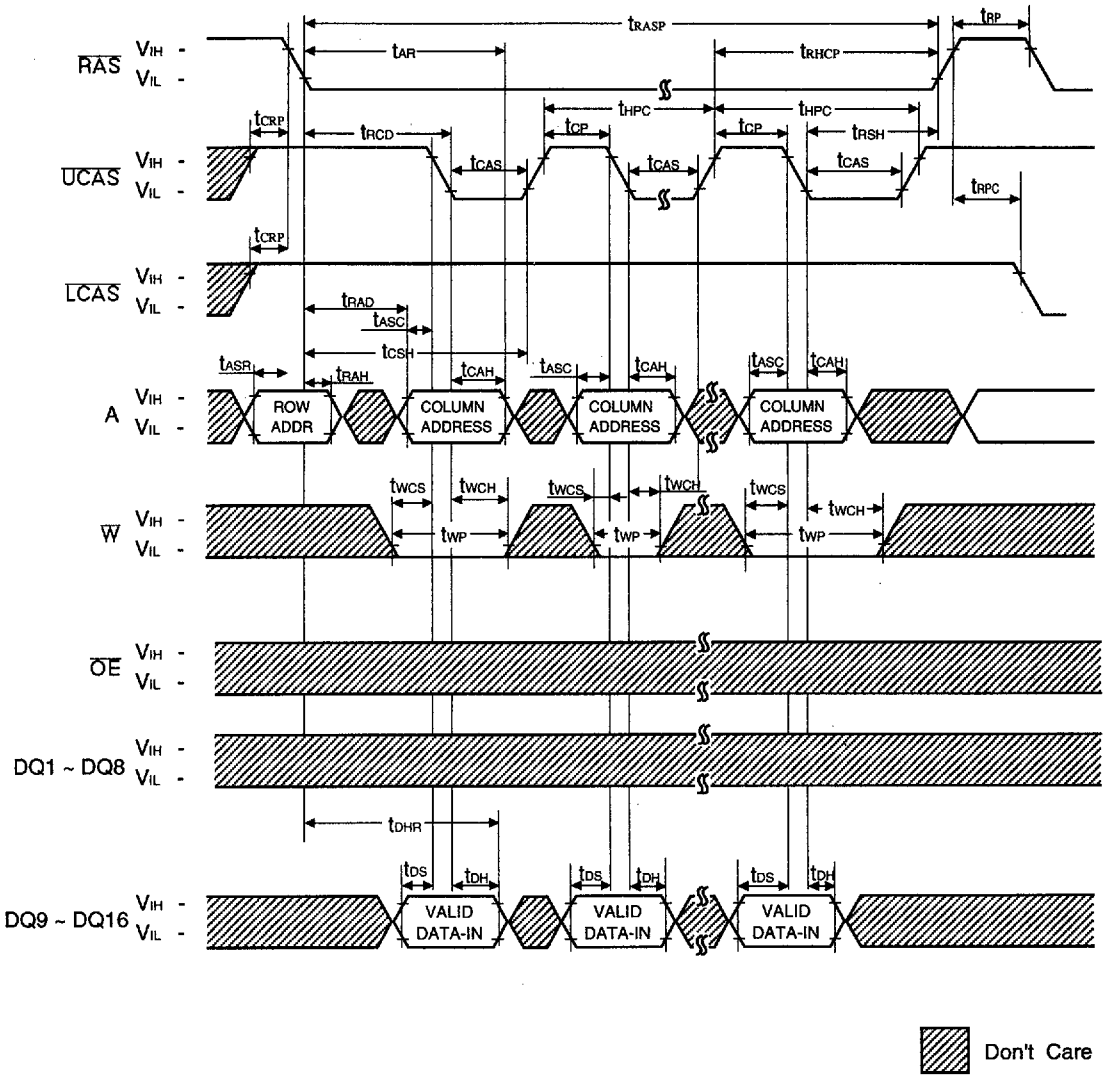
HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open

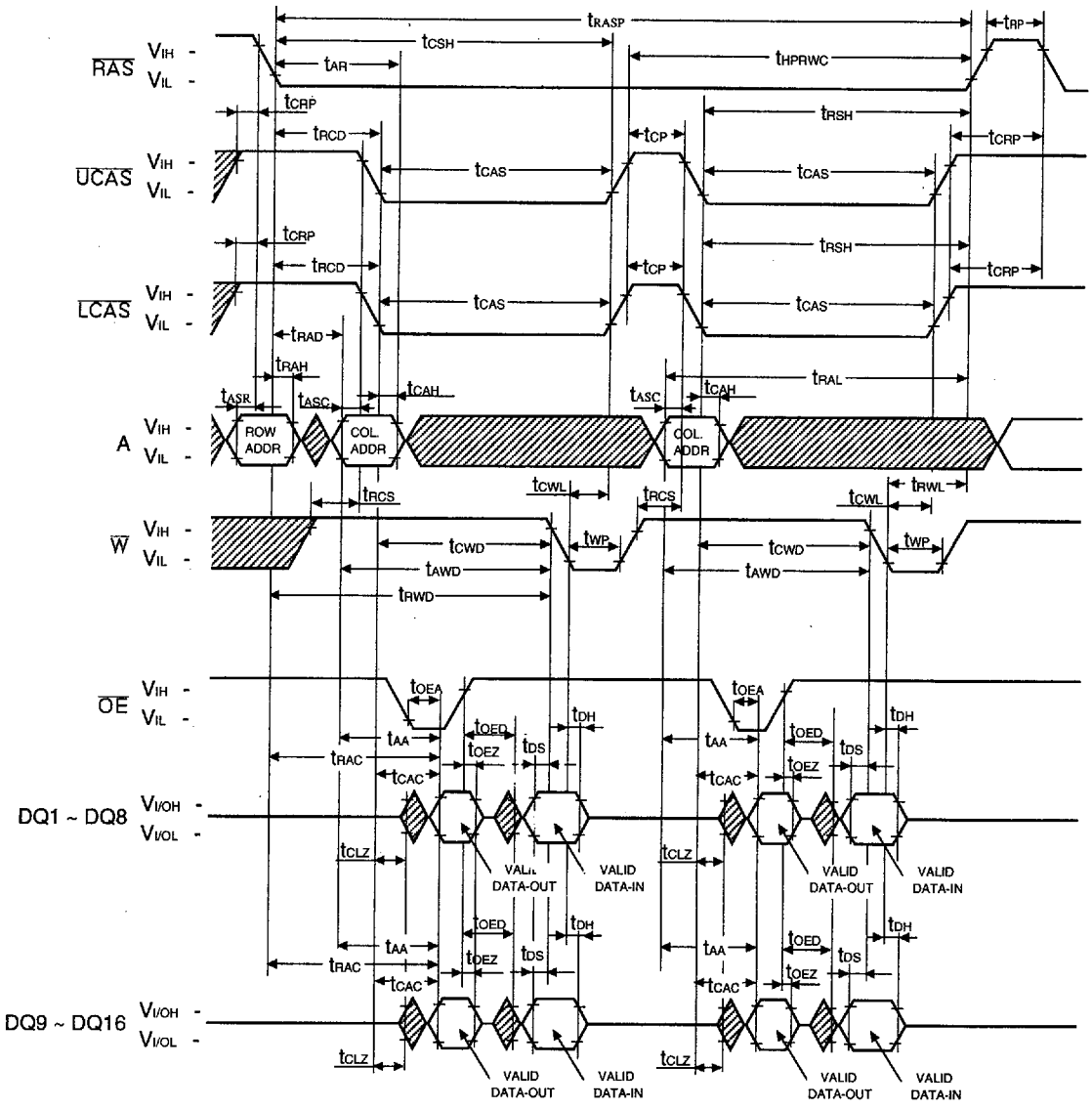


HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

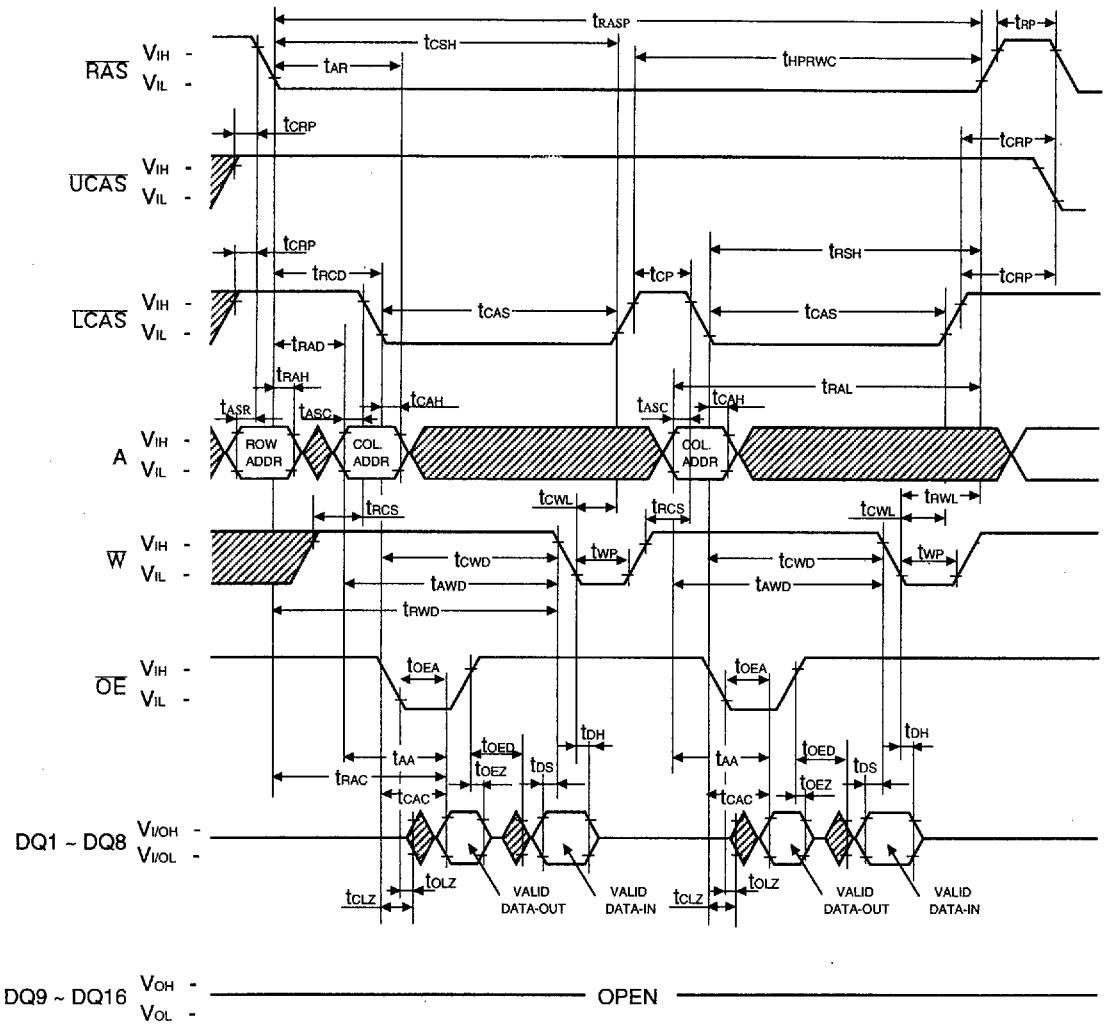
NOTE : D_{OUT} = Open



HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE

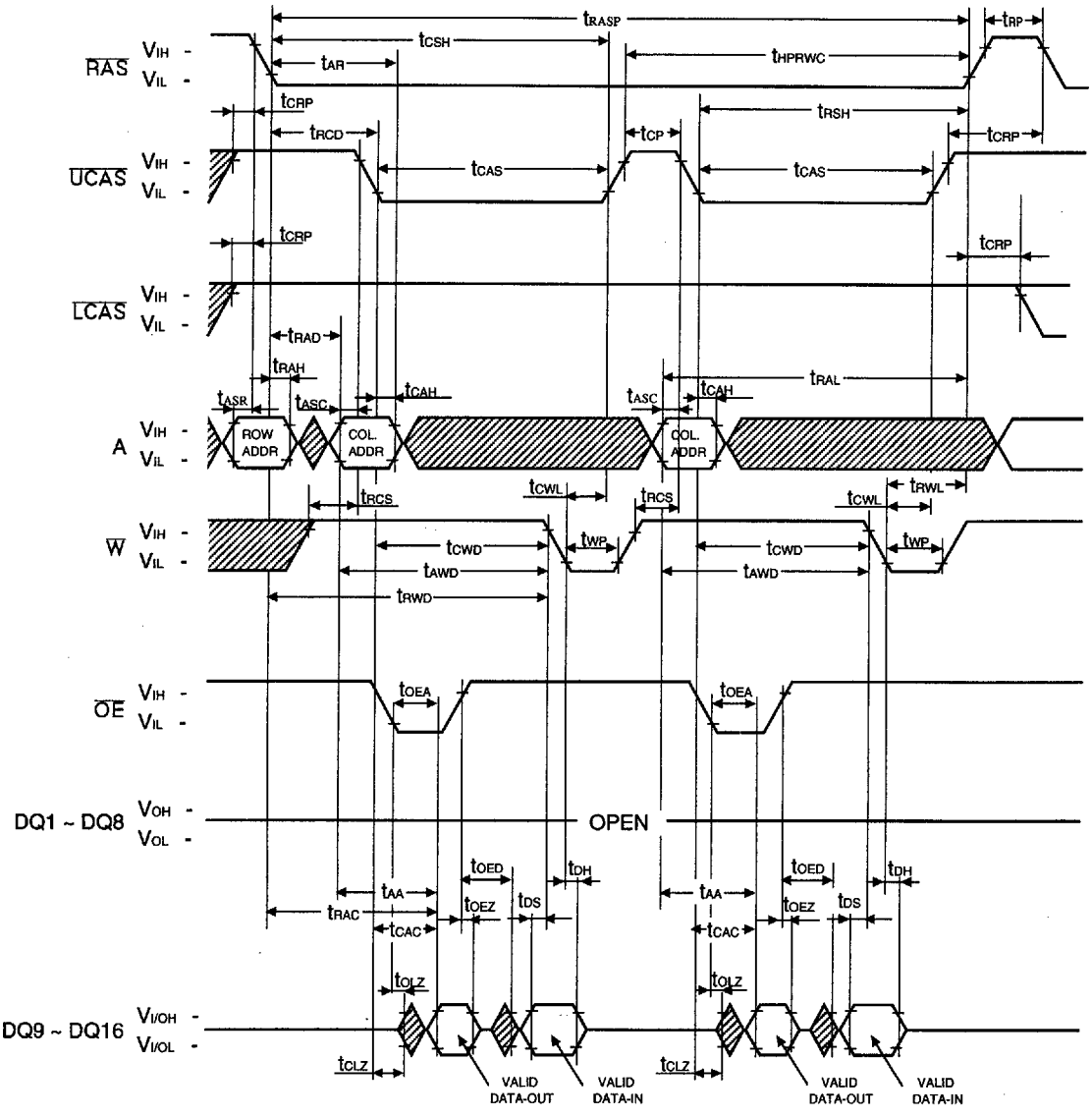


HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



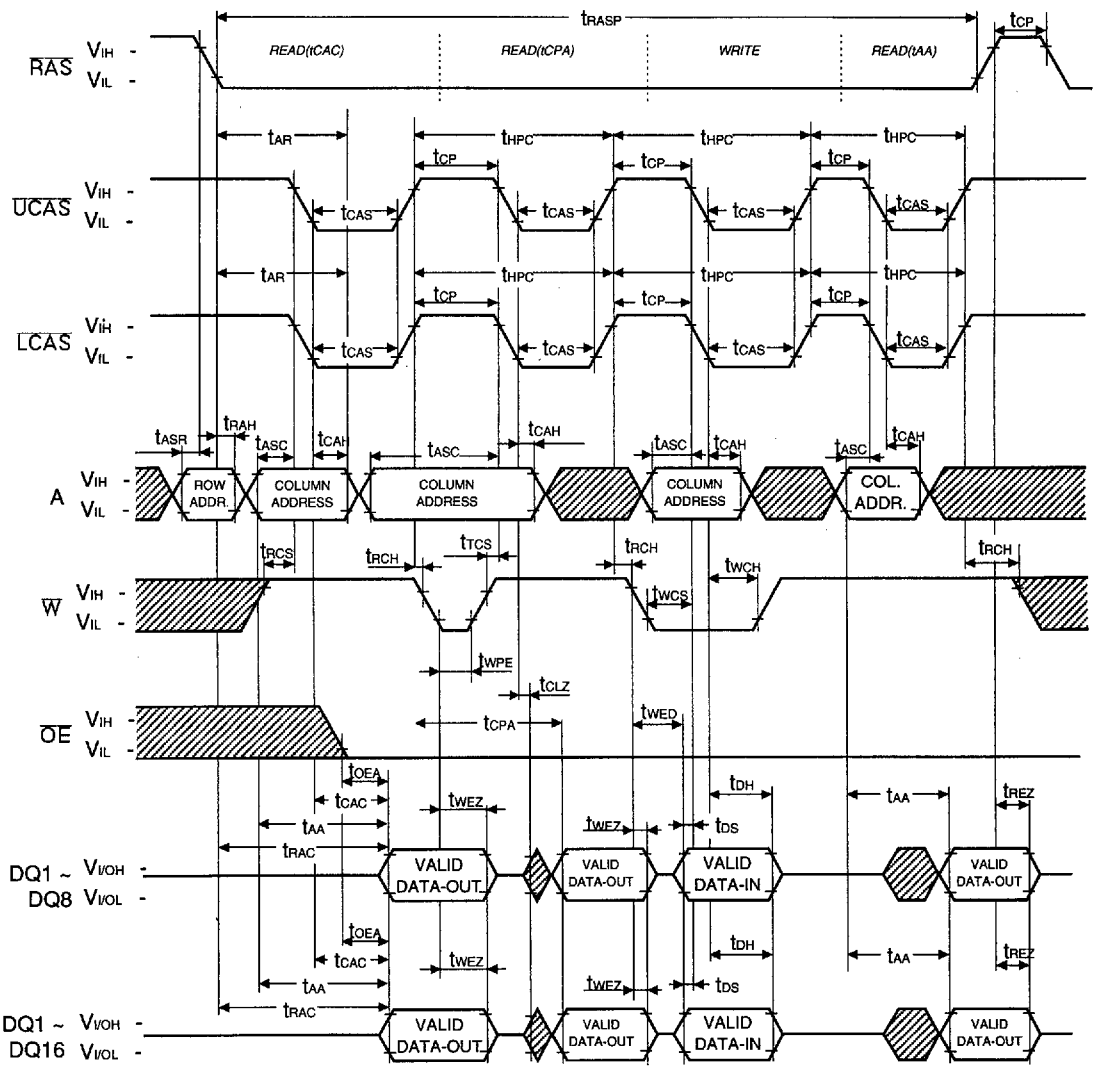
Don't Care

HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



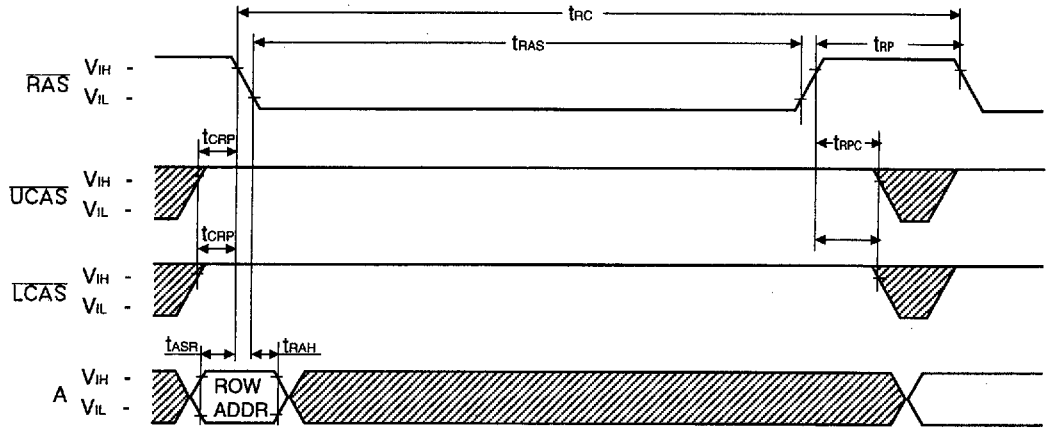
Don't Care

HYPER PAGE READ AND WRITE MIXED CYCLE



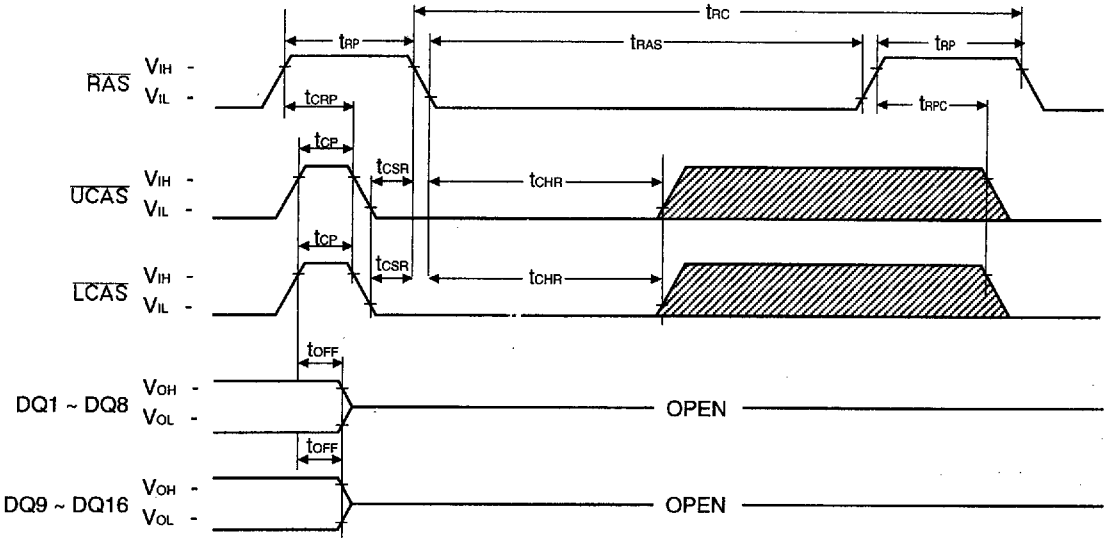
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open



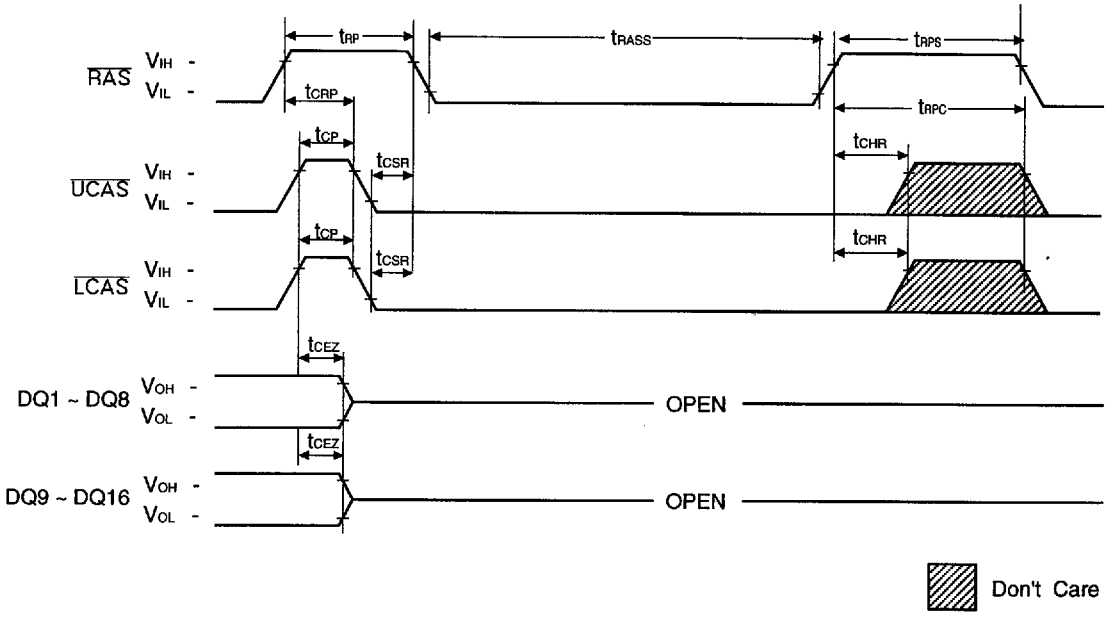
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



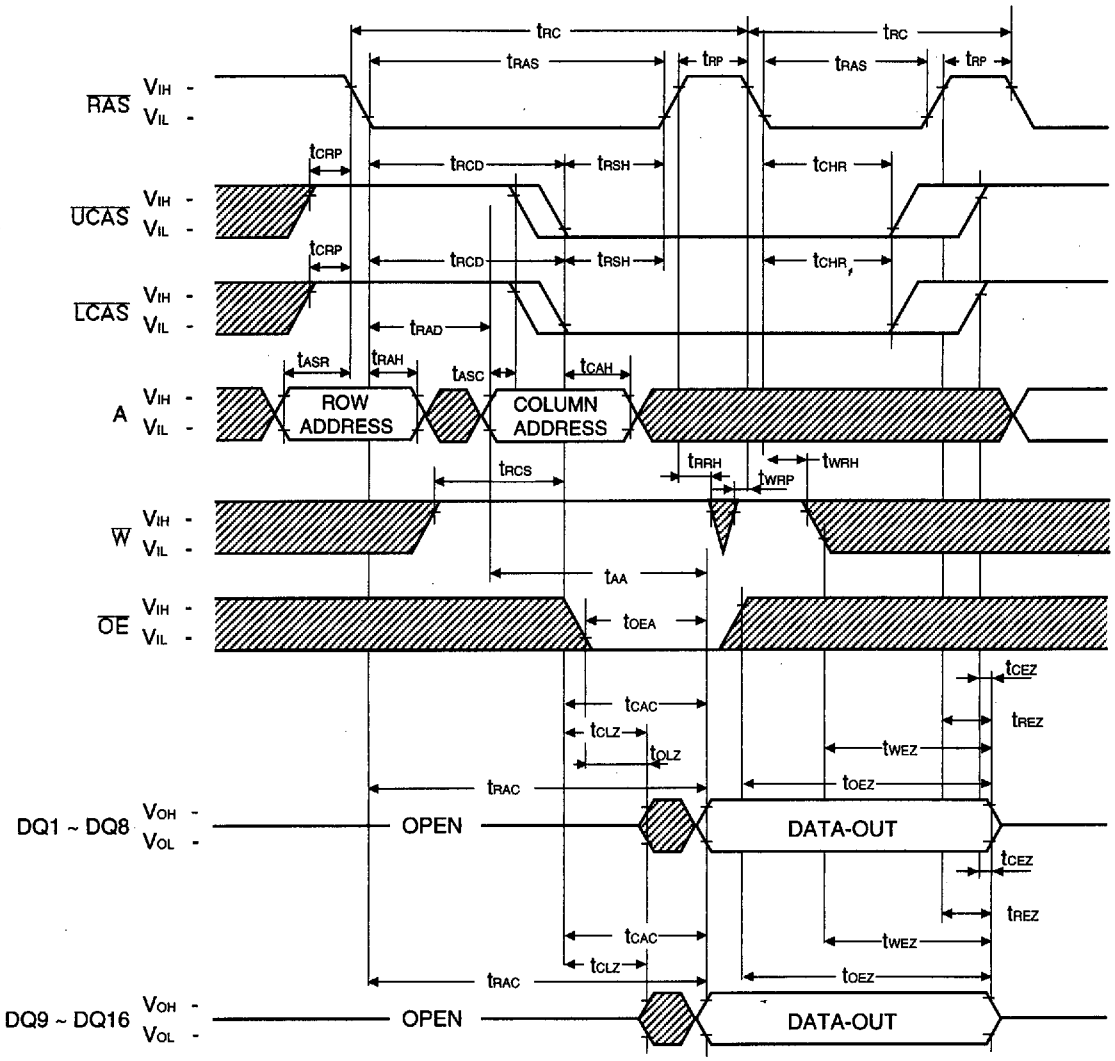
$\overline{CAS}$-BEFORE-$\overline{RAS}$ SELF REFRESH CYCLE(LL-version)

NOTE : $\overline{W}$, $\overline{OE}$, A = Don't Care



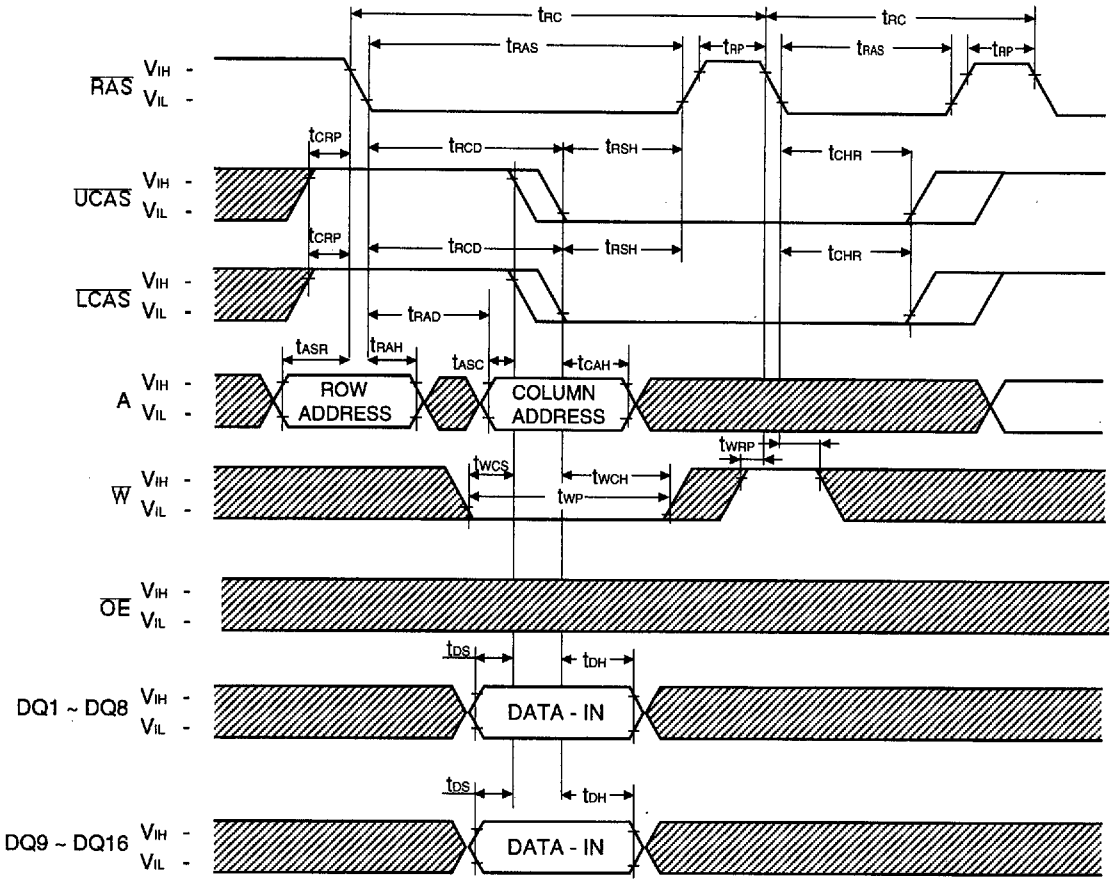
6

HIDDEN REFRESH CYCLE (READ)



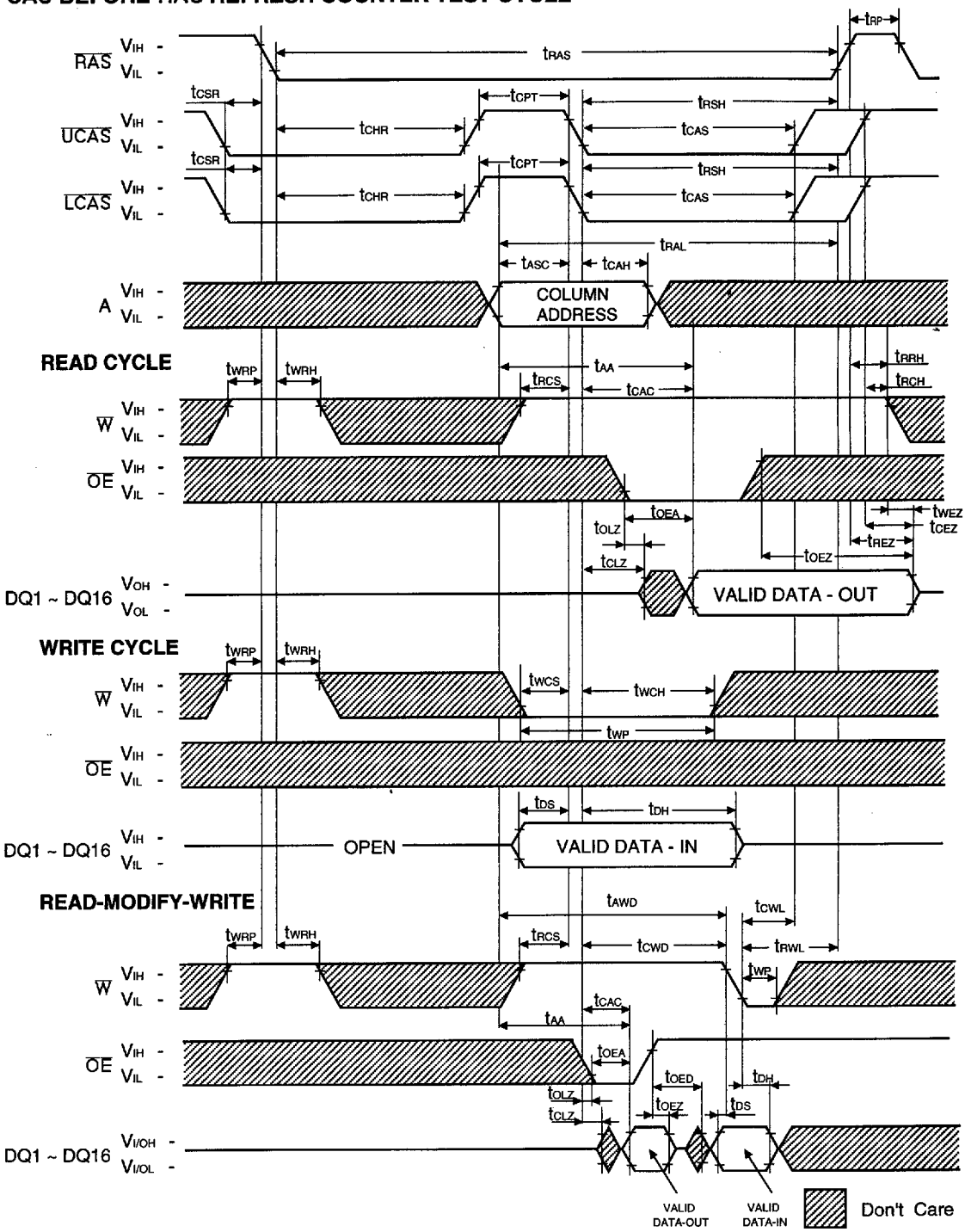
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



Don't Care

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

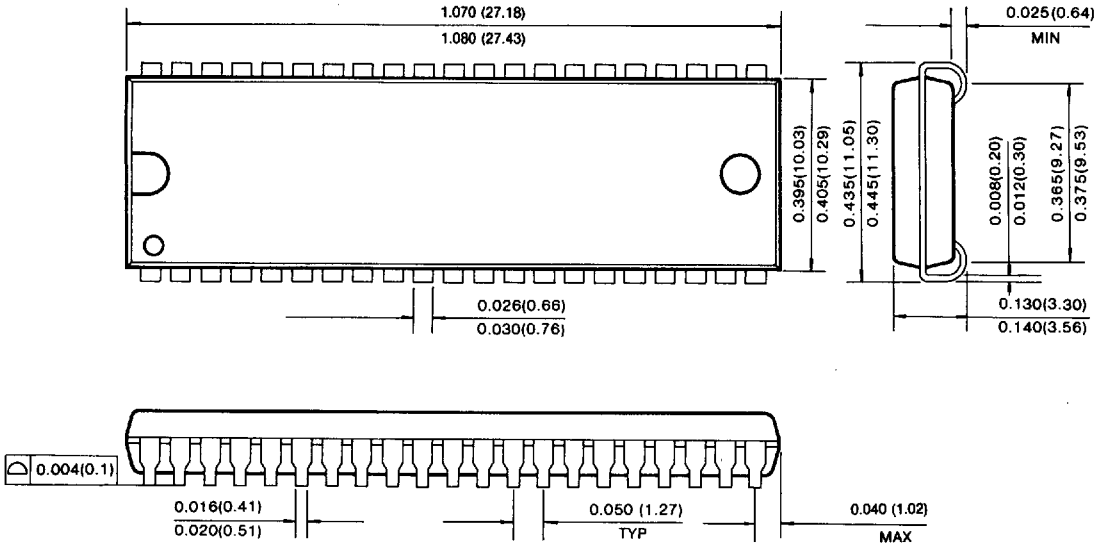


SAMSUNG ELECTRONICS

PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)