

KM416C1004C, KM416C1204C KM416V1004C, KM416V1204C

CMOS DRAM

1M x 16Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 1,048,576 x 16 bit Extended Data Out CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage (+5.0V or +3.3V), refresh cycle (1K Ref. or 4K Ref.), access time (-45, -5 or -6), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 1Mx16 EDO Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

FEATURES

• Part Identification

- KM416C1004C/C-L (5V, 4K Ref.)
- KM416C1204C/C-L (5V, 1K Ref.)
- KM416V1004C/C-L (3.3V, 4K Ref.)
- KM416V1204C/C-L (3.3V, 1K Ref.)

• Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	1K	4K	1K
-45	-	-	550	825
-5	324	504	495	770
-6	288	468	440	715

• Refresh Cycles

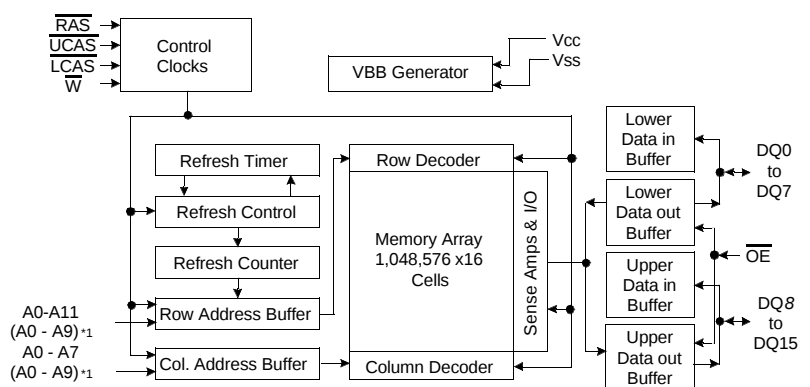
Part NO.	V _{CC}	Refresh cycle	Refresh period	
			Normal	L-ver
C1004C	5V	4K	64ms	128ms
V1004C	3.3V			
C1204C	5V	1K	16ms	
V1204C	3.3V			

• Performance Range

Speed	t _{rac}	t _{cac}	t _{rc}	t _{hpc}	Remark
-45	45ns	13ns	69ns	16ns	5V/3.3V
-5	50ns	15ns	84ns	20ns	5V/3.3V
-6	60ns	17ns	104ns	25ns	5V/3.3V

- Extended Data Out Mode operation (Fast Page Mode with Extended Data Out)
- 2 $\overline{\text{CAS}}$ Byte/Word Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL(5V)/LVTTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in plastic SOJ 400mil and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

FUNCTIONAL BLOCK DIAGRAM

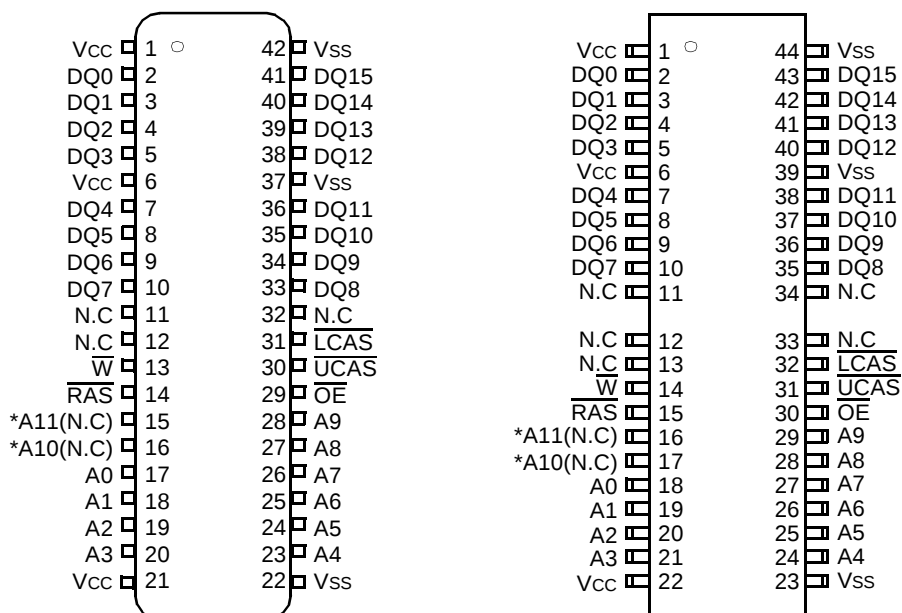


Note) *1 : 1K Refresh

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• KM416C/V10(2)04CT



J : 400mil 42 SOJ
T : 400mil 50(44) TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs (4K Product)
A0 - A9	Address Inputs (1K Product)
DQ0 - 15	Data In/Out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS}}$	Upper Column Address Strobe
$\overline{\text{LCAS}}$	Lower Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+5V)
	Power(+3.3V)
N.C	No Connection

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to +4.6	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to +4.6	-1.0 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	-55 to +150	°C
Power Dissipation	P _D	1	1	W
Short Circuit Output Current	I _{os}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Parameter	Symbol	3.3V			5V			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3*1	2.4	-	V _{CC} +1.0*1	V
Input Low Voltage	V _{IL}	-0.3*2	-	0.8	-1.0*2	-	0.8	V

*1 : V_{CC}+1.3V/15ns(3.3V), V_{CC}+2.0V/20ns(5V), Pulse width is measured at V_{CC}

*2 : -1.3V/15ns(3.3V), -2.0V/20ns(5V), Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Max	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{IN} +0.3V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	uA
	Output High Voltage Level(I _{OH} =-2mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =2mA)	V _{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V _{IN} ≤V _{IN} +0.5V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	uA
	Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	uA
	Output High Voltage Level(I _{OH} =-5mA)	V _{OH}	2.4	-	V
	Output Low Voltage Level(I _{OL} =4.2mA)	V _{OL}	-	0.4	V

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DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max				Units
			KM416V1004C	KM416V1204C	KM416C1004C	KM416C1204C	
I _{CC1}	Don't care	-45	100	150	100	150	mA
		-5	90	140	90	140	mA
		-6	80	130	80	130	mA
I _{CC2}	Normal L	Don't care	1	1	2	2	mA
			1	1	1	1	mA
I _{CC3}	Don't care	-45	100	150	100	150	mA
		-5	90	140	90	140	mA
		-6	80	130	80	130	mA
I _{CC4}	Don't care	-45	110	110	110	110	mA
		-5	100	100	100	100	mA
		-6	90	90	90	90	mA
I _{CC5}	Normal L	Don't care	0.5	0.5	1	1	mA
			200	200	200	200	uA
I _{CC6}	Don't care	-45	100	150	110	150	mA
		-5	90	140	90	140	mA
		-6	80	130	80	130	mA
I _{CC7}	L	Don't care	300	200	350	250	uA
I _{CCS}	L	Don't care	150	150	200	200	uA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{IH}$)

I_{CC3}* : $\overline{RAS}$ -only Refresh Current ($\overline{UCAS}=\overline{LCAS}=V_{IH}$, $\overline{RAS}$, Address cycling @t_{RC}=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}=V_{IL}$, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @t_{HPC}=min.)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6}* : $\overline{CAS}$ -Before- $\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @t_{RC}=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$, $\overline{LCAS}$ =0.2V,

DQ=Don't care, T_{RC}=31.25us(4K/L-ver), 125us(1K/L-ver)

T_{RA}S=T_{RA}Smin~300ns

I_{CCS} : Self Refresh Current

$\overline{RAS}=\overline{UCAS}=\overline{LCAS}=V_{IL}$, $\overline{W}=\overline{OE}=A_0 \sim A_{11}=V_{CC}-0.2V$ or 0.2V,

DQ0 ~ DQ15=V_{CC}-0.2V, 0.2V or Open

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one Hyper page mode cycle time, t_{HPC}.

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CAPACITANCE (TA=25°C, VCC=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A11]	CIN1	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ15]	CDQ	-	7	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, See note 1,2)

Test condition (5V device) : VCC=5.0V±10%, VIH/VIL=2.4/0.8V, VOH/VOL=2.0/0.8V

Test condition (3.3V device) : VCC=3.3V±0.3V, VIH/VIL=2.2/0.7V, VOH/VOL=2.0/0.8V

Parameter	Symbol	-45		-5		-6		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	79		84		104		ns	
Read-modify-write cycle time	tRWC	105		115		140		ns	
Access time from $\overline{\text{RAS}}$	tRAC		45		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		14		15		17	ns	3,4,5
Access time from column address	tAA		23		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	3		3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	tCEZ	3	13	3	13	3	15	ns	6,19
$\overline{\text{OE}}$ to output in Low-Z	tOLZ	3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	45	10K	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		13		17		ns	
$\overline{\text{CAS}}$ hold time	tCSH	36		40		50		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	7	10K	8	10K	10	10K	ns	18
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	19	31	20	35	20	43	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	14	22	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	9		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	11
Column address hold time	tCAH	7		8		10		ns	11
Column address to $\overline{\text{RAS}}$ lead time	tRAL	23		25		30		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	8
Write command hold time	tWCH	8		10		10		ns	
Write command pulse width	tWP	8		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	10		13		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	7		8		10		ns	14

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-45		-5		-6		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	t _{DS}	0		0		0		ns	9,17
Data hold time	t _{DH}	7		8		10		ns	9,17
Refresh period (1K, Normal)	t _{REF}		16		16		16	ms	
Refresh period (4K, Normal)	t _{REF}		64		64		64	ms	
Refresh period (L-ver)	t _{REF}		128		128		128	ms	
Write command set-up time	t _{WCS}	0		0		0		ns	7
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t _{CWD}	28		32		36		ns	7,13
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t _{RWD}	59		67		79		ns	7
Column address $\overline{\text{W}}$ delay time	t _{AWD}	37		42		49		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	t _{CPWD}	39		47		54		ns	7
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CSR}	5		5		5		ns	15
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CHR}	10		10		10		ns	16
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t _{RPC}	5		5		5		ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		25		28		35	ns	3
Hyper Page mode cycle time	t _{HPC}	18		20		25		ns	18
Hyper Page read-modify-write cycle time	t _{HPRWC}	39		47		56		ns	18
$\overline{\text{CAS}}$ precharge time (Hyper Page cycle)	t _{CP}	7		8		10		ns	12
$\overline{\text{RAS}}$ pulse width (Hyper Page cycle)	t _{RASP}	45	200K	50	200K	60	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	27		30		35		ns	
$\overline{\text{OE}}$ access time	t _{OEA}		13		13		15	ns	3
$\overline{\text{OE}}$ to data delay	t _{OED}	10		13		15		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	t _{OEZ}	3	13	3	13	3	15	ns	6
$\overline{\text{OE}}$ command hold time	t _{OEH}	10		13		15		ns	
Output data hold time	t _{DOH}	4		5		5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	t _{REZ}	3	13	3	13	3	15	ns	6,19
Output buffer turn off delay from $\overline{\text{W}}$	t _{WEZ}	3	13	3	13	3	15	ns	6
$\overline{\text{W}}$ to data delay	t _{WED}	15		15		15		ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	t _{OCH}	5		5		5		ns	
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	t _{CHO}	5		5		5		ns	
$\overline{\text{OE}}$ precharge time	t _{OEP}	5		5		5		ns	
$\overline{\text{W}}$ pulse width (Hyper Page Cycle)	t _{WPE}	5		5		5		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	t _{RASS}	100		100		100		us	20,21,22
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	t _{RPS}	79		90		110		ns	20,21,22
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	t _{CHS}	-50		-50		-50		ns	20,21,22

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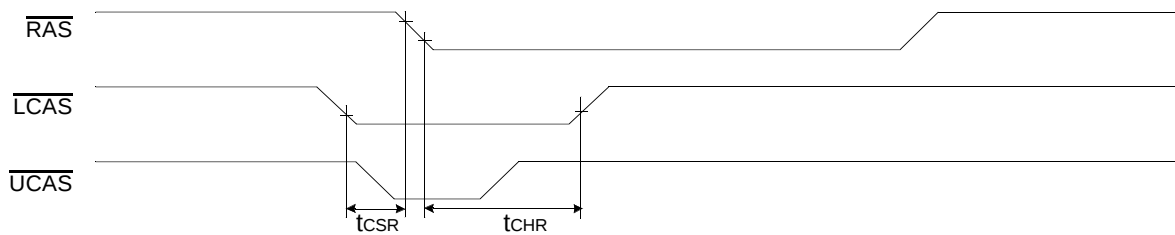
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{IH}/V_{IL} . $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V)/1TTL(3.3V) loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{W}}$ falling edge in $\overline{\text{OE}}$ controlled write cycle and read-modify-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .

KM416C/V10(2)04C/C-L Truth Table

$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	DQ0 - DQ7	DQ8-DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

11. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.
12. t_{CP} is specified from the later $\overline{CAS}$ rising edge in the previous cycle to the earlier $\overline{CAS}$ falling edge in the next cycle.
13. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
14. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
15. t_{CSR} is referenced to the earlier $\overline{CAS}$ falling edge before $\overline{RAS}$ transition low.
16. t_{CHR} is referenced to the later $\overline{CAS}$ rising edge after $\overline{RAS}$ transition low.

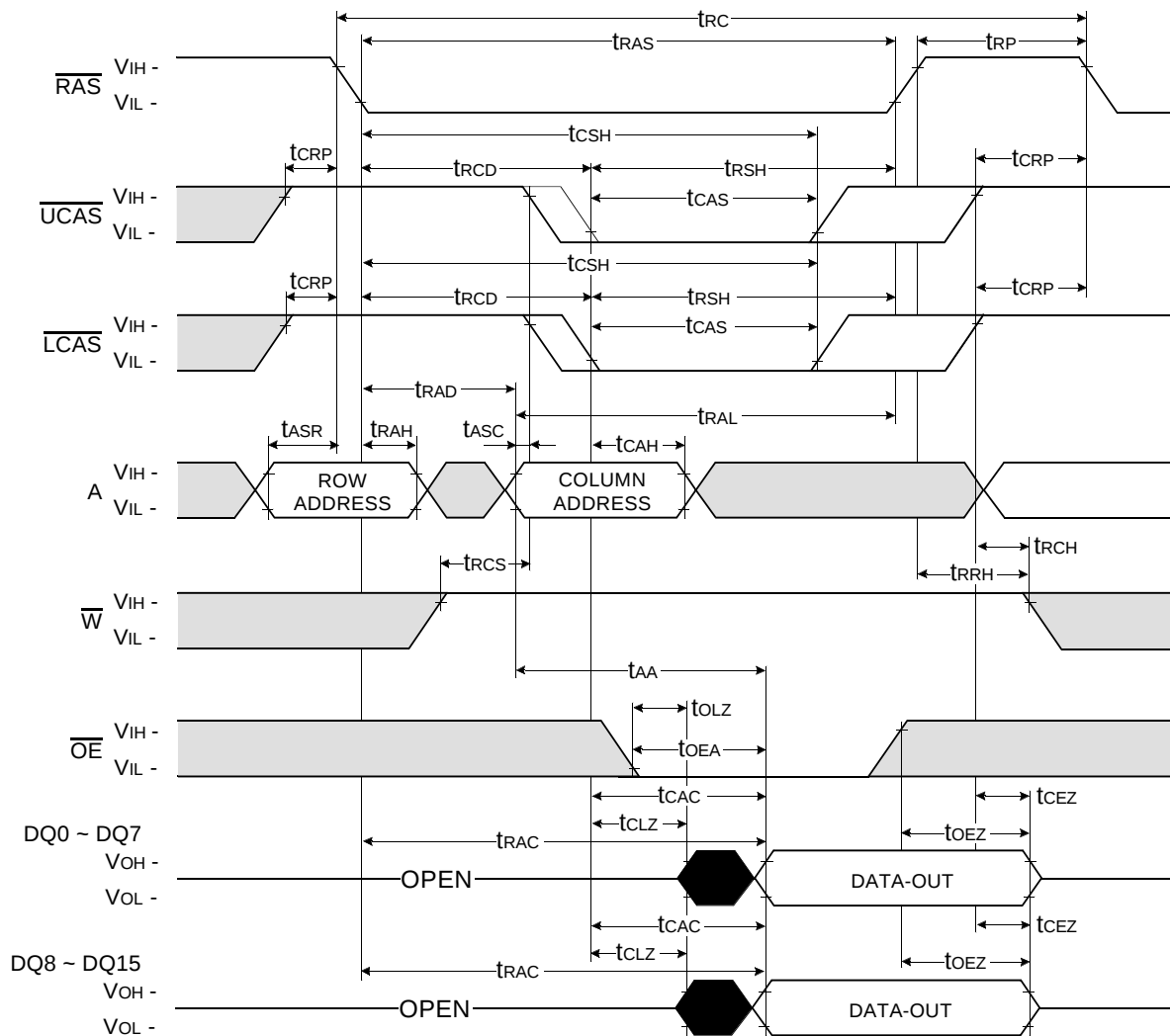


17. t_{DS} , t_{DH} is independently specified for lower byte DQ(0-7), upper byte DQ(8-15)
18. $t_{ASC} \geq 6ns$, assume $t_r = 2.0ns$.
19. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going.
 If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
20. If $t_{RASS} \geq 100\mu s$, then $\overline{RAS}$ precharge time must use t_{RPS} instead of t_{RP} .
21. For $\overline{RAS}$ -only refresh and burst $\overline{CAS}$ -before- $\overline{RAS}$ refresh mode, 4096(4K)/1024(1K) cycles of burst refresh must be executed within 64ms/16ms before and after self refresh, in order to meet refresh specification.
22. For distributed $\overline{CAS}$ -before- $\overline{RAS}$ with 15.6 μs interval, $\overline{CAS}$ -before- $\overline{RAS}$ refresh should be executed with in 15.6 μs immediately before and after self refresh in order to meet refresh specification.

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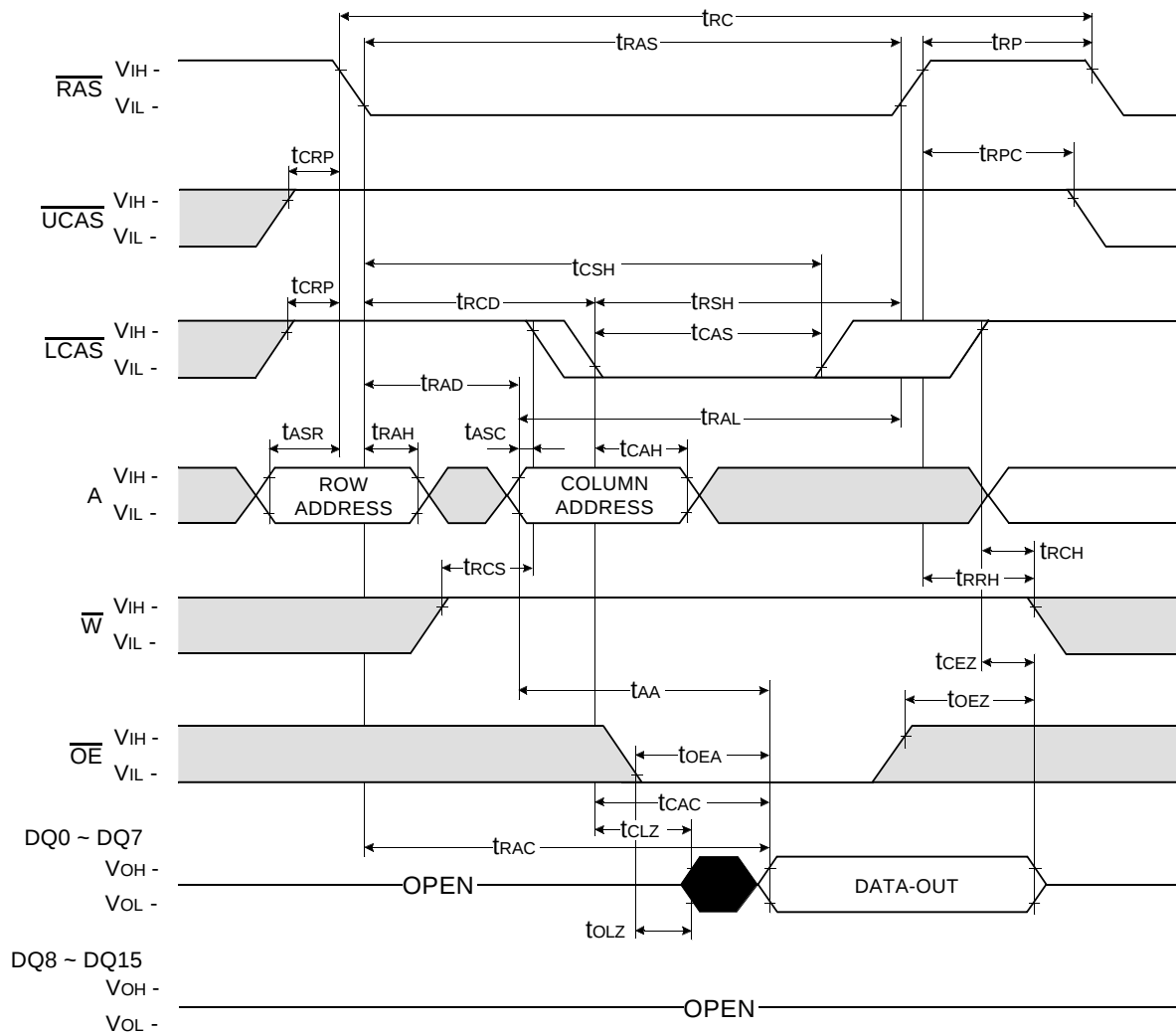
WORD READ CYCLE



Don't care
 Undefined

LOWER BYTE READ CYCLE

NOTE : DIN = OPEN

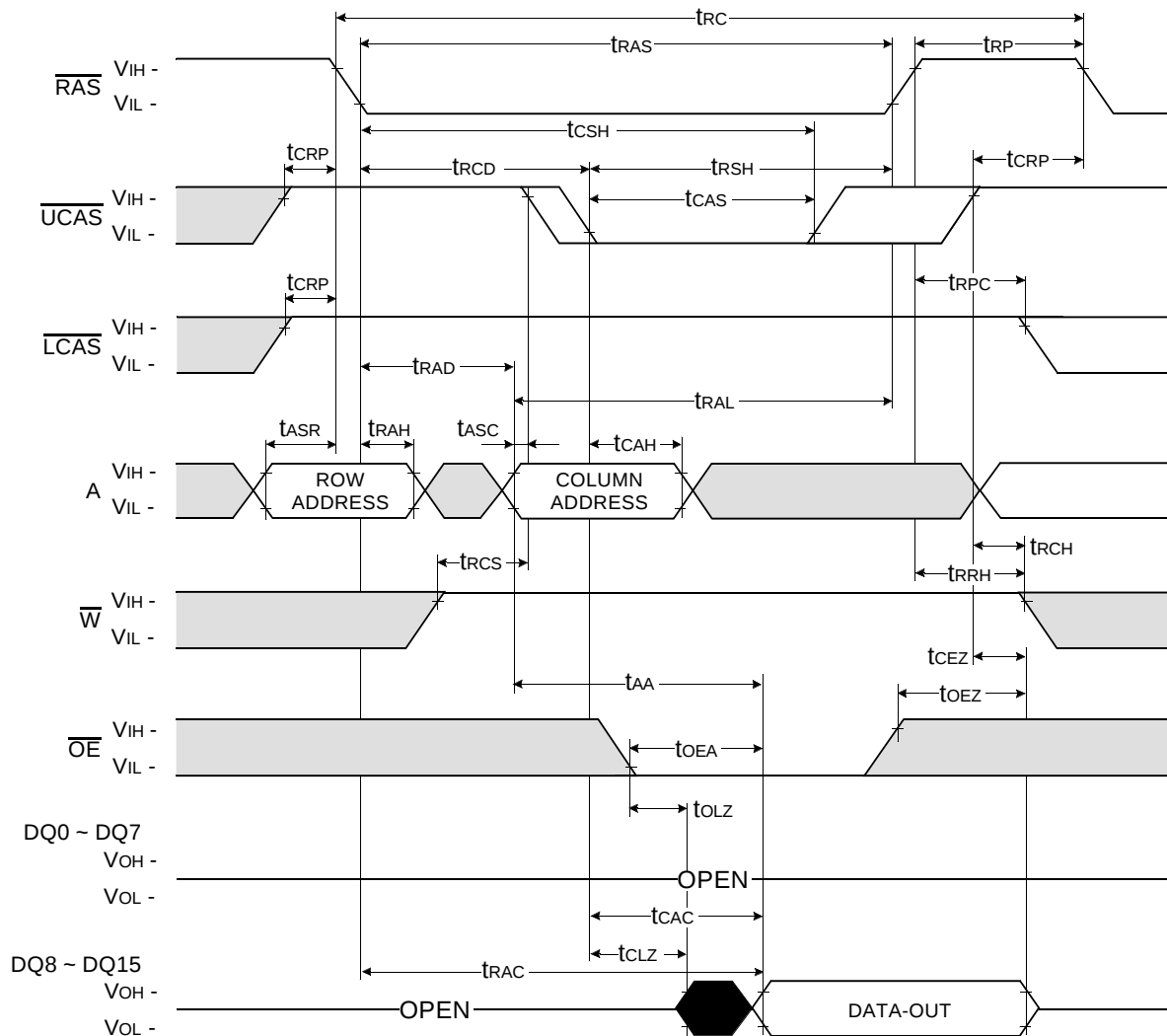


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UPPER BYTE READ CYCLE

NOTE : DIN = OPEN

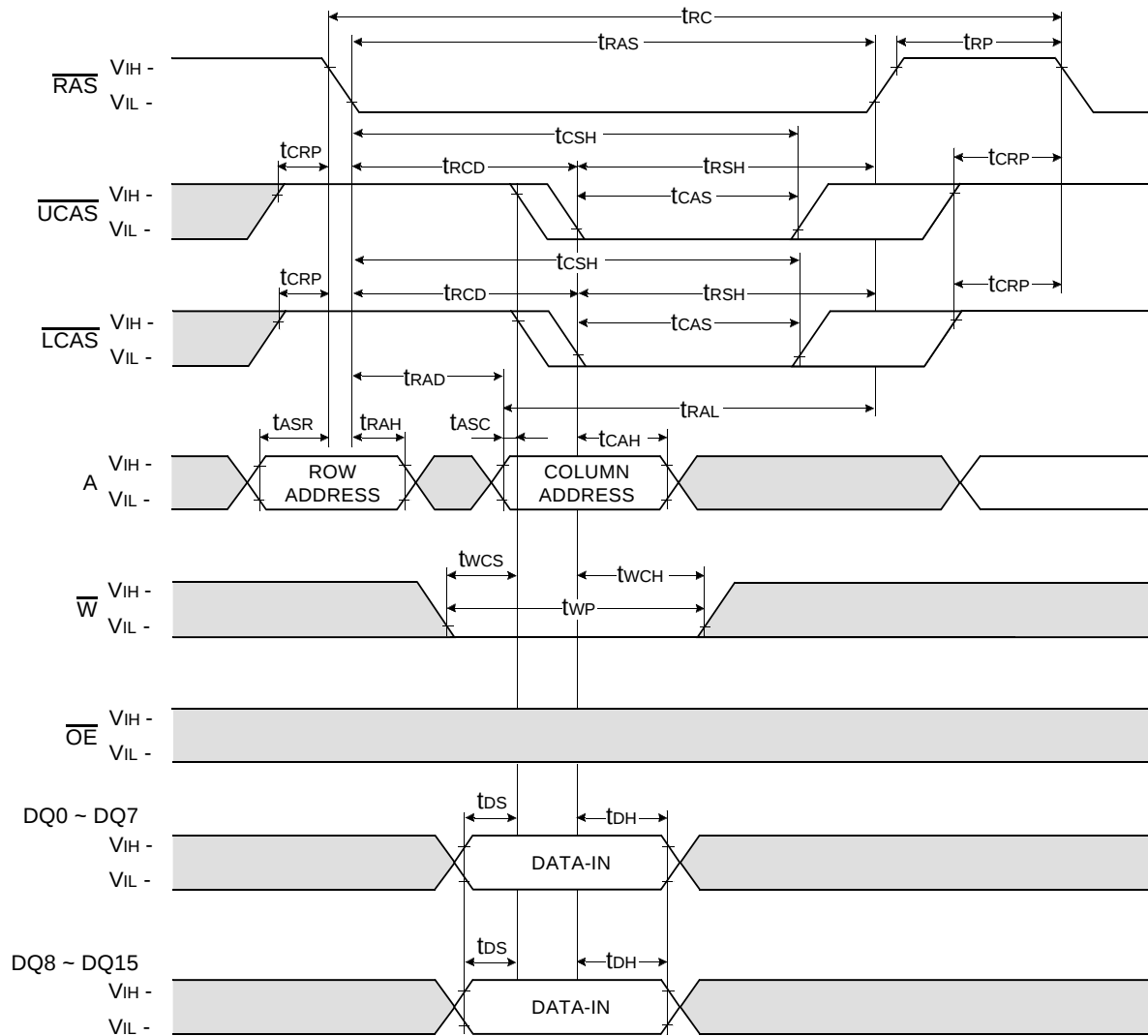


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WORD WRITE CYCLE (EARLY WRITE)

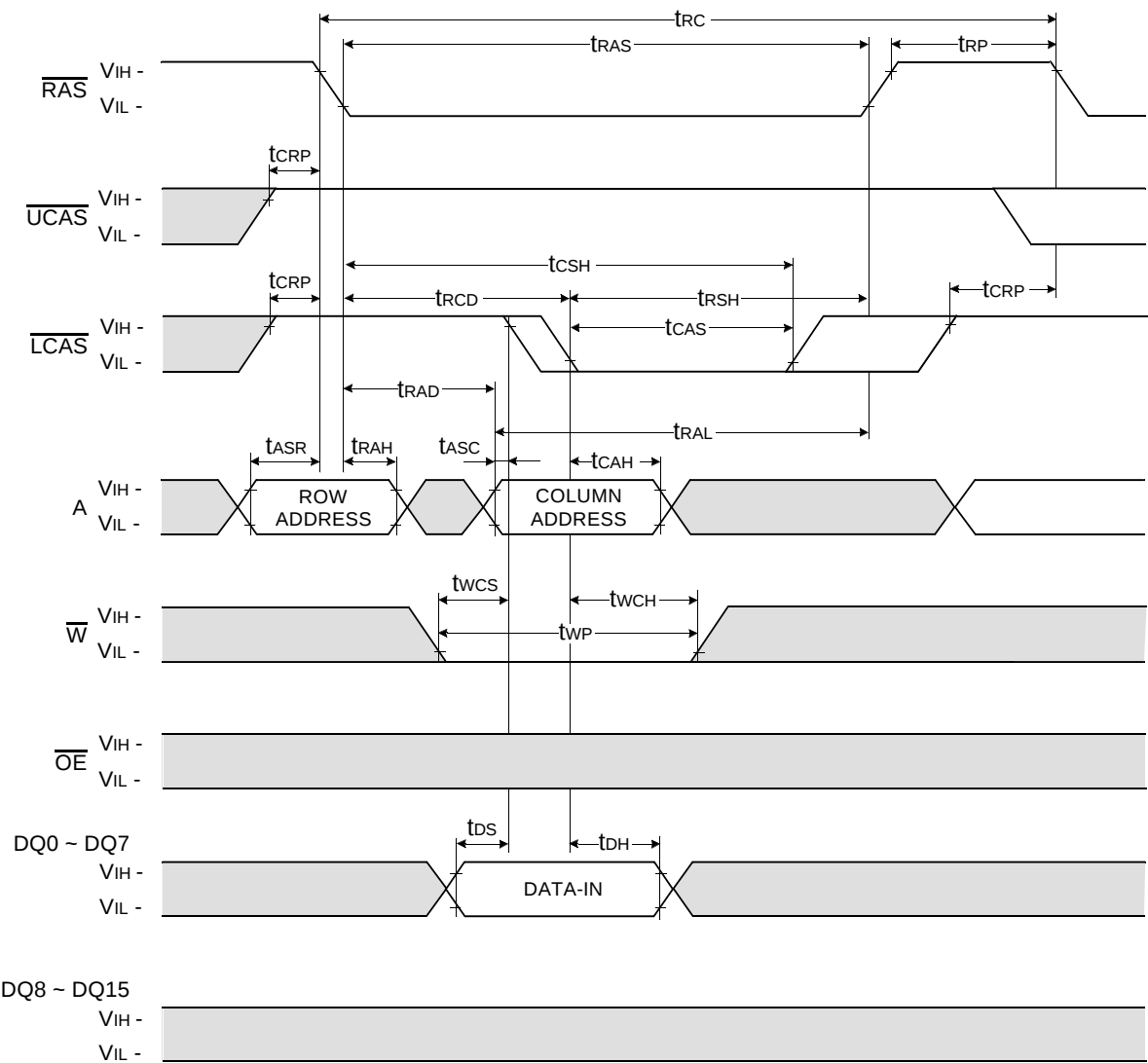
NOTE : DoUT = OPEN



Don't care
Undefined

LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



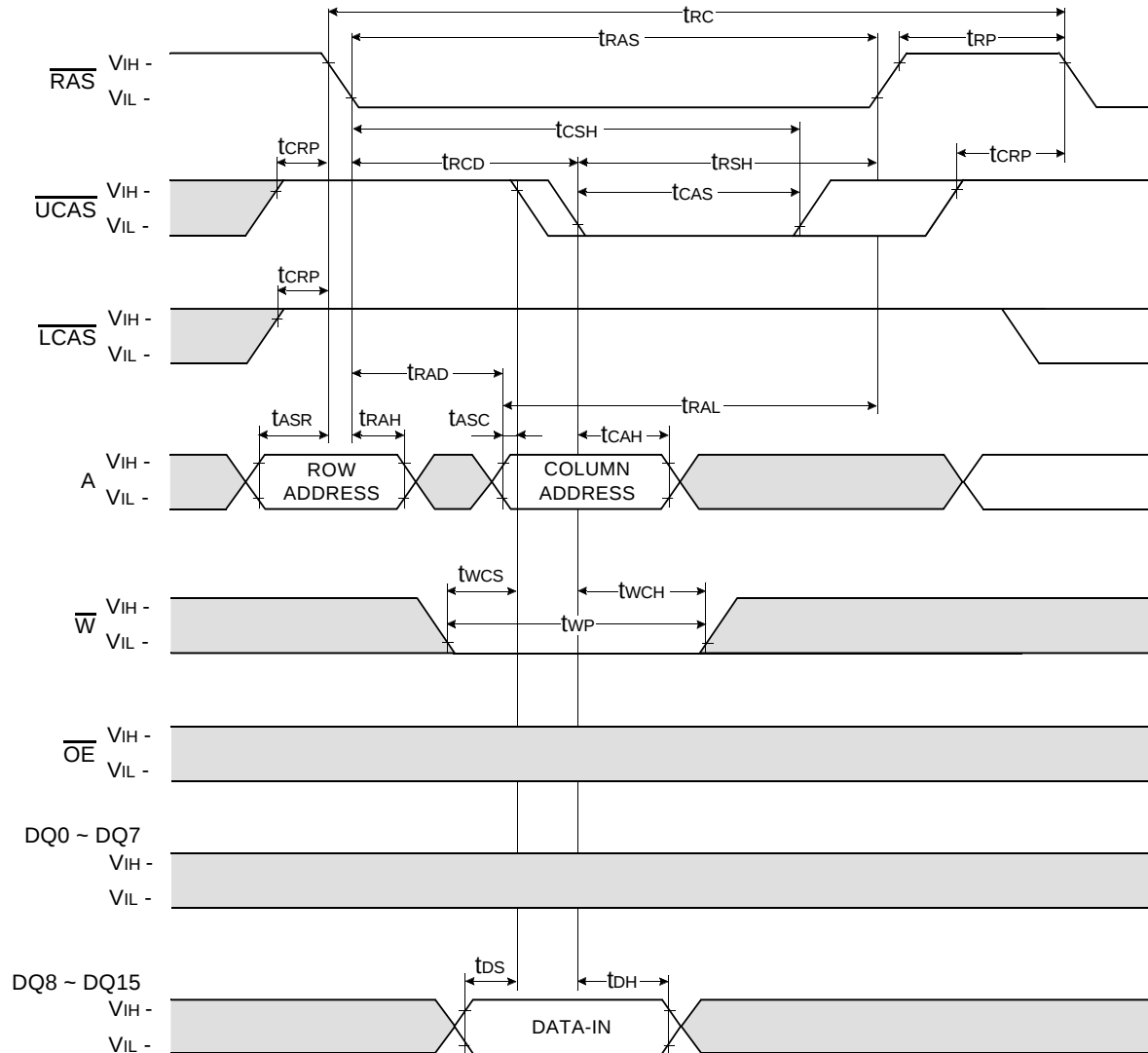
Don't care
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UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



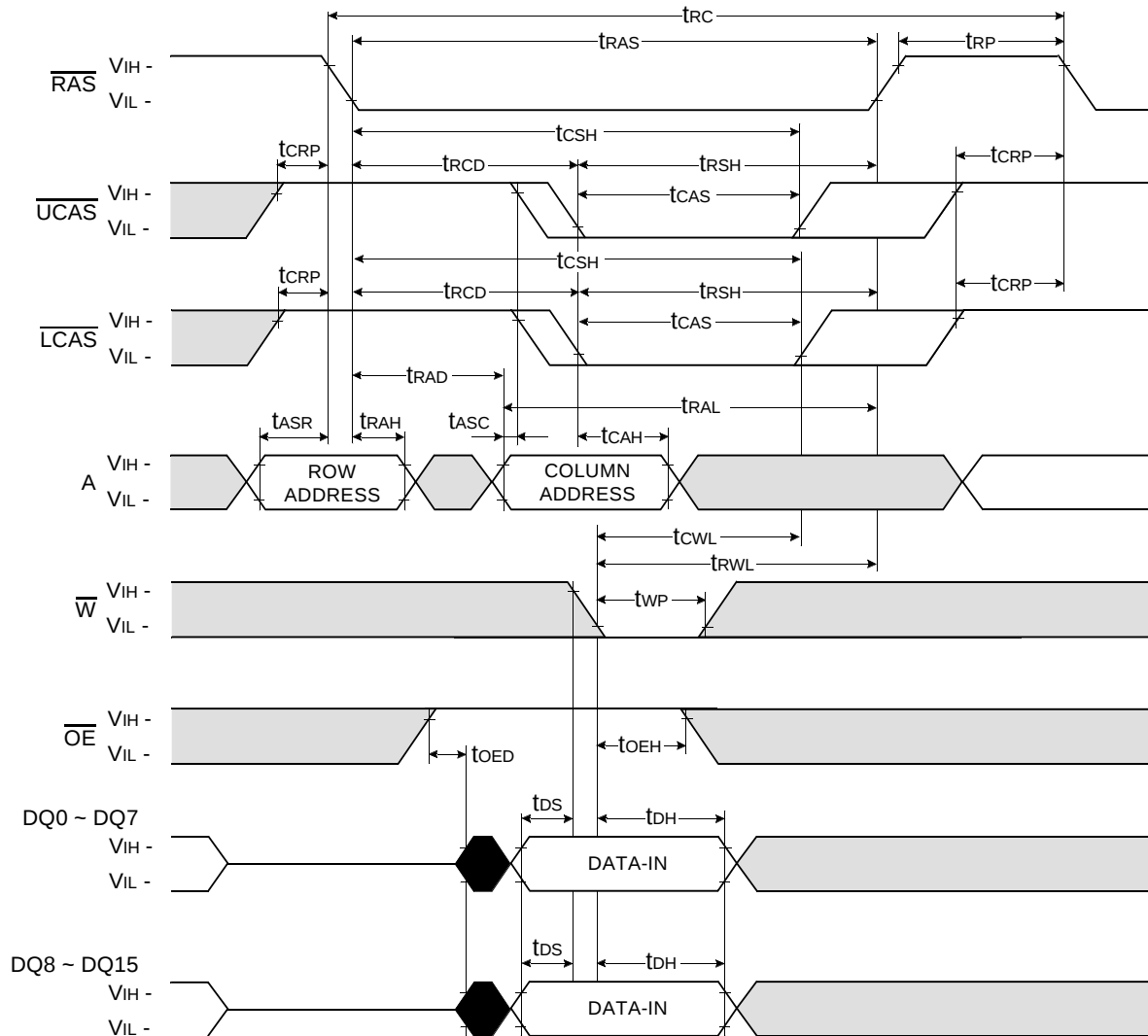
Don't care
Undefined

KM416C1004C, KM416C1204C KM416V1004C, KM416V1204C

CMOS DRAM

WORD WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

NOTE : DoUT = OPEN



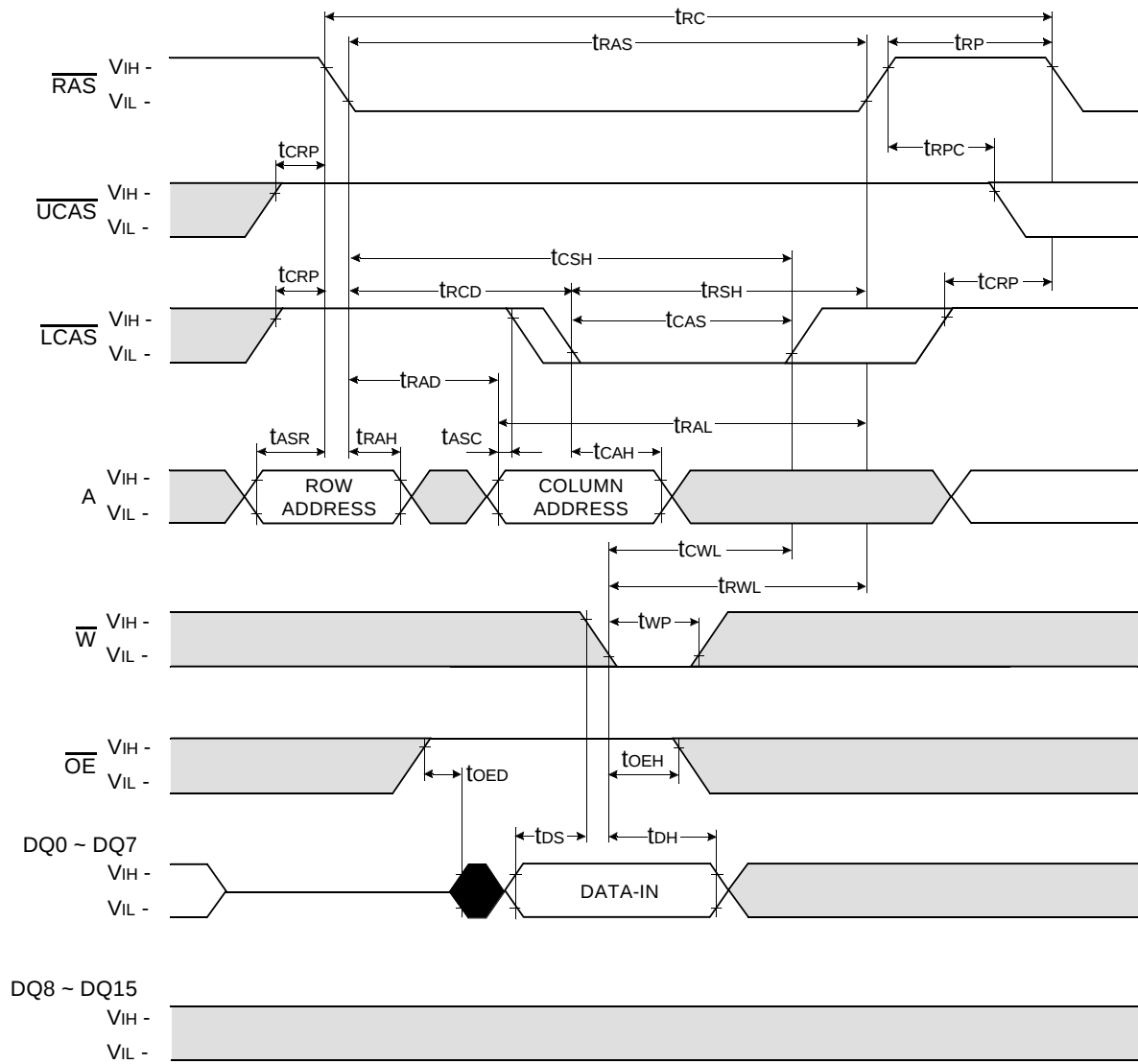
Don't care
Undefined

KM416C1004C, KM416C1204C KM416V1004C, KM416V1204C

CMOS DRAM

LOWER BYTE WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

NOTE : DoUT = OPEN



Don't care

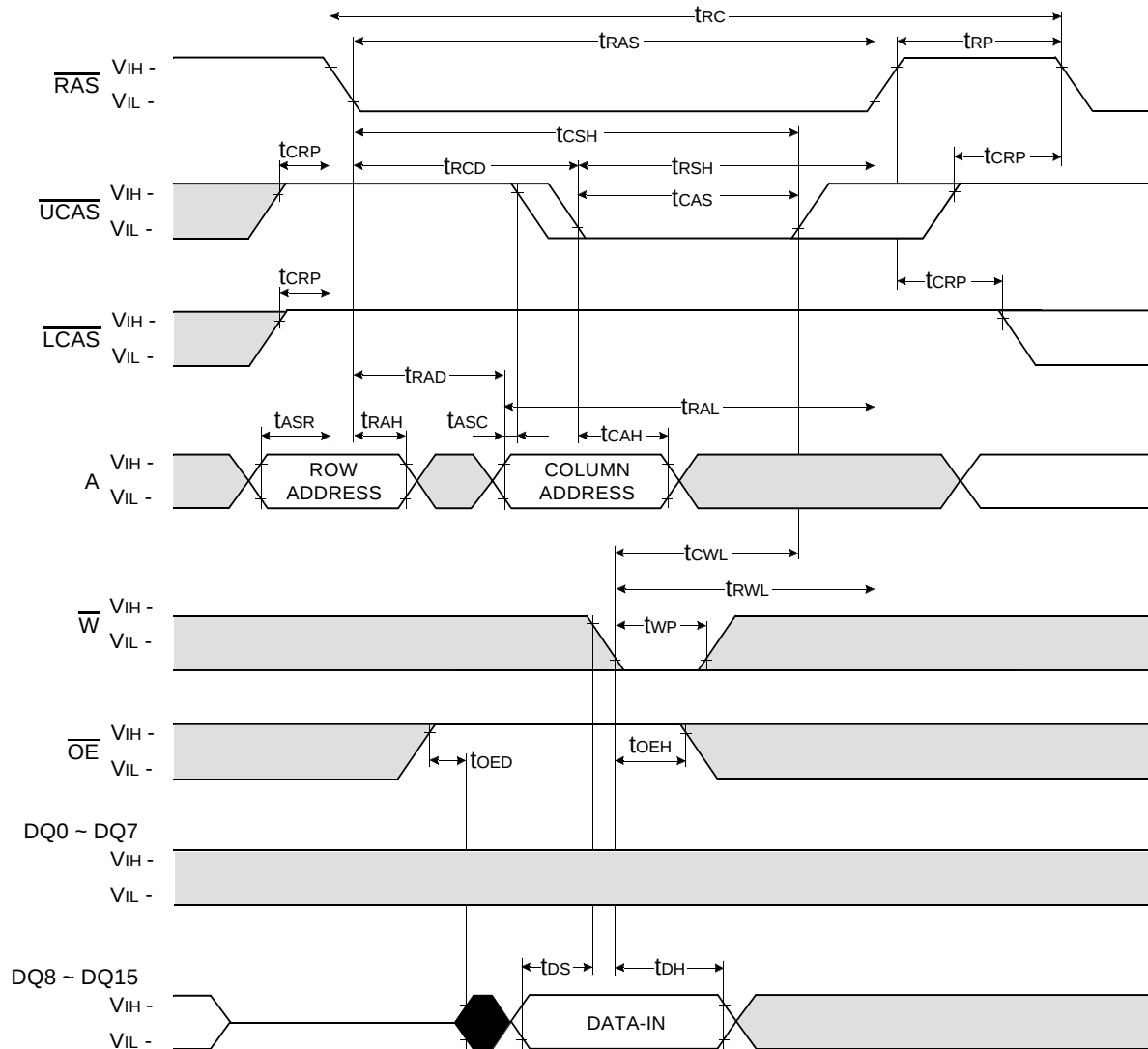
Undefined

KM416C1004C, KM416C1204C KM416V1004C, KM416V1204C

CMOS DRAM

UPPER BYTE WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

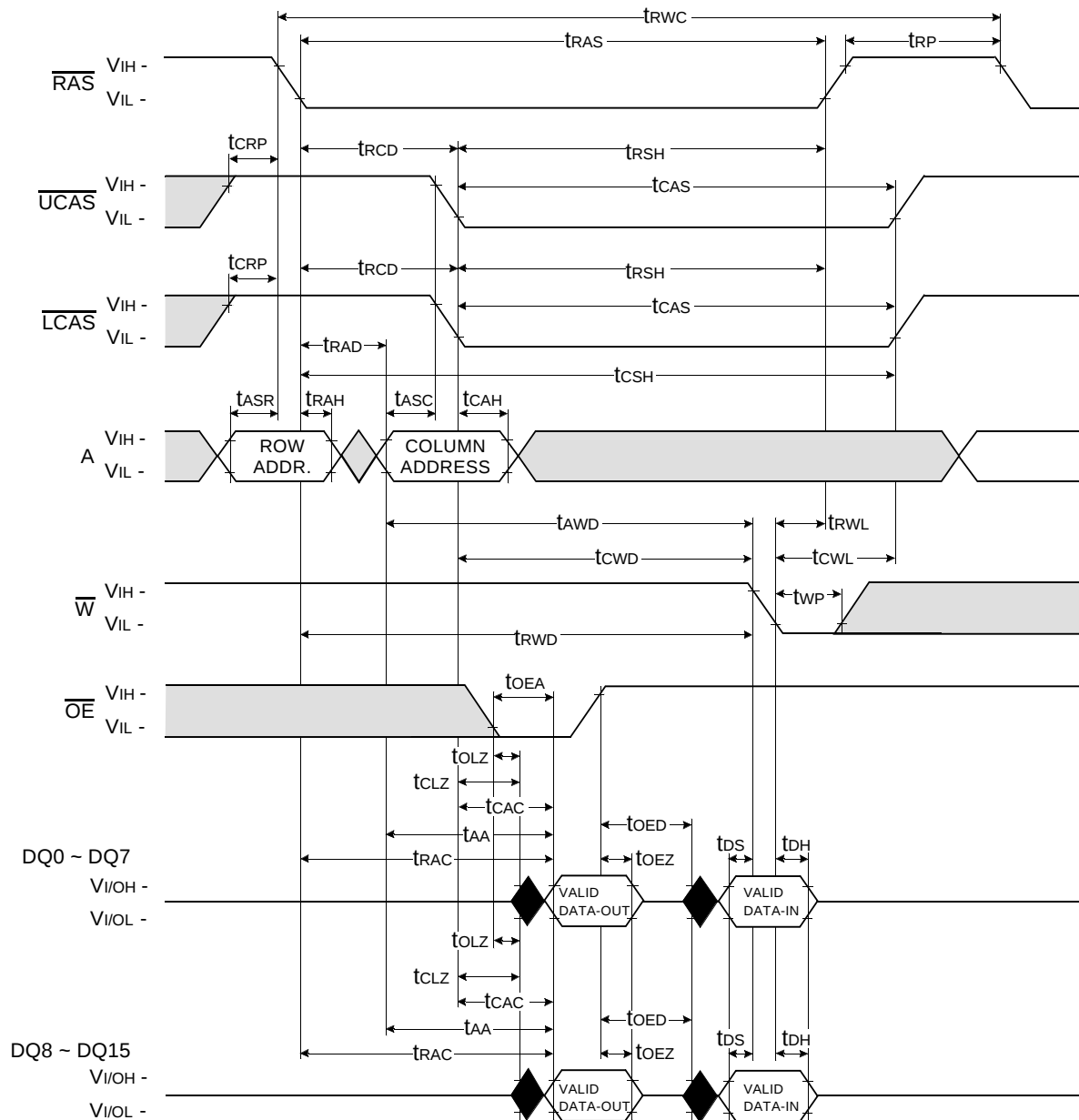
NOTE : DOUT = OPEN



KM416C1004C, KM416C1204C
KM416V1004C, KM416V1204C

CMOS DRAM

WORD READ - MODIFY - WRITE CYCLE

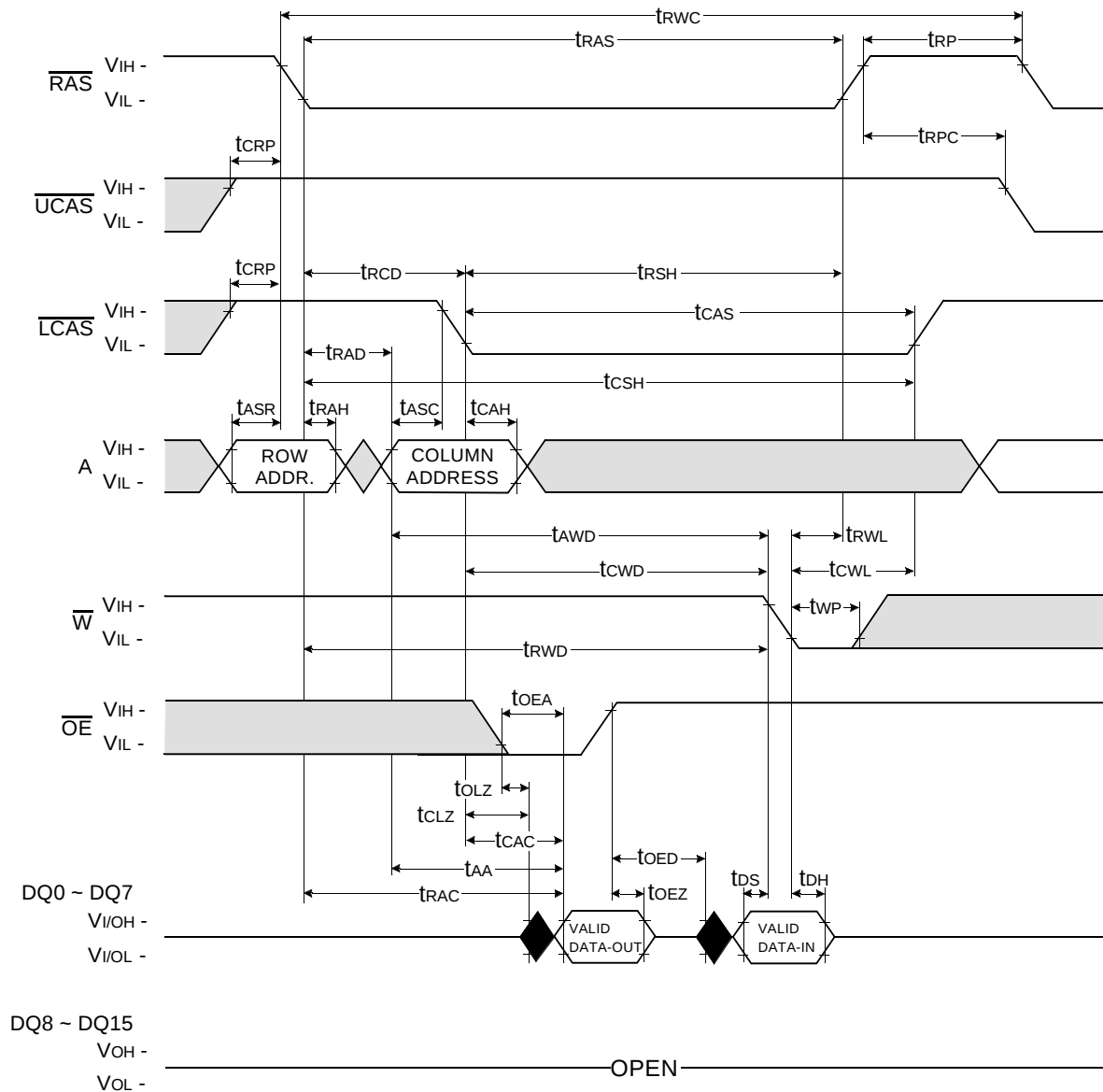


Don't care
 Undefined

KM416C1004C, KM416C1204C
KM416V1004C, KM416V1204C

CMOS DRAM

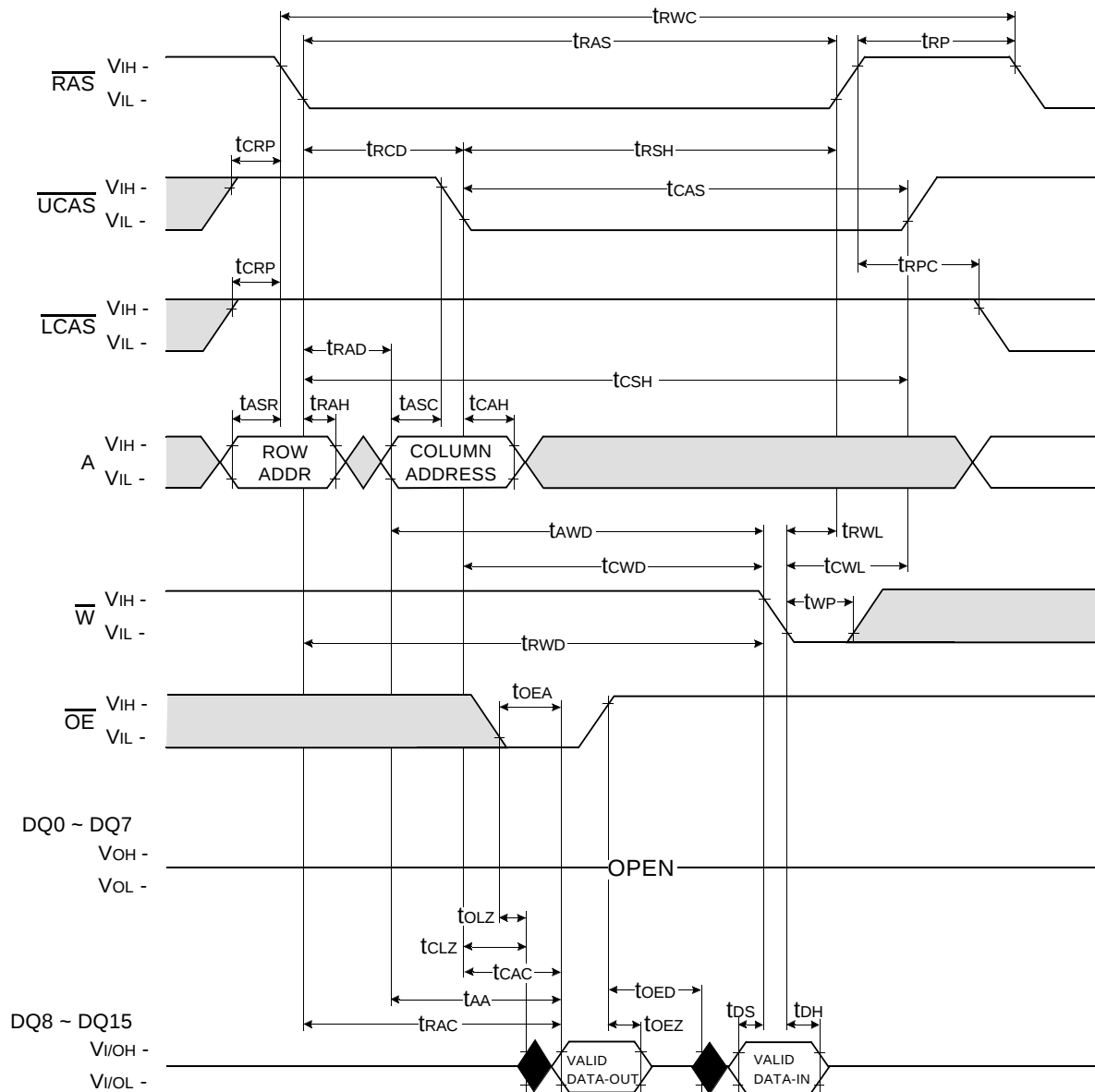
LOWER-BYTE READ - MODIFY - WRITE CYCLE



KM416C1004C, KM416C1204C
KM416V1004C, KM416V1204C

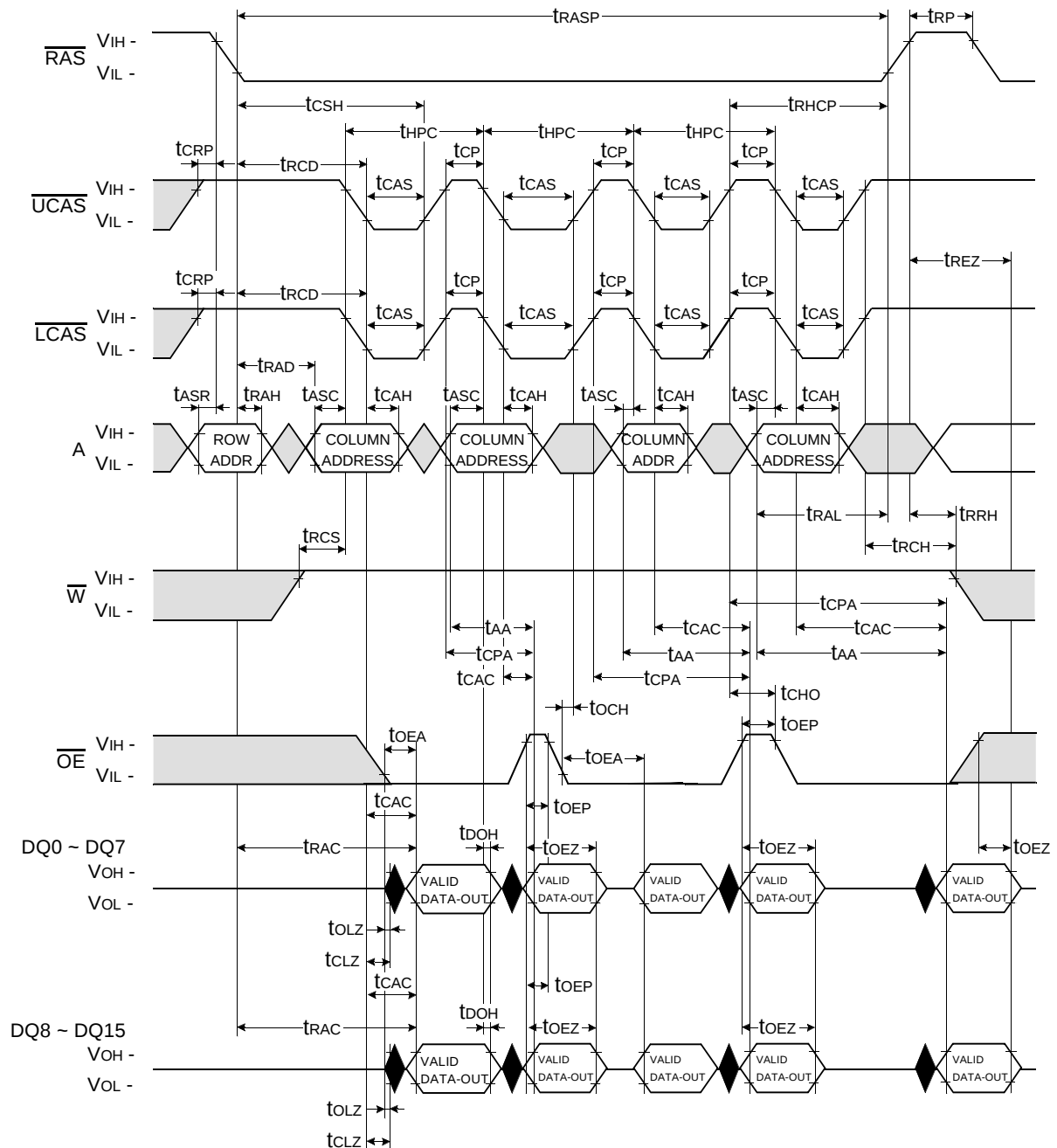
CMOS DRAM

UPPER-BYTE READ - MODIFY - WRITE CYCLE



Don't care
 Undefined

HYPER PAGE MODE WORD READ CYCLE



Don't care
 Undefined

The timing diagram shows the relationship between several control and data signals over time. The signals are:

- RAS**: Row Address Strobe, active low.
- UCAS**: Universal Chip Address Strobe, active low.
- LCAS**: Local Chip Address Strobe, active low.
- A**: Address bus, multiplexed for ROW ADDRESS and COLUMN ADDRESS.
- W**: Write Enable, active low.
- OE**: Output Enable, active low.
- DQ0 ~ DQ7**: Data bus for the first 8 bits.
- DQ8 ~ DQ15**: Data bus for the next 8 bits, shown as OPEN.

Key timing parameters labeled include:

- t_{RASP} : RAS pulse width.
- t_{CRP} : RAS-to-UCAS setup time.
- t_{CSH} : UCAS setup time before LCAS.
- t_{RCD} : RAS-to-LCAS delay.
- t_{CAS} : LCAS setup time before column address.
- t_{CP} : Column address setup time before write enable.
- t_{CAH} : Column address hold time after write enable.
- t_{ASC} : Address setup time before output enable.
- t_{AA} : Address-to-output delay.
- t_{CPA} : Column address-to-output delay.
- t_{CAC} : Column address-to-output delay.
- t_{CH} : Column address-to-output delay.
- t_{CHO} : Column address-to-output delay.
- t_{OE} : Output enable pulse width.
- t_{AC} : Access time from output enable to valid data.
- t_{DOH} : Data output hold time after output enable deassertion.
- t_{OEZ} : Output enable to output delay.
- t_{OLZ} : Output load time.
- t_{CLZ} : Output clock load time.
- t_{RPC} : RAS-to-column address delay.
- t_{REZ} : RAS-to-output delay.
- t_{RRH} : Row address-to-output delay.
- t_{RCH} : Row address-to-output delay.
- t_{TRP} : RAS-to-output delay.



CMOS DRAM

[illegible]

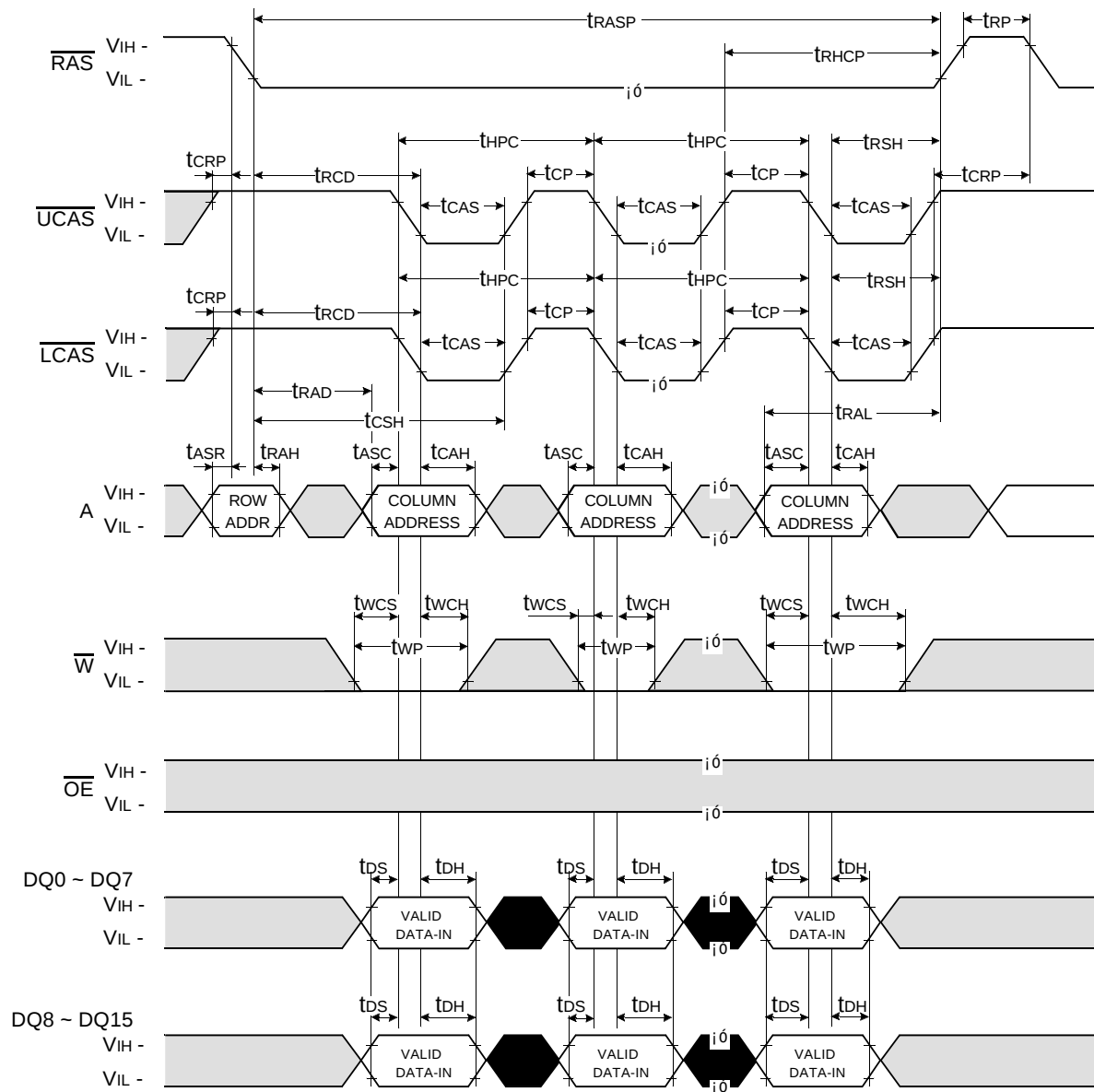
Undefined

KM416C1004C, KM416C1204C KM416V1004C, KM416V1204C

CMOS DRAM

HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



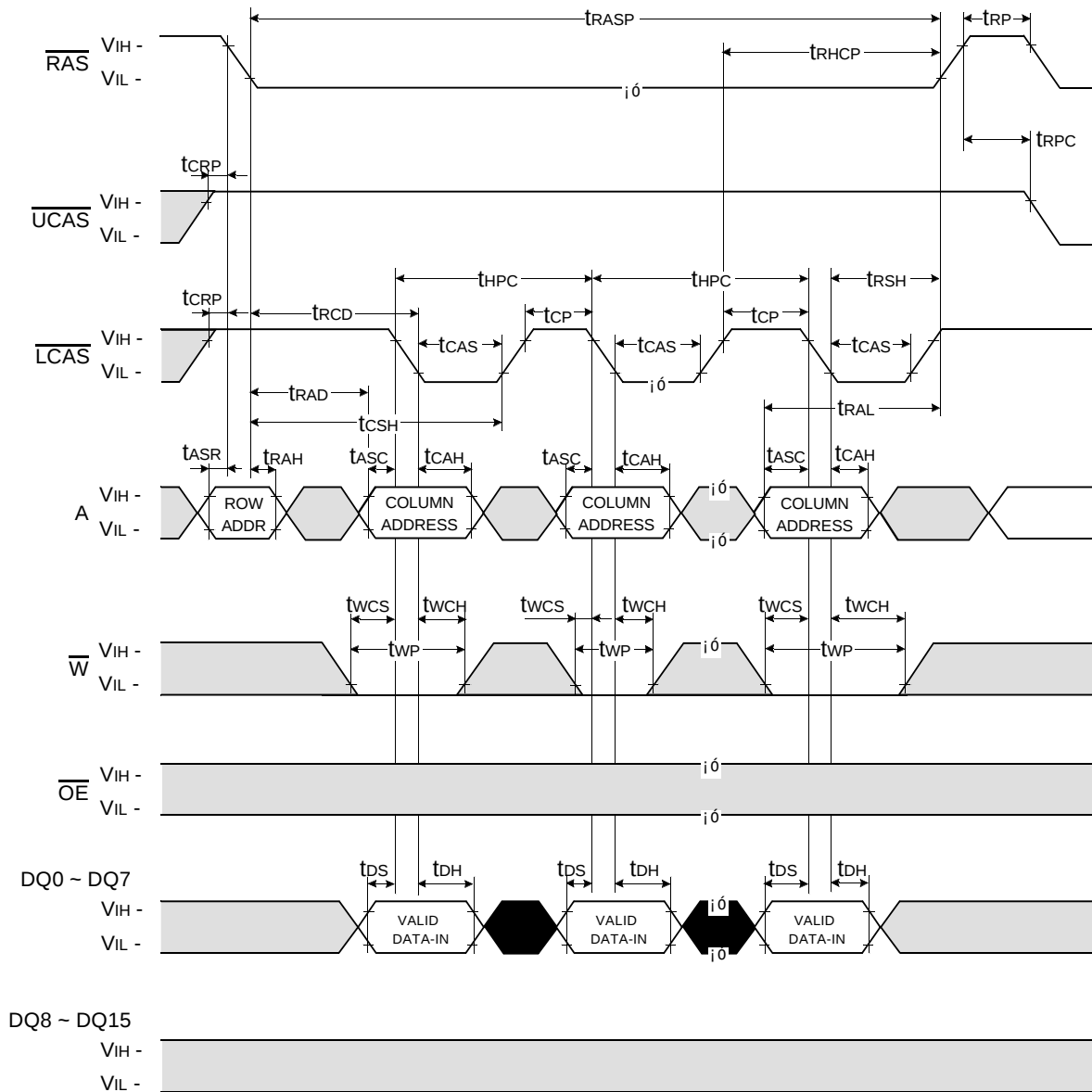
Don't care
Undefined

KM416C1004C, KM416C1204C KM416V1004C, KM416V1204C

CMOS DRAM

HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

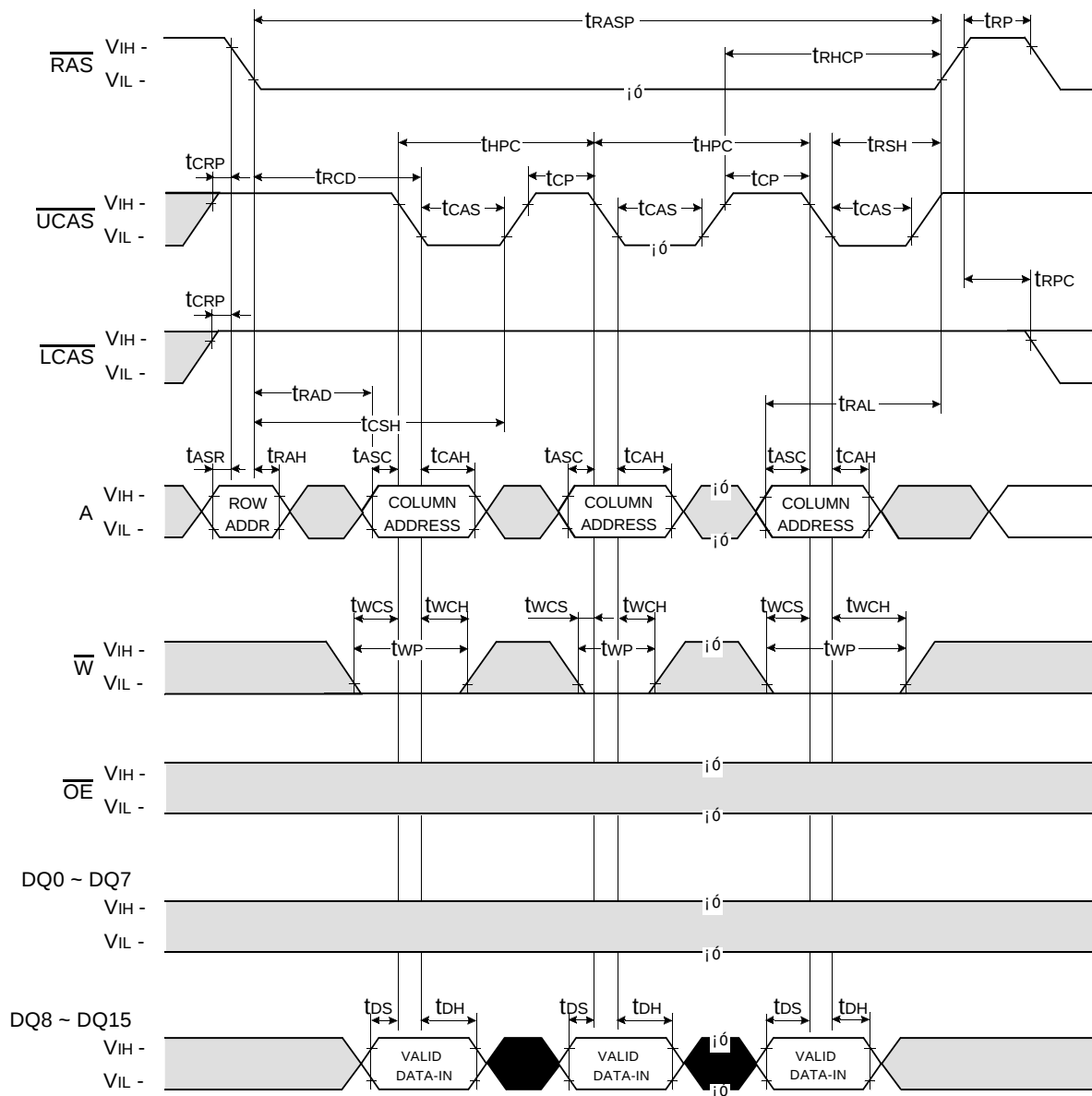
NOTE : DoUT = OPEN



Don't care
Undefined

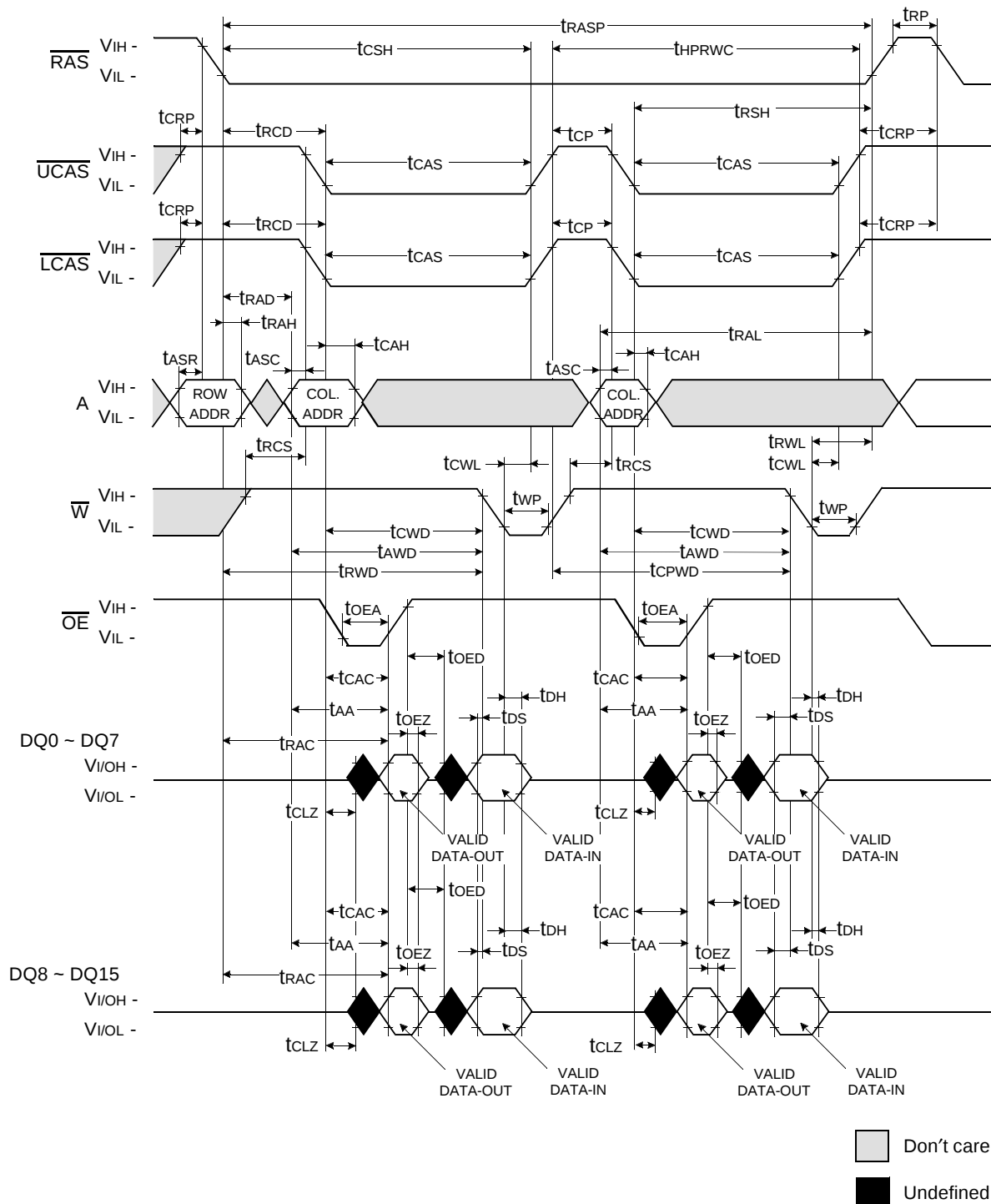
HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



Don't care
 Undefined

HYPER PAGE MODE WORD READ - MODIFY - WRITE CYCLE



CMOS DRAM

 Don't care

 Undefined

CMOS DRAM

[illegible]

 Don't care

 Undefined

CMOS DRAM

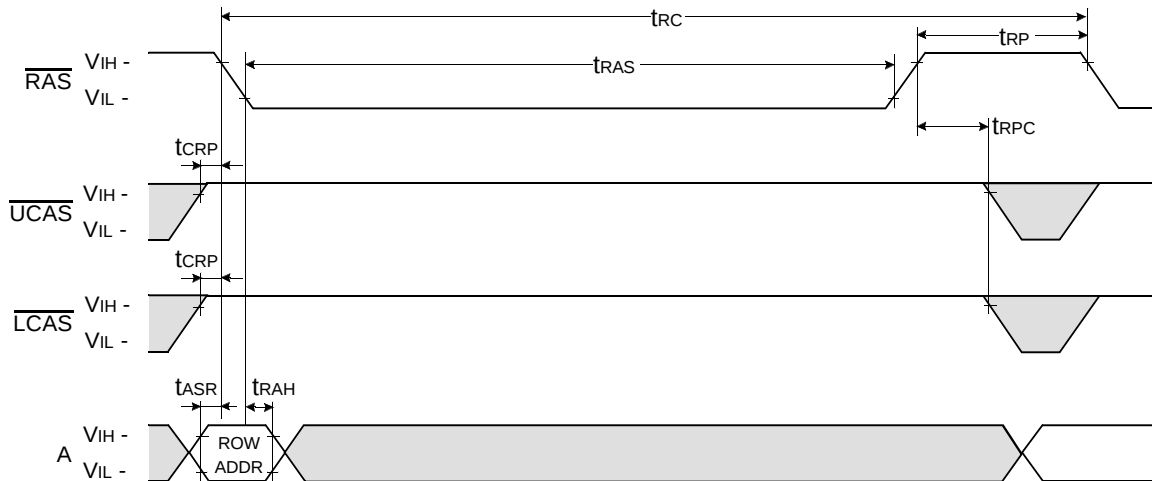
[illegible]

Undefined

$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE

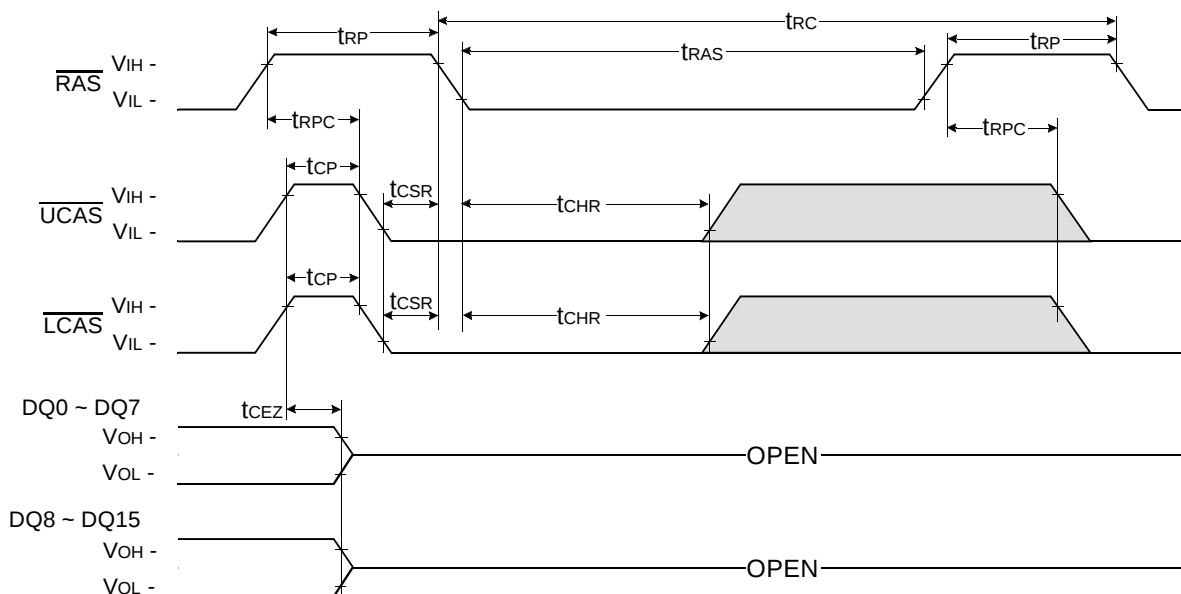
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



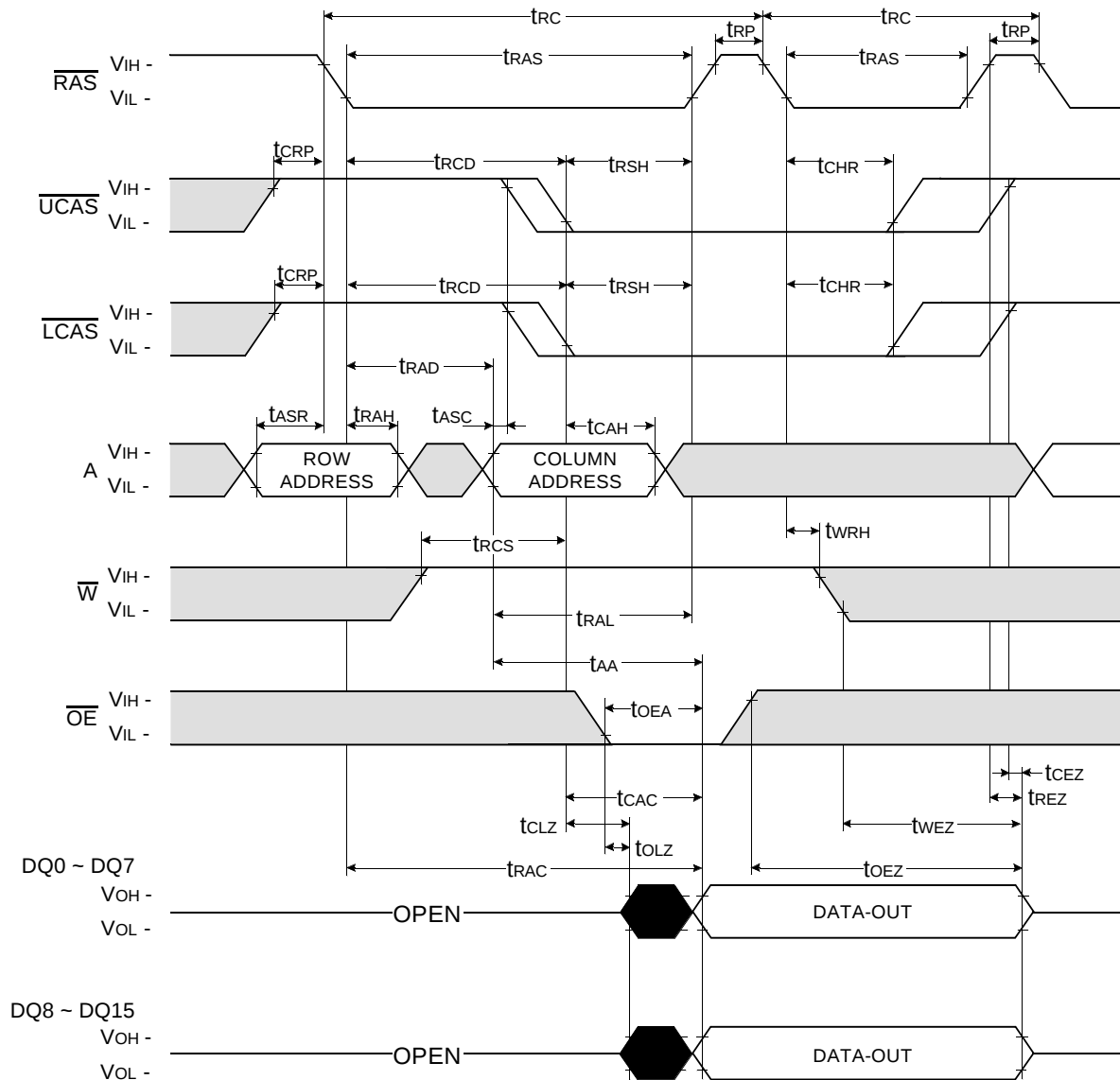
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care
 Undefined

HIDDEN REFRESH CYCLE (READ)



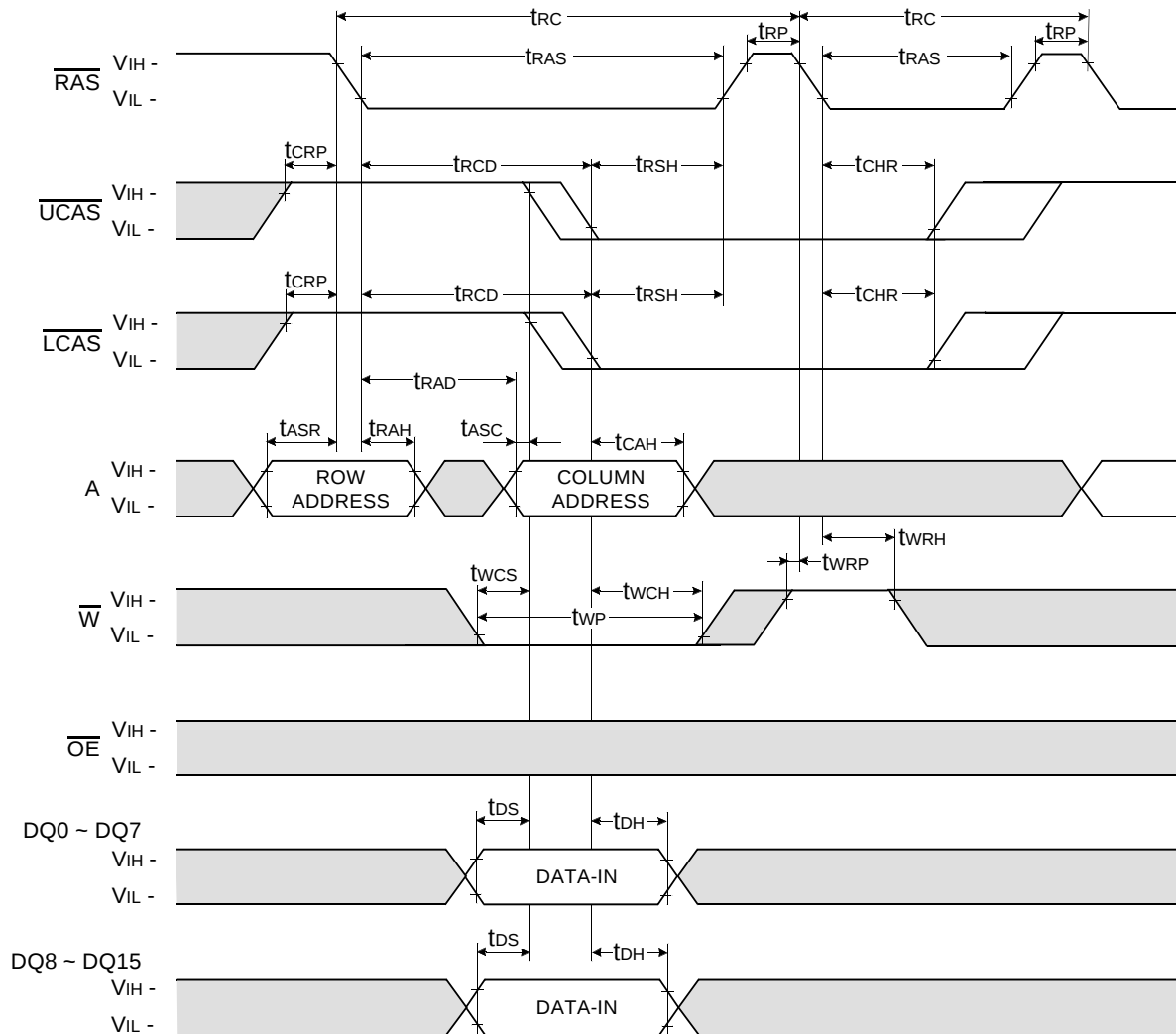
Don't care
Undefined

KM416C1004C, KM416C1204C KM416V1004C, KM416V1204C

CMOS DRAM

HIDDEN REFRESH CYCLE (WRITE)

NOTE : DoUT = OPEN



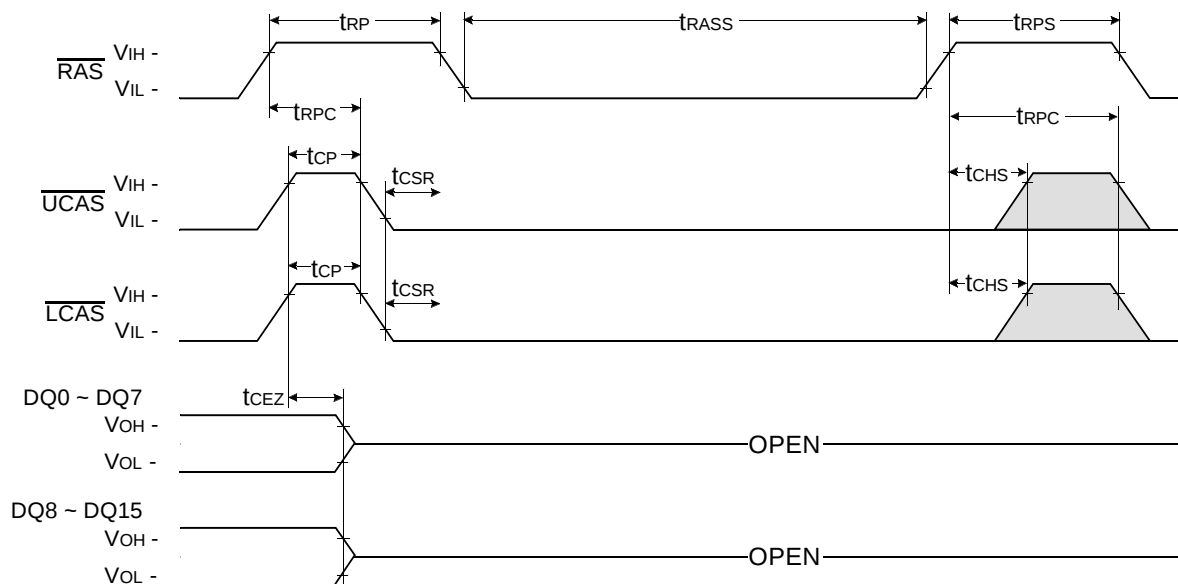
Don't care
Undefined

KM416C1004C, KM416C1204C KM416V1004C, KM416V1204C

CMOS DRAM

$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



□ Don't care
■ Undefined

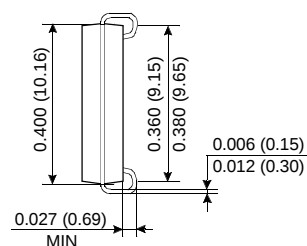
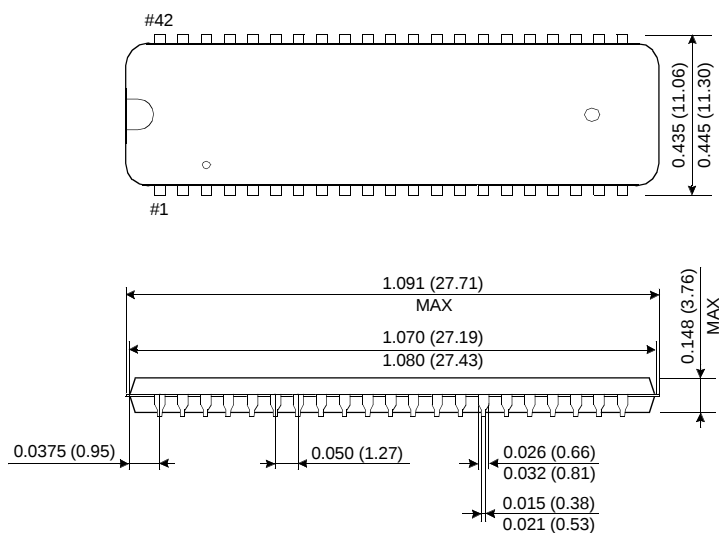
KM416C1004C, KM416C1204C **KM416V1004C, KM416V1204C**

CMOS DRAM

PACKAGE DIMENSION

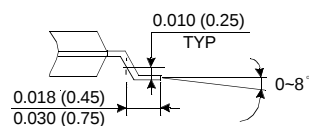
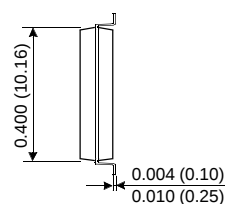
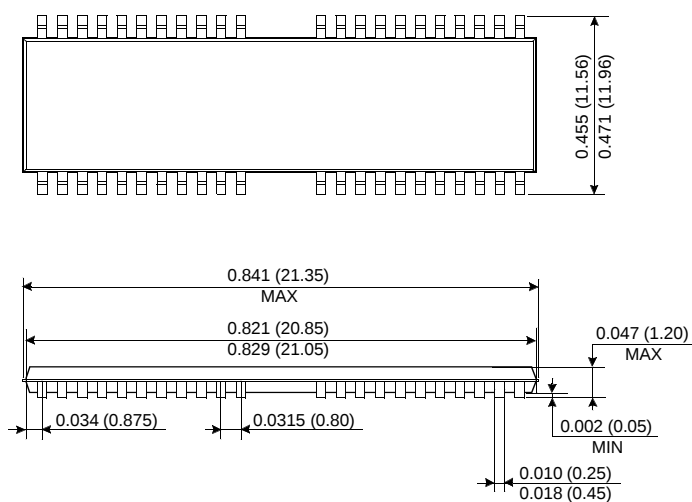
42 SOJ 400mil

Units : Inches (millimeters)



50(44) TSOP(II) 400mil

Units : Inches (millimeters)



SAMSUNG

ELECTRONICS