64K×4 Bit CMOS VIDEO RAM

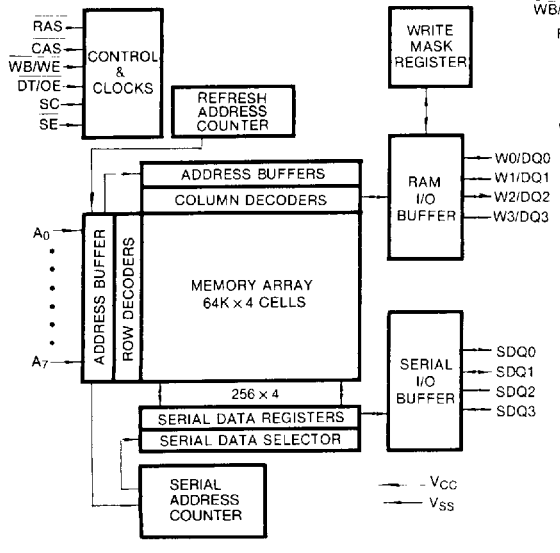
FEATURES

- **Dual Port Architecture**
  64K x 4 bits RAM port
  256 x 4 bits SAM port
- **Performance range:**

item	-10	-12
RAM access time (t_{RAC})	100ns	120ns
RAM access time (t_{CAC})	25ns	30ns
RAM cycle time (t_{RC})	180ns	220ns
RAM Page mode cycle (t_{PC})	60ns	75ns
SAM access time	25ns	35ns
SAM cycle time	30ns	40ns
RAM active current	65mA	55mA
SAM active current	40mA	35mA
RAM & SAM standby	3mA	3mA

- **Fast Page Mode**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read and Serial Write**
- **Read Transfer and Write Transfer**
- **Real Time Read Transfer capability**
- **Write per Bit masking on RAM write cycles**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only and Hidden Refresh**
- **Common data I/O using three-state RAM output control**
- **All inputs and outputs TTL compatible**
- **Refresh: 256 cycles/4ms**
- **Single +5V ± 10% supply voltage.**
- **Plastic 24-pin 400 mil ZIP or DIP.**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Samsung KM424C64 is a CMOS 64K x 4 bit Dual Port DRAM. It consists of a 64K x 4 dynamic random access memory (RAM) port and 256 x 4 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 256 rows of 1024 bits. It operates like a conventional 64K x 4 CMOS DRAM. The RAM port has a write per bit mask capability.

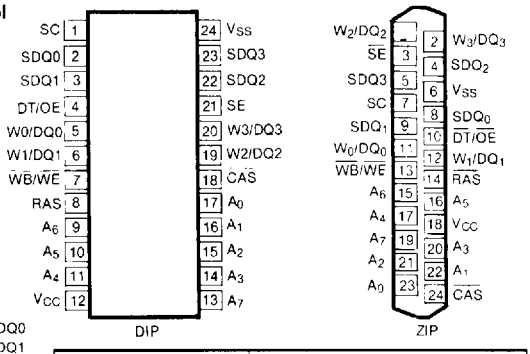
The SAM port consists of four 256 bit high speed shift registers that are connected to the RAM array through a 1024 bit data transfer gate. The SAM port has serial read and write capabilities.

Data may be internally transferred bi-directionally between the RAM and SAM ports using read or write transfers.

Refresh is accomplished by familiar DRAM refresh modes. The KM424C64 supports $\overline{RAS}$-only, Hidden, and $\overline{CAS}$-before-$\overline{RAS}$ refresh for the RAM port. The SAM port does not require refresh.

All inputs and I/O's are TTL level compatible. All address lines and Data inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
SC	Serial Clock
SDQ0 -SDQ3	Serial Data Input/Output
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{WB/WE}$	Write Per Bit/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
W0/DQ0-W3/DQ3	Data Write Mask/Input/Output
$\overline{SE}$	Serial Enable
A0-A8	Address Inputs
Vcc	Power(+5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

*Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, $T_A = 0$ to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter(RAM Port)			SAM Port	Symbol	KM424C64		Unit
					−10	−12	
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = min)			Standby	I_{CC1}	65	55	mA
			Active	$I_{CC1}A$	100	85	mA
Standby Current	$\overline{RAS}$, $\overline{CAS}$, $\overline{DT/OE}$	$\overline{SE}$ = V_{IH}, SC = V_{IL}	Standby	I_{CC2}	3	3	mA
	$\overline{WB/WE}$ = V_{IH}	$\overline{SE}$ = V_{IL}, SC = Cycling	Active	$I_{CC2}A$	40	35	mA
$\overline{RAS}$ Only Refresh Current* ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @ t_{RC} = min)			Standby	I_{CC3}	65	55	mA
			Active	$I_{CC3}A$	100	85	mA
Fast Page Mode Current* ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling @ t_{PC} = min)			Standby	I_{CC4}	50	40	mA
			Active	$I_{CC4}A$	85	70	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = min)			Standby	I_{CC5}	65	55	mA
			Active	$I_{CC5}A$	100	85	mA
Data Transfer Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = min)			Standby	I_{CC6}	75	65	mA
			Active	$I_{CC6}A$	110	95	mA

*NOTE: I_{CC1}/A, I_{CC3}/A, I_{CC4}/A, I_{CC5}/A, and I_{CC6}/A are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

INPUT/OUTPUT CURRENTS (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any input $0 \le V_{IN} \le 6.5V$, all other pins not under test = 0 volts.)	I_{IL}	−10	10	μA
Output Leakage Current (Data out is disabled, $0V \le VOUT \le 5.5V$)	I_{OL}	−10	10	μA
Output High Voltage Level (RAM I_{OH} = −5mA, SAM I_{OH} = −2mA)	V_{OH}	2.4	—	V
Output Low Voltage level (RAM I_{OL} = 4.2mA, SAM I_{OL} = 2mA)	V_{OL}	—	0.4	V

CAPACITANCE (T_A = 25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_7)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, $\overline{SE}$, SC)	C_{IN2}	—	7	pF
Input/Output Capacitance (W_0/DQ_0-W_3/DQ_3)	C_{DQ}	—	7	pF
Input/Output Capacitance (SDQ_0 -SDQ_3)	C_{SDQ}	—	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC} = 5.0V ± 10%. See notes 1, 2)

Parameter	Symbol	-10		-12		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	180		220		ns	
Read-modify-write cycle time	t_{RWC}	245		295		ns	
Fast page mode cycle time	t_{PC}	60		75		ns	
Fast page mode read-modify-write	t_{PRWC}	125		145		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		25		30	ns	4
Access time from column address	t_{AA}		50		60	ns	3,11
Access time from $\overline{CAS}$ precharge	t_{CPA}		55		65	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	5		5		ns	3
Output buffer turn-off delay	t_{OFF}	0	30	0	35	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	70		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	100	100,000	120	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		ns	
$\overline{CAS}$ pulse width	t_{CAS}	25		30		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	75	25	90	ns	5,6
$\overline{RAS}$ to column address delay time	t_{RAD}	20	50	20	60	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	15		20		ns	
$\overline{CAS}$ precharge time (Fast page)	t_{CP}	15		20		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	50		60		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	9
Write command hold time	t_{WCH}	20		25		ns	

STANDARD OPERATION (Continued)

Parameter	Symbol	-10		-12		Unit	Notes
		Min	Max	Min	Max		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	75		85		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25		30		ns	
Data set-up time	t_{DS}	0		0		ns	10
Data hold time	t_{DH}	20		25		ns	10
Data hold referenced to $\overline{RAS}$	t_{DHR}	75		85		ns	
Write command set-up time	t_{WCS}	0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		70		ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	135		160		ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	85		100		ns	8
$\overline{CAS}$ set-up time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	10		10		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	20		25		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		ns	
Access time from output enable	t_{OEA}		25		30	ns	
Output enable to data input delay	t_{OED}	20		25		ns	
Output buffer turnoff delay from $\overline{OE}$	t_{OEZ}	0	25	0	30	ns	7
Output enable command hold time	t_{OEH}	25		30		ns	
Data to $\overline{CAS}$ delay	t_{DZC}	0		0		ns	
Data to output enable delay	t_{DZO}	0		0		ns	
Refresh period (256 cycles)	t_{REF}		4		4	ms	
$\overline{WB}$ Set-up time	t_{WSR}	0		0		ns	
$\overline{WB}$ hold time	t_{RWH}	15		20		ns	
Write per bit mask data set-up	t_{MS}	0		0		ns	
Write per bit mask data hold	t_{MH}	15		20		ns	
$\overline{DT}$ high set-up time	t_{THS}	0		0		ns	
$\overline{DT}$ high hold time	t_{THH}	15		20		ns	
$\overline{DT}$ low set-up time	t_{TLS}	0		0		ns	
$\overline{DT}$ low hold time	t_{TLH}	15		20		ns	
$\overline{DT}$ low hold ref to column address (real time read transfer)	t_{ATH}	35		40		ns	

STANDARD OPERATION (Continued)

Parameter	Symbol	-10		-12		Unit	Notes
		Min	Max	Min	Max		
$\overline{DT}$ low hold ref to $\overline{RAS}$ (real time read transfer)	t_{RTH}	80		95		ns	
$\overline{DT}$ low hold ref to $\overline{CAS}$ (real time read transfer)	t_{CTH}	30		35		ns	
$\overline{SE}$ set-up referenced to $\overline{RAS}$	t_{ESR}	0		0		ns	
$\overline{SE}$ hold time referenced to $\overline{RAS}$	t_{REH}	15		20		ns	
$\overline{DT}$ to $\overline{RAS}$ precharge delay	t_{TRD}	10		10		ns	
$\overline{DT}$ to $\overline{CAS}$ precharge delay time	t_{TCD}	10		10		ns	
$\overline{DT}$ precharge time	t_{TP}	30		35		ns	
$\overline{RAS}$ to first SC delay (read transfer)	t_{RSD}	100		120		ns	
$\overline{CAS}$ to first SC delay (read transfer)	t_{CSD}	50		60		ns	
Last SC to $\overline{DT}$ lead time	t_{TSL}	0		0		ns	
$\overline{DT}$ to first SC delay (read transfer)	t_{TSD}	20		20		ns	
Last SC to $\overline{RAS}$ set-up (serial input)	t_{SRS}	30		40		ns	
$\overline{RAS}$ to first $\overline{SC}$ delay time (serial input)	t_{SRD}	25		25		ns	
$\overline{RAS}$ to serial input delay	t_{SDD}	50		60		ns	
Serial out buffer turn-off delay from $\overline{RAS}$ (pseudo write transfer)	t_{SDZ}	10	50	10	60	ns	7
Serial input to first SC delay	t_{SZS}	0		0		ns	
SC cycle time	t_{SCC}	30		40		ns	
SC pulse width (SC high time)	t_{SC}	10		15		ns	
SC precharge (SC low time)	t_{SCP}	10		15		ns	
Access time from SC	t_{SCA}		25		35	ns	4
Serial output hold time from SC	t_{SOH}	5		5		ns	
Serial input set-up time	t_{SDS}	0		0		ns	
Serial input hold time	t_{SDH}	20		30		ns	
Access time from $\overline{SE}$	t_{SEA}		25		35	ns	4
$\overline{SE}$ pulse width	t_{SE}	25		35		ns	
$\overline{SE}$ precharge time	t_{SEP}	25		35		ns	
Serial out buffer turn-off from $\overline{SE}$	t_{SEZ}	0	20	0	30	ns	7
Serial input to $\overline{SE}$ delay time	t_{SZE}	0		0		ns	
Serial write enable set-up	t_{SWS}	5		10		ns	
Serial write enable hold time	t_{SWH}	15		20		ns	

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NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 SC cycles before proper device operation is achieved ($\overline{DT}/\overline{OE}$ = HIGH). If the internal refresh counter is used, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. RAM port outputs are measured with a load equivalent to 2 TTL loads and 100pF.
4. SAM port outputs are measured with a load equivalent to 2 TTL loads and 50pF. D_{OUT} comparator level: V_{OH}/V_{OL} = 2.0/0.8V.
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max).
7. The parameters, t_{OFF}(max), t_{OEZ}(max), t_{SDZ}(max) and t_{SEZ}(max), define the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} < t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RCD}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

DEVICE INFORMATION

All operation modes of KM424C64 are determined by $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ at the falling edge of $\overline{RAS}$. The truth table of the operation modes is shown in table 1.

Table 1. Operation truth table

$\overline{RAS}$	$\overline{CAS}$	ADDRESS	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	FUNCTION
H	H	*	*	*	*	Standby
	L	*	*	*	*	$\overline{CAS}$-before-$\overline{RAS}$ Refresh
	H	row/column	H→L	H	*	READ
⎺_	H	row/column	H	H→L	*	WRITE
	H	row	H	*	*	$\overline{RAS}$-only Refresh
	H	row/column	H	L	*	WRITE-per-Bit
	H	row/tap	L	H	*	READ Transfer
	H	row/tap	L	L	L	WRITE Transfer
	H	row/tap	L	L	H	Pseudo-Write Transfer

Device Operation

The KM424C64 contains 262,144 memory locations. sixteen address bits are required to address a particular 4-bit word in the memory array. Since the KM424C64 has only 8 address input pins, time multiplexed addressing is used to input 8 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operation of the KM424C64 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 8 address input pins is changed from a row address to a column address and is strobed in by CAS. This is the beginning of any KM424C64 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

RAS and CAS Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time. t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM424C64 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements. loss of data integrity can occur.

Read

A read cycle is achieved by maintaining $\overline{WB}/\overline{WE}$ high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition. If $\overline{CAS}$ goes low before t_{RCD}(max) and if the column address is valid before t_{RAD}(max) then the access time to valid data is specified by t_{RAC}(min). However, if $\overline{CAS}$ goes low after t_{RCD}(max) or if the column address becomes valid after t_{RAD}(max), access is specified by t_{CAC} or t_{AA}.

The KM424C64 has common data I/O pins. The $\overline{DT}/\overline{OE}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{DT}/\overline{OE}$ must be low for the period of time defined by t_{OEA}.

Write

The KM424C64 can perform early write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$. In any type of write cycle Data-in must be valid at or before the falling edge of $\overline{WB}/\overline{WE}$ whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{WB}/\overline{WE}$ low before $\overline{CAS}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the outputs remain in the Hi-Z state. In the early write cycle $\overline{DT}/\overline{OE}$ must meet $\overline{DT}/\overline{OE}$ high set-up and hold time as $\overline{RAS}$ falls but otherwise does not affect any circuit operation during the $\overline{CAS}$ active period.

Read-Modify-Write: In this cycle, valid data from the addressed cells appears at the outputs before and during the time that data is being written into the same cell locations. In this cycle read operation is achieved by bringing $\overline{DT}/\overline{OE}$ low with $\overline{RAS}$ and $\overline{CAS}$ low. The access time to valid data is specified by t_{OEA}. After $\overline{DT}/\overline{OE}$ goes high, the data to be written is stored by $\overline{WB}/\overline{WE}$ with set-up and hold times referenced to this signal.

Late Write: This cycle shows the timing flexibility of ($\overline{DT}$/OE) which can be activated just after ($\overline{WB}/\overline{WE}$) falls, even when ($\overline{WB}/\overline{WE}$) is brought low after $\overline{CAS}$.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Write-Per-Bit

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}/\overline{WE}$ is held 'low' at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the Wi/DQi pins is latched onto the write-mask register (WM1). When a '0' is sensed on any of the Wi/DQi pins, their corresponding write circuits are disabled and new data will not be written.

When a '1' is sensed on any of the Wi/DQi pins, their corresponding write circuits will remain enabled so that new data is written. The write mask data is valid for only one cycle.The truth table of the write-per-bit function is shown in table 2.

Table 2. Truth Table for Write-per-Bit Function

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Wi/DQi	FUNCTION
⎺_	H	H	H	*	WRITE ENABLE
	H	H	L	1	WRITE ENABLE
				0	WRITE MASK

Data Output

The KM424C64 has a three state output buffers which are controlled by $\overline{CAS}$ and $\overline{DT}/\overline{OE}$. When either $\overline{CAS}$ or $\overline{DT}/\overline{OE}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be presented at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM424C64 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Refresh

The data in the KM424C64 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 256 rows every 4 ms. Any operation cycle performed in the RAM port refreshes the 1024 bits selected by the row addresses or an on-chip refresh address counter. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 256 row addresses, (A_0-A_7).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM424C64 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The KM424C64 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM424C64 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Transfer Operation

The KM424C64 features bi-directional transfer capability from RAM to SAM and from SAM to RAM. A transfer consists of loading 256 words by 4-bits of data from one port into the other. During a data transfer cycle, RAM port and SAM port can't operate independently. Data transfer cycle includes are following operations.

i) Data is transferred between RAM memory cell on the specified row address and SAM data register (except pseudo write transfer).
ii) Direction of data transfer is defined.
iii) Serial read or serial write is selected.
iv) SAM start address (the address to be accessed first after the termination of transfer cycle in the SAM data register) is specified.

There are three types of transfer operations: read transfer, write transfer and pseudo-write transfer. As shown in table 3, the type of transfer operation is determined by $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ at the falling edge of $\overline{RAS}$.

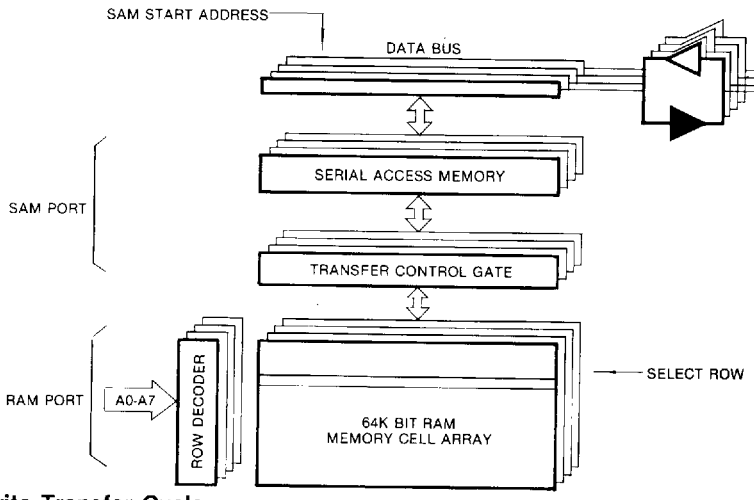
Table 3. Truth Table for Transfer Operation

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	FUNCTION	TRANSFER DIRECTION
⎺_	H	L	H	*	Read transfer cycle	RAM→SAM
	H	L	L	L	Write transfer cycle	SAM→RAM
	H	L	L	H	Pseudo write transfer cycle	—

Read-Transfer Cycle

A read-transfer consists of loading a selected row of data from the RAM array into the SAM register. A read-transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and WB/$\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The actual data transfer is completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SDQ lines are set into the output mode. In a read/real-time read-transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and becomes valid on the SDQ lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock(SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 2. BLOCK diagram of RAM and SAM PORT during read transfer



Write Transfer Cycle

A write transfer cycle consists of loading the content of the SAM data register into a selected row of RAM array. A write transfer is accomplished by $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transfered. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SDQ lines are in the input mode so that serial data synchronized with SC can be loaded. When two consecutive write transfer operations are performed, there is a delay in availability between the last bit of the previous row and the first bit of the new row. Consequently the SC clock must be held at a constant V_{IL} or V_{IH} after the SC precharge time t_{SCP} has been satisfied. A rising edge of the SC clock must not occur until after a specified delay t_{RSD} from the falling edge of $\overline{RAS}$.

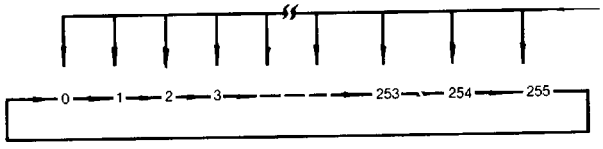
Pseudo Write Transfer Cycle

The pseudo write transfer cycle switches SDQ lines from serial read mode to serial write mode. It doesn't perform data transfer. A pseudo write transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. The pseudo write transfer cycle must be performed after a read transfer cycle if the subsequent operation is a write transfer cycle. There is a timing delay associated with the switching of the SDQ lines from serial output mode to serial input mode. During this period, the SC clock must be held at a constant V_{IL} or V_{IH} after the t_{SC} precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{RSD} from the falling edge of $\overline{RAS}$.

SAM Port Operation

The KM424C64 is provided with a 256 word by 4 bit serial access memory (SAM). High speed read and write operation may be performed through the SAM port independent of the RAM port operations, except during transfer operation. The preceding transfer operation determines the direction of data flow through the SAM registers. Data may be read out of the SAM port after a read transfer cycle (RAM→SAM) has been performed. Data can be shifted out of the SAM port starting at any of the 256 bit locations. This tap location corresponds to the column address selected at the falling edge of $\overline{CAS}$

during the read transfer cycle. The SAM register is configured as a circular data register. The data is shifted sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit.



Tap location started by column address of read-transfer cycle.

Subsequent real time read transfer may be performed on the fly as many times as desired within the refresh constraint of the RAM memory array. A pseudo write transfer cycle must be performed in order to write data into the SAM port. This cycle switches the SAM port operation from output mode to input mode. Data is not transferred during a pseudo write transfer cycle. A write transfer cycle (SAM→RAM) may then be performed. The data in the SAM register is loaded into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The start address of SAM registers is determined by the column address selected at the falling edge of $\overline{CAS}$.

Table 4. Truth Table for SAM Operation

Preceding Transfer Cycle	SAM port operation	$\overline{DT}/\overline{OE}$ (at the falling edge of $\overline{RAS}$)	SC	$\overline{SE}$	Function
read-transfer	serial output mode	L*	——	L	Serial read enable
				H	Serial read disable
write-transfer	serial input mode		⊓	L	Serial write enable

*When simultaneous operation is being performed on the RAM port and the SAM port, $\overline{DT}/\overline{OE}$ must be held high at the falling edge of $\overline{RAS}$ so as to prevent a false transfer cycle.

Serial Clock (SC)

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SDQ pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 8 bit serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle. When the pointer reaches the most significant address location (decimal 255), the next SC clock will be placed at the least significant address location (decimal 0).

Serial Enable ($\overline{SE}$)

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control.

When $\overline{SE}$ is high, serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when SE is high.

Serial Input/Output (SDQ0-SDQ3)

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a pseudo write is performed, the SAM port operation is switched from output mode to input mode. During subsequent write transfer cycle, the SAM port remains in the input mode.

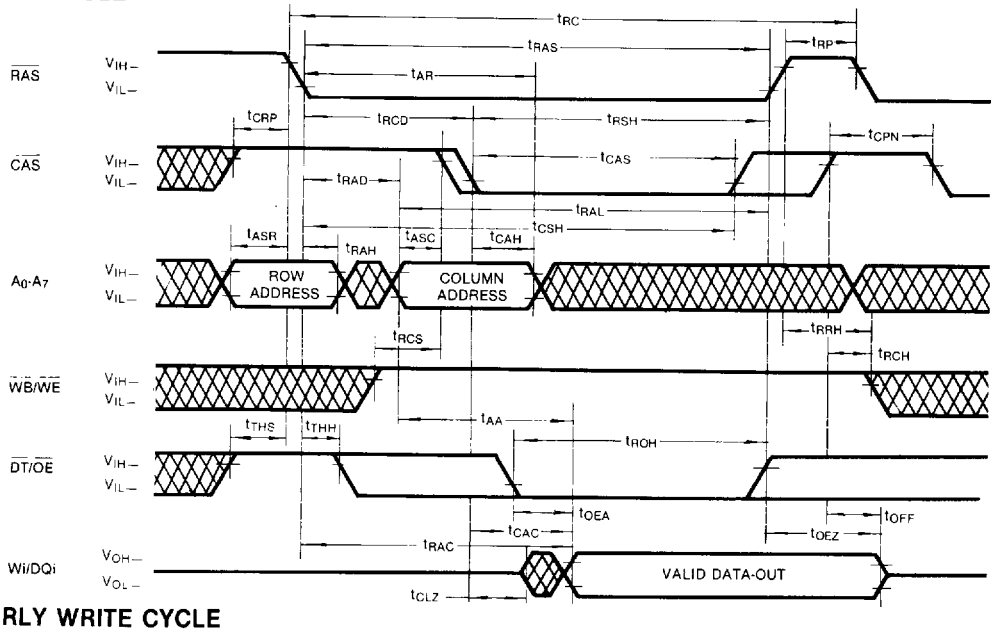
Power-up

If $\overline{RAS} = V_{IL}$ during power-up, the KM424C64 could possibly begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

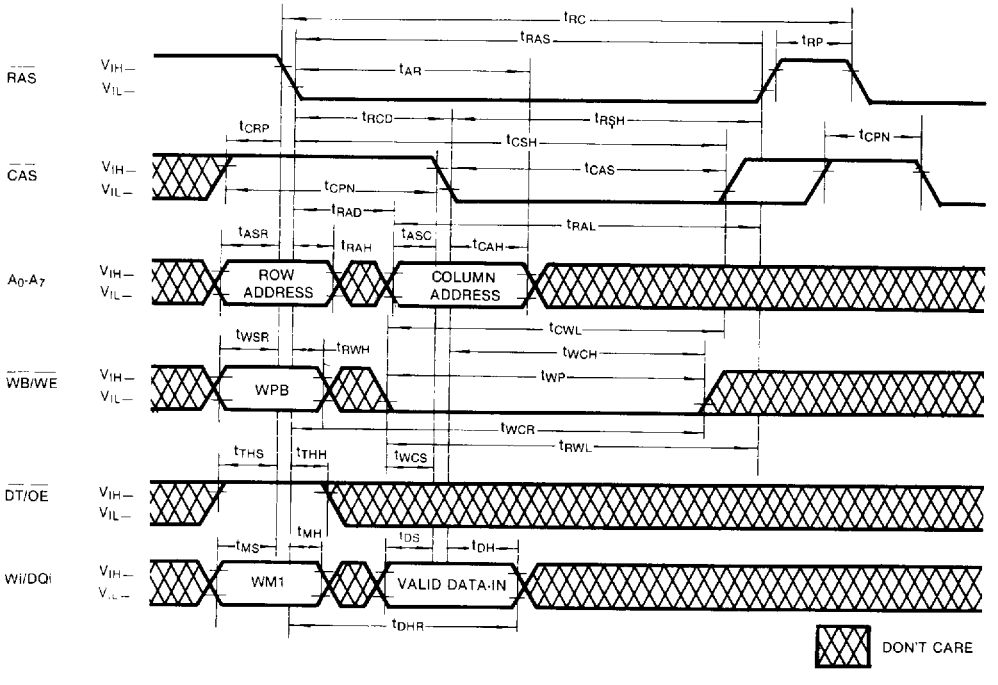
An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured.

TIMING DIAGRAMS

READ CYCLE

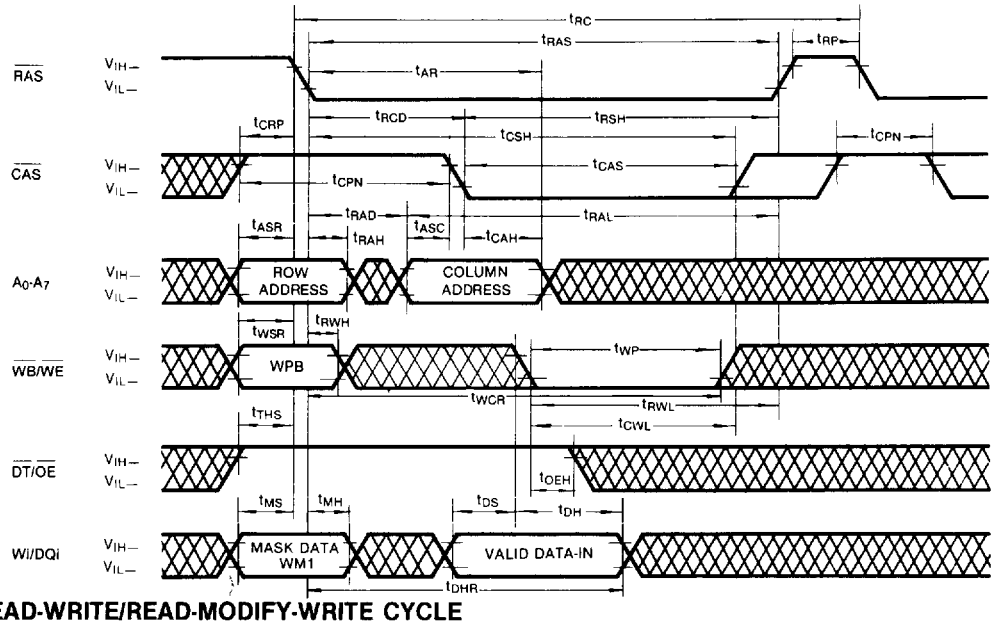


EARLY WRITE CYCLE

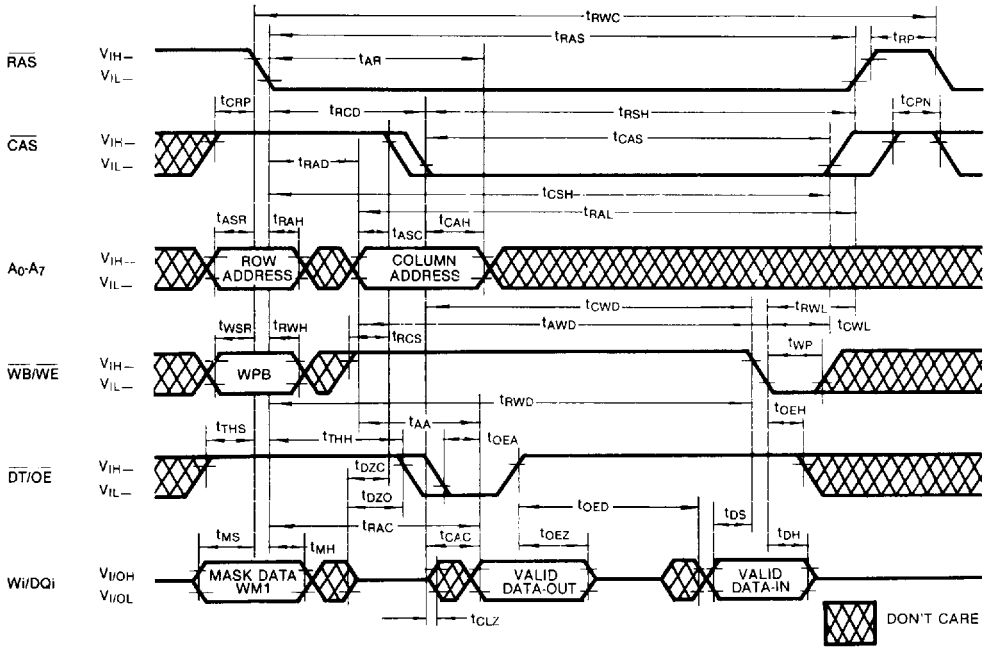


TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

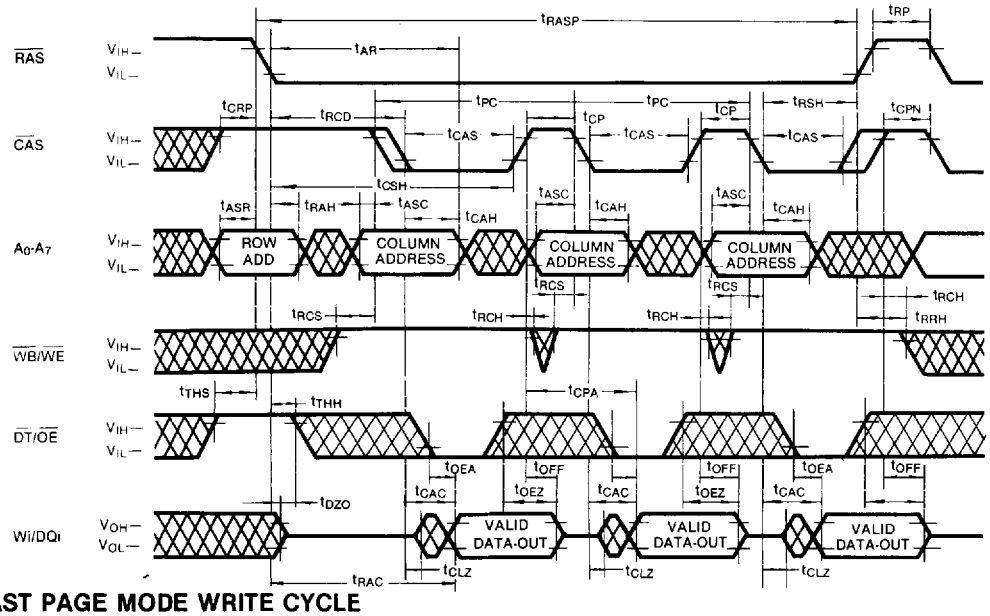


READ-WRITE/READ-MODIFY-WRITE CYCLE

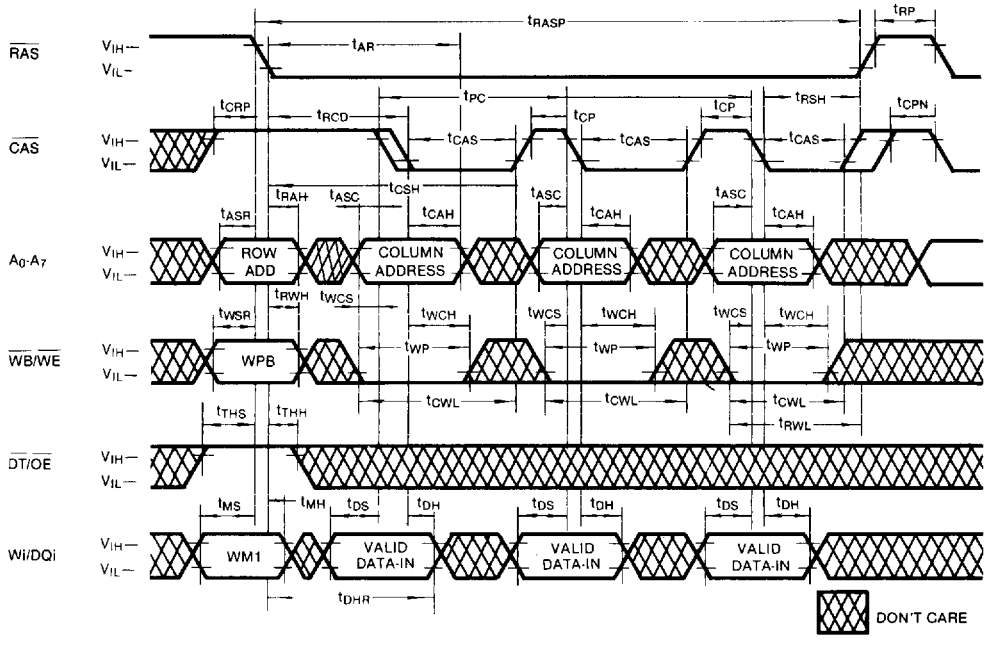


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE

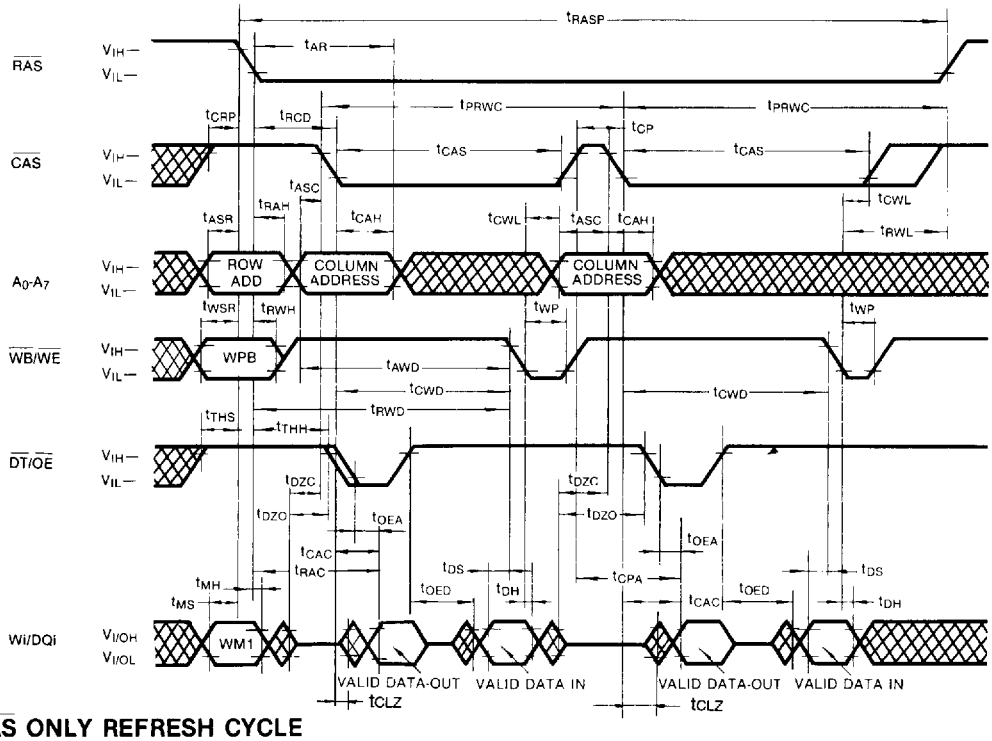


FAST PAGE MODE WRITE CYCLE

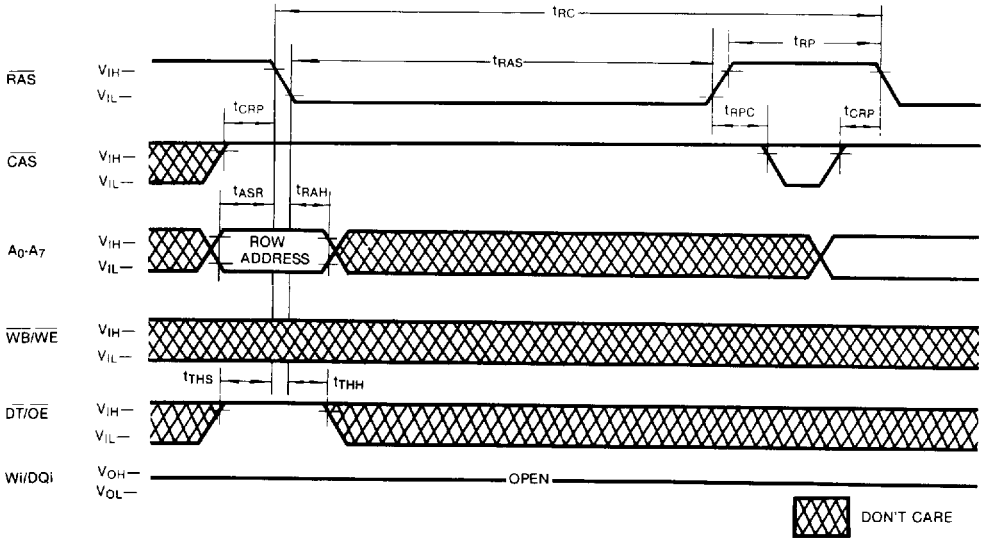


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

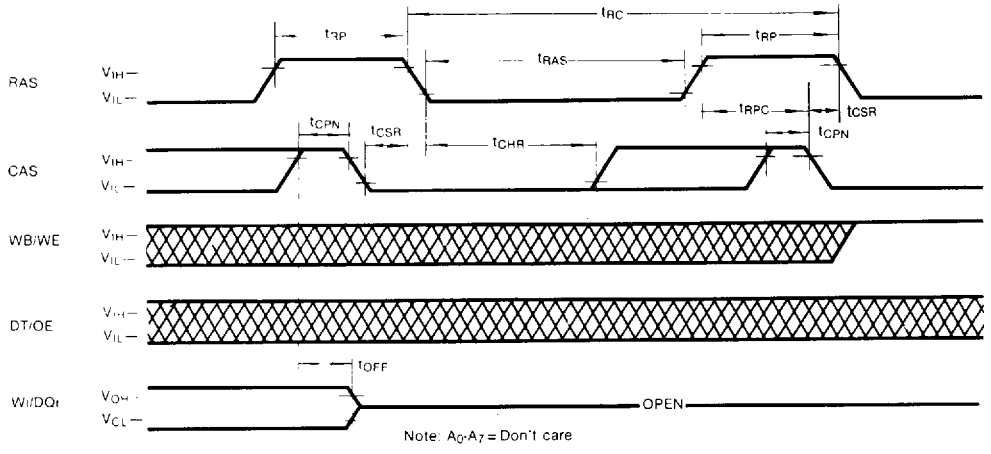


RAS ONLY REFRESH CYCLE

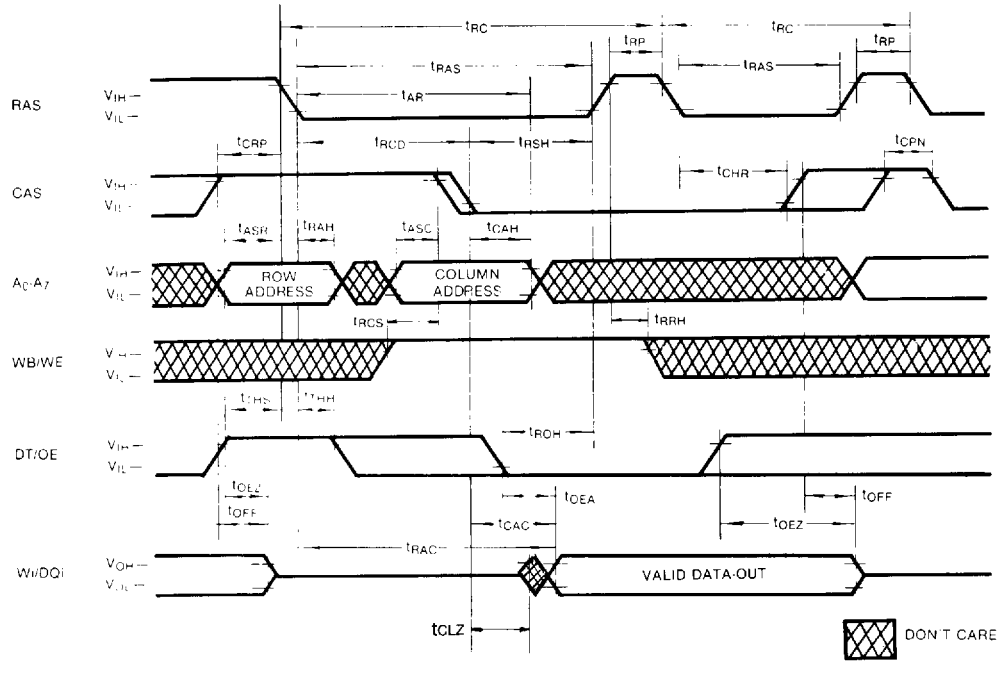


TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH CYCLE

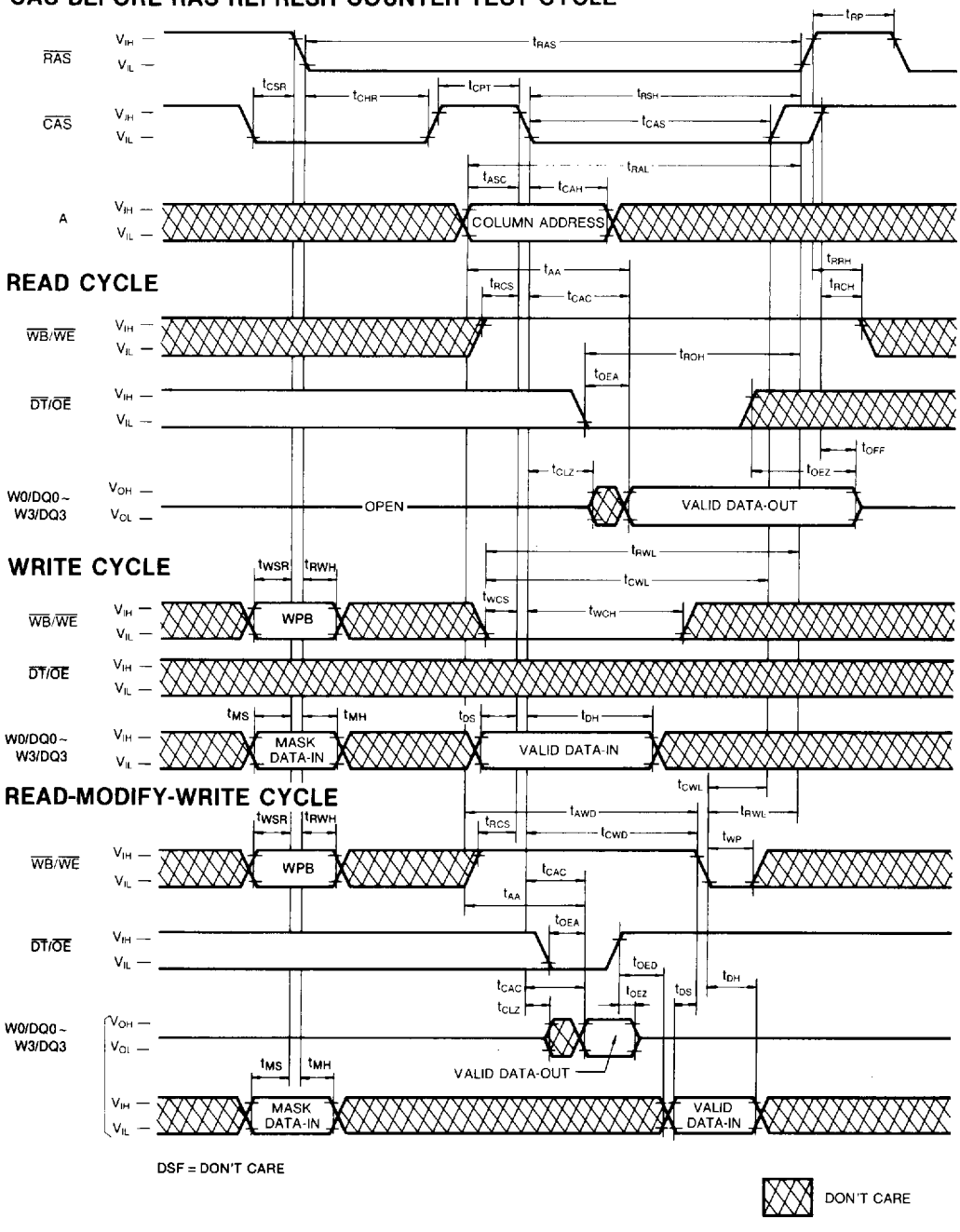


HIDDEN REFRESH CYCLE



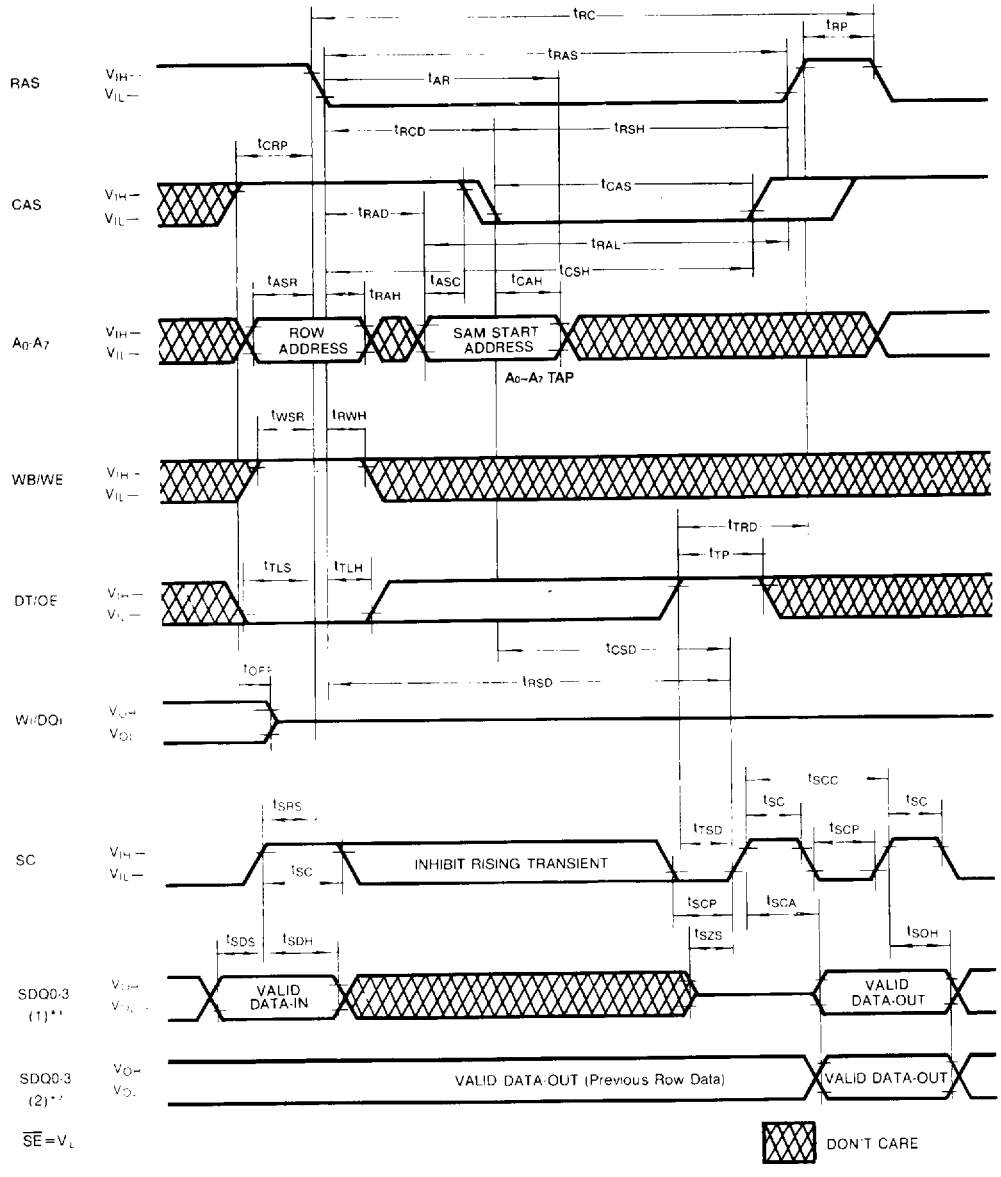
TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

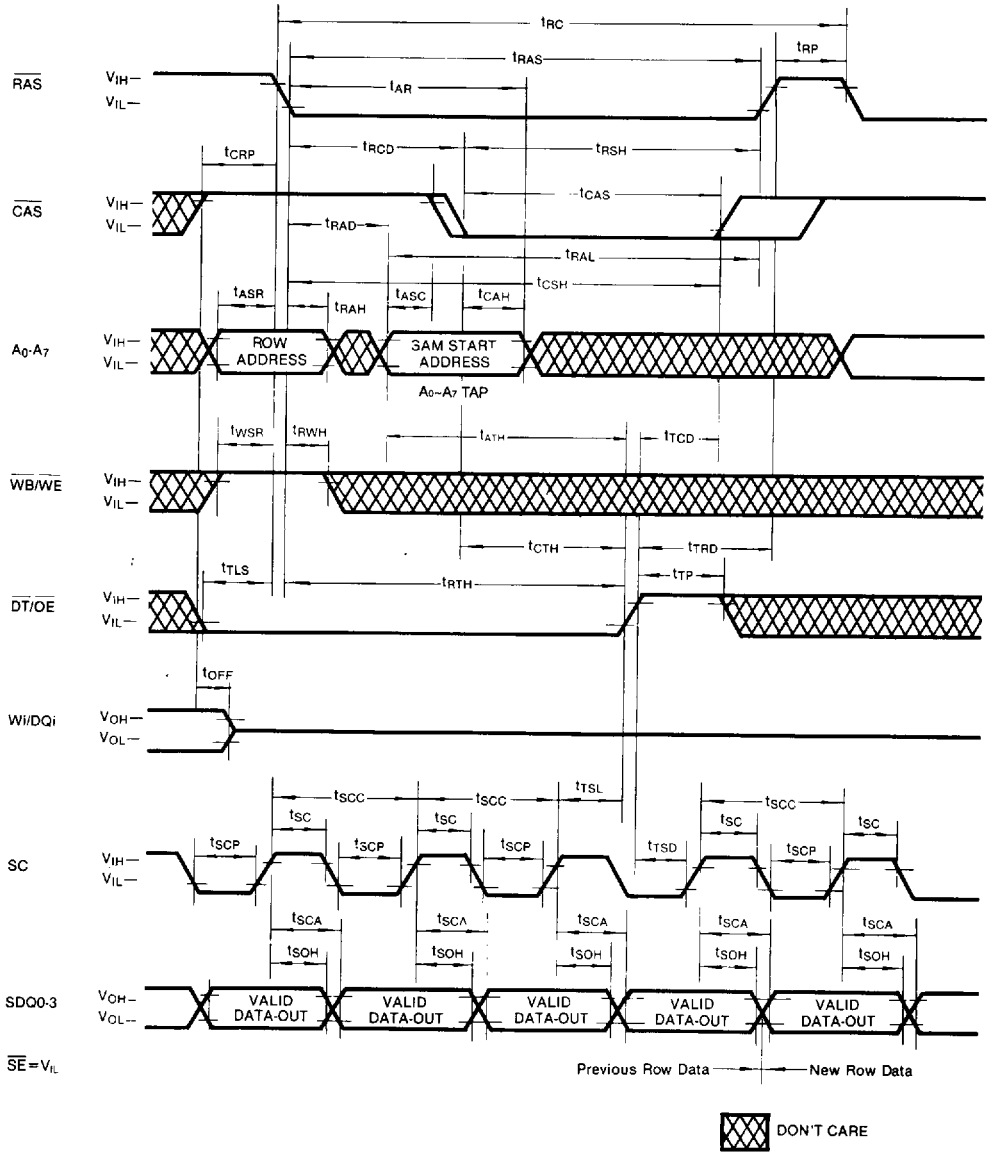
READ TRANSFER CYCLE



*1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as Read Transfer Cycle (1)
*2. When the previous data transfer cycle is a read transfer cycle, it is defined as Read Transfer Cycle (2).

TIMING DIAGRAMS (Continued)

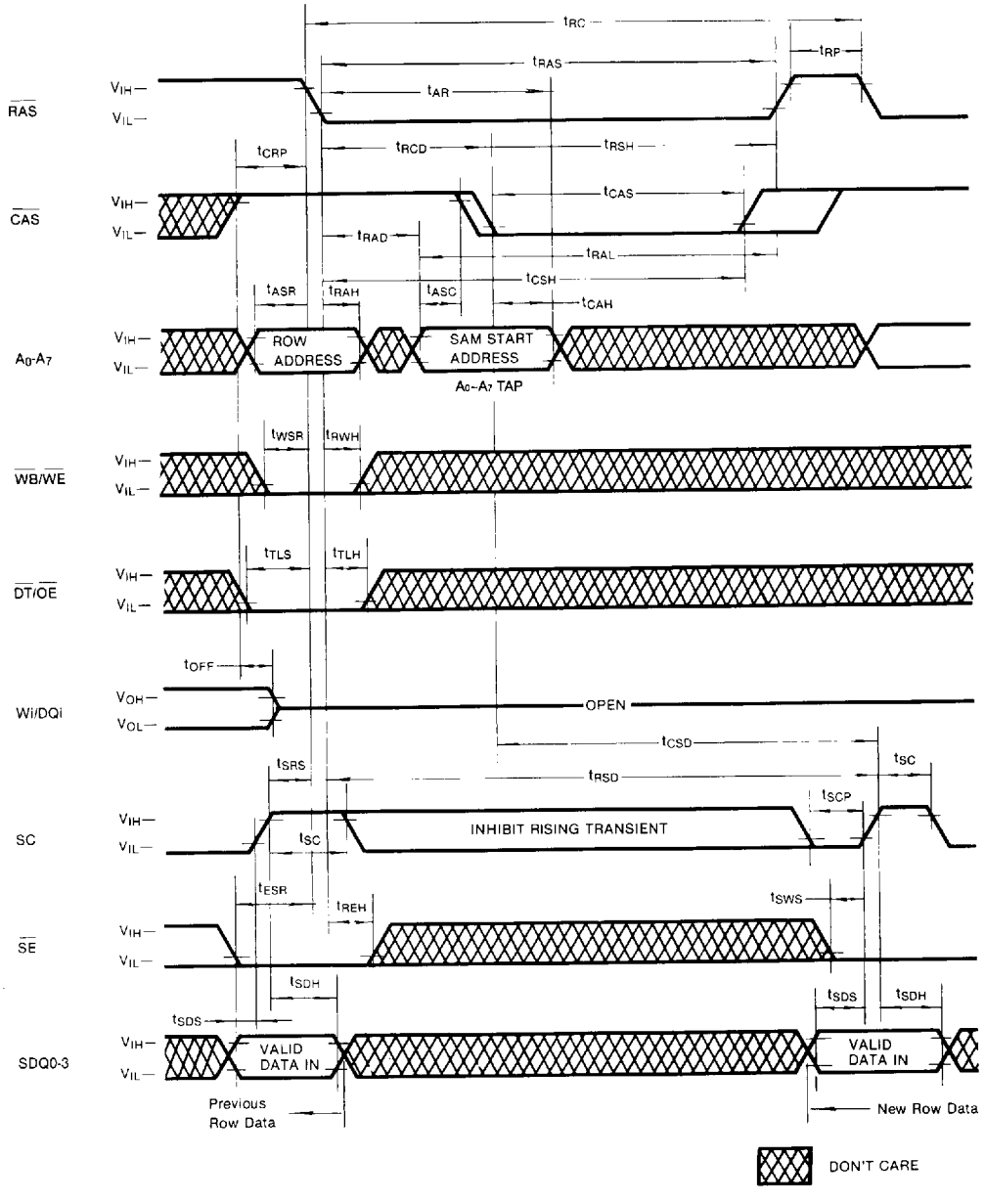
REAL TIME READ TRANSFER CYCLE



SAMSUNG ELECTRONICS

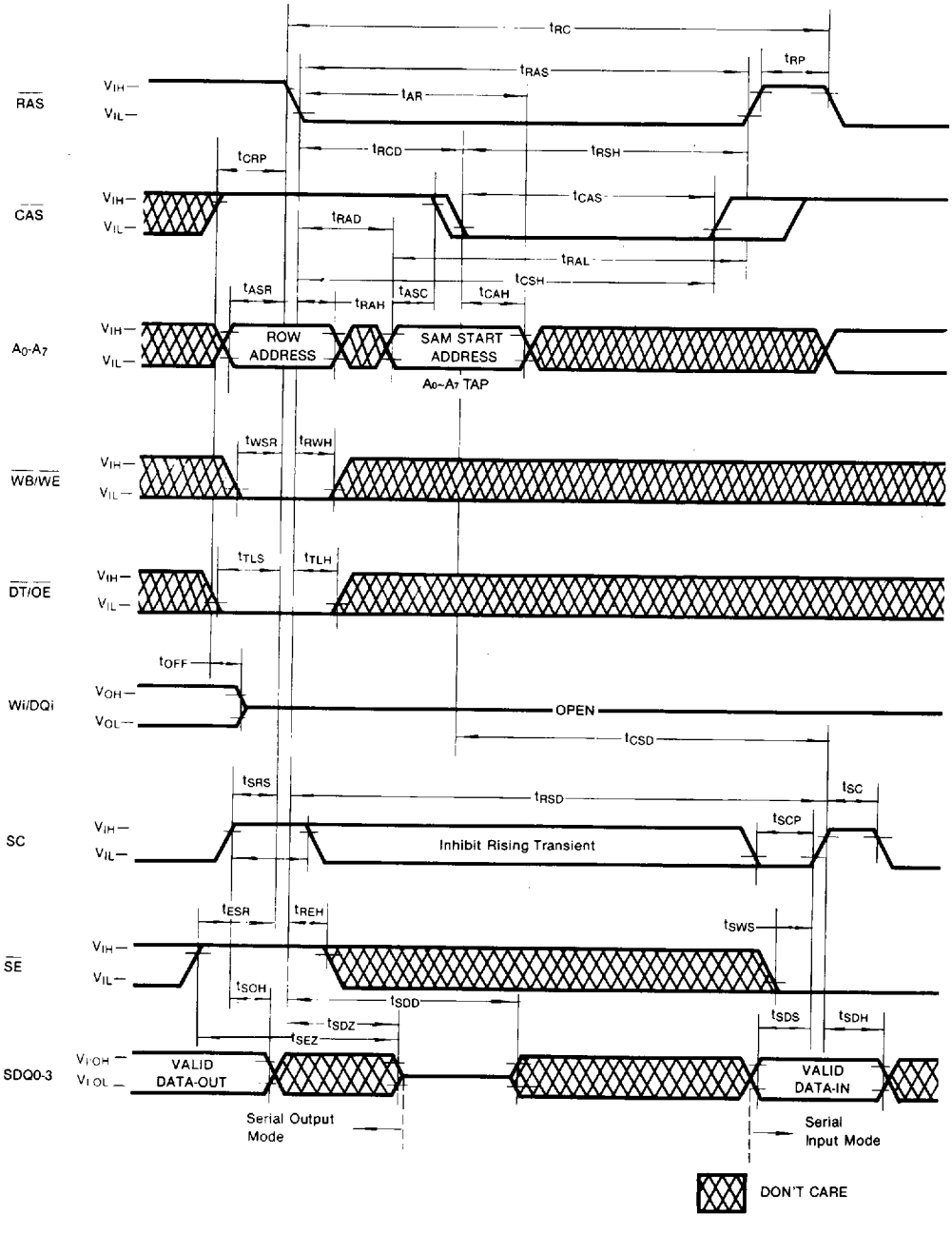
TIMING DIAGRAMS (Continued)

WRITE TRANSFER CYCLE



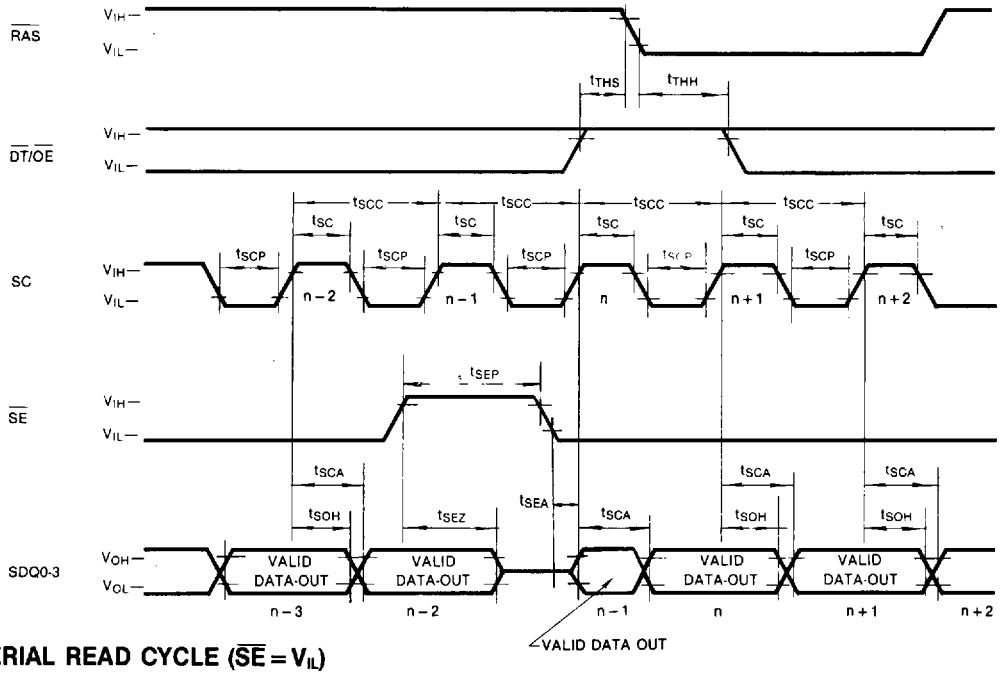
TIMING DIAGRAMS (Continued)

PSEUDO WRITE TRANSFER CYCLE

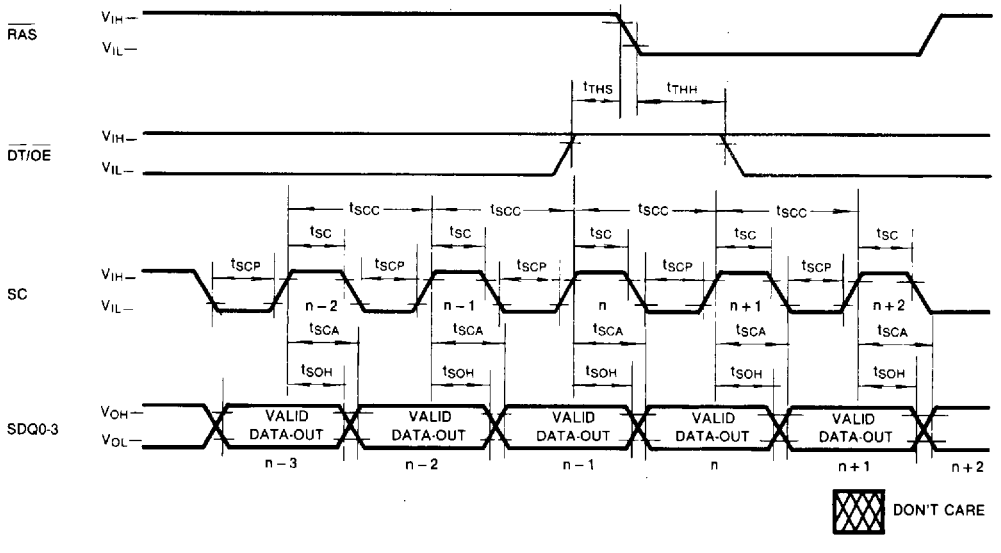


TIMING DIAGRAMS (Continued)

SERIAL READ CYCLE ($\overline{SE}$ CONTROLLED OUTPUTS)

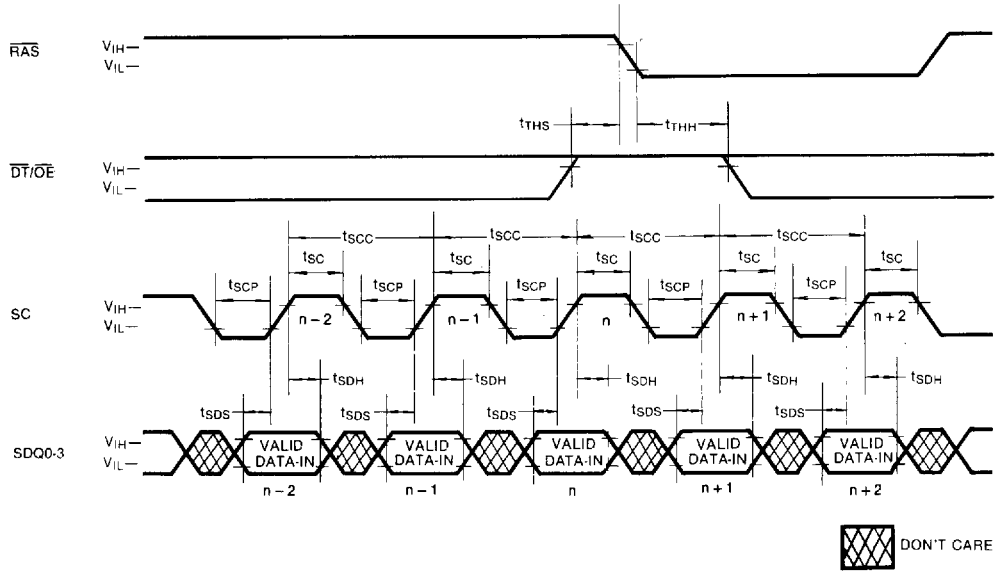


SERIAL READ CYCLE ($\overline{SE} = V_{IL}$)



TIMING DIAGRAMS (Continued)

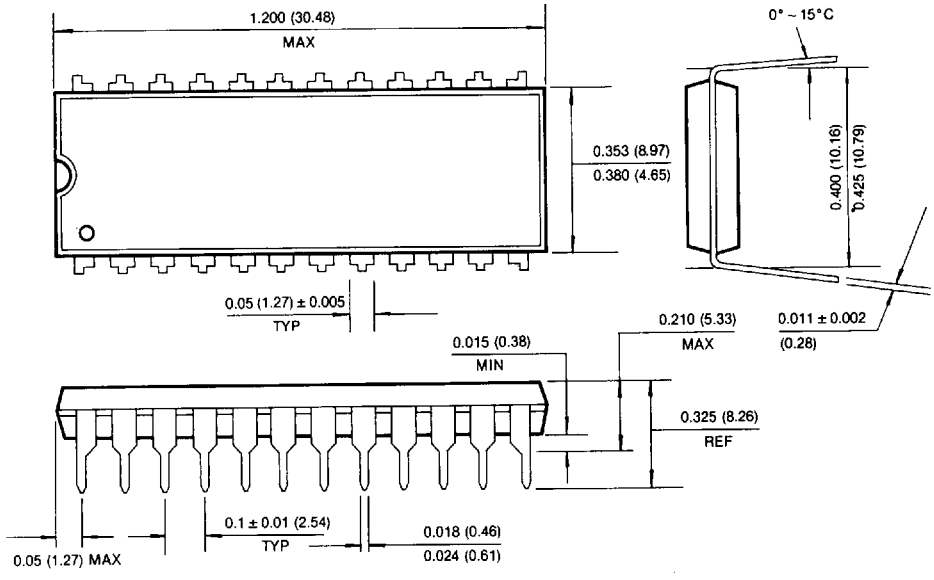
SERIAL WRITE CYCLE ($\overline{SE} = V_{IL}$)



PACKAGE DIMENSIONS

24-PIN PLASTIC DIP

Units: Inches (millimeters)



24-PIN PLASTIC ZIP