1M x 1Bit High-Speed CMOS SRAM

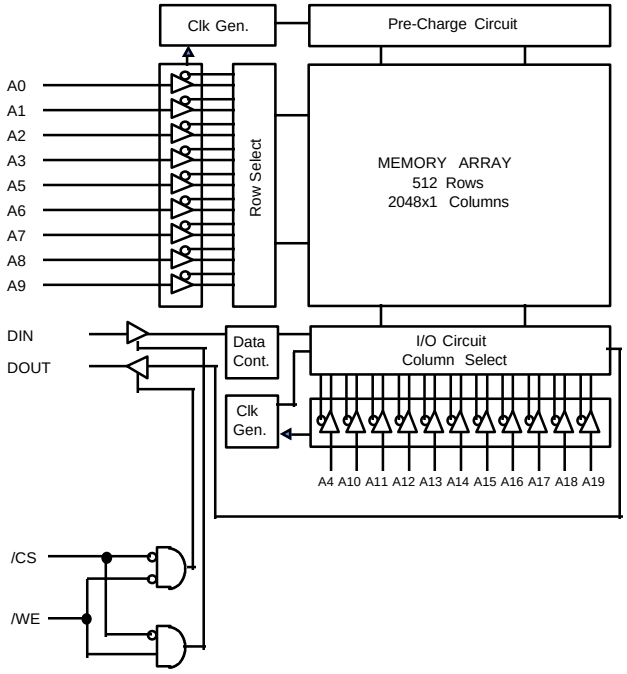
FEATURES

- Fast Access Time 20, 25, 35ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 40 mA(Max.)
  - (CMOS): 2 mA(Max.)
  - 0.5 mA(Max.) - L-ver.
  - Operating KM611001/L -20 : 130 mA(Max.)
  - KM611001/L -25 : 110 mA(Max.)
  - KM611001/L -35 : 100 mA(Max.)
- Single 5.0V ± 10% Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage : 2V(Min.)- L-Ver Only
- Standard Pin Configuration
  - KM611001P/LP : 28-DIP-400
  - KM611001J/LJ : 28-SOJ-400A

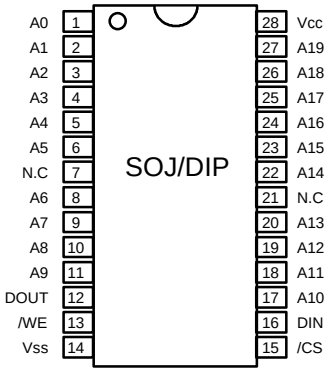
GENERAL DESCRIPTION

The KM611001/L is a 1,048,576-bit high-speed Static Random Access Memory organized as 1,048,576 words by 1 bit. The KM611001/L has separate input and output lines for fast read and write access. The device is fabricated using Samsung`s advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM611001/L is packaged in a 400 mil 28-pin plastic DIP or SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION *(TOP VIEW)*



PIN DESCRIPTION

Pin Name	Pin Function
A0-A19	Address Inputs
/WE	Write Enable
/CS	Chip Select
DIN	Data Input
DOUT	Data Output
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	$V_{IN,OUT}$	- 0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	- 0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	Tstg	- 65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input High Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) = -2.0 (Pulse Width ≤ 10ns) for I ≤ 20mA

** V_{IH}(Max) = V_{CC}+2.0V(Pulse width ≤ 10ns) for I ≤ 20mA

DC AND OPERATING CHARACTERISTICS

(T_A= 0 to 70 °C, V_{CC}=5.0V ± 10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	ILI	VIN=Vss to Vcc		-2	2	µA
Output Leakage Current	ILO	/CS=VIH or /OE=VIH or /WE=VIL V_{OUT}=Vss to Vcc		-2	2	µA
Operating Current	ICC	Min. Cycle, 100% Duty /CS=VIL, VIN=VIH or VIL, IOUT=0mA	20ns	-	130	mA
			25ns	-	110	
			35ns	-	100	
Standby Current	ISB	Min. Cycle, /CS=VIH		-	40	mA
	ISB1	f=0MHz, /CS ≥ Vcc-0.2V, VIN ≥ Vcc -0.2V or VIN ≤ 0.2V	Normal	-	2	mA
			L-ver	-	0.5	
Output Low Voltage	VOL	IOL=8mA		-	0.4	V
Output High Voltage	VOH	IOH = - 4mA		2.4	-	V

CAPACITANCE*(f=1MHz, TA =25 °C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	CIN	VIN=0V	-	7	pF
Input/Output Capacitance	CI/O	VI/O=0V	-	7	pF

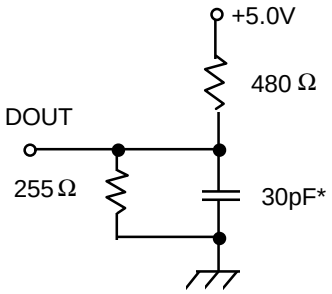
* Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

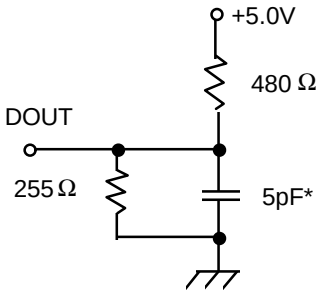
TEST CONDITIONS ON DATA RAM (TA= 0 to 70 °C, Vcc=5.0V± 10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3 V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
for tHZ, tLZ, tWHZ, tOW, tOLZ, & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM611001/L-20		KM611001/L-25		KM611001/L-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	20	-	25	-	35	-	ns
Address Access Time	tAA	-	20	-	25	-	35	ns
Chip Select to Output	tCO	-	20	-	25	-	35	ns
Chip Enable to Low-Z Output	tLZ	5	-	5	-	5	-	ns
Chip Disable to High-Z Output	tHZ	0	12	0	15	0	15	ns
Output Hold from Address Change	tOH	3	-	5	-	5	-	ns
Chip Select to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Select to Power Down Time	tPD	-	20	-	25	-	35	ns

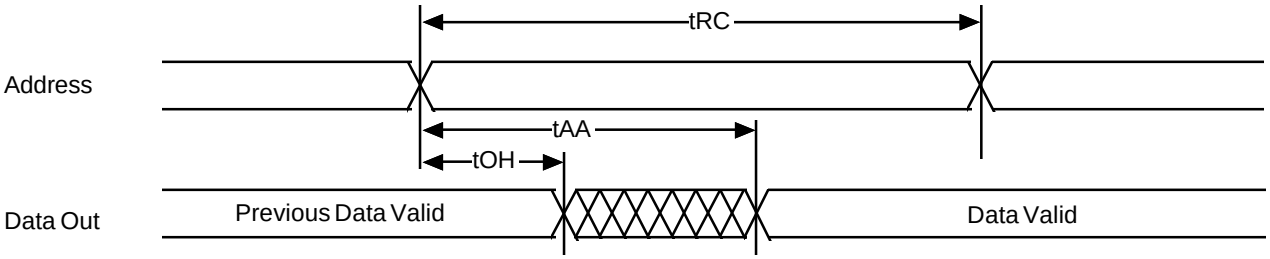
WRITE CYCLE

Parameter	Symbol	KM611001/L-20		KM611001/L-25		KM611001/L-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	20	-	25	-	35	-	ns
Chip Select to End of Write	tCW	17	-	20	-	30	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	17	-	20	-	30	-	ns
Write Pulse Width(/OE High)	tWP	15	-	20	-	25	-	ns
Write Pulse Width(/OE Low)	tWP	20	-	25	-	35	-	ns
Write Recovery Time	tWR	2	-	3	-	3	-	ns
Write to Output High-Z	tWHZ	0	8	0	10	0	12	ns
Data to Write Time Overlap	tDW	12	-	15	-	20	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	0	-	ns

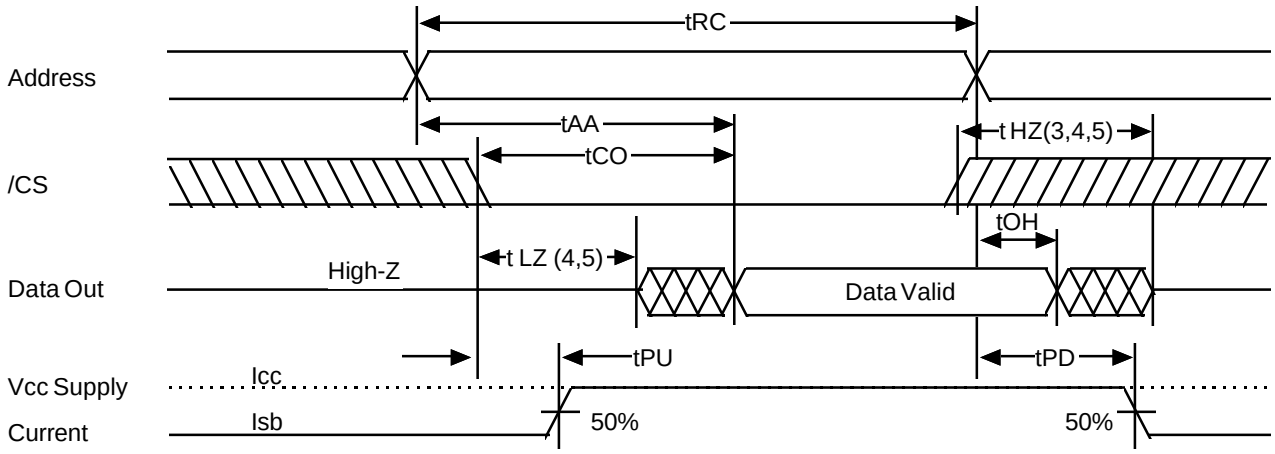
TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1) (Address Controlled)

(/CS=VIL, /WE=VIH)



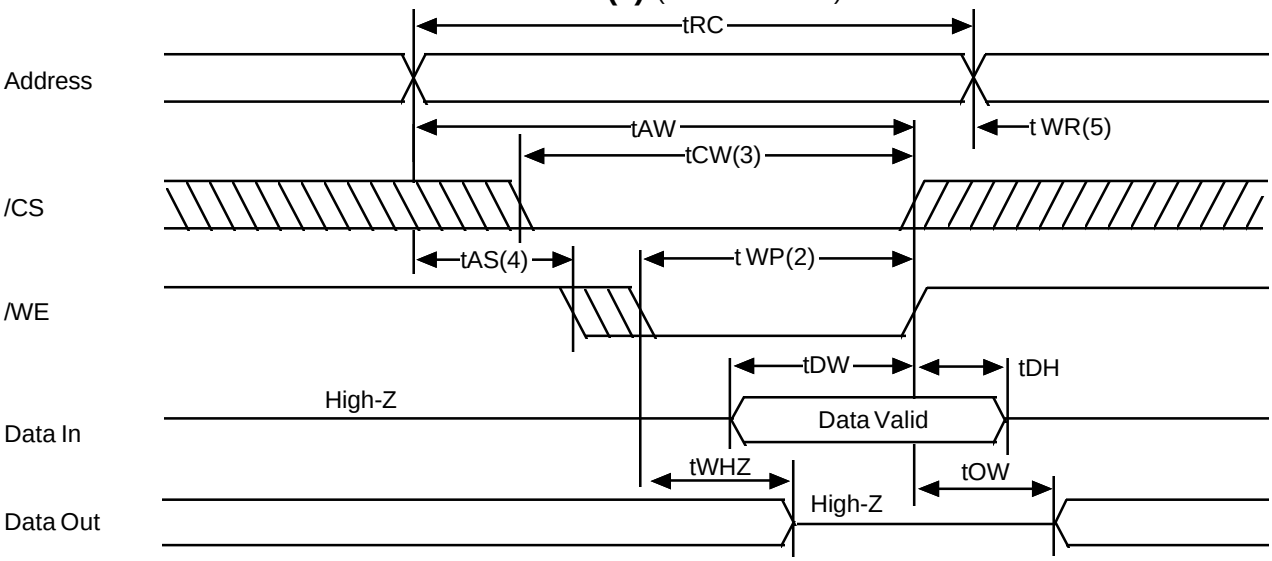
TIMING WAVE FORM OF READ CYCLE(2) (/WE=VIH)



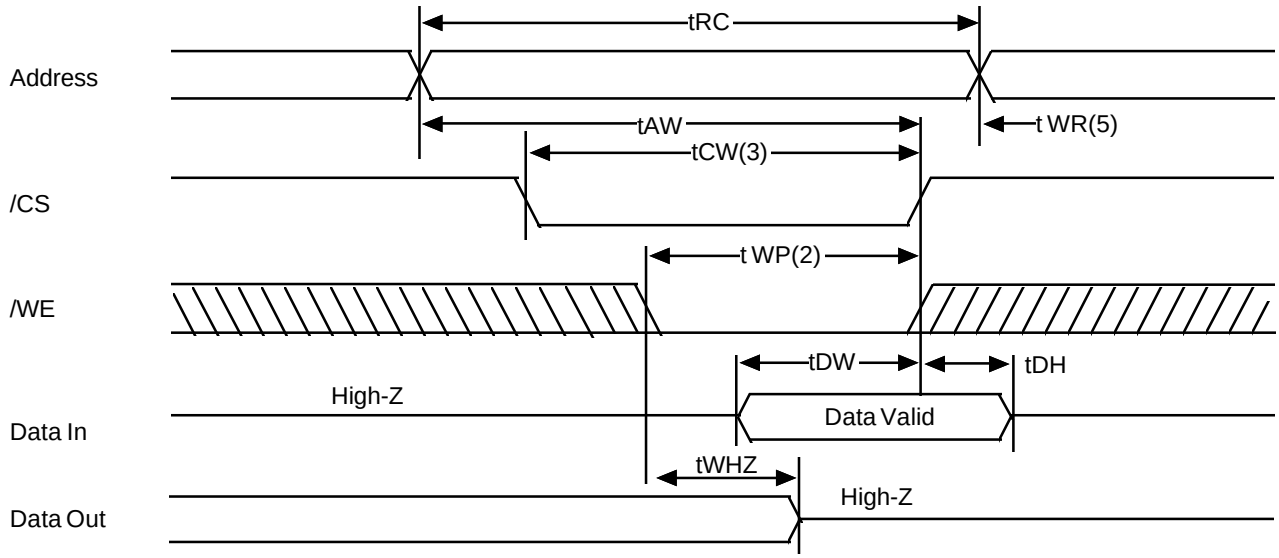
NOTES (READ CYCLE)

1. /WE is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. tHZ is defined as the time at which the output achieve the open circuit condition and is not referenced to VOH or VOL levels.
4. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
5. Transition is measured ± 200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with /CS=VIL
7. Address valid prior to coincident with /CS transition low.

TIMING WAVE FORM OF WRITE CYCLE(1) (/WE=Controlled)



TIMING WAVE FORM OF WRITE CYCLE(2) (/CS=Controlled)



NOTES (WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and a low /WE. A write begins at the latest transition among /CS going low and /WE going low; A write ends at the earliest transition among /CS going high and /WE going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of /CS going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS, or /WE going high.
6. If /CS goes low simultaneously with /WE going low or after /WE going low, the outputs remain high impedance state.
7. Dout is the read data of the new address.

FUNCTIONAL DESCRIPTION

/CS	/WE	Mode	I/O Pin	Supply Current
H	X*	Not Select	High-Z	ISB, ISB1
L	H	Read	DOUT	ICC
L	L	Write	DIN	ICC

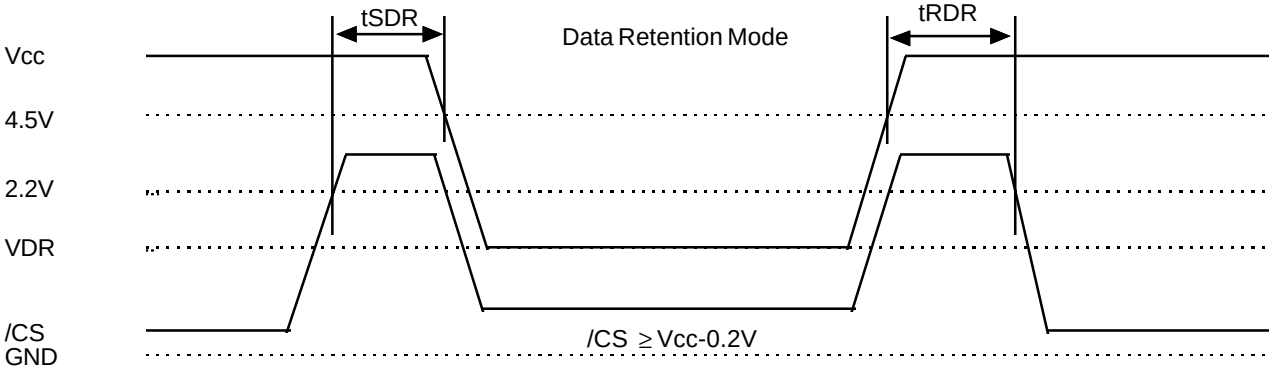
*Note : X means Don't Care.

DATA RETENTION CHARACTERISTICS* (TA= 0 to 70 °C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	VDR	/CS ≥ Vcc-0.2V	2.0	-	5.5	V
Data Retention Current	IDR	Vcc=3.0V, /CS ≥ Vcc-0.2V VIN ≥ Vcc-0.2V or VIN ≤ 0.2V	-	-	0.1	mA
Data Retention Set-Up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Wave form(below)	5	-	-	ms

* L-version only

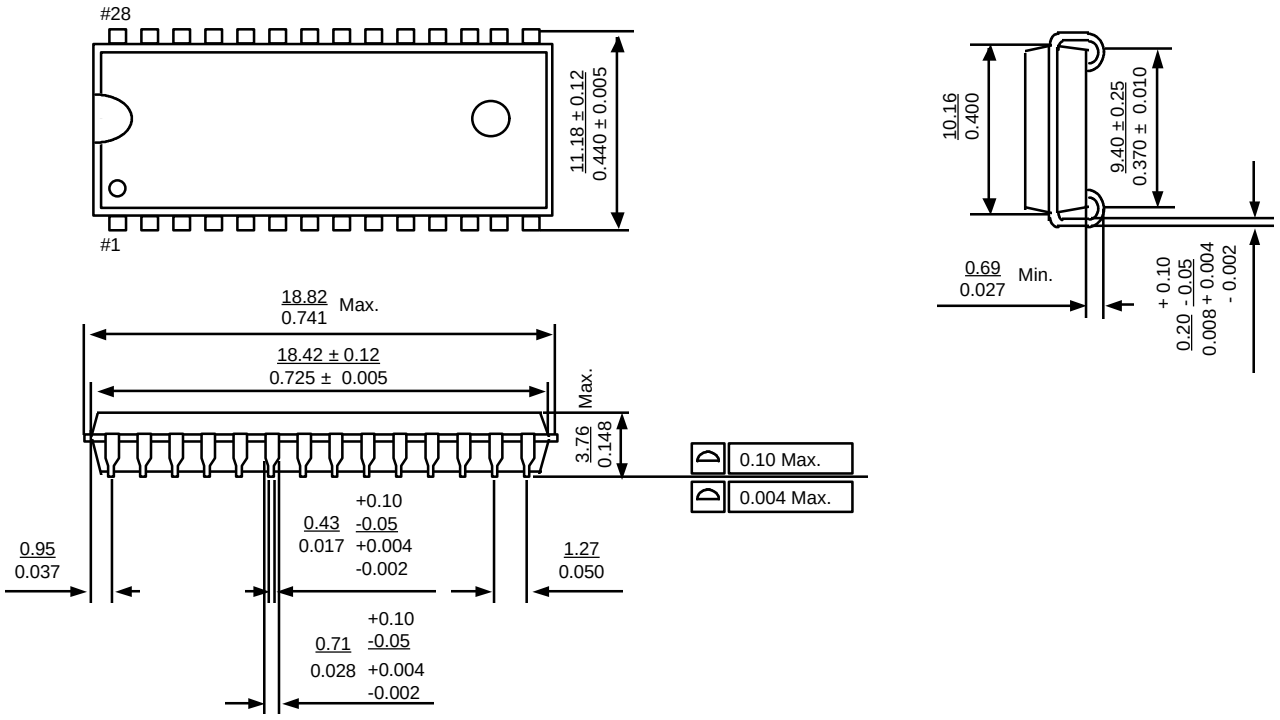
DATA RETENTION WAVE FORM (/CS Controlled)



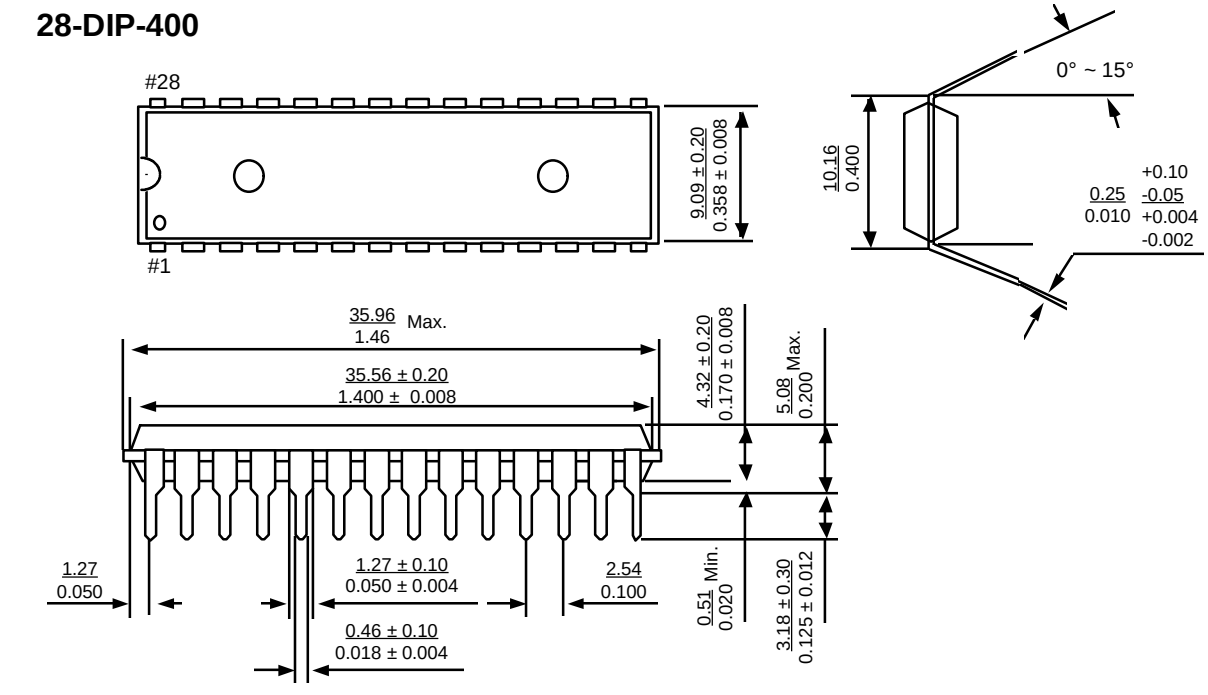
PACKAGE DIMENSIONS

Unit: mm / Inch

28-SOJ-400A



28-DIP-400



*Note : Do not include mold protrusion