

Document Title**64K x16 bit Super Low Power and Low Voltage Full CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	March 15, 1996	Advance
0.1	Revise - Erase 100ns part from KM616FS1000 Family - Add 150ns part on KM616FS1000 Family - Add 32-sTSOP1 new package - Add high power version ISB1=5.0μA(Max) - Change V _{DR} (Min) 1.0 to 1.5V	June 3, 1996	Preliminary
1.0	Finalize - Concept change high power version to low low power version ISB1=5.0μA(Max) - Change super low power version with special handling ISB1=1.0μA(Max) - Reduce I _{cc} & I _{cc1} Read : 15mA to 10mA Write : 25mA to 20mA	December 1, 1996	Final
2.0	Revise - Change datasheet format - Erase reverse type package	February 26, 1998	Final

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64Kx16 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology : Full CMOS
- Organization : 64Kx16 bit
- Power Supply Voltage
 - KM616FV1000 Family : 3.0V ~ 3.6V
 - KM616FS1000 Family : 2.3V ~ 3.3V
 - KM616FR1000 Family : 1.8V ~ 2.7V
- Low Data Retention Voltage : 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type : 44-TSOP2-400F

GENERAL DESCRIPTION

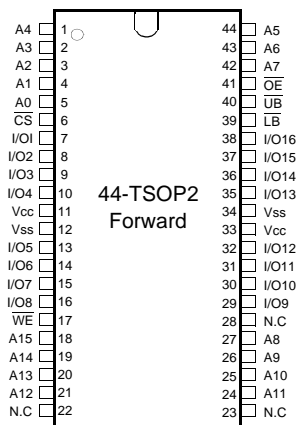
The KM616FV1000, KM616FS1000 and KM616FR1000 families are fabricated by SAMSUNG's advanced Full CMOS process technology. The families support various operating temperature ranges for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max)	Operating (I _{CC2} , Max)	
KM616FV1000	Commercial(0~70°C)	3.0~3.6V	70 ¹⁾ /85@V _{CC} =3.3±0.3V	5μA ²⁾	80mA	44-TSOP2 Forward
KM616FS1000		2.3~3.3V	70 ¹⁾ /85@V _{CC} =3.0±0.3V 120 ¹⁾ /150@V _{CC} =2.5±0.2V		80mA 50mA	
KM616FR1000		1.8~2.7V	300 ¹⁾ @V _{CC} =2.0±0.2V		20mA	
KM616FV1000I	Industrial(-40~85°C)	3.0~3.6V	70 ¹⁾ /85@V _{CC} =3.3±0.3V		80mA	
KM616FS1000I		2.3~3.3V	70 ¹⁾ /85@V _{CC} =3.0±0.3V 120 ¹⁾ /150@V _{CC} =2.5±0.2V		80mA 50mA	
KM616FR1000I		1.8~2.7V	300 ¹⁾ @V _{CC} =2.0±0.2V		20mA	

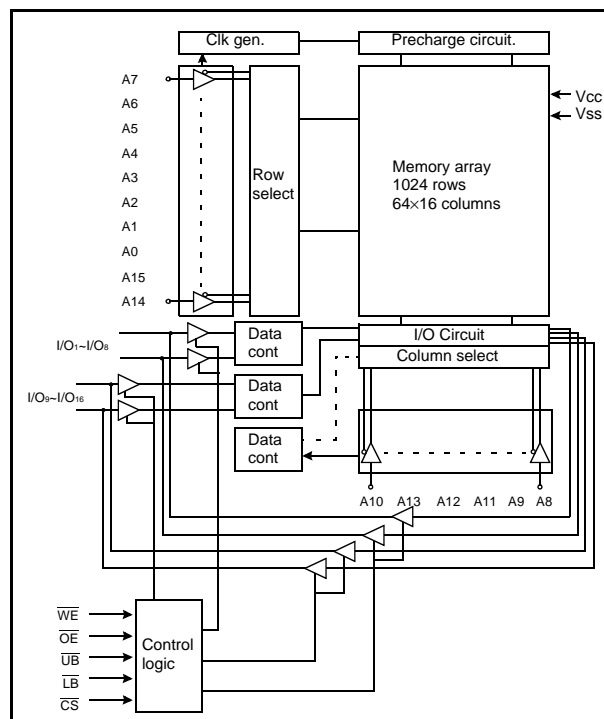
1. The parameter is measured with 30pF test load.
2. Super low power product=1μA with special handling.

PIN DESCRIPTION



Name	Function	Name	Function
\overline{CS}	Chip Select Input	\overline{LB}	Lower Byte(I/O _{1~8})
\overline{OE}	Output Enable Input	\overline{UB}	Upper Byte(I/O _{9~16})
\overline{WE}	Write Enable Input	Vcc	Power
A _{0~A15}	Address Inputs	Vss	Ground
I/O _{1~I/O16}	Data Inputs/Outputs	N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
KM616FV1000T-7 KM616FV1000T-8	44-TSOP2 F, 70ns, 3.3V, LL 44-TSOP2 F, 85ns, 3.3V, LL	KM616FV1000TI-7 KM616FV1000TI-8	44-TSOP2 F, 70ns, 3.3V, LL 44-TSOP2 F, 85ns, 3.3V, LL
KM616FS1000T-12 KM616FS1000T-15	44-TSOP2 F, 120/70ns, 2.5/3.0V, LL 44-TSOP2 F, 150/85ns, 2.5/3.0V, LL	KM616FS1000TI-12 KM616FS1000TI-15	44-TSOP2 F, 120/70ns, 2.5/3.0V, LL 44-TSOP2 F, 150/85ns, 2.5/3.0V, LL
KM616FR1000T-30	44-TSOP2 F, 300ns, 2.0/2.5V, LL	KM616FR1000TI-30	44-TSOP2 F, 300ns, 2.0/2.5V, LL

FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
L	H	H	X ¹⁾	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to 3.6V ²⁾	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 4.0V ³⁾	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-55 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM616FV1000, KM616FS1000, KM616FR1000
		-40 to 85	°C	KM616FV1000I, KM616FS1000I, KM616FR1000I
Soldering temperature and time	T _{SOLDER}	260°C, 5sec(Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. V_{IN}/V_{OUT}=-0.2 to 3.9V for KM616FV1000 Family.

3. V_{CC}=-0.2 to 4.6V for KM616FV1000 Family.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit	
Supply voltage	V _{CC}	KM616FV1000 Family	3.0	3.3	3.6	V	
		KM616FS1000 Family	2.3	2.5/3.0	3.3		
		KM616FR1000 Family	1.8	2.0/2.5	2.7		
Ground	V _{SS}	All Family	0	0	0	V	
Input high voltage	V _{IH}	KM616FV1000 Family	V _{CC} =3.3±0.3V	2.2	-	V _{CC} +0.2 ²⁾	V
		KM616FS1000 Family	V _{CC} =3.0±0.3V	2.2			
			V _{CC} =2.5±0.2V	2.0			
		KM616FR1000 Family	V _{CC} =2.5±0.2V	2.0			
V _{CC} =2.0±0.2V	1.6						
Input low voltage	V _{IL}	All Family	-0.2 ³⁾	-	0.4	V	

Note

 1 Commercial Product : T_A=0 to 70°C, unless otherwise specified

 Industrial Product : T_A=-40 to 85°C, unless otherwise specified

 2. Overshoot : V_{CC} + 1.0V in case of pulse width ≤20ns

3. Undershoot : -1.0V in case of pulse width ≤20ns

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

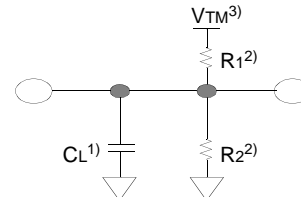
Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	\overline{CS} =V _{IH} or \overline{OE} =V _{IH} or \overline{WE} =V _{IL} , V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply current	I _{CC}	I _{IO} =0mA, \overline{CS} =V _{IL} , V _{IN} =V _{IL} or V _{IH} , Read	-	-	2	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, \overline{CS} ≤0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	Read	-	-	5	mA
			Write	-	-	20	
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, \overline{CS} =V _{IL} , V _{IN} =V _{IL} or V _{IH}	V _{CC} =3.3V@70ns	-	-	65	mA
			V _{CC} =2.7V@120ns	-	-	55	
V _{CC} =2.2V@300ns			-	-	20		
Output low voltage	V _{OL}	I _{OL} 2.1mA at V _{CC} =3.0/3.3V 0.5mA at V _{CC} =2.5V 0.33mA at V _{CC} =2.0V	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} -1.0mA at V _{CC} =3.0/3.3V -0.5mA at V _{CC} =2.5V -0.44mA at V _{CC} =2.0V	2.4	-	-	V	
			2.0	-	-		
			1.6	-	-		
Standby Current(TTL)	I _{SB}	\overline{CS} =V _{IH} , Other inputs=V _{IL} or V _{IH}	-	-	0.3	mA	
Standby Current(CMOS)	I _{SB1}	\overline{CS} ≥V _{CC} -0.2V, Other inputs=0-V _{CC}	-	-	5 ¹⁾	μA	

1. Super low power product=1μA with special handling.

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

- Input pulse level : 0.4 to 2.2V for Vcc=3.3V, 3.0V, 2.5V
0.4 to 1.8V for Vcc=2.0V
- Input rising and falling time : 5ns
- Input and output reference voltage : 1.5V for Vcc=3.3V, 3.0V
1.1V for Vcc=2.5V
0.9V for Vcc=2.0V
- Output load (See right) :CL=100pF+1TTL
CL=30pF+1TTL



1. Including scope and jig capacitance
2. R1=3070Ω, R2=3150Ω
3. VTM=2.8V for Vcc=3.0/3.3V
=2.3V for Vcc=2.5V
=1.8V for Vcc=2.0V

AC CHARACTERISTICS

(Commercial product :TA=0 to 70°C, Industrial product : TA=-40 to 85°C
KM616FV1000 Family : Vcc=3.0~3.6V, KM616FS1000 Family : Vcc=2.3~3.3V,
KM616FR1000 Family : Vcc=1.8~2.7V)

Parameter List	Symbol	Speed Bins										Units	
		70ns		85ns		120ns		150ns		300ns			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read	Read cycle time	tRC	70	-	85	-	120	-	150	-	300	-	ns
	Address access time	tAA	-	70	-	85	-	120	-	150	-	300	ns
	Chip select to output	tCO	-	70	-	85	-	120	-	150	-	300	ns
	Output enable to valid output	tOE	-	35	-	45	-	60	-	75	-	150	ns
	UB, LB Access Time	tBA	-	35	-	45	-	60	-	75	-	150	ns
	Chip select to low-Z output	tLZ	10	-	10	-	20	-	20	-	50	-	ns
	Output enable to low-Z output	tOLZ, tBLZ	5	-	5	-	20	-	20	-	30	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	35	0	40	0	60	ns
	Output disable to high-Z output	tOHZ, tBHZ	0	25	0	25	0	35	0	40	0	60	ns
	Output hold from address change	tOH	10	-	15	-	15	-	15	-	30	-	ns
Write	Write cycle time	tWC	70	-	85	-	120	-	150	-	300	-	ns
	Chip select to end of write	tCW	65	-	70	-	100	-	120	-	300	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	65	-	70	-	100	-	120	-	300	-	ns
	Write pulse width	tWP	55	-	60	-	80	-	100	-	200	-	ns
	UB, LB Valid to End of Write	tBW	65	-	70	-	100	-	120	-	300	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	35	0	40	0	60	ns
	Data to write time overlap	tdW	30	-	35	-	50	-	60	-	120	-	ns
	Data hold from write time	tdH	0	-	0	-	0	-	0	-	0	-	ns
End write to output low-Z	tOW	5	-	5	-	5	-	5	-	20	-	ns	

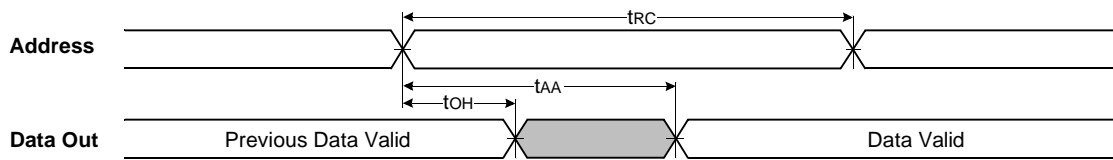
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	VDR	CS ≥ Vcc-0.2V	1.5	-	3.6	V
Data retention current	IDR	Vcc=3.0V	-	-	5.0 ¹⁾	μA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	trDR		tRC	-	-	

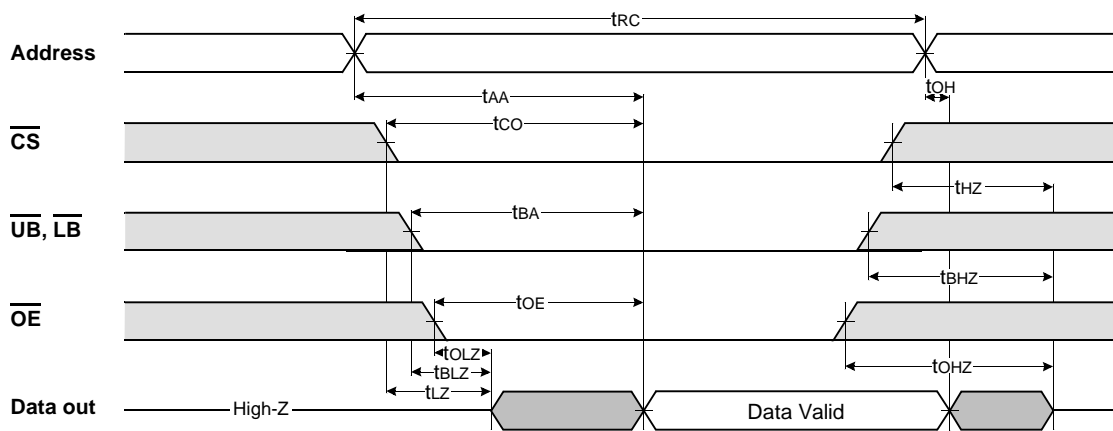
1. Super low power product=1μA with special handling.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, \overline{UB} or/and $\overline{LB}=V_{IL}$)



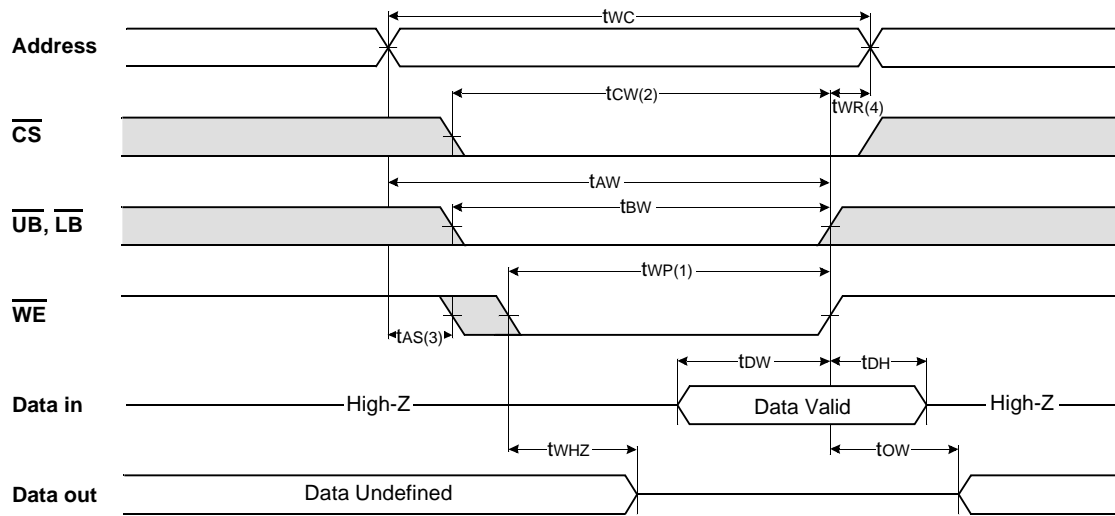
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



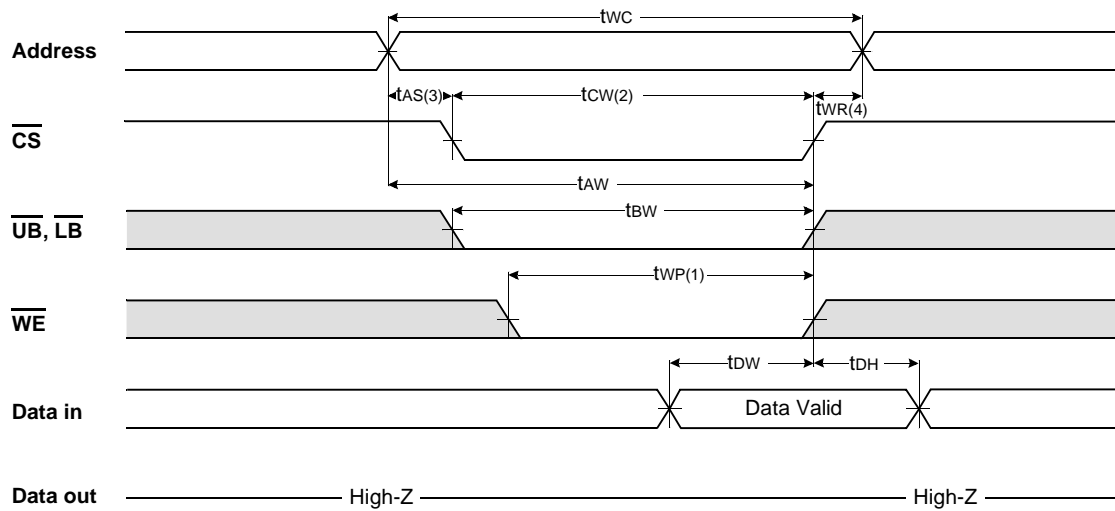
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

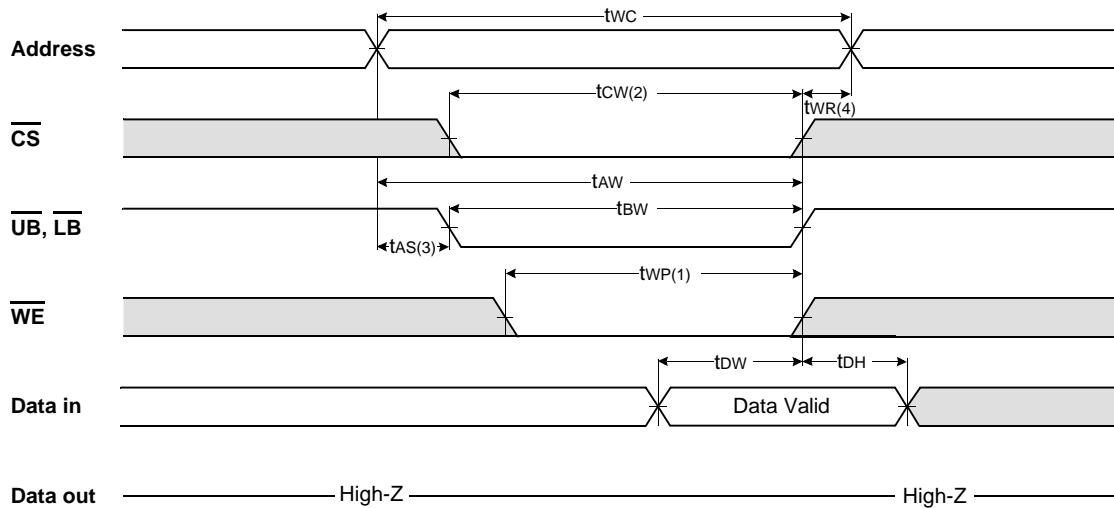
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{CS} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{UB} , \overline{LB} Controlled)

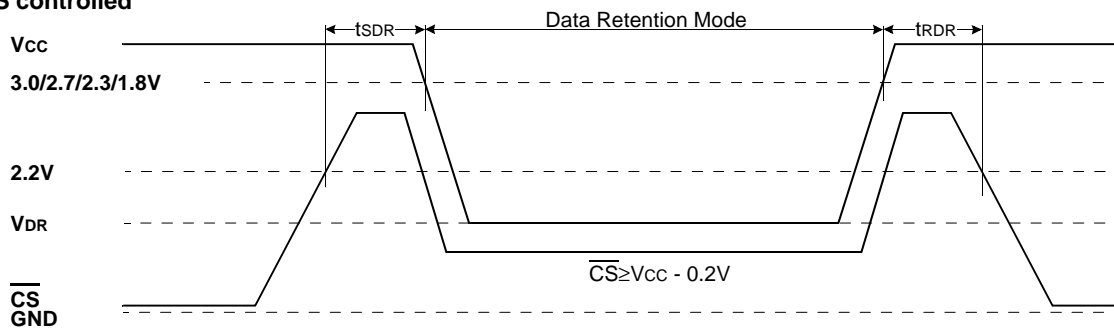


NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.

DATA RETENTION WAVE FORM

\overline{CS} controlled



PACKAGE DIMENSIONS

Unit : millimeter(inch)

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)

