Document Title

32Kx8 bit Low Power and Low Voltage CMOS Static RAM

Revision History

Revision No.	History	Draft Data	Remark
0.0	Design target	February 12, 1993	Advance
0.1	Initial draft	November 2, 1993	Preliminary
1.0	Finalize	September 24, 1994	Final
2.0	Revised	August 12, 1995	Final
3.0	Revised - One datasheet for commercial, extended, industrial product. - Increased KM62V256C Family's I_{CC2} 30 to 35mA. - Increased tDW 50 to 60ns for KM62U256C Family. - Remove SOP package from KM62V256C Family.	April 1, 1997	Final
4.0	Revised - Change datasheets format. - Improved power dissipation : 0.7W→1W	February 12, 1998	Final

32Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : Poly Load
- Organization : 32Kx8
- Power Supply Voltage
  KM62V256C family : 2.7~3.3V
  KM62U256C family : 3.0~3.6V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 28-SOP-450, 28-TSOP1-0813.4F/R

GENERAL DESCRIPTION

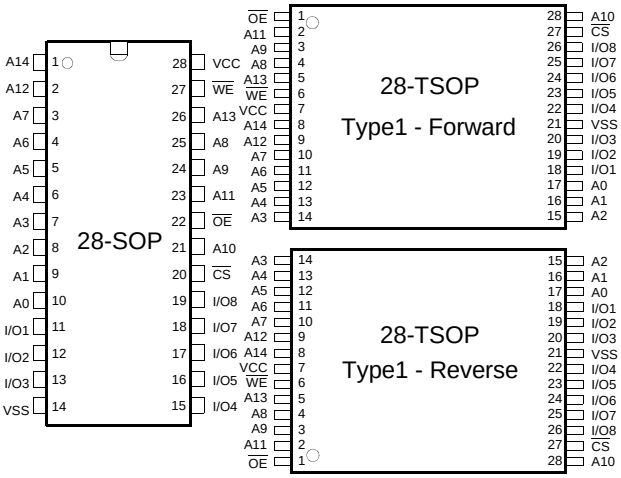
The KM62V256C and KM62U256C families are fabricated by SAMSUNG′s advanced CMOS process technology. The families support various operating temperature ranges and has various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2}, Max)	
KM62V256CL-L	Commercial(0~70°C)	3.0 ~ 3.6V	70[1]/100	10µA	35mA	28-SOP[2] 28-TSOP1-F/R
KM62U256CL-L		2.7 ~ 3.3V	85[1]/100	10µA		
KM62V256CLE-L	Extended(-25~85°C)	3.0 ~ 3.6V	70[1]/100	20µA		
KM62U256CLE-L		2.7 ~ 3.3V	85[1]/100	15µA		
KM62V256CL-L	Industrial(-40~85°C)	3.0 ~ 3.6V	70[1]/100	20µA		
KM62U256CLI-L		2.7 ~ 3.3V	85[1]/100	15µA		

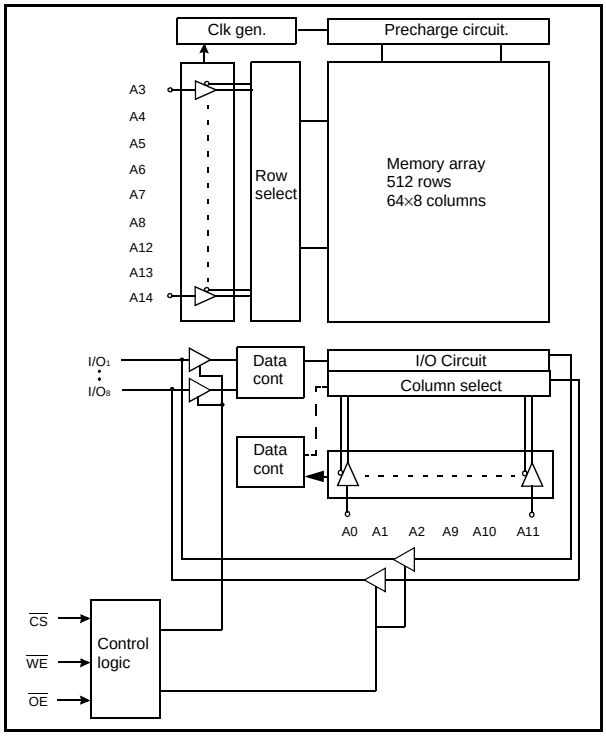
1. The parameter is measured with 30pF test load.
2. The device with 100ns SOP package in 3.0~3.6V Vcc range which is not produced.

PIN DESCRIPTION



Pin Name	Function
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
A_0~A_{14}	Address Inputs
I/O_1~I/O_8	Data Inputs/Outputs
Vcc	Power
Vss	Ground

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Commercial Temperature Products (0~70°C)		Extended Temperature Products (-25~85°C)		Industrial Temperature Products (-40~85°C)	
Part Name	**Function**	**Part Name**	**Function**	**Part Name**	**Function**
KM62V256CLG-7L	28-SOP, 70ns, 3.3V	KM62V256CLGE-7L	28-SOP, 70ns, 3.3V	KM62V256CLGI-7L	28-SOP, 70ns, 3.3V
KM62V256CLG-10L	28-SOP, 100ns, 3.3V	KM62V256CLGE-10L	28-SOP, 100ns, 3.3V	KM62V256CLGI-10L	28-SOP, 100ns, 3.3V
KM62V256CLTG-7L	28-TSOP F, 70ns, 3.3V	KM62V256CLTGE-7L	28-TSOP F, 70ns, 3.3V	KM62V256CLTGI-7L	28-TSOP F, 70ns, 3.3V
KM62V256CLTG-10L	28-TSOP F, 100ns, 3.3V	KM62V256CLTGE-10L	28-TSOP F, 100ns, 3.3V	KM62V256CLTGI-10L	28-TSOP F, 100ns, 3.3V
KM62V256CLRG-7L	28-TSOP R, 70ns, 3.3V	KM62V256CLRGE-7L	28-TSOP R, 70ns, 3.3V	KM62V256CLRGI-7L	28-TSOP R, 70ns, 3.3V
KM62V256CLRG-10L	28-TSOP R, 100ns, 3.3V	KM62V256CLRGE-10L	28-TSOP R, 100ns, 3.3V	KM62V256CLRGI-10L	28-TSOP R, 100ns, 3.3V
KM62U256CLG-8L	28-SOP, 85ns, 3.0V	KM62U256CLGE-8L	28-SOP, 85ns, 3.0V	KM62U256CLGI-8L	28-SOP, 85ns, 3.0V
KM62U256CLG-10L	28-SOP, 100ns, 3.0V	KM62U256CLGE-10L	28-SOP, 100ns, 3.0V	KM62U256CLGI-10L	28-SOP, 100ns, 3.0V
KM62U256CLTG-8L	28-TSOP F, 85ns, 3.0V	KM62U256CLTGE-8L	28-TSOP F, 85ns, 3.0V	KM62U256CLTGI-8L	28-TSOP F, 85ns, 3.0V
KM62U256CLTG-10L	28-TSOP F, 100ns, 3.0V	KM62U256CLTGE-10L	28-TSOP F, 100ns, 3.0V	KM62U256CLTGI-10L	28-TSOP F, 100ns, 3.0V
KM62U256CLRG-8L	28-TSOP R, 85ns, 3.0V	KM62U256CLRGE-8L	28-TSOP R, 85ns, 3.0V	KM62U256CLRGI-8L	28-TSOP R, 85ns, 3.0V
KM62U256CLRG-10L	28-TSOP R, 100ns, 3.0V	KM62U256CLRGE-10L	28-TSOP R, 100ns, 3.0V	KM62U256CLRGI-10L	28-TSOP R, 100ns, 3.0V

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X[1)]	X[1)]	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X[1)]	L	Din	Write	Active

1. X means don't care(Must be low or high state.)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to V_{CC}+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 4.6	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	°C	-
Operating Temperature	T_A	0 to 70	°C	KM62V256CL-L, KM62U256CL-L
		-25 to 85	°C	KM62V256CLE-L, KM62U256CLE-L
		-40 to 85	°C	KM62V256CLI-L, KM62U256CLI-L
Soldering temperature and time	T_{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	Vcc	KM62V256C Family KM62U256C Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	Vss	All	0	0	0	V
Input high voltage	V_{IH}	KM62V256C, KM62U256C Family	2.2	-	Vcc+0.3V[2)]	V
Input low voltage	V_{IL}	KM62V256C, KM62U256C Family	-0.3[3)]	-	0.4	V

Note:
1. Commercial Product : T_A=0 to 70°C, otherwise specified
   Extended Product : T_A=-25 to 85°C, unless otherwise specified
   Industrial Product : T_A=-40 to 85°C, otherwise specified
2. Overshoot : V_{CC}+3.0V in case of pulse width ≤ 30ns
3. Undershoot : -3.0V in case of pulse width ≤ 30ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

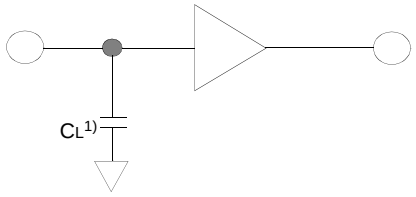
Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	µA
Operating power supply	I_{CC}	I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}		-	1.0	2.0	mA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS}$≤0.2V, V_{IN}≤0.2V, V_{IN}≥Vcc -0.2V		-	2.5	5	mA
	I_{CC2}	Cycle time=Min,100% duty, I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}		-	20	35	mA
Output low voltage	V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-1.0mA		2.2	-	-	V
Standby Current(TTL)	I_{SB}	$\overline{CS}$=V_{IH}, Other inputs=V_{IH} or V_{IL}		-	-	0.3	mA
Standby Current(CMOS)	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, Other inputs=0~Vcc	KM62V256CL-L KM62V256CLE-L KM62V256CLI-L	- - -	1.5 1.5 1.5	10 20 20	µA
			KM62U256CL-L KM62U256CLE-L KM62U256CLI-L	- - -	1.0 1.0 1.0	10 15 15	µA

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V
Input rising and falling time : 5ns
Input and output reference voltage :1.5V
Output load(see right) : C_L=100pF+1TTL
$^{1)}C_L$=30pF+1TTL

1. KM62V256CL-7L Family, KM62U256CL-8L Family



1. Including scope and jig capacitance

AC CHARACTERISTICS (KM62V256C Family : Vcc=3.0~3.6V, KM62U256C Family : Vcc=2.7~3.3V

Commercial product :T_A=0 to 70°C, Extended product :T_A=-25 to 85°C, Industrial product : T_A=-40 to 85°C)

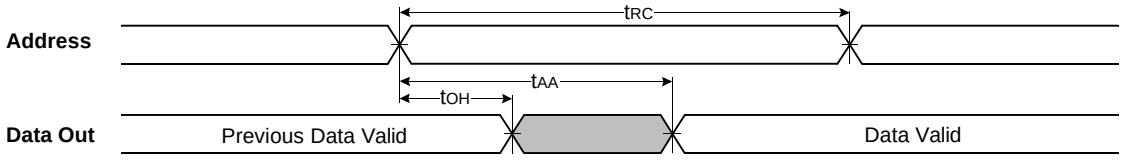
Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	70	-	85	-	100	-	ns
	Address access time	t_{AA}	-	70	-	85	-	100	ns
	Chip select to output	t_{CO}	-	70	-	85	-	100	ns
	Output enable to valid output	t_{OE}	-	35	-	40	-	50	ns
	Chip select to low-Z output	t_{LZ}	10	-	10	-	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t_{HZ}	0	30	0	30	0	35	ns
	Output disable to high-Z output	t_{OHZ}	0	30	0	30	0	35	ns
	Output hold from address change	t_{OH}	5	-	10	-	15	-	ns
Write	Write cycle time	t_{WC}	70	-	85	-	100	-	ns
	Chip select to end of write	t_{CW}	60	-	70	-	70	-	ns
	Address set-up time	t_{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t_{AW}	60	-	70	-	70	-	ns
	Write pulse width	t_{WP}	50	-	60	-	60	-	ns
	Write recovery time	t_{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	25	0	25	0	30	ns
	Data to write time overlap	t_{DW}	50	-	60	-	60	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	10	-	10	-	ns

DATA RETENTION CHARACTERISTICS

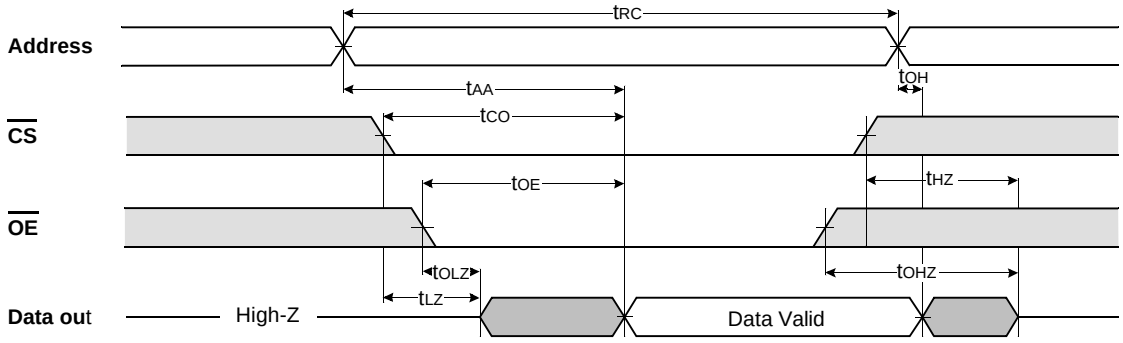
Item	Symbol		Test Condition	Min	Typ	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS}$≥Vcc-0.2V	2.0	-	3.6	V
Data retention current	I_{DR}	KM62V256CL-L KM62U256CL-L	Vcc=3.0V $\overline{CS}$≥Vcc-0.2V	- -	1 0.6	8 8	µA
		KM62V256CLE-L KM62U256CLE-L		- -	1 0.6	10 10	
		KM62V256CLI-L KM62U256CLI-L		- -	1 0.6	10 10	
Data retention set-up time	t_{SDR}		See data retention waveform	0	-	-	ms
Recovery time	t_{RDR}			5	-	-	

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



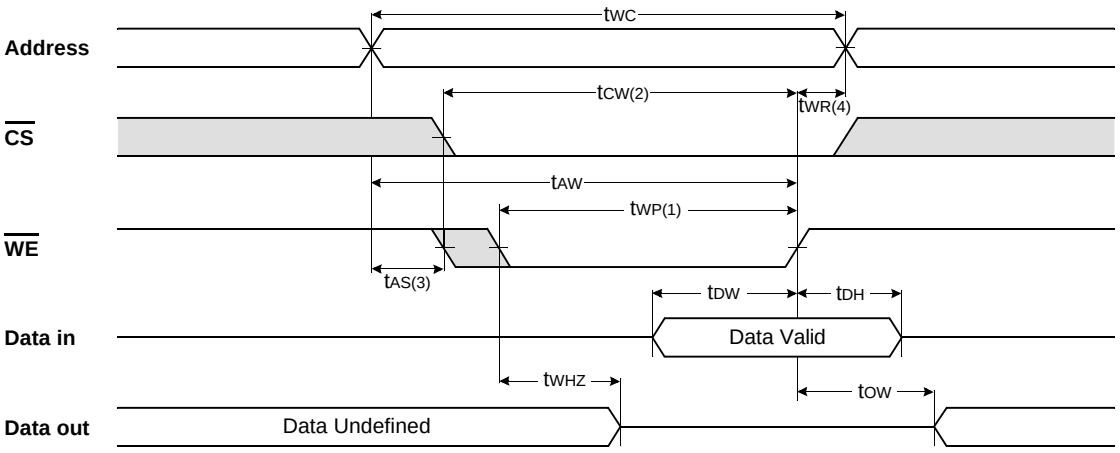
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



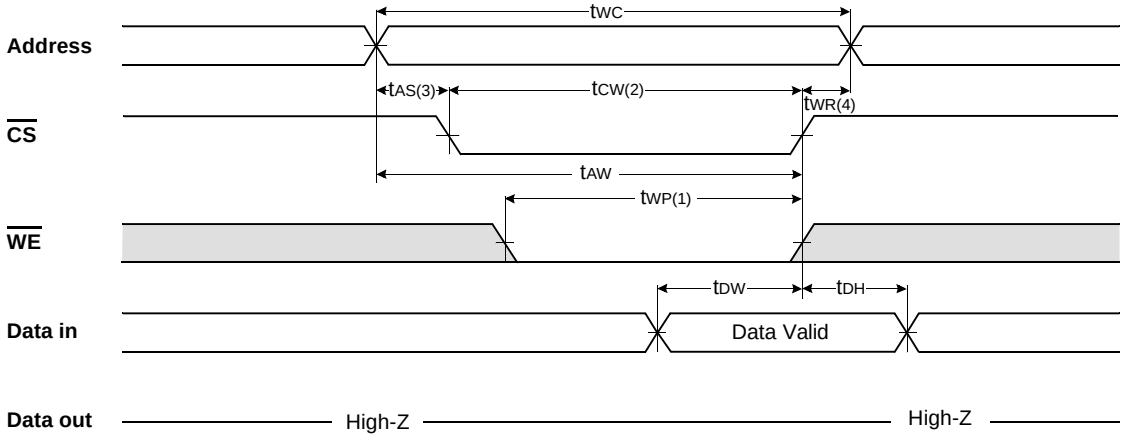
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)

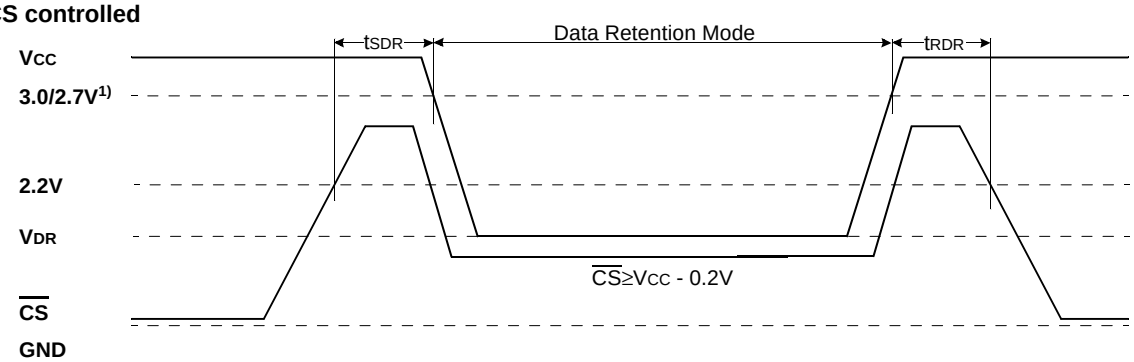


NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going Low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the begining of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

$\overline{CS}$ controlled

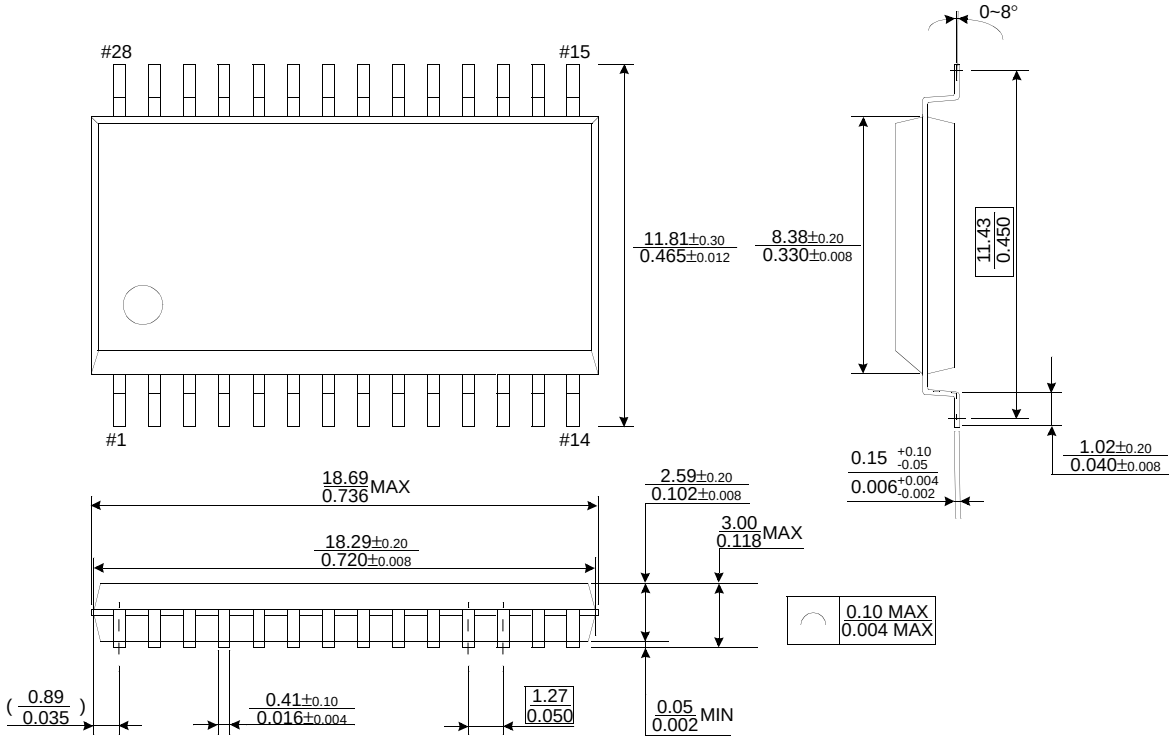


1. 3.0V for KM62V256C Family, 2.7V for KM62U256C Family.

PACKAGE DIMENSIONS

Units : millimeter(inch)

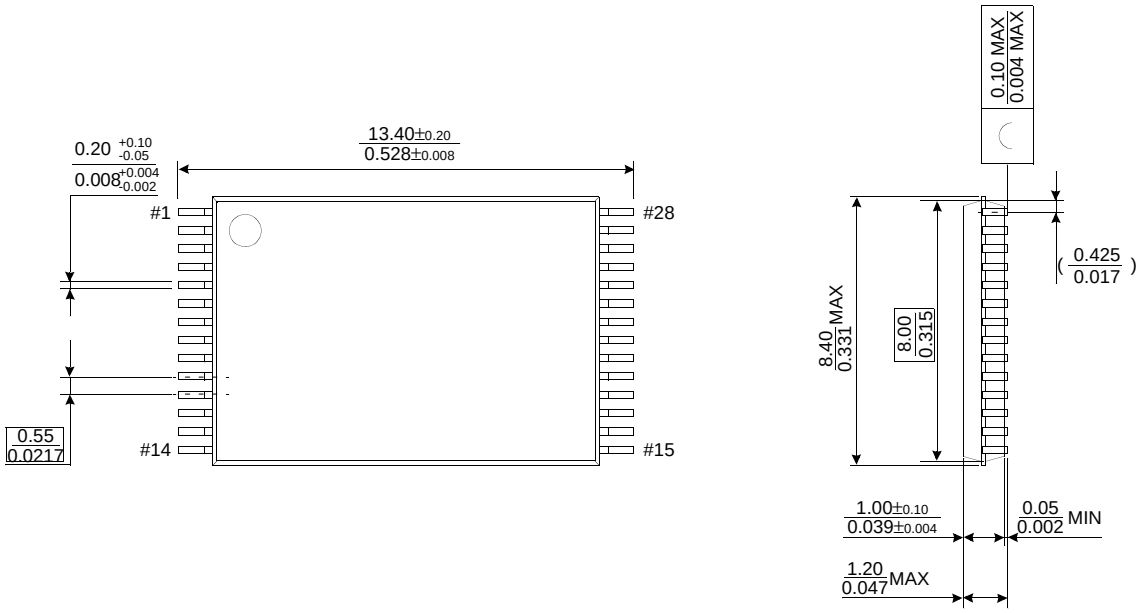
28 PIN PLASTIC SMALL OUTLINE PACKAGE(450mil)



PACKAGE DIMENSIONS

Units : millimeter(inch)

28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4R)