Document Title

512Kx8 bit Low Power CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial draft	October 20,1998	Preliminary
1.0	Finalize	April 12, 1999	Final

512Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 512Kx8
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-DIP-600, 32-SOP-525, 32-TSOP2-400F/R

GENERAL DESCRIPTION

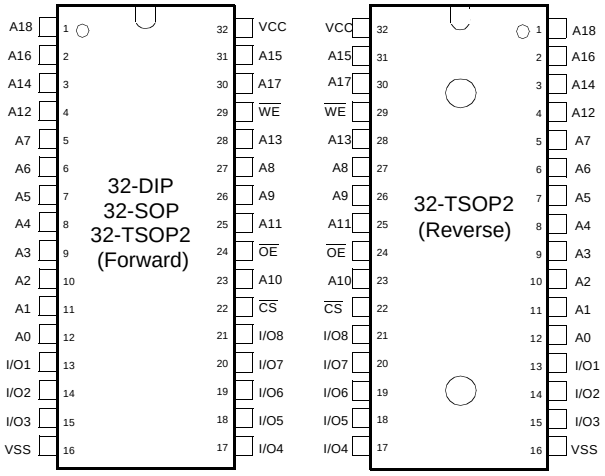
The KM684000C families are fabricated by SAMSUNG′s advanced CMOS process technology. The families support various operating temperature ranges and various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2}, Max)	
KM684000CL	Commercial (0~70°C)	4.5~5.5V	55[1]/70ns	80μA	55mA	32-DIP,32-SOP 32-TSOP2-F/R
KM684000CL-L				20μA		
KM684000CLI	Inderstrial (-40~85°C)			100μA		32-SOP 32-TSOP2-F/R
KM684000CLI-L				30μA		

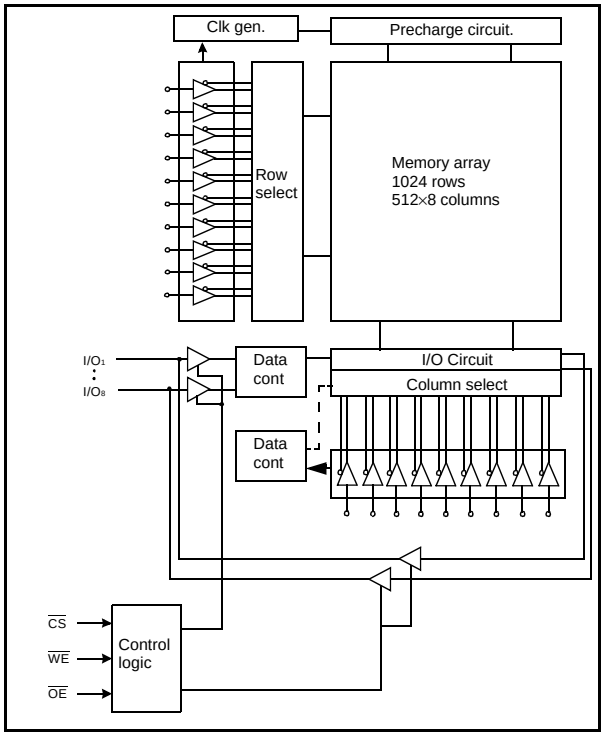
1. The parameter is measured with 50pF test load.

PIN DESCRIPTION



Pin Name	Function
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
A_0~A_{18}	Address Inputs
I/O_1~I/O_8	Data Inputs/Outputs
Vcc	Power
Vss	Ground

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	**Function**	**Part Name**	**Function**
KM684000CLP-5	32-DIP, 55ns, Low Power	KM684000CLGI-5	32-SOP, 55ns, Low Power
KM684000CLP-5L	32-DIP, 55ns, Low Low Power	KM684000CLGI-5L	32-SOP, 55ns, Low Low Power
KM684000CLP-7	32-DIP, 70ns, Low Power	KM684000CLGI-7	32-SOP, 70ns, Low Power
KM684000CLP-7L	32-DIP, 70ns, Low Low Power	KM684000CLGI-7L	32-SOP, 70ns, Low Low Power
KM684000CLG-5	32-SOP, 55ns, Low Power	KM684000CLTI-5L	32-TSOP2-F, 55ns, Low Low Power
KM684000CLG-5L	32-SOP, 55ns, Low Low Power	KM684000CLTI-7L	32-TSOP2-F, 70ns, Low Low Power
KM684000CLG-7	32-SOP, 70ns, Low Power	KM684000CLRI-5L	32-TSOP2-R, 55ns, Low Low Power
KM684000CLG-7L	32-SOP, 70ns, Low Low Power	KM684000CLRI-7L	32-TSOP2-R, 70ns, Low Low Power
KM684000CLT-5L	32-TSOP2-F, 55ns, Low Low Power		
KM684000CLT-7L	32-TSOP2-F, 70ns, Low Low Power		
KM684000CLR-5L	32-TSOP2-R, 55ns, Low Low Power		
KM684000CLR-7L	32-TSOP2-R, 70ns, Low Low Power		

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode	Power
H	X[1)]	X[1)]	High-Z	Deselected	Standby
L	H	H	High-Z	Output disbaled	Active
L	L	H	Dout	Read	Active
L	X[1)]	L	Din	Write	Active

1. X means don't care.(Must be in low or high state.)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	°C	-
Operating Temperature	T_A	0 to 70	°C	KM684000CL/L-L
		-40 to 85	°C	KM684000CLI/LI-L

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5[2)]	V
Input low voltage	V_{IL}	-0.5[3)]	-	0.8	V

Note:
1. Commercial Product : T_A=0 to 70°C, otherwise specified
   Industrial Product : T_A=-40 to 85°C, otherwise specified
2. Overshoot : V_{CC}+3.0V in case of pulse width ≤ 30ns
3. Undershoot : -3.0V in case of pulse width ≤ 30ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

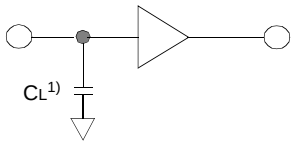
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	µA
Operating power supply current	I_{CC}	I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, Read		-	-	10	mA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA $\overline{CS}$≤0.2V, V_{IN}≥0.2V or V_{IN}≥Vcc-0.2V		-	-	8	mA
	I_{CC2}	Cycle time=Min, 100% duty, I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}		-	-	55	mA
Output low voltage	V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)	I_{SB}	$\overline{CS}$=V_{IH}, Other inputs = V_{IL} or V_{IH}		-	-	3	mA
Standby Current(CMOS)	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, Other inputs=0~Vcc	KM684000CL	-	-	80	µA
			KM684000CL-L	-	-	20	
			KM684000CLI	-	-	100	
			KM684000CLI-L	-	-	30	

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.8 to 2.4V
Input rising and falling time : 5ns
Input and output reference voltage : 1.5V
Output load (See right) : C_L=100pF+1TTL
C_L=50pF+1TTL



1. Including scope and jig capacitance

AC CHARACTERISTICS (V_{CC}=4.5~5.5V, KM684000C Family:T_A=0 to 70°C, KM684000CI Family:T_A=-40 to 85°C)

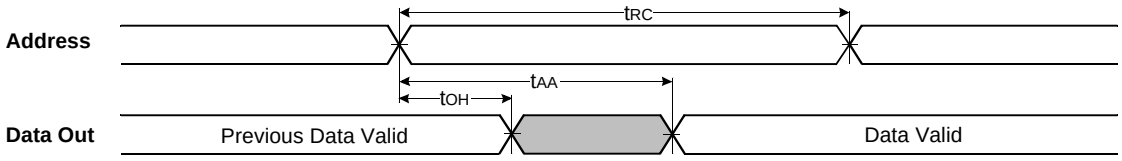
Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	55	-	70	-	ns
	Address access time	t_{AA}	-	55	-	70	ns
	Chip select to output	t_{CO}	-	55	-	70	ns
	Output enable to valid output	t_{OE}	-	25	-	35	ns
	Chip select to low-Z output	t_{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t_{HZ}	0	20	0	25	ns
	Output disable to high-Z output	t_{OHZ}	0	20	0	25	ns
	Output hold from address change	t_{OH}	10	-	10	-	ns
Write	Write cycle time	t_{WC}	55	-	70	-	ns
	Chip select to end of write	t_{CW}	45	-	60	-	ns
	Address set-up time	t_{AS}	0	-	0	-	ns
	Address valid to end of write	t_{AW}	45	-	60	-	ns
	Write pulse width	t_{WP}	40	-	50	-	ns
	Write recovery time	t_{WR}	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	20	0	25	ns
	Data to write time overlap	t_{DW}	25	-	30	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

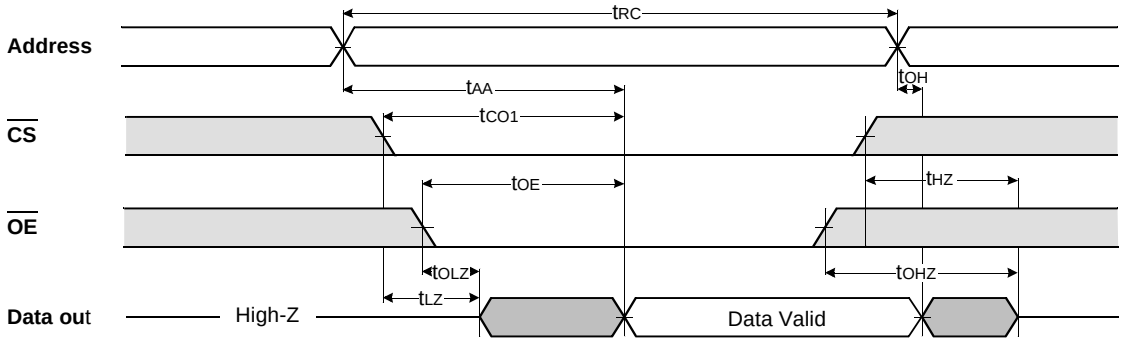
Item	Symbol	Test Condition		Min	Typ	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS}$≥Vcc-0.2V		2.0	-	5.5	V
Data retention current	I_{DR}	Vcc=3.0V, $\overline{CS}$≥Vcc-0.2V	KM684000CL	-	-	40	µA
			KM684000CL-L	-	-	15	
			KM684000CLI	-	-	50	
			KM684000CLI-L	-	-	20	
Data retention set-up time	t_{SDR}	See data retention waveform		0	-	-	ms
Recovery time	t_{RDR}			5	-	-	

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



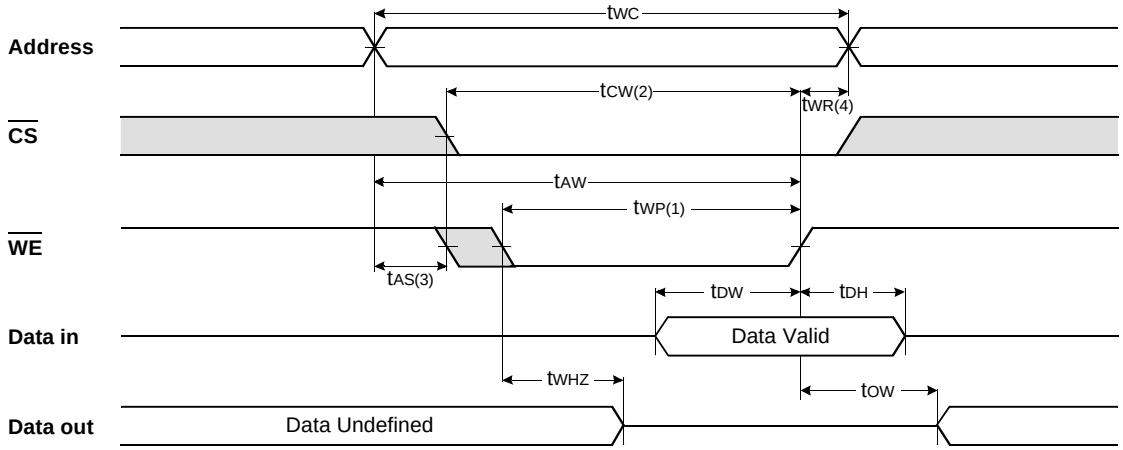
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



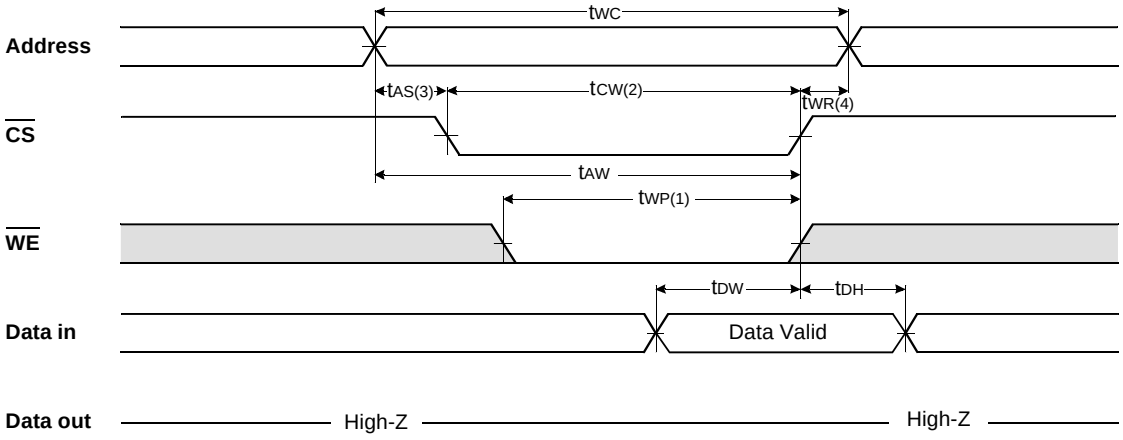
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)

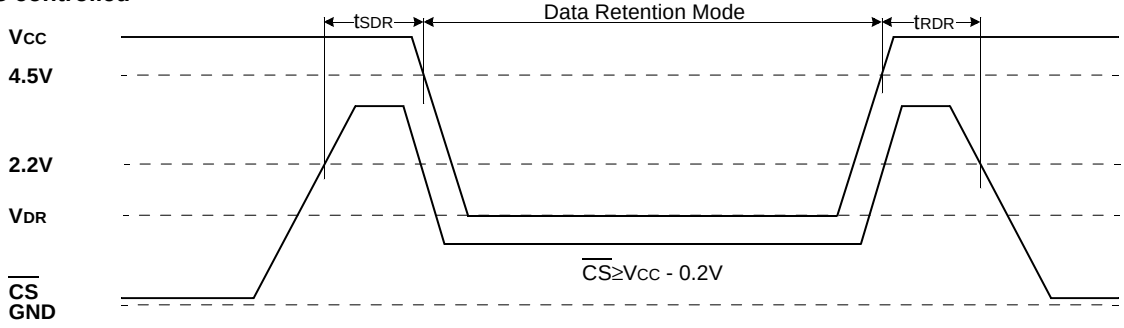


NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going Low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the begining of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

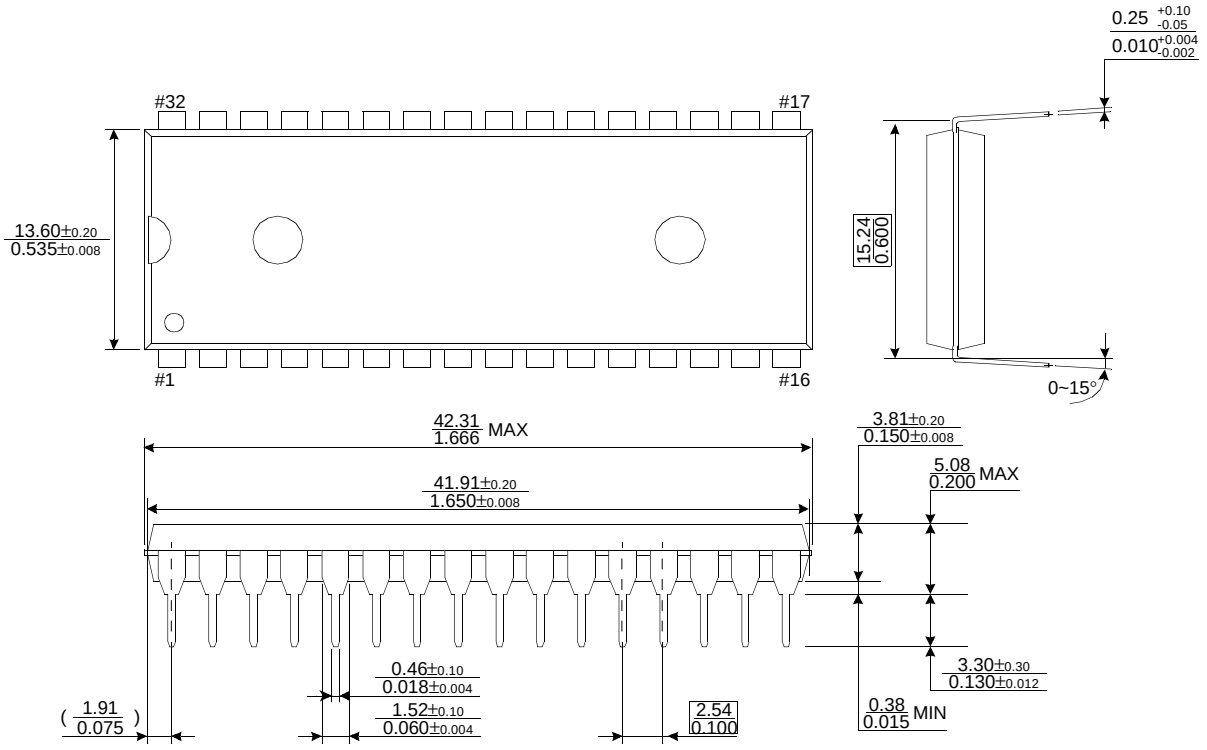
$\overline{CS}$ controlled



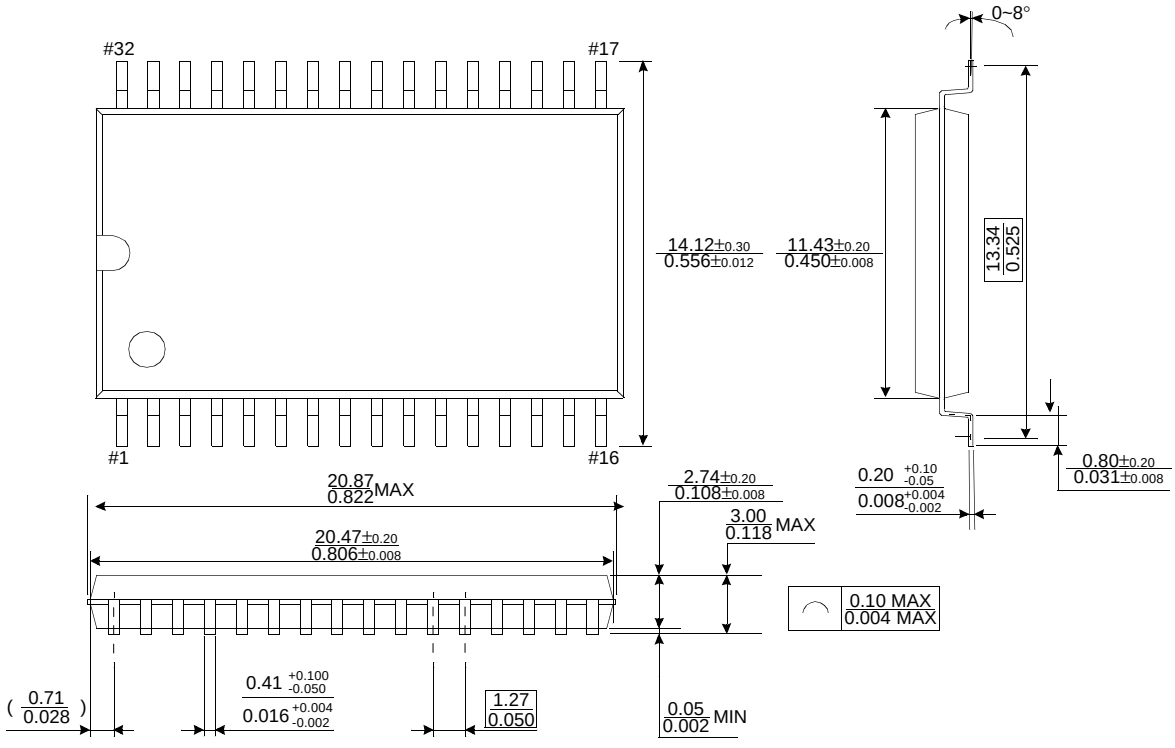
PACKAGE DIMENSIONS

Units : millimeter(Inch)

32 PIN DUAL INLINE PACKAGE (600mil)



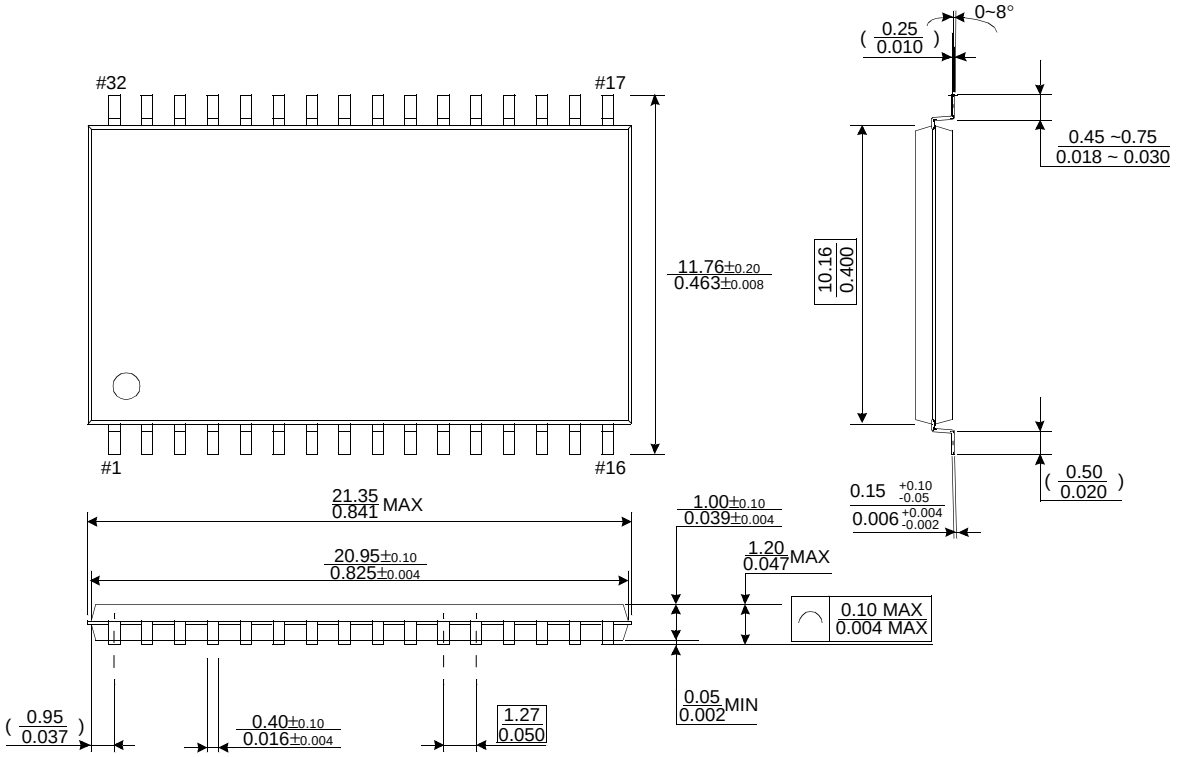
32 PIN PLASTIC SMALL OUTLINE PACKAGE (525mil)



PACKAGE DIMENSIONS

Units : millimeter(Inch)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)