

Document Title

64Kx8 bit Low Power CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	January 10th 1998	Advance

The attached datasheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions about device. If you have any questions, please contact the SAMSUNG branch office near you.

KM68512B Family

64Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.4 μ m CMOS
- Organization : 64Kx8
- Power Supply Voltage : Single 5V $\pm$ 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 32-TSOP I -0820F

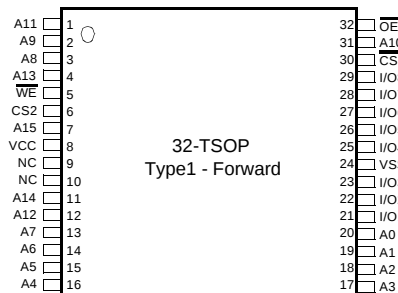
GENERAL DESCRIPTION

The KM68512B family is fabricated by SAMSUNG 's advanced CMOS process technology. The family support various operating temperature ranges and small package type for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

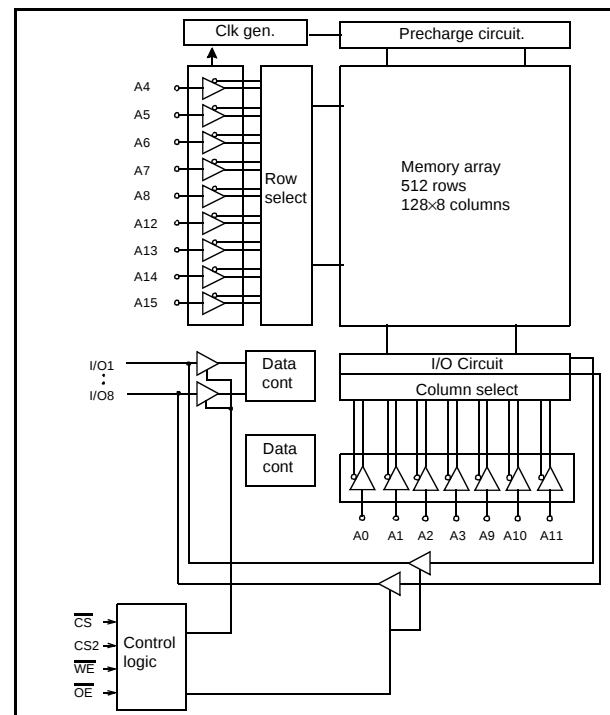
Product Family	Operating Temperature	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (Icc2, Max)	
KM68512BL-L	Commercial(0~70 °C)	5V $\pm$ 0.5V	55/70	10 μ A	60mA	32-TSOP1-F
KM68512BLI-L	Industrial(-40~85 °C)		70	15 μ A		

PIN DESCRIPTION



Name	Function
A0~A15	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$, CS2	Chip Select Inputs
$\overline{OE}$	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



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KM68512B Family

Advance
CMOS SRAM

PRODUCT LIST

Commercial Temperature Product (0~70°C)		Industrial Temperature Products (-40~85°C)	
Part Name	Function	Part Name	Function
KM68512BLT-5L	32-TSOP1-F, 55ns, LL-pwr	KM68512BLTI-7L	32-TSOP1-F, 70ns, LL-pwr
KM68512BLT-7L	32-TSOP1-F, 70ns, LL-pwr		

FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X	L	Din	Write	Active

1. X means don't care.(Must be low or high state)

ABSOLUTE MAXIMUM RATINGS ¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} ,V _{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to 7.0	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM68512BL
		-40 to 85	°C	KM68512BLI
Soldering temperature and time	T _{SOLDER}	260°C, 10sec(Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.5V ²⁾	V
Input low voltage	V _{IL}	-0.5 ³⁾	-	0.8	V

Note

- Commercial Product : T_A=0 to 70°C, unless otherwise specified
Industrial Product : T_A=-40 to 85°C, unless otherwise specified
- Overshoot : V_{CC}+3.0V in case of pulse width≤30ns
- Undershoot : -3.0V in case of pulse width≤30ns
- Overshoot and undershoot is sampled, not 100% tested

CAPACITANCE ¹⁾(f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	6	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	8	pF

- Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

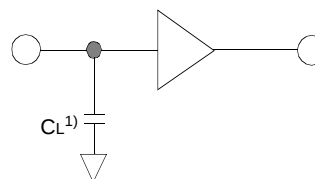
Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$ or CS ₂ =V _{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply	I _{CC}	I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH} , Read	-	7	10	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA CS ₁ ≤0.2V, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	Read	-	5	mA
			Write	-	30	mA
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	-	-	60	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS}_1=V_{IH}$, CS ₂ =V _{IL} , Other inputs =V _{IL} or V _{IH}	-	-	3	mA
Standby Current (CMOS)	I _{SB1}	$\overline{CS}_1 \geq V_{CC}-0.2V$, CS ₂ ≥V _{CC} -0.2V or CS ₂ ≤0.2V	-	1	10 ¹⁾	μA

- Industrial product = 15μA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.8 to 2.4V
 Input rising and falling time : 5ns
 Input and output reference voltage :1.5V
 Output load(see right) : $C_L=100\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS ($V_{CC}=4.5\sim 5.5\text{V}$, KM68512B Family : $T_A=0$ to 70°C , KM68512BI Family : $T_A=-40$ to 85°C)

Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	55	-	70	-	ns
	Address access time	t _{AA}	-	55	-	70	ns
	Chip select to output	t _{CO}	-	55	-	70	ns
	Output enable to valid output	t _{OE}	-	25	-	35	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	20	0	25	ns
	Output disable to high-Z output	t _{OHZ}	0	20	0	25	ns
	Output hold from address change	t _{OH}	10	-	10	-	ns
Write	Write cycle time	t _{WC}	55	-	70	-	ns
	Chip select to end of write	t _{CW}	45	-	60	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	45	-	60	-	ns
	Write pulse width	t _{WP}	40	-	55	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	20	0	25	ns
	Data to write time overlap	t _{DW}	20	-	30	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	ns

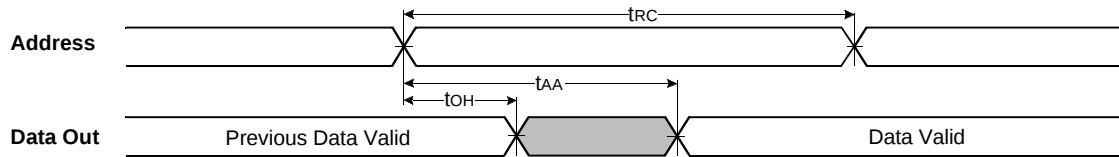
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS}_1 \geq V_{CC}-0.2\text{V}$	2.0	-	5.5	V
Data retention current	I_{DR}	$V_{CC}=3.0\text{V}$, $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$	KM68512BL-L	-	0.5	μA
			KM68512BLI-L	-	15	
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t_{RDR}		5	-	-	

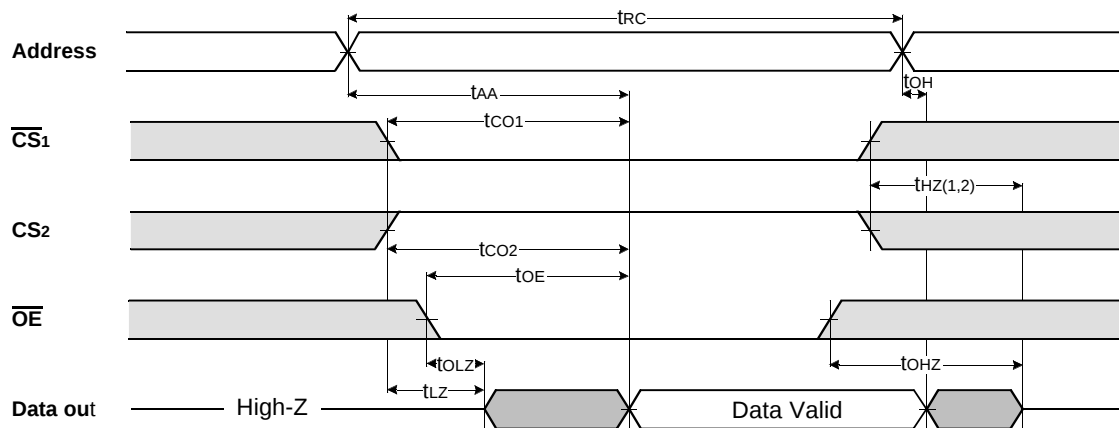
1. $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$, $CS_2 \geq V_{CC}-0.2\text{V}$ ($\overline{CS}_1$ controlled) or $CS_2 \leq 0.2\text{V}$ (CS_2 controlled).

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



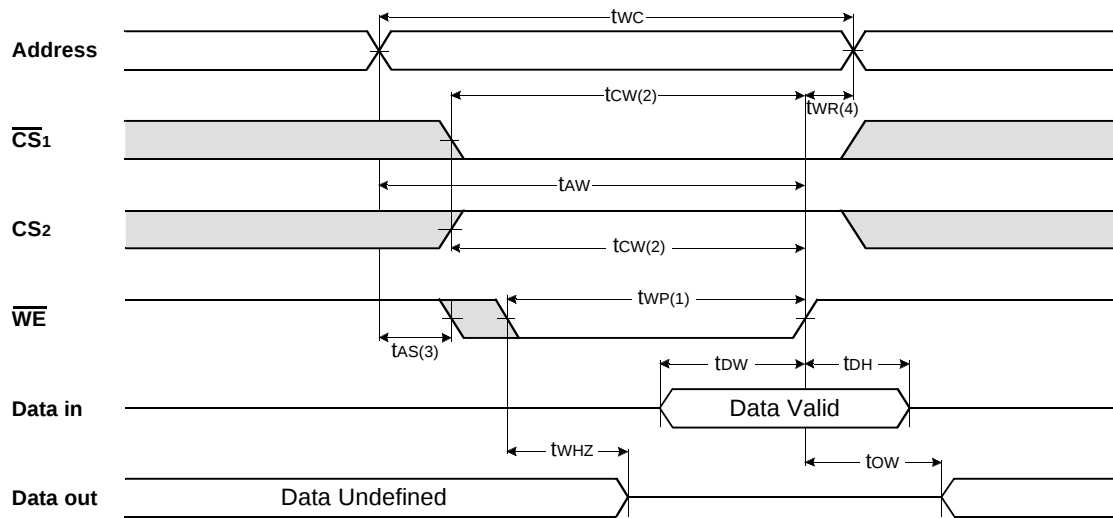
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



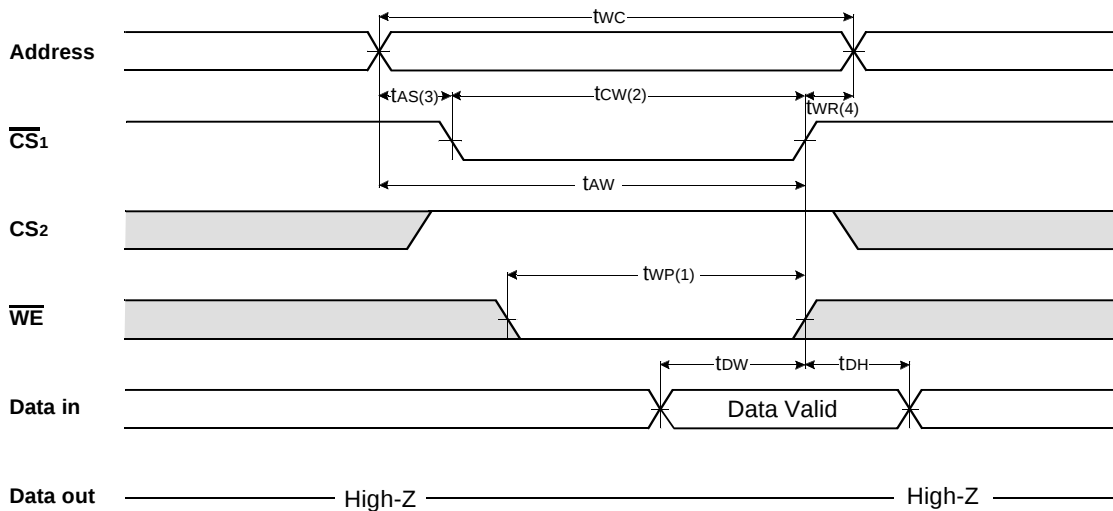
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



The diagram illustrates the timing relationships for the 28C02 EPROM. The signals shown are Address, CS1, CS2, WE, Data in, and Data out. The timing parameters are defined as follows:

- Address:** The duration of the address pulse is t_{WC} .
- CS1:** The setup time before the address pulse is $t_{AS}(3)$. The pulse width is $t_{CW}(2)$. The delay from the falling edge of CS1 to the start of the data valid period is $t_{WR}(4)$.
- CS2:** The pulse width is t_{AW} .
- WE:** The setup time before the address pulse is $t_{WP}(2)$. The pulse width is $t_{WP}(1)$.
- Data in:** The data is valid for a duration of t_{DW} after the address pulse. The delay from the falling edge of WE to the start of the data valid period is t_{DH} .
- Data out:** The data output is in a High-Z state during the data valid period.

1. A write occurs during the overlap of a low $\overline{CS}_1$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}_1$ goes low, CS_2 going high and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}_1$ going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}_1$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. $t_{WR(1)}$ applied in case a write ends as $\overline{CS}_1$ or $\overline{WE}$ going high $t_{WR(2)}$ applied in case a write ends as CS_2 going to low.

The diagram illustrates the timing for Data Retention Mode. It shows the relationship between the supply voltage V_{CC} and the data retention voltage V_{DR} during two transitions. The signal $\overline{CS}_1$ is shown as a low-level pulse. The voltage levels are marked at V_{CC} , 4.5V, 2.2V, V_{DR} , and $\overline{CS}_1$ GND. The time intervals t_{SDR} and t_{RDR} are indicated for the first and second transitions, respectively. A note specifies $\overline{CS}_1 \geq V_{CC} - 0.2V$ during the retention period.

Timing diagram for CS2 controlled Data Retention Mode. The diagram shows the relationship between VCC, CS2, and VDR signals. VCC is high during normal operation and drops to 4.5V* during Data Retention Mode. CS2 transitions from high to low, with tSDR being the delay from CS2 falling to VDR falling. VDR drops to 0.4V during Data Retention Mode, with CS2 ≤ 0.2V. tRDR is the delay from CS2 rising to VDR rising. The duration of Data Retention Mode is indicated by a double-headed arrow.

PACKAGE DIMENSIONS

Units : Millimeters(Inches)

32-THIN SMALL OUTLINE PACKAGE TYPE I (0820F)

