

DRAM MODULE

KMM332F400CS-L KMM332F410CS-L

KMM332F400CS-L & KMM332F410CS-L Fast Page with EDO Mode

4M x 32 DRAM SODIMM Using 4MX4, 4K & 2K Ref., 3.3V, Low power/Self-Refresh

GENERAL DESCRIPTION

The Samsung KMM332F40(1)0CS is a 4Mx32bits Dynamic RAM high density memory module. The Samsung KMM332F40(1)0CS consists of eight CMOS 4Mx4bits DRAMs in 24-pinTSOPII packages mounted on a 72-pin six layer zig-zag glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM332F40(1)0CS is a Small Out-line Dual In-line Memory Module with edge connections and is intended for mounting into 72-pin dual readout zigzag edge connector sockets.

PERFORMANCE RANGE

Speed	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}
-L5	50ns	13ns	90ns	25ns
-L6	60ns	15ns	110ns	30ns

FEATURES

- Part Identification
 - KMM332F400CS-L5/L6
(4096 cycles/128ms Ref, TSOP, Low Power, 50/60ns)
 - KMM332F410CS-L5/L6
(2048 cycles/128ms Ref, TSOP, Low Power, 50/60ns)
- Fast Page with EDO Mode Operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self refresh capability
- LVTTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- JEDEC standard PDPin & pinout (72pin)
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ18
2	DQ0	38	DQ19
3	DQ1	39	Vss
4	DQ2	40	$\overline{\text{CAS0}}$
5	DQ3	41	$\overline{\text{CAS2}}$
6	DQ4	42	$\overline{\text{CAS3}}$
7	DQ5	43	$\overline{\text{CAS1}}$
8	DQ6	44	$\overline{\text{RAS0}}$
9	DQ7	45	NC
10	Vcc	46	NC
11	PD1	47	$\overline{\text{W}}$
12	A0	48	NC
13	A1	49	DQ20
14	A2	50	DQ21
15	A3	51	DQ22
16	A4	52	DQ23
17	A5	53	DQ24
18	A6	54	DQ25
19	A10	55	NC
20	NC	56	DQ27
21	DQ9	57	DQ28
22	DQ10	58	DQ29
23	DQ11	59	DQ31
24	DQ12	60	DQ30
25	DQ13	61	Vcc
26	DQ14	62	DQ32
27	DQ15	63	DQ33
28	A7	64	DQ34
29	A11	65	NC
30	Vcc	66	PD2
31	A8	67	PD3
32	A9	68	PD4
33	NC	69	PD5
34	$\overline{\text{RAS2}}$	70	PD6
35	DQ16	71	PD7
36	NC	72	Vss

PIN NAMES

Pin Name	Function
A0 - A11	Address Inputs (4K ref)
A0 - A10	Address Inputs (2K ref)
DQ(0 -7,9-16, 18-25,27-34)	Data In/Out
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS0}}, \overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{CAS0}} - \overline{\text{CAS3}}$	Column Address Strobe
PD1 -PD7	Presence Detect
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	NC	NC
PD3	Vss	Vss
PD4	NC	NC
PD5	Vss	NC
PD6	Vss	NC
PD7	NC	NC

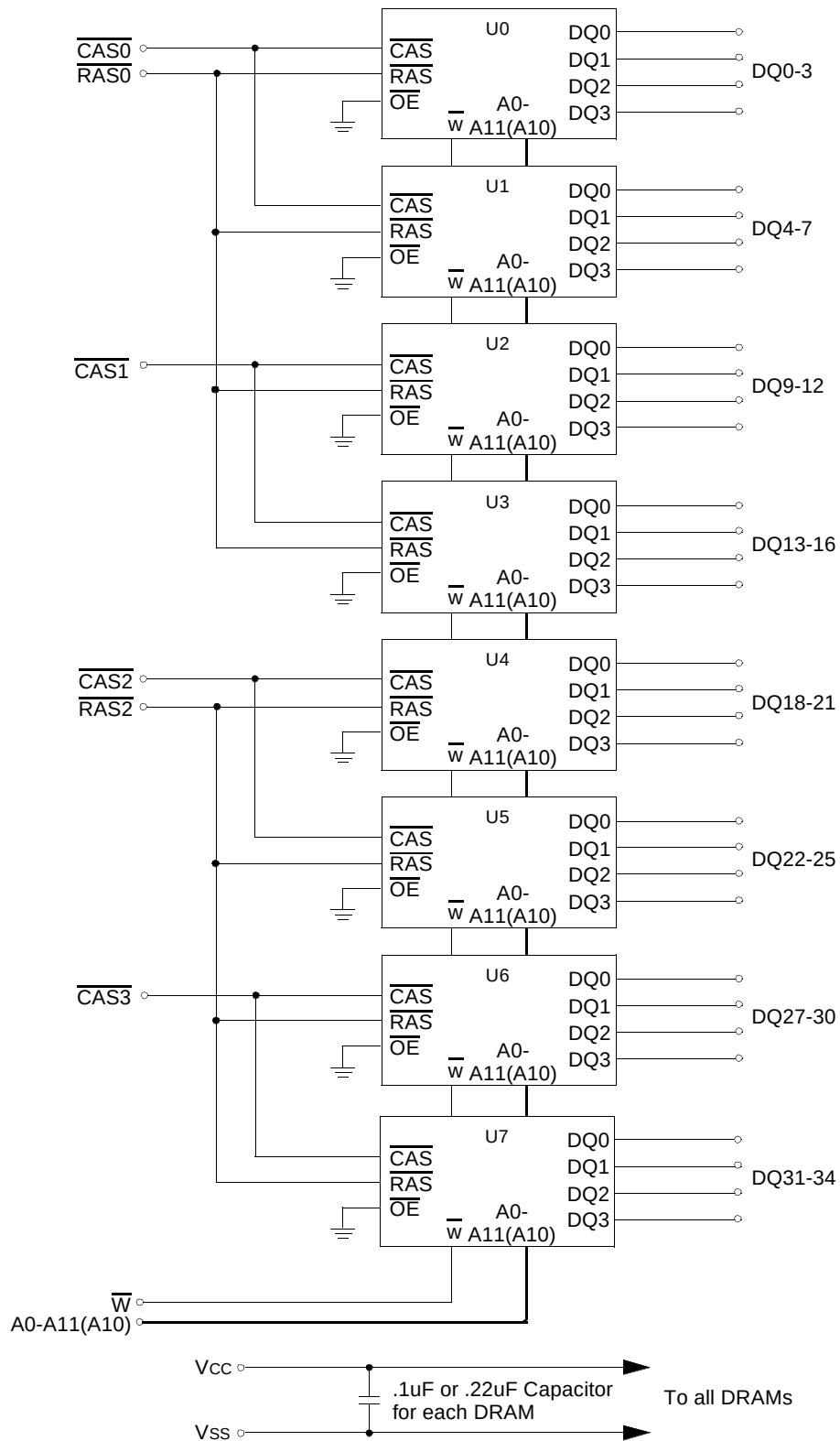
* Pin Connection Charging Available

NOTE : A11 is used for only KMM332F400CS (4K ref.)

DRAM MODULE

KMM332F400CS-L
KMM332F410CS-L

FUNCTIONAL BLOCK DIAGRAM



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KMM332F410CS-L

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative Vss	V _{IN} , V _{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to +4.6	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	8	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3* ¹	V
Input Low Voltage	V _{IL}	-0.3* ²	-	0.8	V

*1 : V_{CC}+1.3V/15ns, Pulse width is measured at V_{CC}.

*2 : -1.3V/15ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM332F400CS		KMM332F410CS		Unit
		Min	Max	Min	Max	
I _{CC1}	-L5	-	720	-	880	mA
	-L6	-	640	-	800	mA
I _{CC2}	Don't care	-	8	-	8	mA
I _{CC3}	-L5	-	720	-	880	mA
	-L6	-	640	-	800	mA
I _{CC4}	-L5	-	640	-	720	mA
	-L6	-	560	-	640	mA
I _{CC5}	Don't care	-	1.6	-	1.6	mA
I _{CC6}	-L5	-	720	-	880	mA
	-L6	-	640	-	800	mA
I _{CC7}	Don't care	-	2000	-	2000	uA
I _{CCS}	Don't care	-	1600	-	1600	uA
I _{I(L)}	Don't care	-40	40	-40	40	uA
	I _{O(L)}	-5	5	-5	5	uA
V _{OH}	Don't care	2.4	-	2.4	-	V
	V _{OL}	-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @trc=min)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}=V_{IH}$, $\overline{RAS}$ cycling @trc=min)

I_{CC4} : EDO Mode Current * ($\overline{RAS}=V_{IL}$, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6} : $\overline{CAS}$ -Before- $\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @trc=min)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$ =0.2V)

DQ0-31=Don't care, trc=31.25us (4K Ref.), 62.5us (2K Ref.) , t_{RAS}=t_{ASmin}~300ns

I_{CCS} : Self Refresh Current ($\overline{RAS}=\overline{CAS}=V_{IL}$, $\overline{W}=\overline{OE}=A0-A11=V_{CC}-0.2V$ or 0.2V, DQ0-DQ31=V_{CC}-0.2V, 0.2V or OPEN)

I_{I(L)} : Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one EDO mode cycle, t_{HPC}.

DRAM MODULE

KMM332F400CS-L
KMM332F410CS-L

CAPACITANCE (TA = 25°C, Vcc=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A10)]	CIN1	-	60	pF
Input capacitance[W]	CIN2	-	75	pF
Input capacitance[RAS0, RAS2]	CIN3	-	45	pF
Input capacitance[CAS0 - CAS3]	CIN4	-	30	pF
Input/Output capacitance[DQ0-7,9-16,18-25,27-34]	CDQ	-	20	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, Vcc=3.3V±0.3V See notes 1,2.)

Test condition : Vih/Vil=2.0/0.8V, Voh/Vol=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	tCEZ	3	13	3	15	ns	6,11,12
Transition time(rise and fall)	tT	2	50	2	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		15		ns	
$\overline{\text{CAS}}$ hold time	tCSH	43		50		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	8	10K	10	10K	ns	13
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	8		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold referenced to $\overline{\text{CAS}}$	tRCH	0		0		ns	8
Read command hold referenced to $\overline{\text{RAS}}$	tRRH	0		0		ns	8
Write command hold time	tWCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	13		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	8		10		ns	
Data set-up time	tDS	0		0		ns	8
Data hold time	tDH	8		10		ns	8
Refresh period	tREF		128		128	ms	
Write command set-up time	tWCS	0		0		ns	7
$\overline{\text{CAS}}$ setup time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		ns	
$\overline{\text{CAS}}$ precharge time (CBR counter test cycle)	tCPT	20		20		ns	

AC CHARACTERISTICS (Continued)

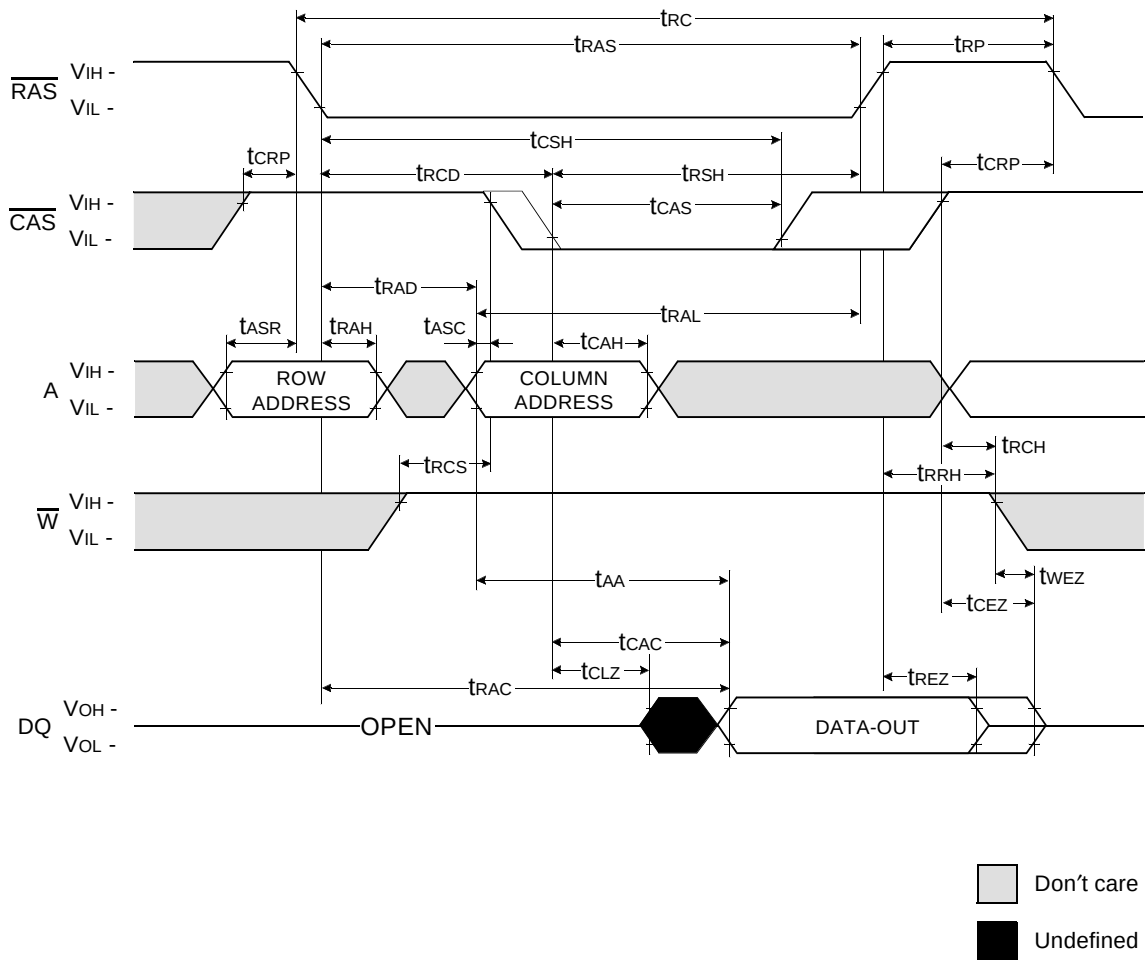
Test condition : $V_{IH}/V_{IL}=2.0/0.8V$, $V_{OH}/V_{OL}=2.0/0.8V$, output loading $C_L=100pF$

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	25		30		ns	13
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C-B-R}$ refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C-B-R}$ refresh)	t_{WRH}	10		10		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	
$\overline{W}$ to data delay	t_{WED}	15		15		ns	6,11,12
$\overline{W}$ pulse width	t_{WPE}	5		5		ns	6,11
$\overline{RAS}$ pulse width (C-B-R self refresh)	t_{RASS}	100		100		us	
$\overline{RAS}$ precharge time (C-B-R self refresh)	t_{RPS}	90		110		ns	
$\overline{CAS}$ hold time (C-B-R self refresh)	t_{CHS}	-50		-50		ns	

NOTES

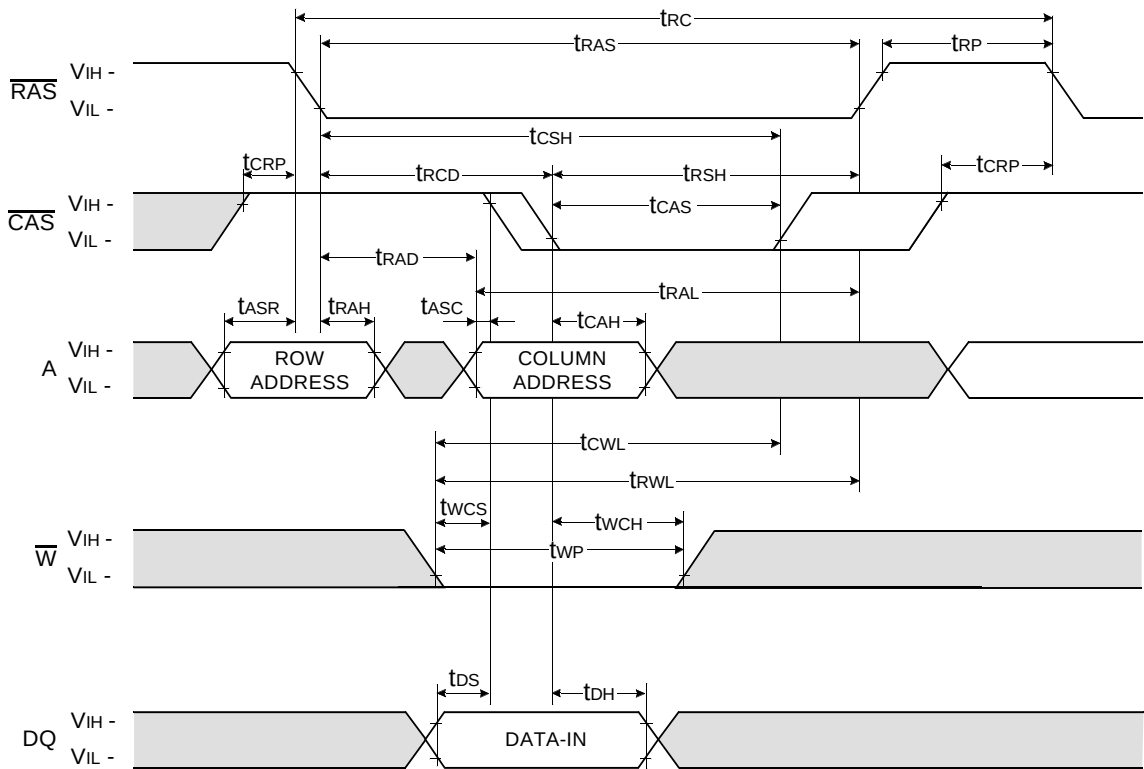
- An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$ -only or $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycles before proper device operation is achieved.
- $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 1 TTL loads and 100pF.
- Operation within the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
- Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
- t_{wcs} is non restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{wcs} \geq t_{wcs}(\text{min})$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
- Operation within the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit access time is controlled by t_{AA} .
- $t_{CEZ}(\text{max})$, $t_{REZ}(\text{max})$, $t_{WEZ}(\text{max})$ and $t_{OEZ}(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
- If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ going.
- $t_{ASC} \geq t_{CP} \text{ min}$

READ CYCLE



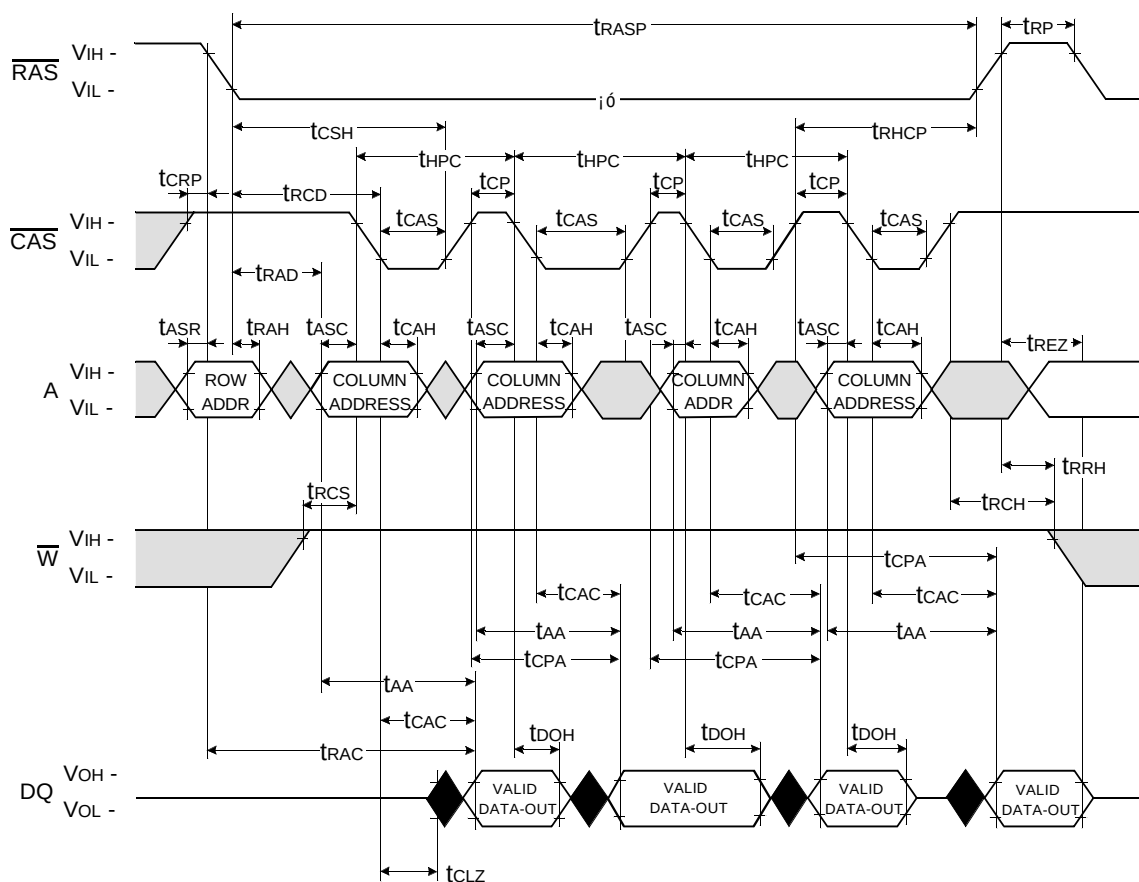
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



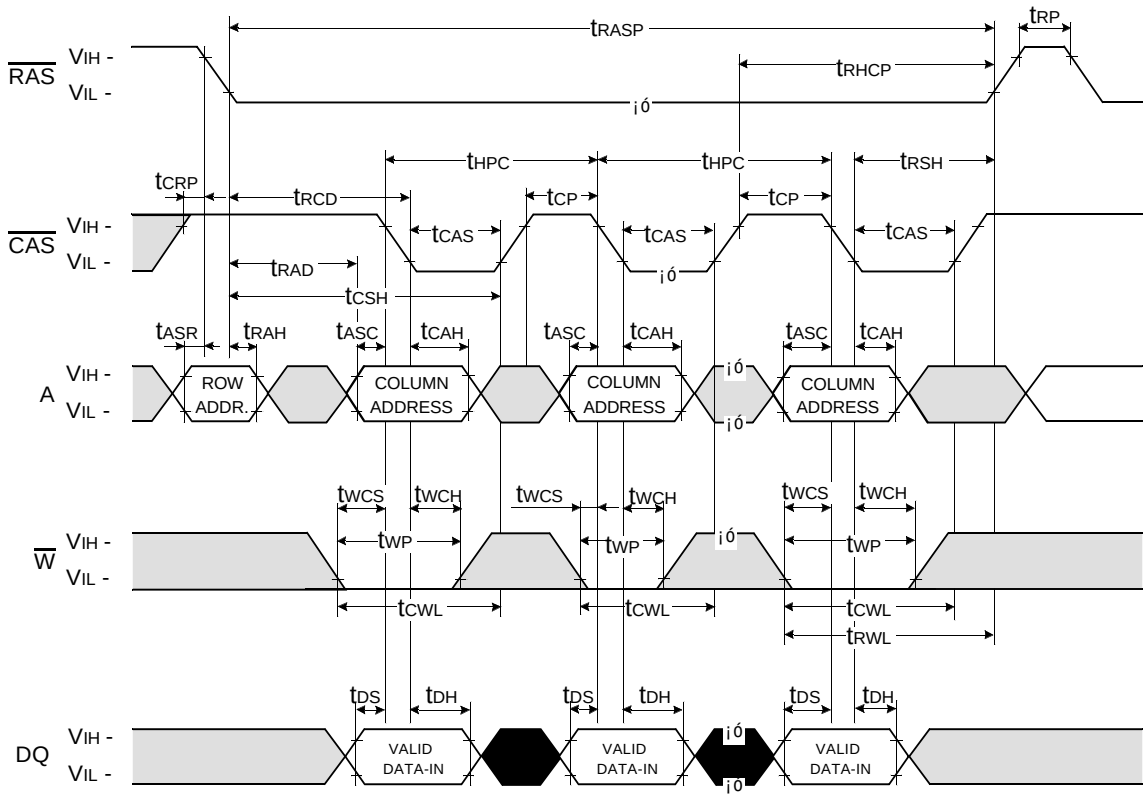
Don't care
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HYPER PAGE READ CYCLE



HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

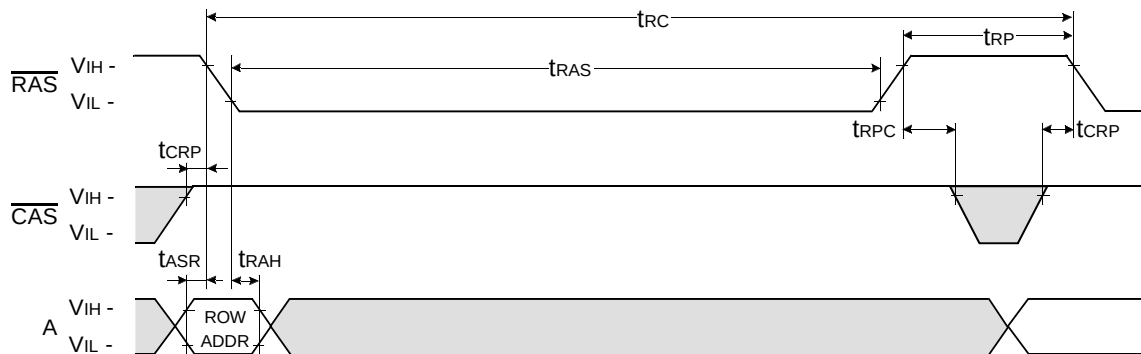


Don't care
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$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE*

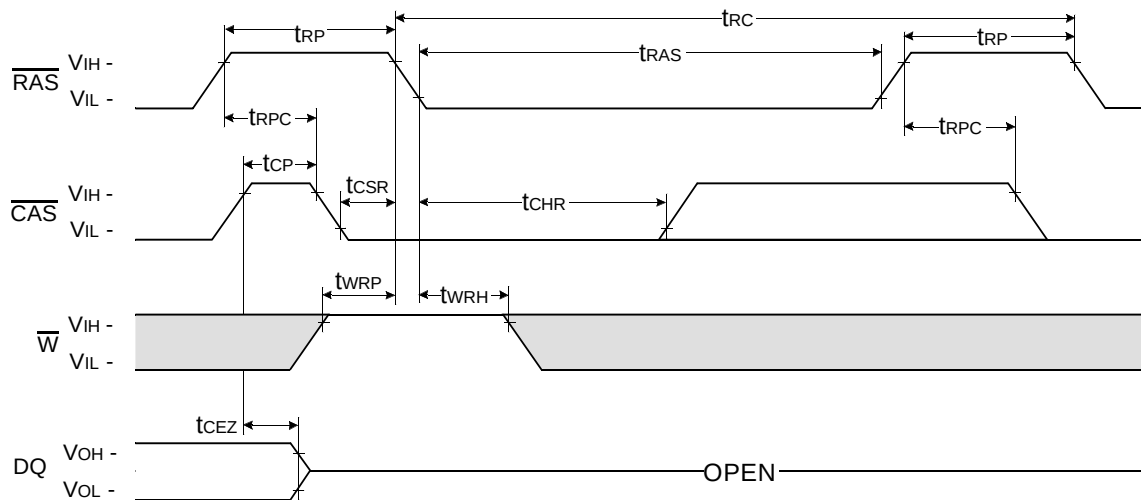
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

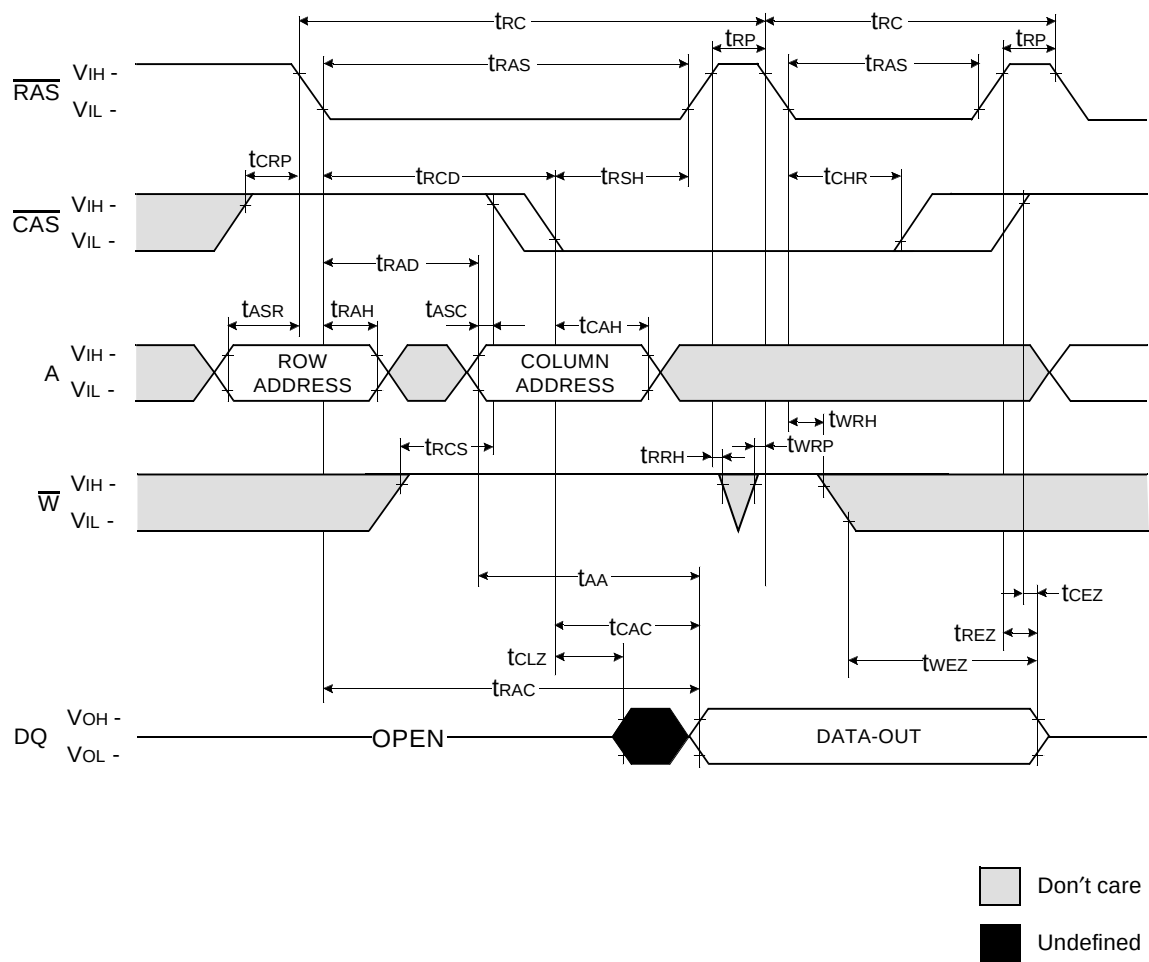
NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care
Undefined

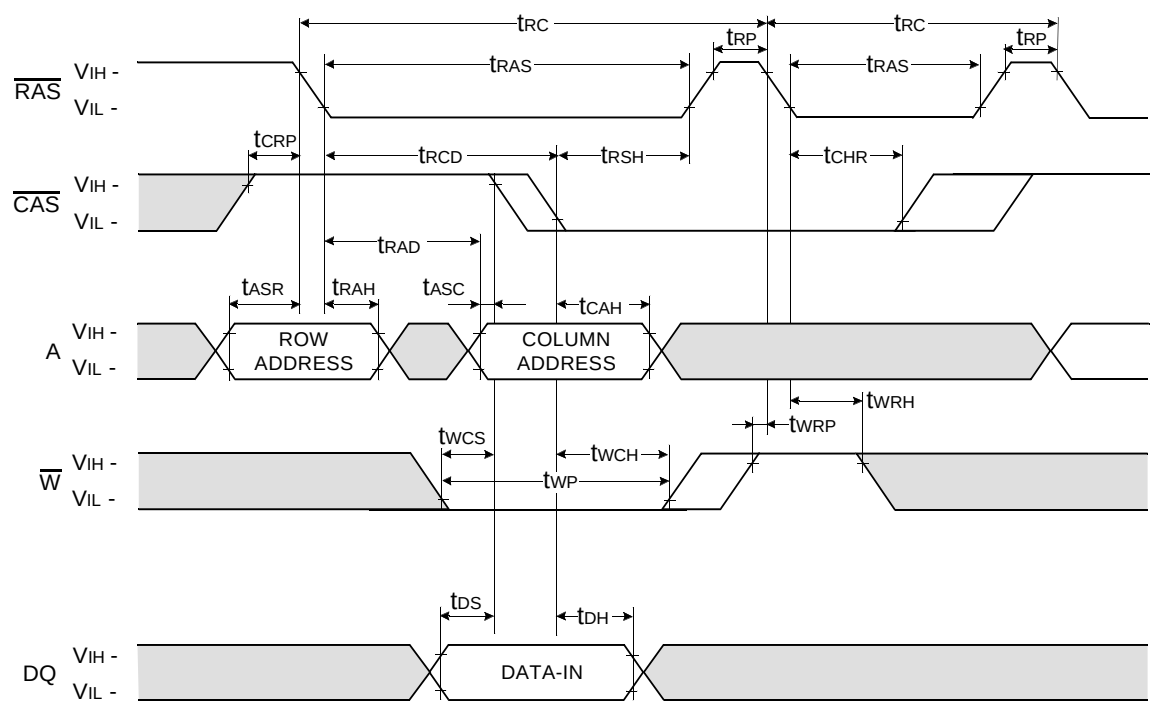
* In $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

HIDDEN REFRESH CYCLE (READ)

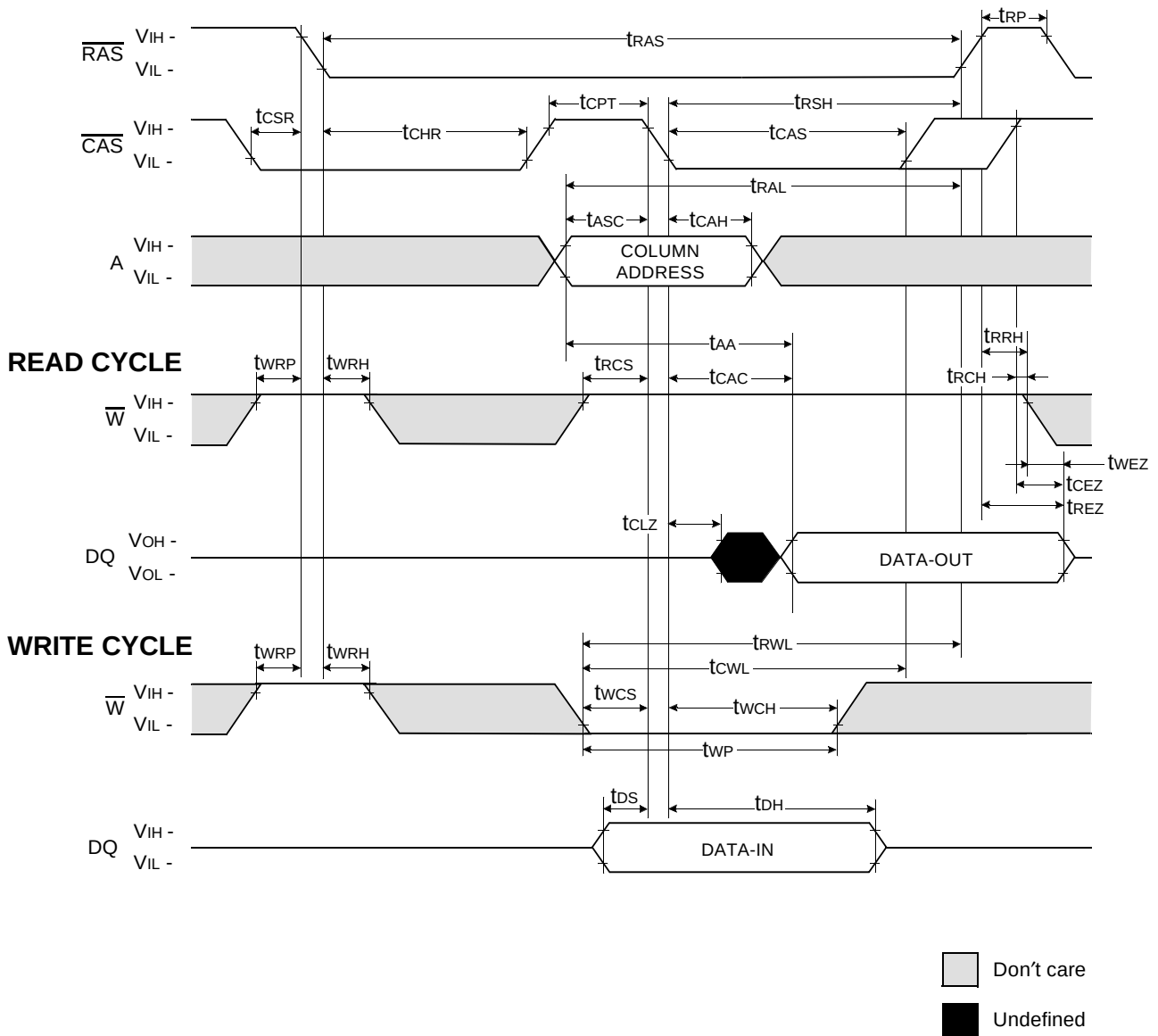


HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



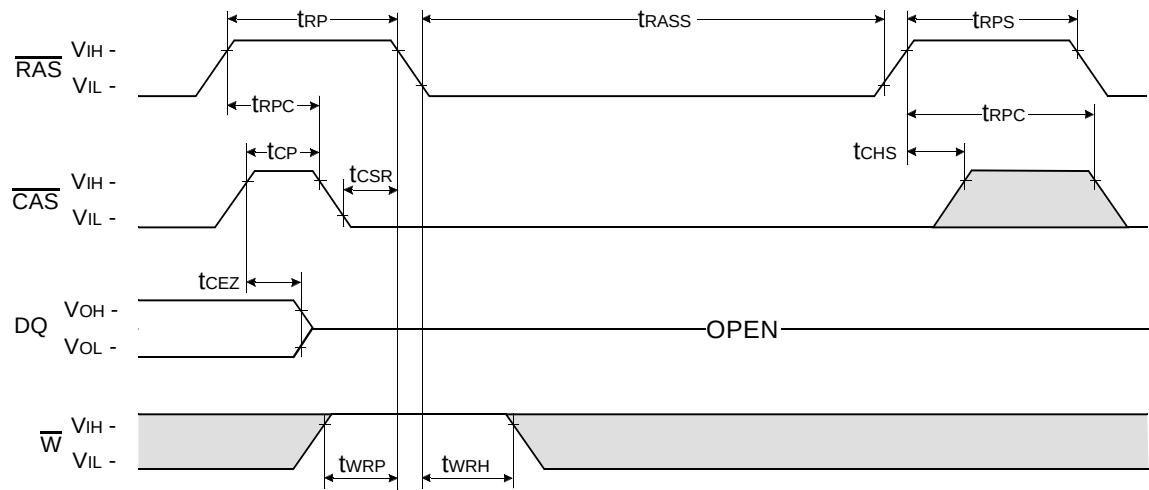
$\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

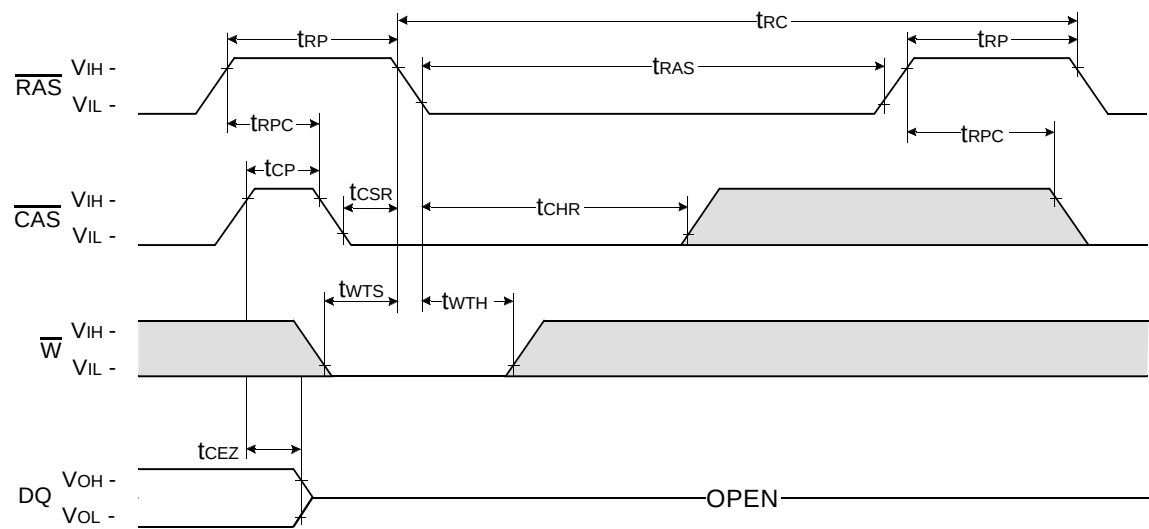
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care



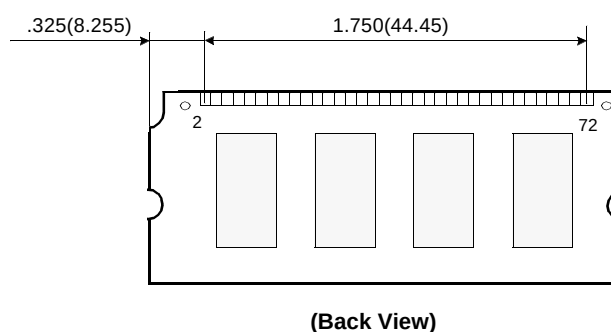
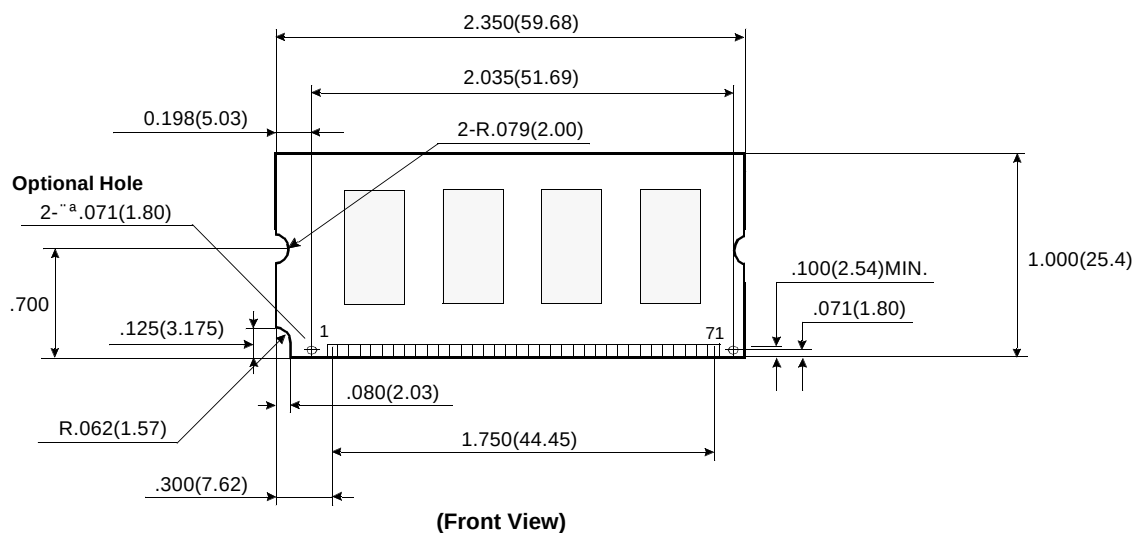
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DRAM MODULE

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KMM332F410CS-L

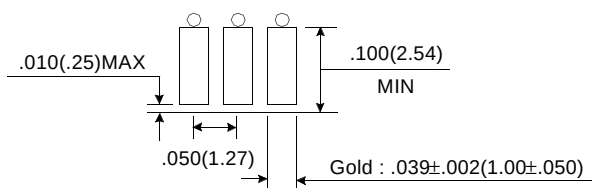
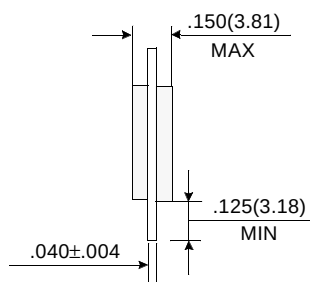
PACKAGE DIMENSIONS

Units : Inches (millimeters)



KMM332F40(1)0CS-L

Gold Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE: The used device is 4Mx4 DRAM, TSOP II

DRAM Part No : KMM332F400CS-L - KM44V4004CS-L (300mil) with Self Refresh

DRAM Part No : KMM332F410CS-L - KM44V4104CS-L (300mil) with Self Refresh

Revision History

Rev 0.0 : Aug. 1997