Buffered 8Mx64 DIMM

(8Mx8 base)

Revision 0.1

June 1998

Revision History

Version 0.0 (Sept. 1997)

•Removed two AC parameters t_{CACP}(access time from $\overline{CAS}$) and t_{AAP}(access time from col. addr.) in *AC CHARACTERISTICS*.

Version 0.1 (June 1998)

• The 3rd. generation of 64M DRAM components are applied for this module.

M364E080(8)3BJ(T)0-C EDO Mode

8M x 64 DRAM DIMM Using 8Mx8, 4K & 8K Refresh, 5V

GENERAL DESCRIPTION

The Samsung M364E080(8)3BJ(T)0-C is a 8Mx64bits Dynamic RAM high density memory module. The Samsung M364E080(8)3BJ(T)0-C consists of eight CMOS 8Mx8bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M364E080(8)3BJ(T)0-C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-C50	50ns	18ns	84ns	20ns
-C60	60ns	20ns	104ns	25ns

FEATURES

Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
M364E0803BJ0-C	SOJ	4K	4K/64ms	
M364E0803BT0-C	TSOP			
M364E0883BJ0-C	SOJ	8K	4K/64ms	8K/64ms
M364E0883BT0-C	TSOP			

- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1250mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V_{SS}	29	$\overline{CAS2}$	57	DQ22	85	V_{SS}	113	$\overline{CAS3}$	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	V_{CC}	87	DQ37	115	RFU	143	V_{CC}
4	DQ2	32	V_{SS}	60	DQ24	88	DQ38	116	V_{SS}	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	V_{CC}	34	A2	62	RFU	90	V_{CC}	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	*DQ26	94	DQ43	122	A11	150	*DQ62
11	*DQ8	39	A12	67	DQ27	95	*DQ44	123	*A13	151	DQ63
12	V_{SS}	40	V_{CC}	68	V_{SS}	96	V_{SS}	124	V_{CC}	152	V_{SS}
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	V_{SS}	71	DQ30	99	DQ47	127	V_{SS}	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	$\overline{RFU}$	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	V_{CC}	101	DQ49	129	*$\overline{RAS3}$	157	V_{CC}
18	V_{CC}	46	$\overline{CAS4}$	74	DQ32	102	V_{CC}	130	$\overline{CAS5}$	158	DQ68
19	DQ14	47	$\overline{CAS6}$	75	DQ33	103	DQ50	131	$\overline{CAS7}$	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	V_{CC}	77	*DQ35	105	DQ52	133	V_{CC}	161	*DQ71
22	*DQ17	50	RSVD	78	V_{SS}	106	*DQ53	134	RSVD	162	V_{SS}
23	V_{SS}	51	RSVD	79	PD1	107	V_{SS}	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	V_{CC}	54	V_{SS}	82	PD7	110	V_{CC}	138	V_{SS}	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	$\overline{RFU}$	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	V_{CC}	112	$\overline{CAS1}$	140	DQ57	168	V_{CC}

NOTE : A12 is used for only M364E0883BJ(T)0-C (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to V_{CC} at the next higher level assembly. PDs will be either open (NC) or driven to V_{SS} via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to V_{SS} without a buffer.

PIN NAMES

Pin Names	Function
A0, B0, A1 - A11	Address Input(4K ref.)
A0, B0, A1 - A12	Address Input(8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
V_{CC}	Power(+5V)
V_{SS}	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked '*' are not used in this module.

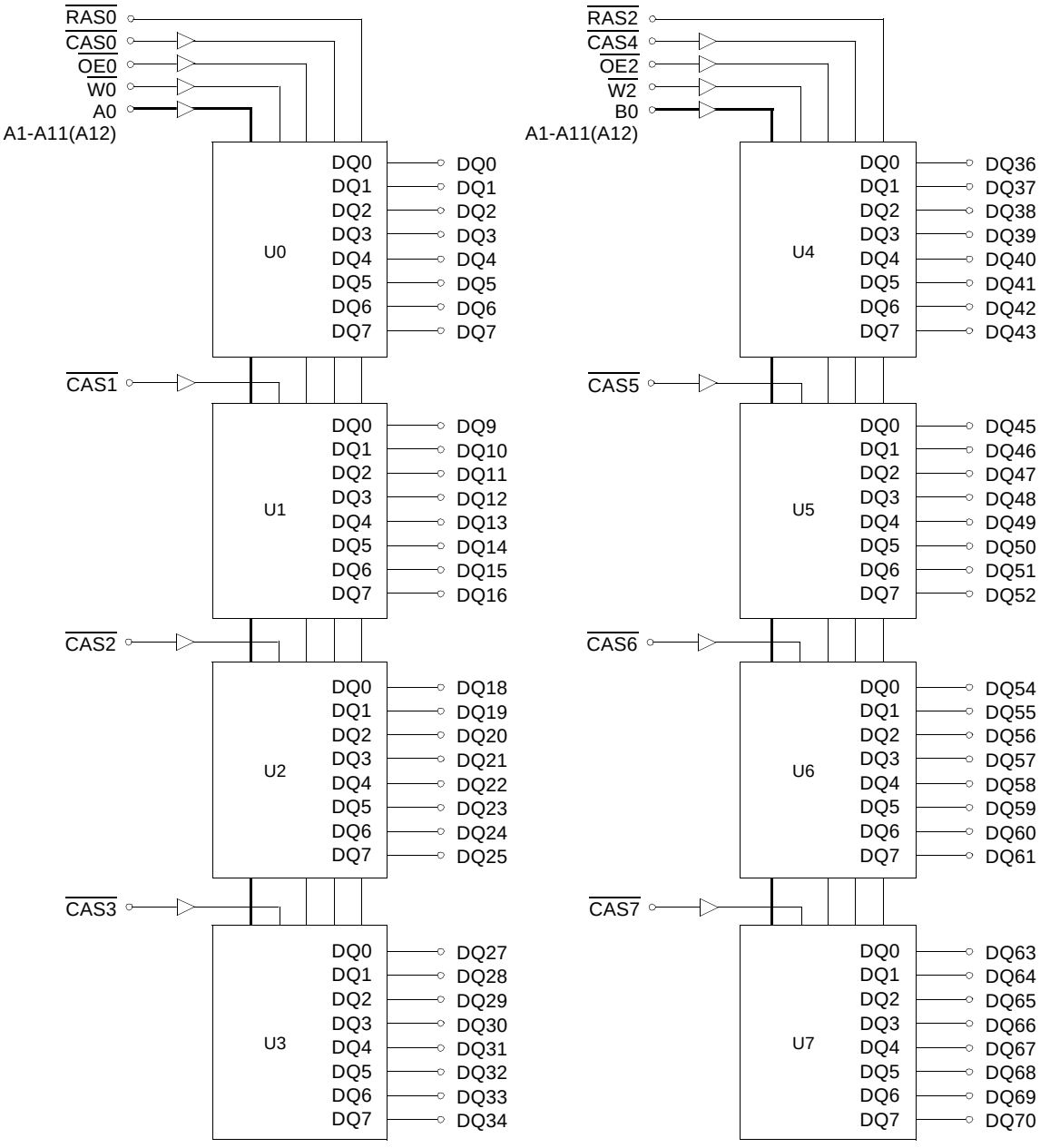
PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	1	1
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	1	1
ID0	0	0
ID1	0	0

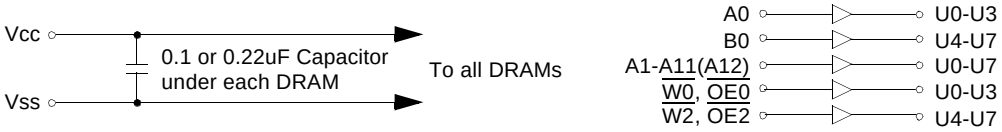
PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only M364E0883BJ(T)0 (8K Ref.)



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7.0	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}*1	V
Input Low Voltage	V_{IL}	-1.0*2	-	0.8	V

*1 : V_{CC}+2.0V at pulse width≤20ns, which is measured at V_{CC}.

*2 : -2.0V at pulse width≤20ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speedl	M364E0803BJ(T)0		M364E0883BJ(T)0		Unit
		Min	Max	Min	Max	
I_{CC1}	-50 -60	- -	960 880	- -	720 640	mA mA
I_{CC2}	Don't care	-	100	-	100	mA
I_{CC3}	-50 -60	- -	960 880	- -	720 640	mA mA
I_{CC4}	-50 -60	- -	880 800	- -	800 720	mA mA
I_{CC5}	Don't care	-	30	-	30	mA
I_{CC6}	-50 -60	- -	960 880	- -	720 640	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-10 -5	10 5	-10 -5	10 5	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	2.4 -	- 0.4	V V

I_{CC1}*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4}*: Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

I_{CC6}*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}Â Vcc)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

*** NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0, B0, A1 - A12]	C_{IN1}	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	38	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	20	pF
Input/Output capacitance[DQ0 - 71]	C_{DQ}	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	133		155		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	
Access time from $\overline{CAS}$	t_{CAC}		18		20	ns	3,4,5,13
Access time from column address	t_{AA}		30		35	ns	3,10,13
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	8		8		ns	3,13
$\overline{OE}$ to output in Low-Z	t_{OLZ}	8		8		ns	3,13
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	8	18	8	18	ns	6,11,13
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		ns	13
$\overline{CAS}$ hold time	t_{CSH}	36		43		ns	13
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	32	18	40	ns	4,13
$\overline{RAS}$ to column address delay time	t_{RAD}	13	20	13	25	ns	10,13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	13
Row address set-up time	t_{ASR}	5		5		ns	13
Row address hold time	t_{RAH}	8		8		ns	13
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	8		10		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	13
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	-2		-2		ns	8,13
Write command set-up time	t_{WCS}	0		0		ns	7
Write command hold time	t_{WCH}	10		10		ns	
Write command pulse width	t_{WP}	10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	18		20		ns	13
Write command to $\overline{CAS}$ lead time	t_{CWL}	8		10		ns	
Data set-up time	t_{DS}	-2		-2		ns	9,13
Data hold time	t_{DH}	13		15		ns	9,13
Refresh period(4K & 8K)	t_{REF}		64		64	ms	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	36		38		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	73		83		ns	7,13

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=5.0V±10%. See notes 1,2.)

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	48		53		ns	7
$\overline{CAS}$ precharge time to $\overline{W}$ delay time	t_{CPWD}	53		60		ns	
$\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10		10		ns	13
$\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	8		8		ns	13
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	3		3		ns	13
Access time from $\overline{CAS}$ precharge	t_{CPA}		33		40	ns	3,13
Hyper page cycle time	t_{HPC}	20		25		ns	12
Hyper page read-modify-write cycle time	t_{HPRWC}	70		77		ns	12
$\overline{CAS}$ precharge time(Hyper page cycle)	t_{CP}	8		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		ns	13
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t_{WRP}	15		15		ns	13
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t_{WRH}	8		8		ns	13
$\overline{OE}$ access time	t_{OEA}		18		20	ns	13
$\overline{OE}$ to data delay	t_{OED}	18		18		ns	13
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	8	18	8	18	ns	13
$\overline{OE}$ command hold time	t_{OEH}	13		15		ns	
Output data hold time($\overline{C}$-B-$\overline{R}$ refresh)	t_{DOH}	10		10		ns	13
Output buffer turn off delay time from $\overline{RAS}$	t_{REZ}	3	15	3	15	ns	6,11
Output buffer turn off delay time from $\overline{W}$	t_{WEZ}	8	18	8	20	ns	6,13
$\overline{W}$ to data delay	t_{WED}	20		20		ns	13
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	
Present Detect Read Cycle							
$\overline{PDE}$ to Valid PD bit	t_{PD}		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	t_{PDOFF}	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

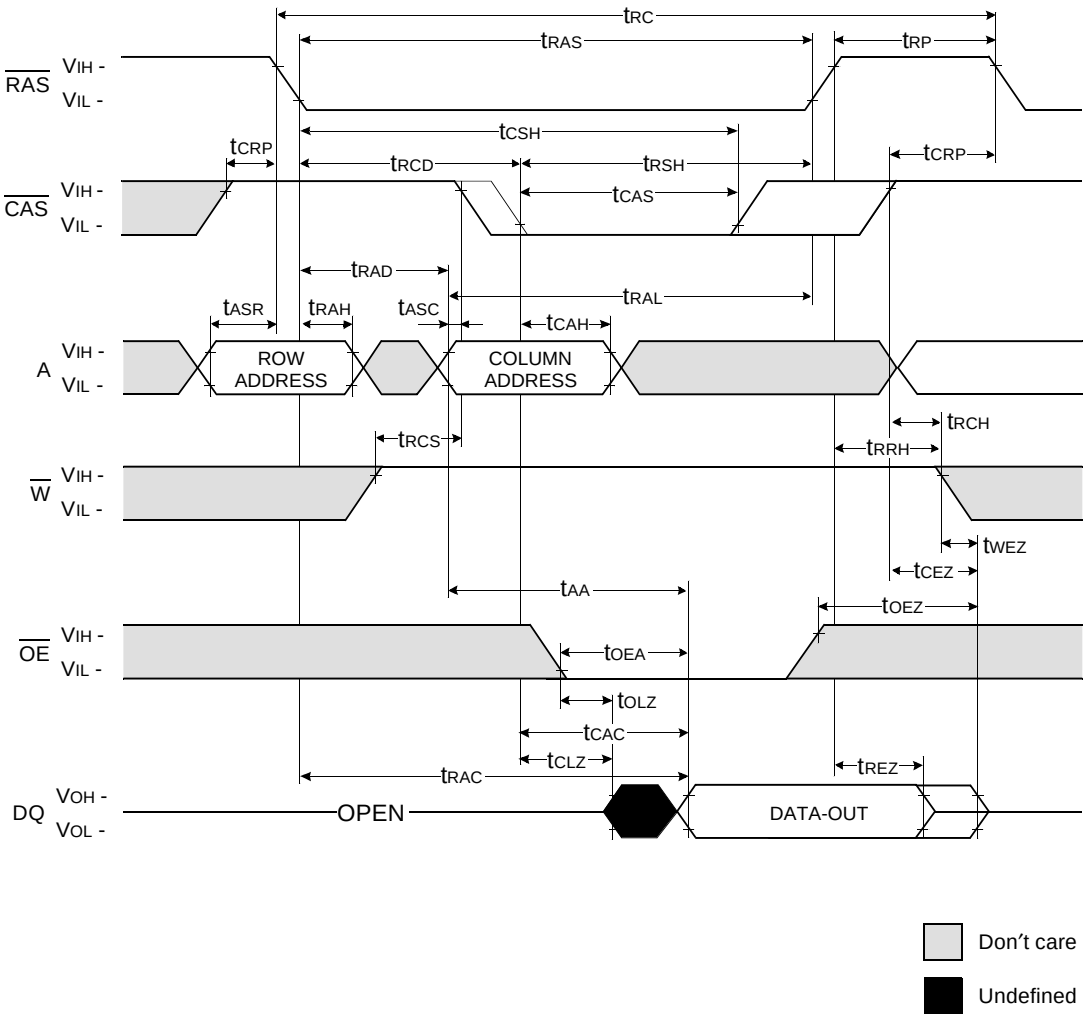
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. $t_{ASC} \geq 6$ns.

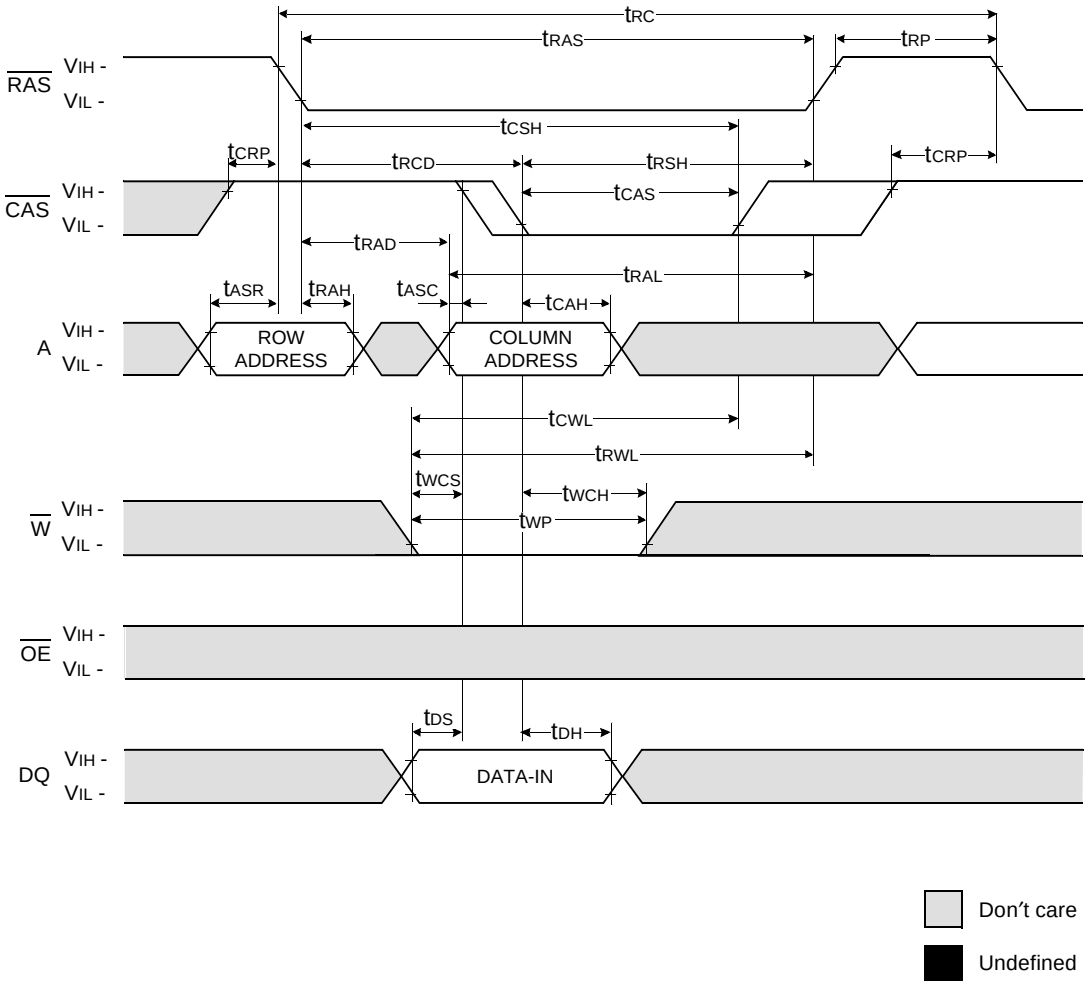
13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

READ CYCLE


tRC
tRAS
tRP
RAS
VIH -
VIL -
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A
ROW ADDRESS
COLUMN ADDRESS
tRCH
tRCS
tRRH
W
tWEZ
tCEZ
tAA
tOEZ
OE
tOEA
tOLZ
tCAC
tCLZ
tREZ
tRAC
DQ
VOH -
VOL -
OPEN
DATA-OUT
Don't care
Undefined

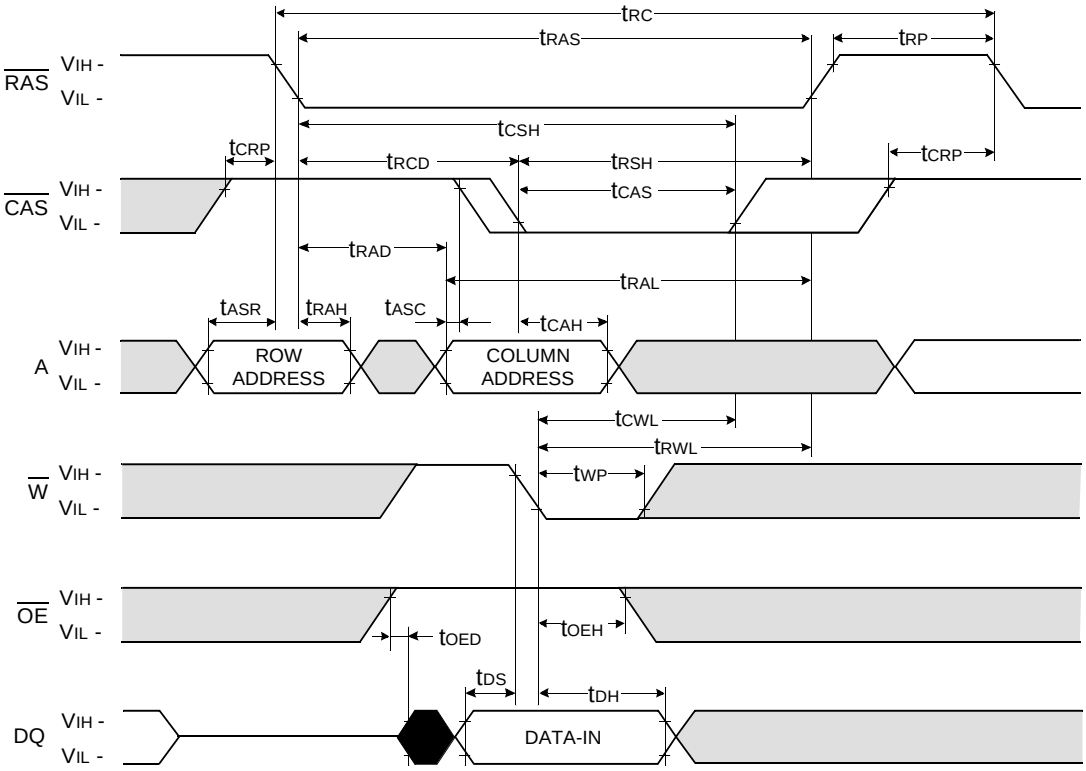
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

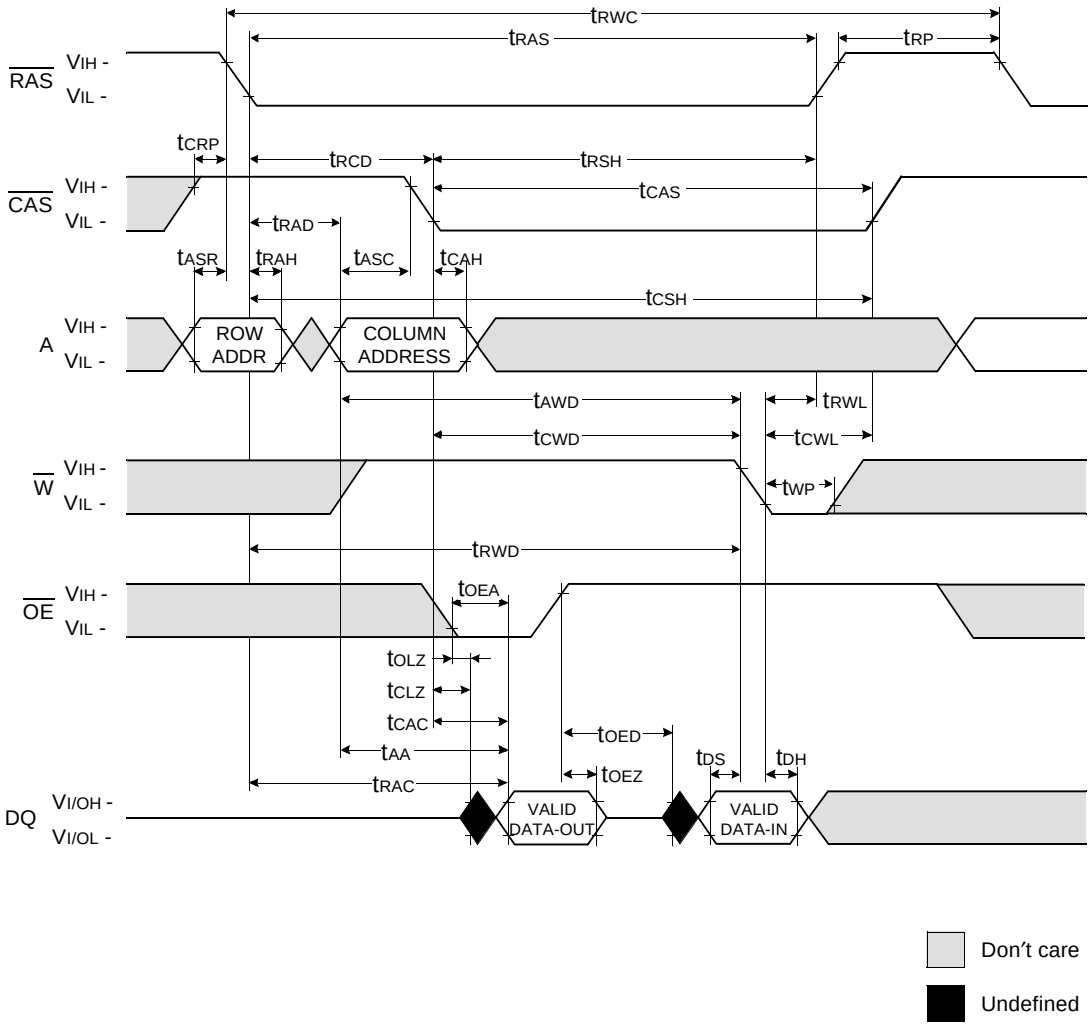


WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

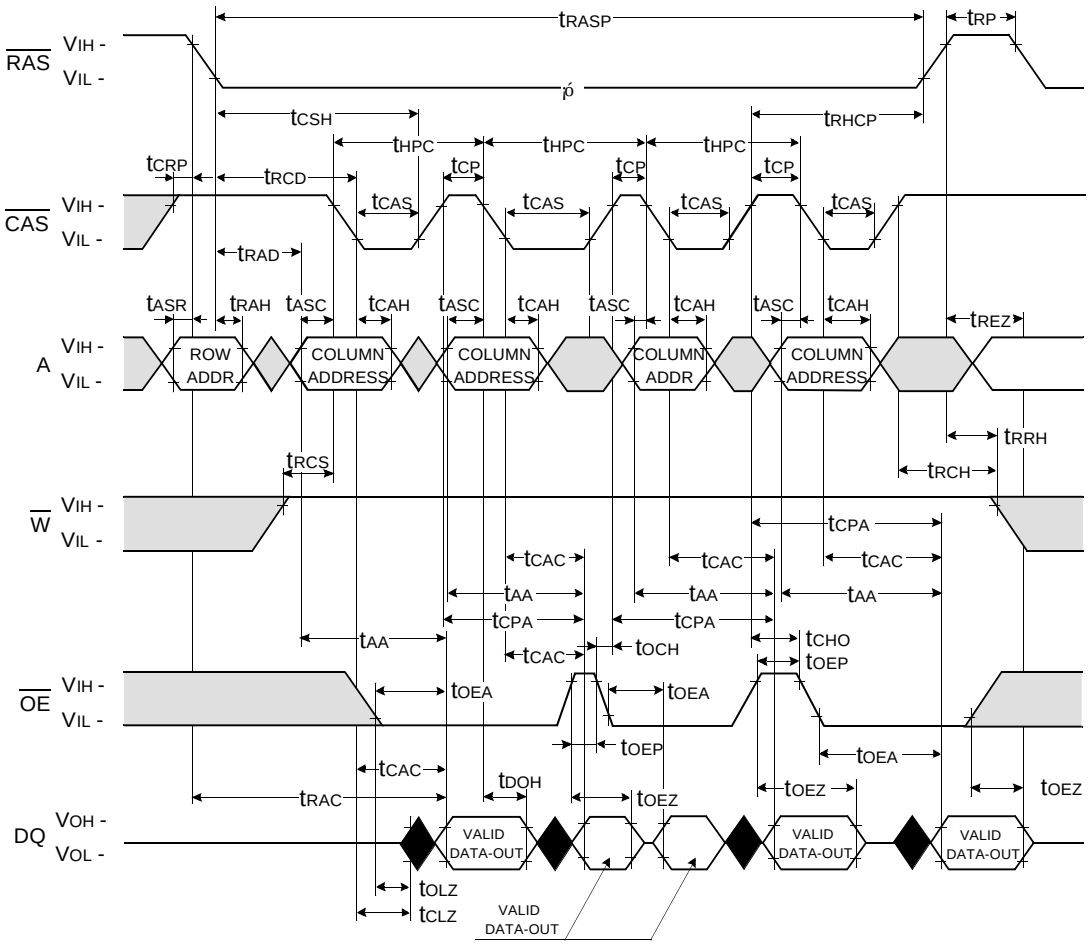
NOTE : DOUT = OPEN



READ - MODIFY - WRITE CYCLE

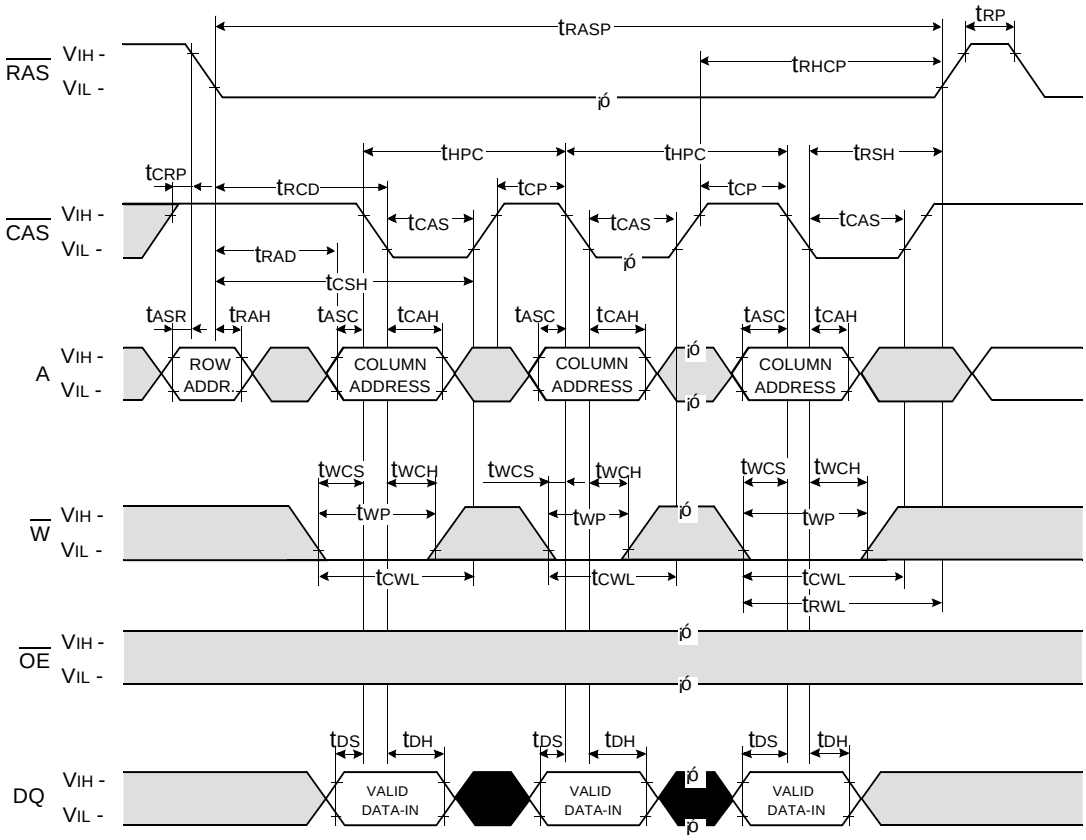


HYPER PAGE READ CYCLE

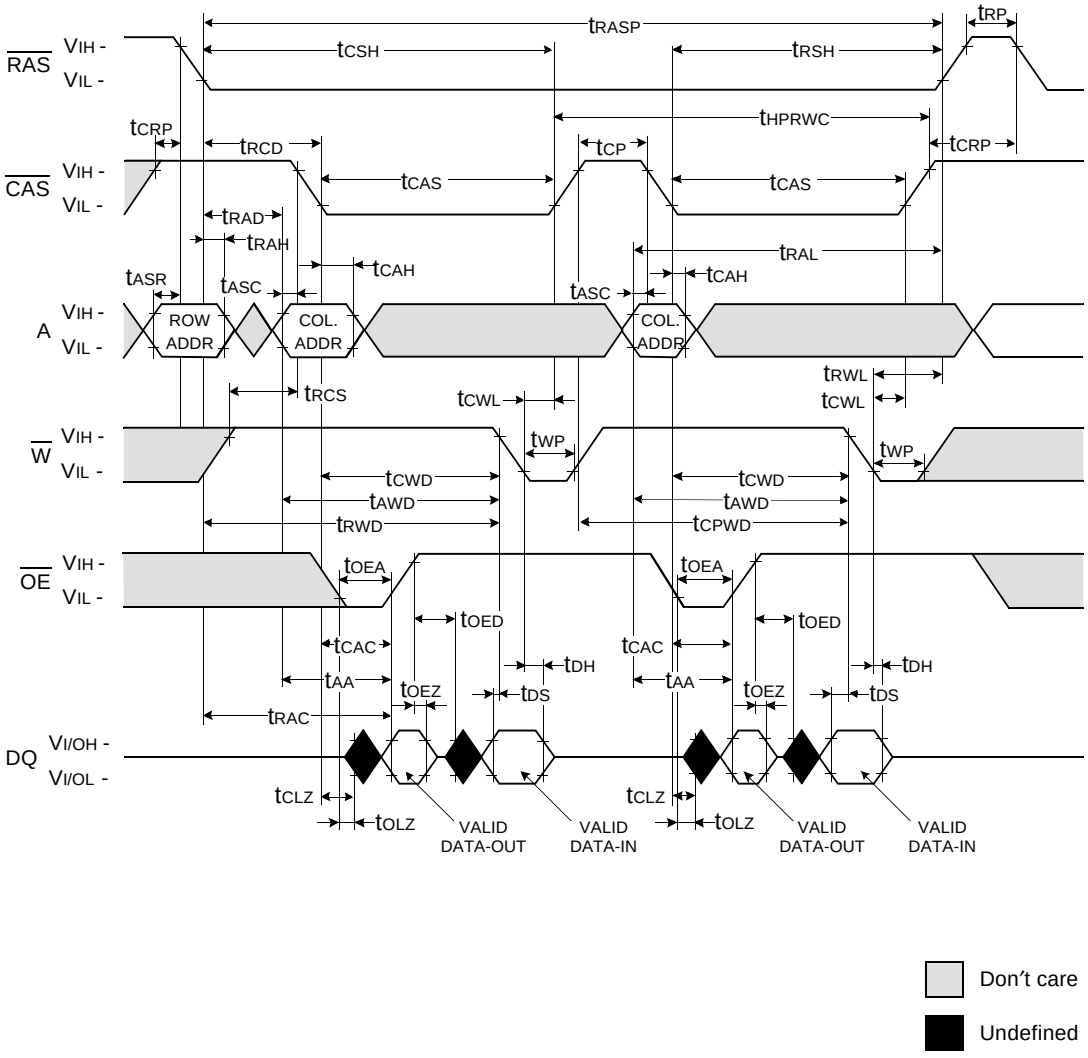


HYPER PAGE WRITE CYCLE (EARLY WRITE)

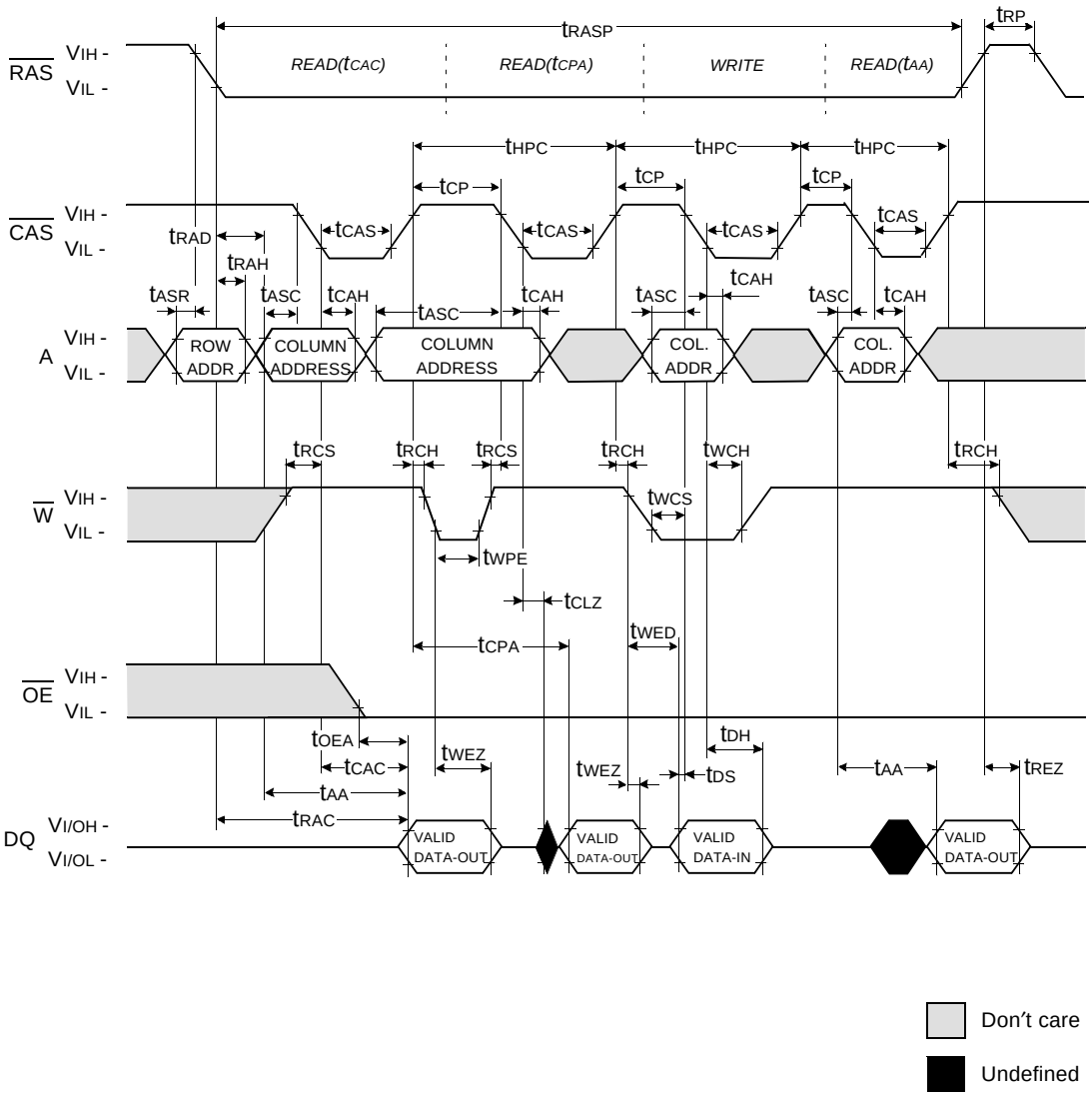
NOTE : DOUT = OPEN



HYPER PAGE READ-MODIFY-WRITE CYCLE



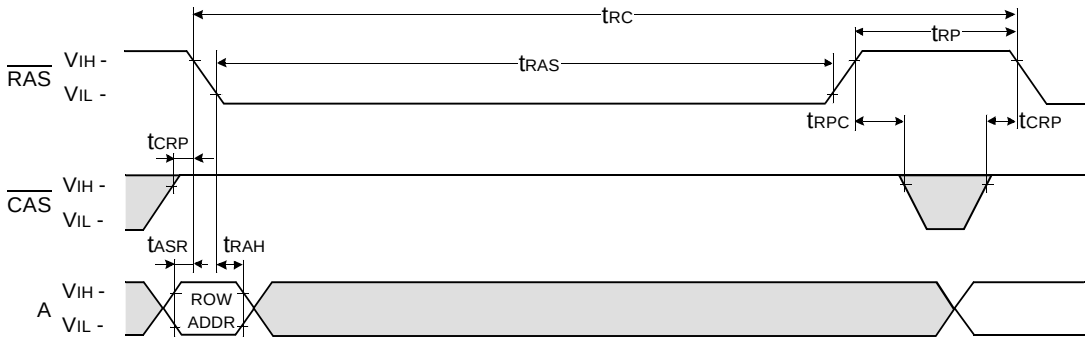
HYPER PAGE READ AND WRITE MIXED CYCLE



$\overline{RAS}$ - ONLY REFRESH CYCLE*

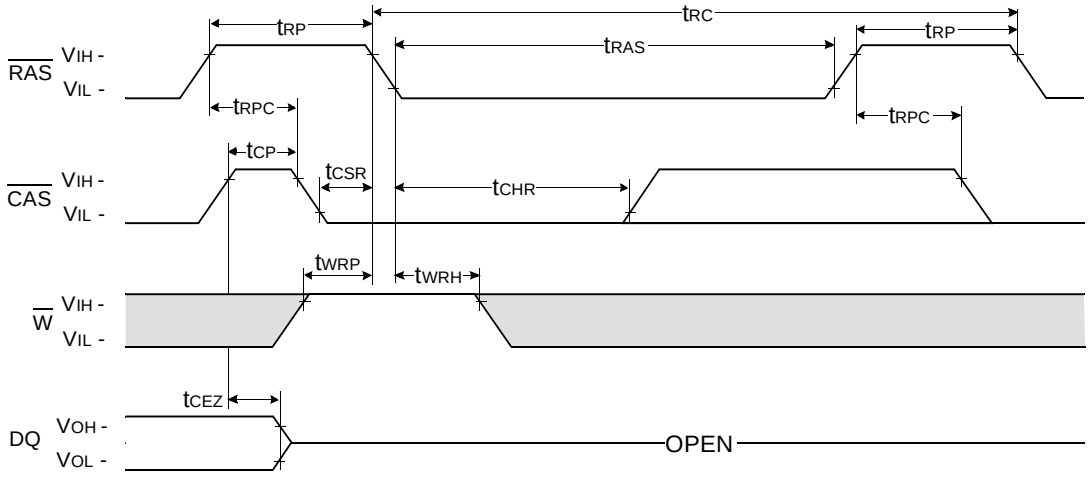
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care

D_{OUT} = OPEN



$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care

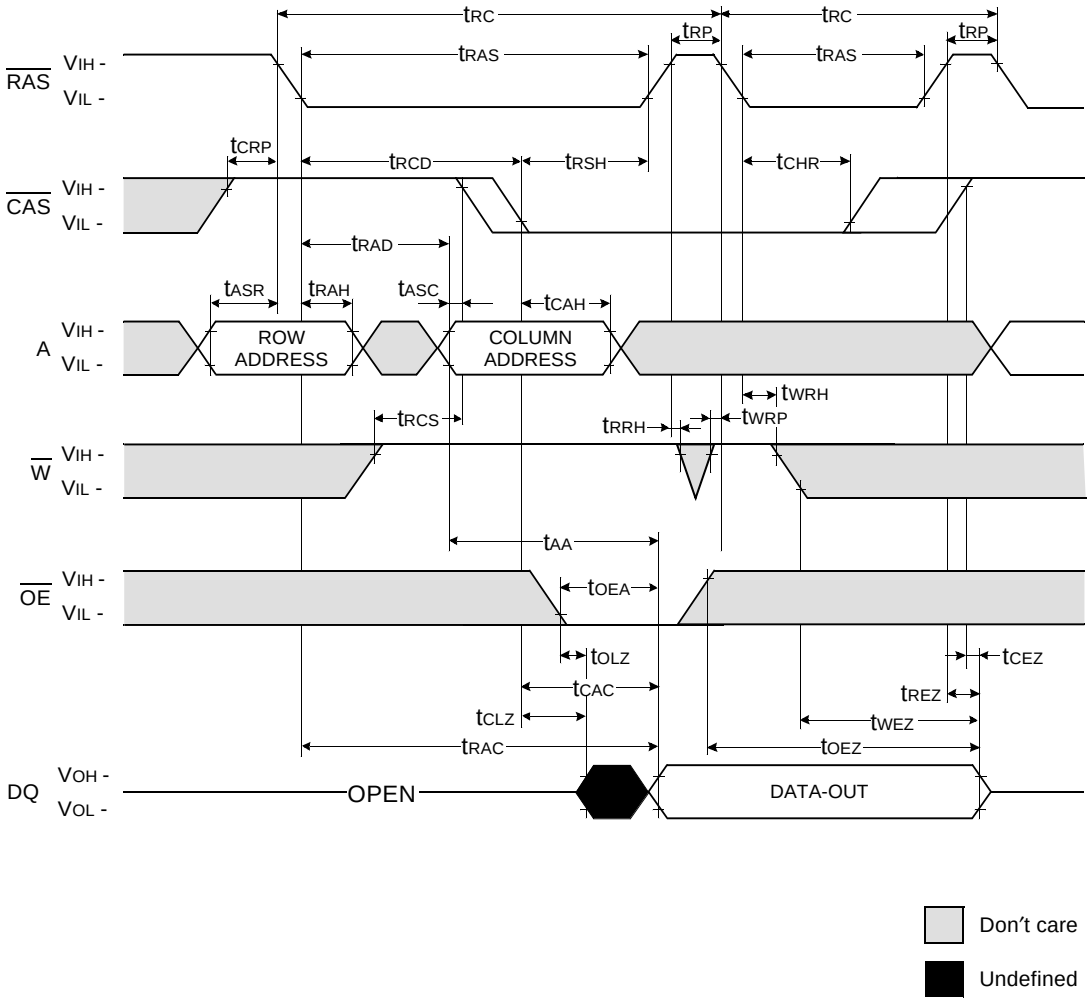


Don't care

Undefined

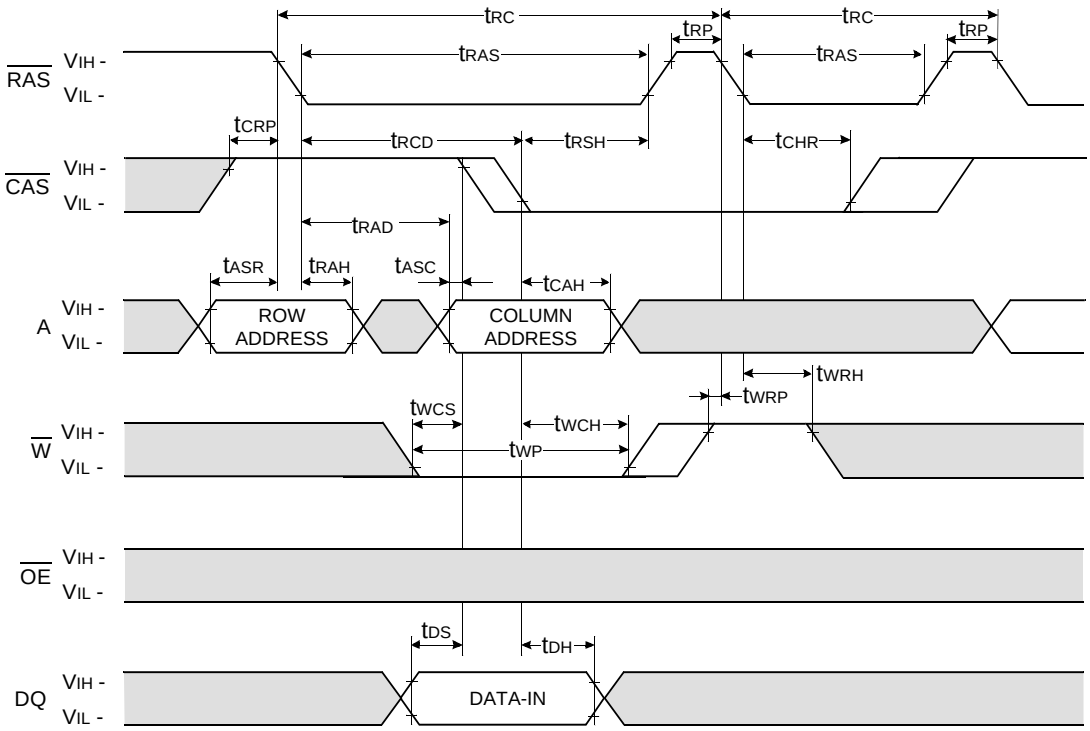
* In $\overline{RAS}$-only refresh cycle of 64Mb A-dile & B-die, when $\overline{CAS}$ signal transits from Low to High, the valid data may be cut off.

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

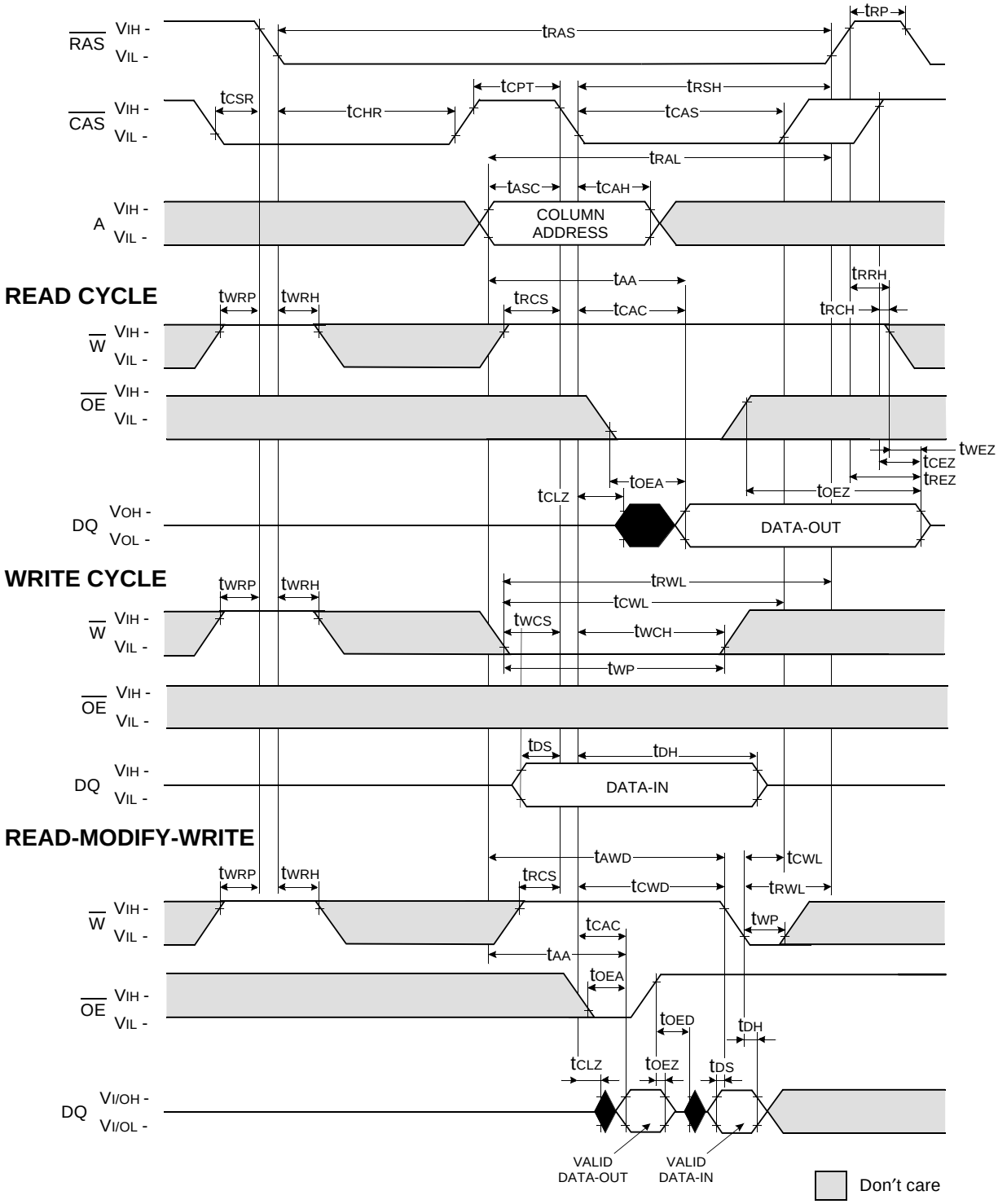
NOTE : DOUT = OPEN



Don't care

Undefined

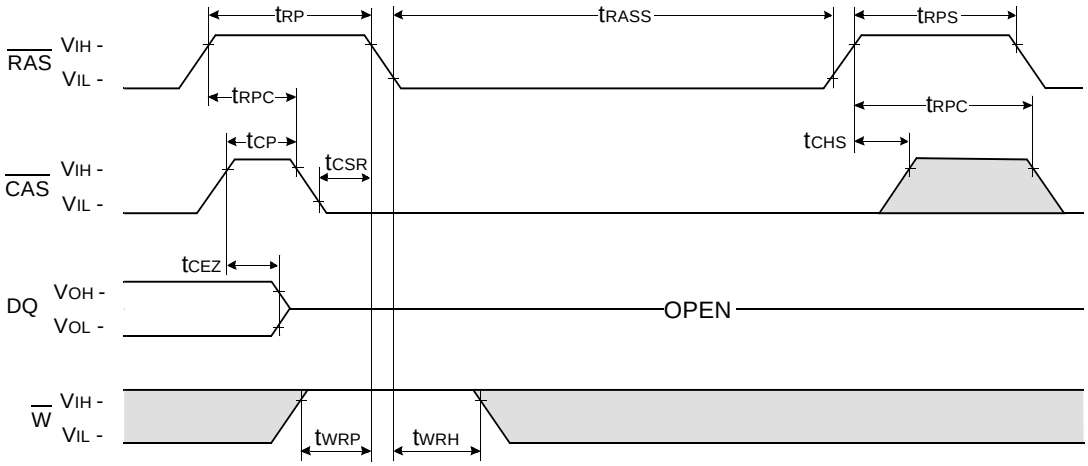
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

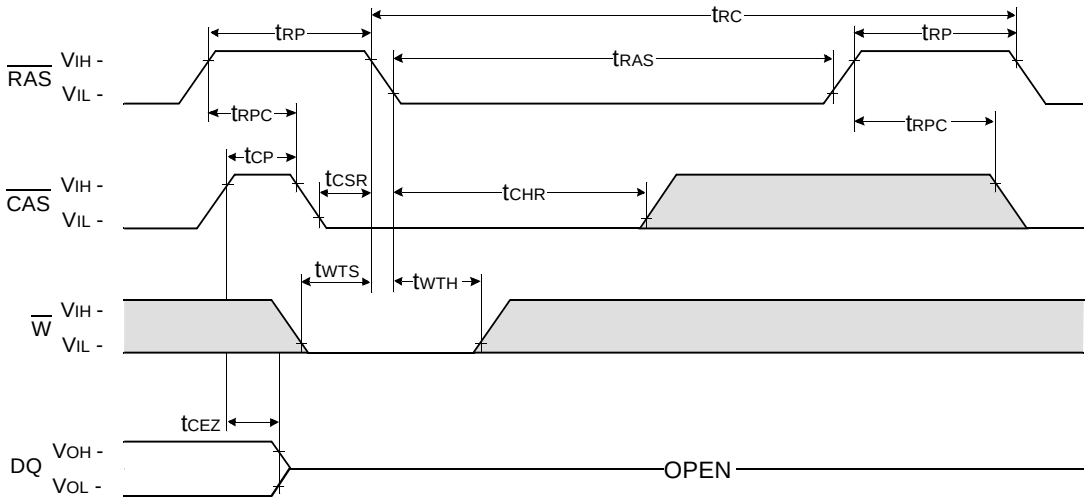
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care

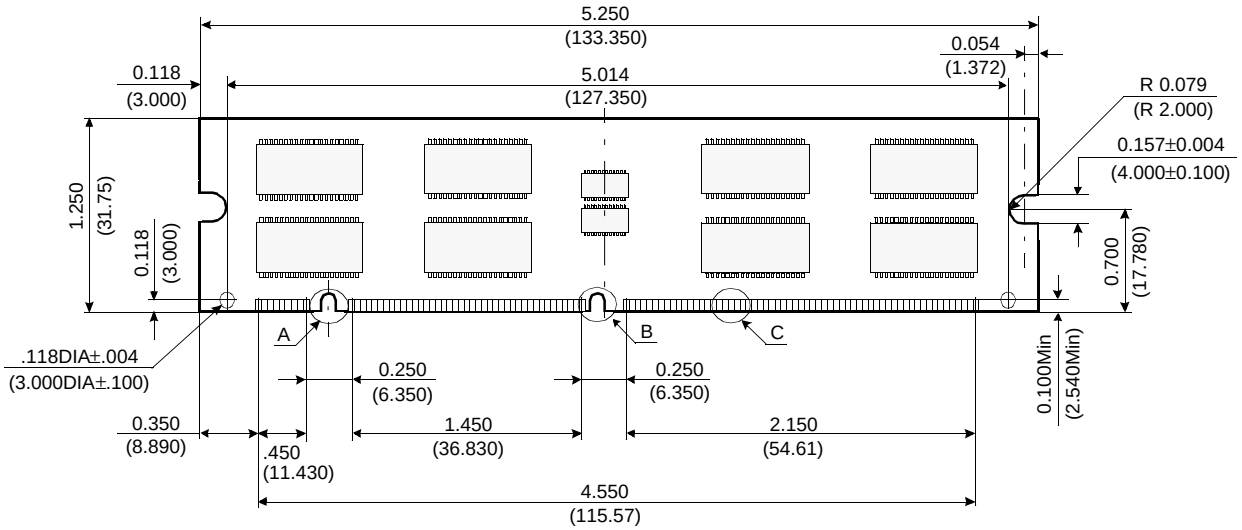


Don't care

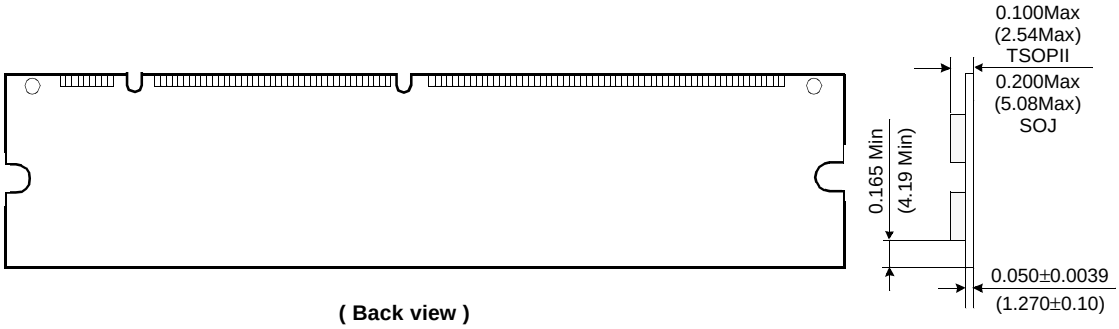
Undefined

PACKAGE DIMENSIONS

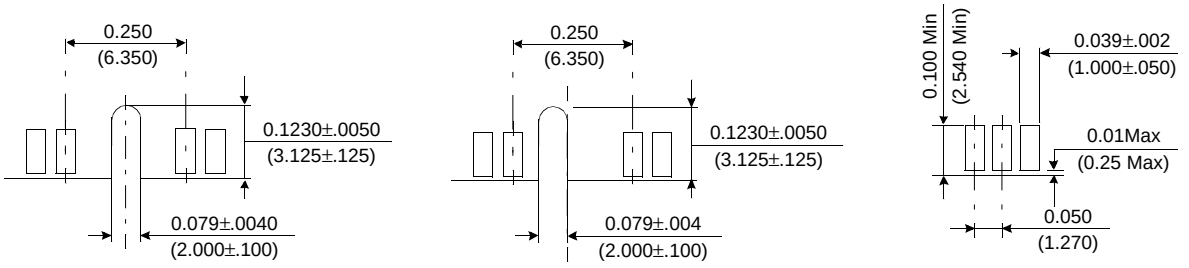
Units : Inches (millimeters)



(Front view)



(Back view)



Detail A **Detail B** **Detail C**

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 DRAM with EDO mode, SOJ or TSOPII.
DRAM Part No. : M364E0803BJ(T)0 - K4E640811B-J, K4E640811B-T
M364E0883BJ(T)0 - K4E660811B-J, K4E660811B-T