DDR SDRAM Unbuffered Module

184pin Unbuffered Module based on 512Mb B-die with 64/72-bit Non ECC/ECC

66 TSOP-II

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Revision History

Revision	Month	Year	History
0.0	February	2003	- First version for internal review
1.0	August	2003	- Revision 1.0 spec release.
1.1	June	2005	- Deleted “B0, AA, A2” speed and changed master format.

184Pin Unbuffered DIMM based on 512Mb B-die (x8, x16)

1.0 Ordering Information

Part Number	Density	Organization	Component Composition	Height
M368L3324BT(U)M-C(L)CC/B3	256MB	32M x 64	32Mx16 (K4H511638B) * 4EA	1,250mil
M368L6523BT(U)M-C(L)CC	512MB	64M x 64	64Mx8 (K4H510838B) * 8EA	1,250mil
M368L6523BT(U)N-C(L)B3				
M381L6523BT(U)M-C(L)CC/B3	512MB	64M x 72	64Mx8 (K4H510838B) * 9EA	1,250mil
M368L2923BT(U)M-C(L)CC	1GB	128M x 64	64Mx8 (K4H510838B) * 16EA	1,250mil
M368L2923BT(U)N-C(L)B3				
M381L2923BT(U)M-C(L)CC/B3	1GB	128M x 72	64Mx8 (K4H510838B) * 18EA	1,250mil

Note : Leaded and Lead-free(Pb-free) can be discriminated by PKG P/N (T : 66 TSOP with Leaded, U : 66 TSOP with Lead-free)

2.0 Operating Frequencies

	CC(DDR400@CL=3)	B3(DDR333@CL=2.5)
Speed @CL2	-	133MHz
Speed @CL2.5	166MHz	166MHz
Speed @CL3	200MHz	-
CL-tRCD-tRP	3-3-3	2.5-3-3

3.0 Feature

- VDD : 2.5V ± 0.2V, VDDQ : 2.5V ± 0.2V for DDR333
- VDD : 2.6V ± 0.1V, VDDQ : 2.6V ± 0.1V for DDR400
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe [DQ] (x4,x8) & [L(U)DQS] (x16)
- Differential clock inputs(CK and $\overline{CK}$)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency : DDR333(2.5 Clock), DDR400(3 Clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
- Serial presence detect with EEPROM
- PCB : Height 1,250 (mil) & single (256, 512MB), double (1GB) sided
- SSTL_2 Interface
- 66pin TSOP II **(Leaded & Pb-Free(RoHS compliant))** package

4.0 Pin Configuration (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	$\overline{RAS}$
2	DQ0	33	DQ24	63	$\overline{WE}$	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	$\overline{CAS}$	96	VDDQ	127	DQ29	157	$\overline{CS0}$
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	$\overline{CS1}$
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	*$\overline{CS2}$	102	NC	133	DQ31	163	*$\overline{CS3}$
11	VSS	42	VSS	72	DQ48	103	NC	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	*$\overline{CK2}$	106	DQ13	137	$\overline{CK0}$	167	*A13
15	VDDQ	46	VDD	76	*CK2	107	DM1	138	$\overline{CK0}$	168	VDD
16	$\overline{CK1}$	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	$\overline{CK1}$	48	A0	78	DQS6	109	DQ14	140	DM8	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	*BA2	144	CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

Note :
1. * : These pins are not used in this module.
2. Pins 44, 45, 47, 49, 51, 134, 135, 140, 142, 144 are used on x72 module (M381~), and are not used on x64 module.
3. Pins 111, 158 are NC for 1row modules & used for 2row modules[M368(81)L2923B].
4. Pins 137, 138 are NC for x16 1Row module (M368L3324B).

5.0 Pin Description

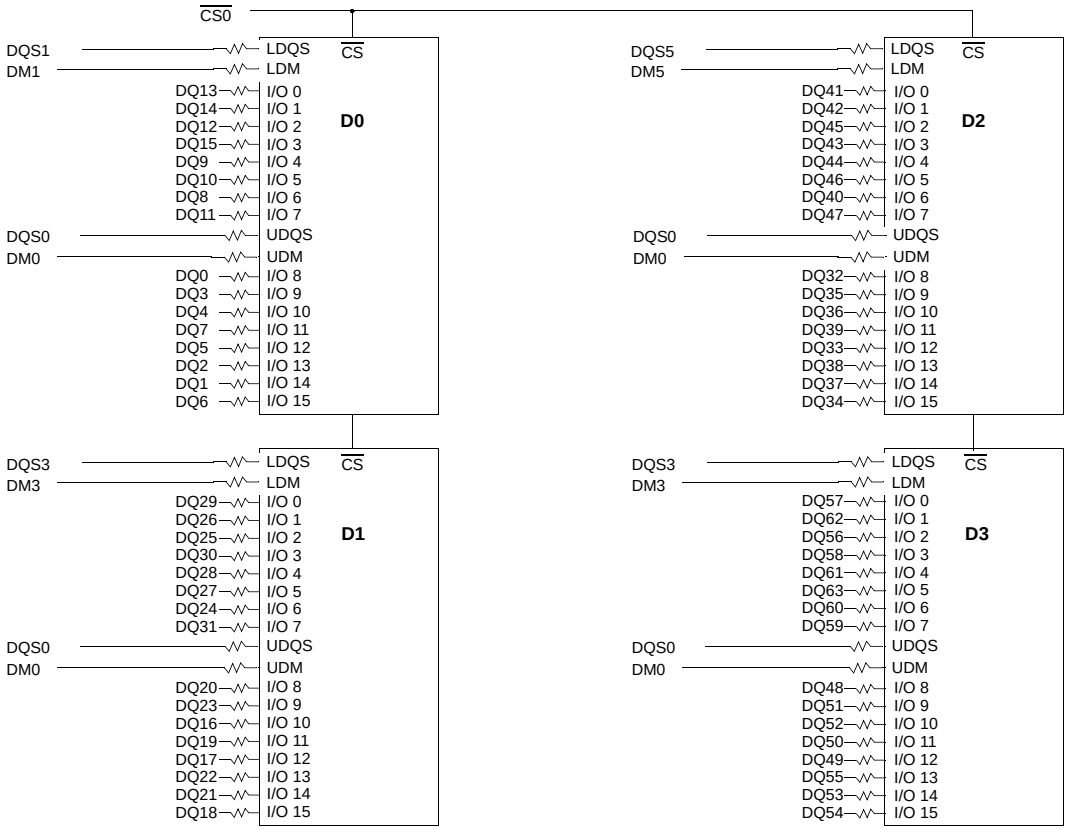
Pin Name	Function	Pin Name	Function
A0 ~ A12	Address input (Multiplexed)	DM0 ~7,8(for ECC)	Data - in mask
BA0 ~ BA1A	Bank Select Address	VDD	Power supply (2.5V for DDR333, 2.6V for DDR400)
DQ0 ~ DQ63	Data input/output	VDDQ	Power Supply for DQS (2.5V for DDR333, 2.6V for DDR400)
DQS0 ~ DQS8	Data Strobe input/output	VSS	Ground
CK0,$\overline{CK0}$ ~ CK2, $\overline{CK2}$	Clock input	VREF	Power supply for reference
CKE0, CKE1(for double banks)	Clock enable input	VDDSPD	Serial EEPROM Power/Supply (2.3V to 3.6V)
$\overline{CS0}$, $\overline{CS1}$(for double banks)	Chip select input	SDA	Serial data I/O
$\overline{RAS}$	Row address strobe	SCL	Serial clock
$\overline{CAS}$	Column address strobe	SA0 ~ 2	Address in EEPROM
$\overline{WE}$	Write enable	VDDID	VDD, VDDQ level detection
CB0 ~ CB7(for x72 module)	Check bit(Data-in/data-out)	NC	No connection

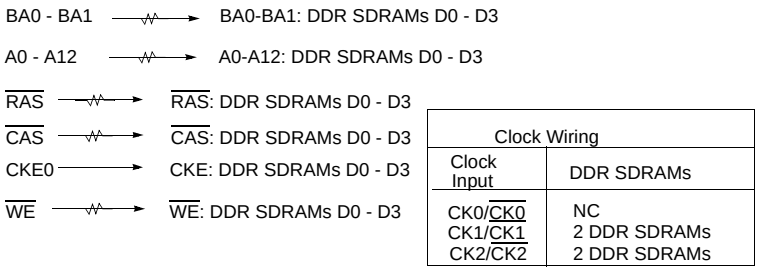
Note : VDDID defines relationship of VDD and VDDQ, and the default status of it is open (VDD=VDDQ)

6.0 Functional Block Diagram

6.1 256MB, 32M x 64 Non ECC Module (M368L3324BT(U))

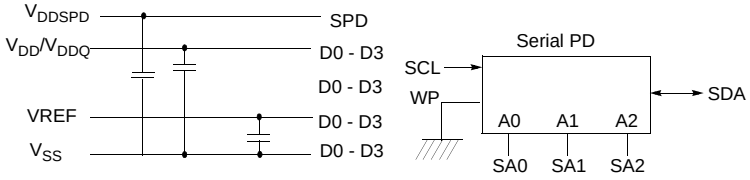
(Populated as 1 bank of x16 DDR SDRAM Module)





Clock Wiring

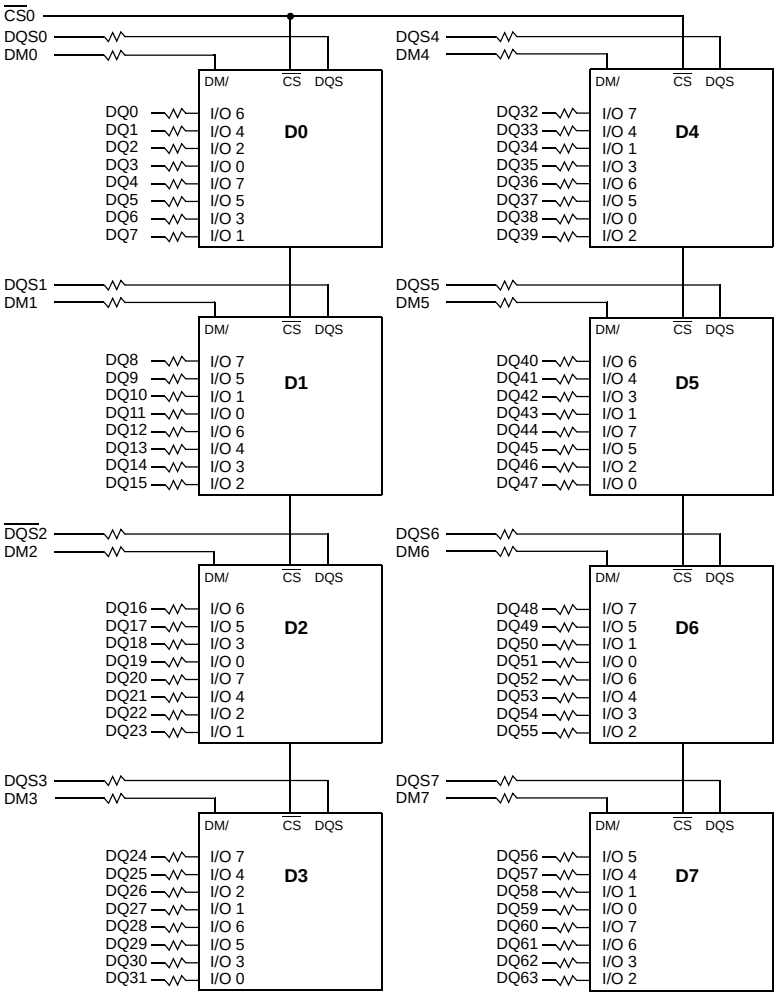
Clock Input	DDR SDRAMs
CK0/CK0	NC
CK1/CK1	2 DDR SDRAMs
CK2/CK2	2 DDR SDRAMs

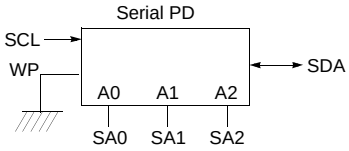


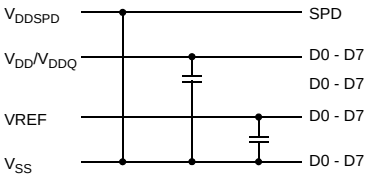
Notes:
1. DQ-to-I/O wiring is shown as recomended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms ± 5%.
4. BAx, Ax, RAS, CAS, WE resistors: 7.5 Ohms ± 5%

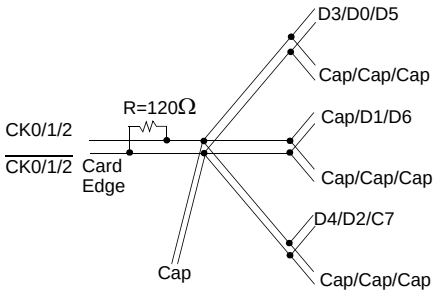
6.2 512MB, 64M x 64 Non ECC Module (M368L6523BT(U))

(Populated as 1 bank of x8 DDR SDRAM Module)









BA0 - BA1 → BA0-BA1 : DDR SDRAMs D0 - D7

A0 - A12 → A0-A12 : DDR SDRAMs D0 - D7

$\overline{RAS}$ → $\overline{RAS}$: DDR SDRAMs D0 - D7

$\overline{CAS}$ → $\overline{CAS}$: DDR SDRAMs D0 - D7

CKE0 → CKE : DDR SDRAMs D0 - D7

$\overline{WE}$ → $\overline{WE}$: DDR SDRAMs D0 - D7

* Clock Wiring	
Clock Input	DDR SDRAMs
*CK0/$\overline{CK0}$	2 DDR SDRAMs
*CK1/$\overline{CK1}$	3 DDR SDRAMs
*CK2/CK2	3 DDR SDRAMs

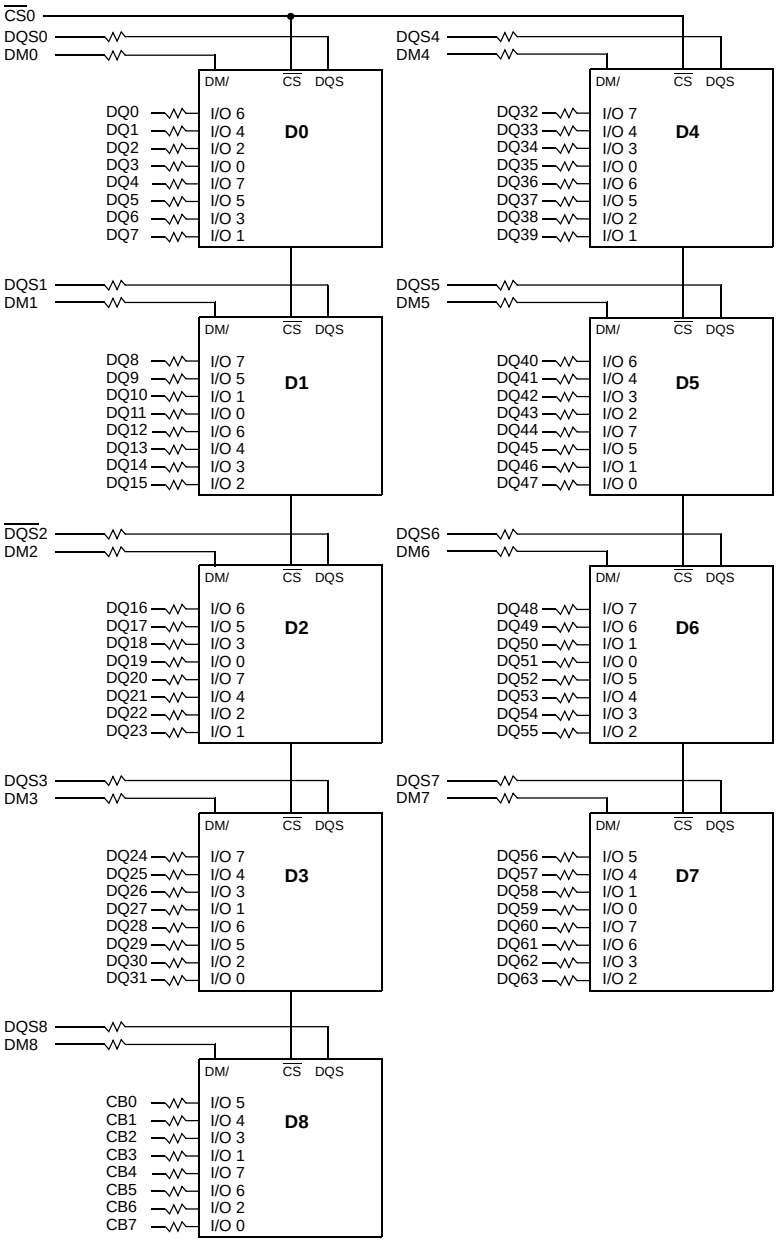
*Clock Net Wiring

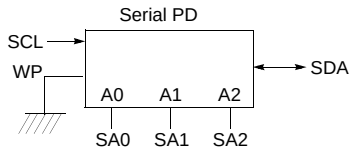
Notes :

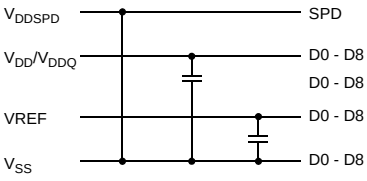
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/$\overline{CS}$ relationships must be maintained as shown.
3. DQ, DQS, $\overline{DM}$/$\overline{DQS}$ resistors: 22 Ohms ± 5%.
4. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: 5.1 Ohms ± 5%

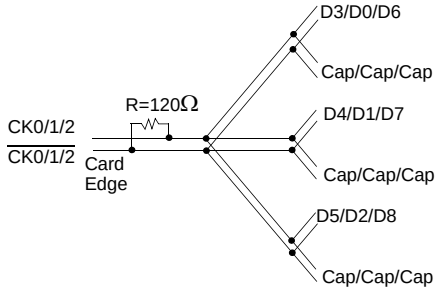
6.3 512MB, 64M x 72 ECC Module (M381L6523BT(U))

(Populated as 1 bank of x8 DDR SDRAM Module)









BA0 - BA1 → BA0-BA1 : DDR SDRAMs D0 - D8

A0 - A12 → A0-A12 : DDR SDRAMs D0 - D8

$\overline{RAS}$ → $\overline{RAS}$: DDR SDRAMs D0 - D8

$\overline{CAS}$ → $\overline{CAS}$: DDR SDRAMs D0 - D8

CKE0 → CKE : DDR SDRAMs D0 - D8

$\overline{WE}$ → $\overline{WE}$: DDR SDRAMs D0 - D8

* Clock Wiring	
Clock Input	DDR SDRAMs
*CK0/$\overline{CK0}$	3 DDR SDRAMs
*CK1/$\overline{CK1}$	3 DDR SDRAMs
*CK2/$\overline{CK2}$	3 DDR SDRAMs

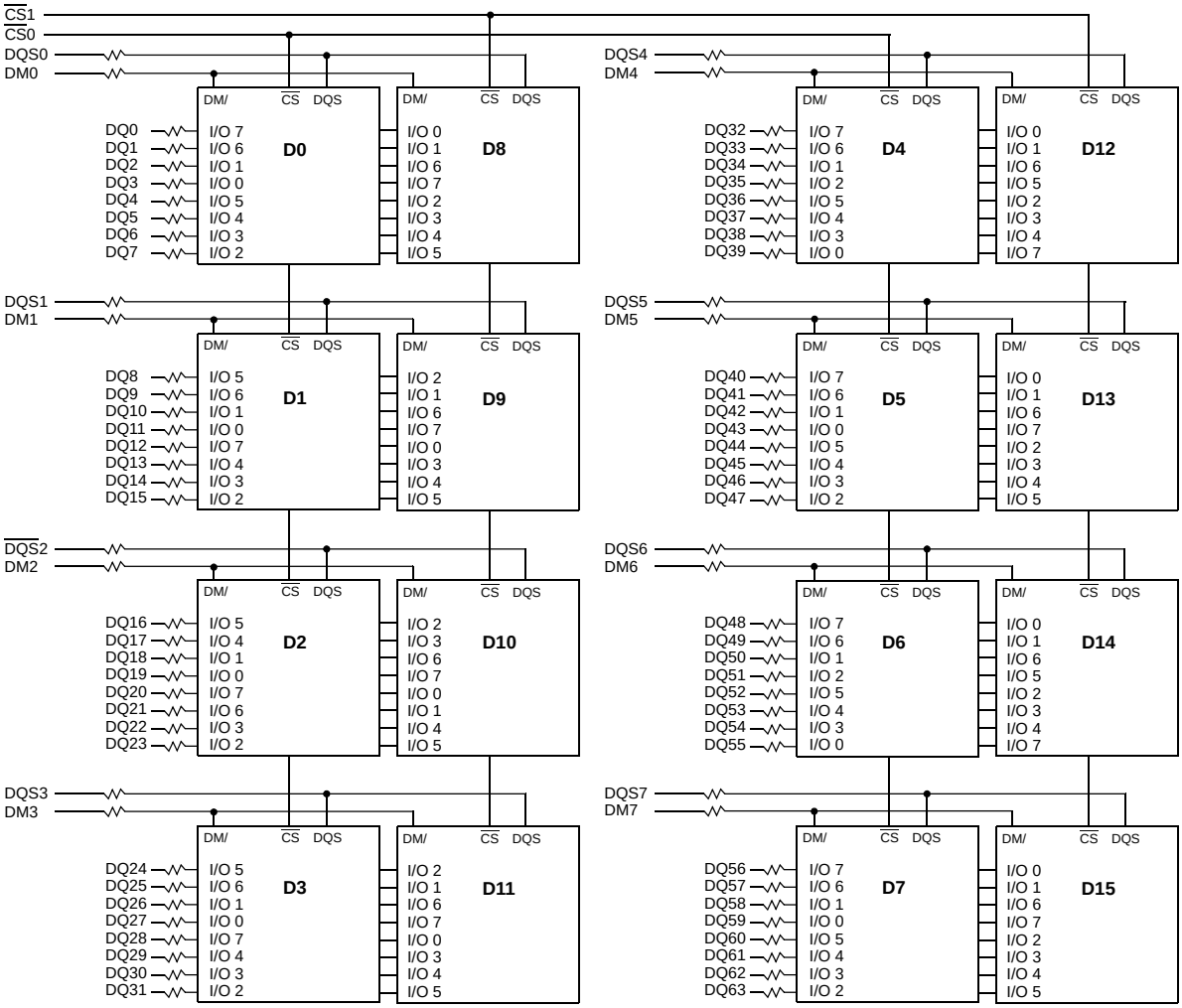
*Clock Net Wiring

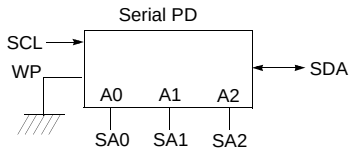
Notes :

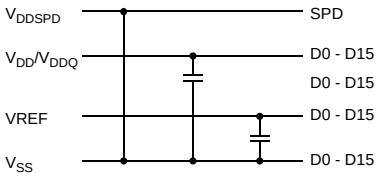
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/$\overline{CS}$ relationships must be maintained as shown.
3. DQ, DQS, DM/$\overline{DQS}$ resistors: 22 Ohms ± 5%.
4. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: 5.1 Ohms ± 5%

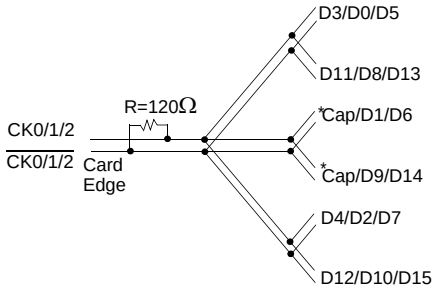
6.4 1GB, 128M x 64 Non ECC Module (M368L2923BT(U))

(Populated as 2 bank of x8 DDR SDRAM Module)









BA0 - BA1 → BA0-BA1 : DDR SDRAMs D0 - D15

A0 - A12 → A0-A12: DDR SDRAMs D0 - D15

$\overline{RAS}$ → $\overline{RAS}$: DDR SDRAMs D0 - D15

$\overline{CAS}$ → $\overline{CAS}$: DDR SDRAMs D0 - D15

CKE 0/1 → CKE : DDR SDRAMs D0 - D15

$\overline{WE}$ → $\overline{WE}$: DDR SDRAMs D0 - D15

* Clock Wiring	
Clock Input	DDR SDRAMs
*CK0/$\overline{CK0}$	4 DDR SDRAMs
*CK1/$\overline{CK1}$	6 DDR SDRAMs
*CK2/$\overline{CK2}$	6 DDR SDRAMs

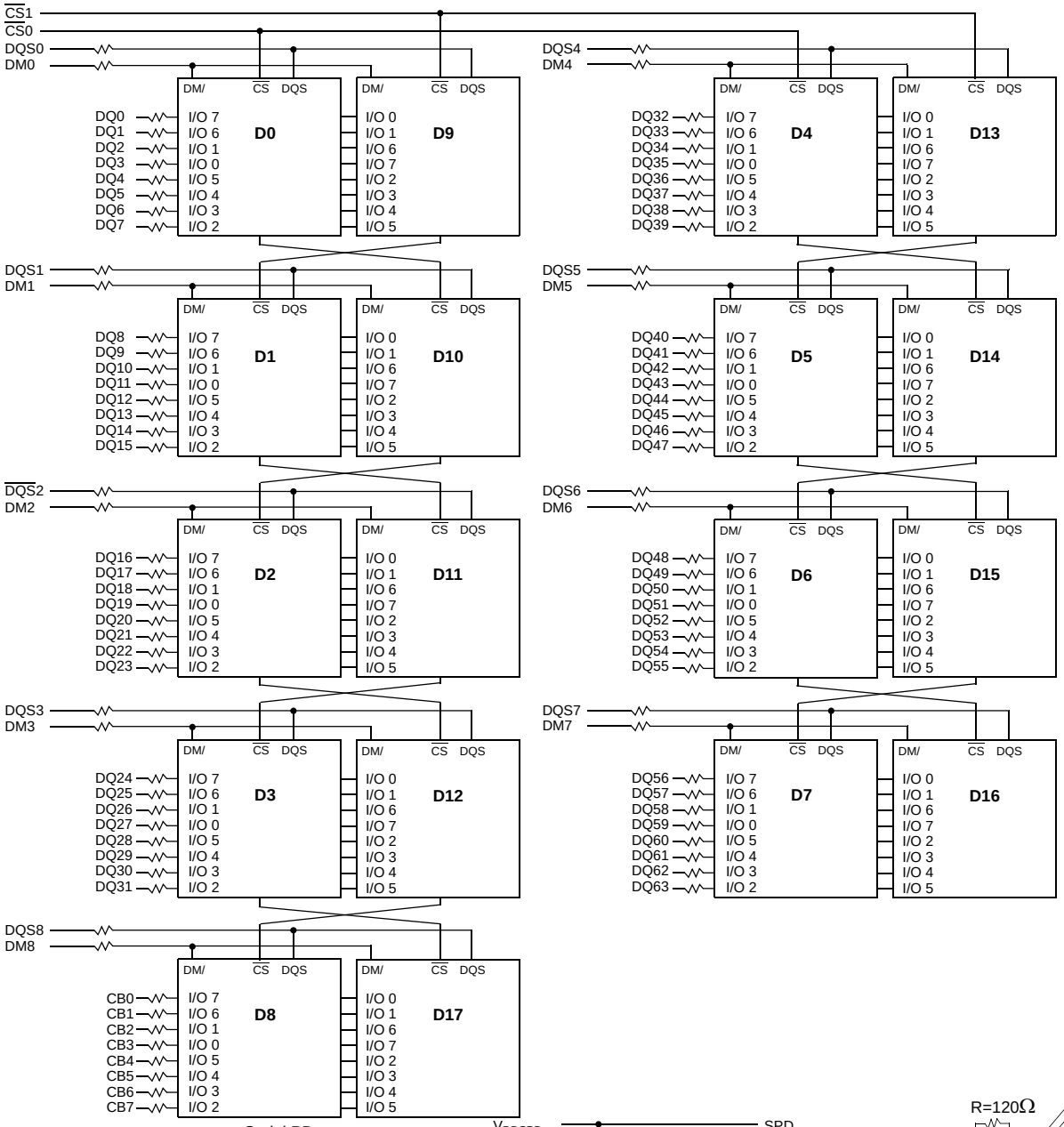
*Clock Net Wiring

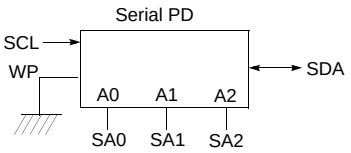
Notes :

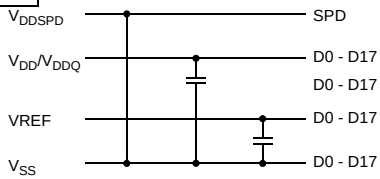
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/$\overline{CS}$ relationships must be maintained as shown.
3. DQ, DQS, $\overline{DM}$/$\overline{DQS}$ resistors: 22 Ohms ± 5%.
4. BAx, Ax, RAS, CAS, WE resistors: 3 Ohms ± 5%

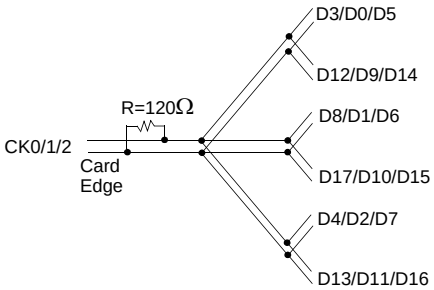
6.5 1GB, 128M x 72 ECC Module (M381L2923BT(U))

(Populated as 2 bank of x8 DDR SDRAM Module)









BA0 - BA1 → BA0-BA1 : DDR SDRAMs D0 - D17

A0 - A12 → A0-A12 : DDR SDRAMs D0 - D17

$\overline{RAS}$ → $\overline{RAS}$: DDR SDRAMs D0 - D17

$\overline{CAS}$ → $\overline{CAS}$: DDR SDRAMs D0 - D17

CKE0/1 → CKE : DDR SDRAMs D0 - D17

$\overline{WE}$ → $\overline{WE}$: DDR SDRAMs D0 - D17

* Clock Wiring	
Clock Input	DDR SDRAMs
*CK0/$\overline{CK0}$	6 DDR SDRAMs
*CK1/$\overline{CK1}$	6 DDR SDRAMs
*CK2/$\overline{CK2}$	6 DDR SDRAMs

*Clock Net Wiring

Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/$\overline{CS}$ relationships must be maintained as shown.
3. DQ, DQS, $\overline{DM}$/$\overline{DQS}$ resistors: 22 Ohms ± 5%.
4. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors:3 Ohms ± 5%

7.0 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	V_{DD},V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.5 * # of component	W
Short circuit current	I_{OS}	50	mA

Note :
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

8.0 DC Operating Conditions

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{DD} of 2.5V for DDR333)	V_{DD}	2.3	2.7	V	
Supply voltage(for device with a nominal V_{DD} of 2.6V for DDR400)	V_{DD}	2.5	2.7	V	
I/O Supply voltage(for device with a nominal V_{DD} of 2.5V for DDR333)	V_{DDQ}	2.3	2.7	V	
I/O Supply voltage(for device with a nominal V_{DD} of 2.6V for DDR400)	V_{DDQ}	2.5	2.7	V	
I/O Reference voltage	V_{REF}	0.49*VDDQ	0.51*VDDQ	V	1
I/O Termination voltage(system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.15	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	V_{IN}(DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	V_{ID}(DC)	0.36	V_{DDQ}+0.6	V	3
V-I Matching: Pullup to Pulldown Current Ratio	VI(Ratio)	0.71	1.4	-	4
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} + 0.84V	I_{OH}	-16.8		mA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} - 0.84V	I_{OL}	16.8		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} + 0.45V	I_{OH}	-9		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} - 0.45V	I_{OL}	9		mA	

Note :
1. V_{REF} is expected to be equal to 0.5*V_{DDQ} of the transmitting device, and to track variations in the dc level of same. Peak-to peak noise on V_{REF} may not exceed +/-2% of the dc value.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.

9.0 DDR SDRAM IDD spec table

9.1 M368L3324BT(U) [(32M x 16) * 4, 256MB Non ECC Module]

(V_{DD}=2.7V, T = 10°C)

Symbol		CC(DDR400@CL=3)	B3(DDR333@CL=2.5)	Unit	Notes
IDD0		660	500	mA	
IDD1		760	620	mA	
IDD2P		20	20	mA	
IDD2F		120	120	mA	
IDD2Q		100	100	mA	
IDD3P		220	120	mA	
IDD3N		400	200	mA	
IDD4R		920	780	mA	
IDD4W		1,120	860	mA	
IDD5		1,060	1,000	mA	
IDD6	Normal	20	20	mA	
	Low power	12	12	mA	Optional
IDD7A		1,800	1,620	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

9.2 M368L6523BT(U) [(64M x 8) * 8, 512MB Non ECC Module]

(V_{DD}=2.7V, T = 10°C)

Symbol		CC(DDR400@CL=3)	B3(DDR333@CL=2.5)	Unit	Notes
IDD0		1,320	1,000	mA	
IDD1		1,480	1,200	mA	
IDD2P		40	40	mA	
IDD2F		240	240	mA	
IDD2Q		200	200	mA	
IDD3P		440	240	mA	
IDD3N		760	400	mA	
IDD4R		1,600	1,320	mA	
IDD4W		1,920	1,520	mA	
IDD5		2,120	2,000	mA	
IDD6	Normal	40	40	mA	
	Low power	24	24	mA	Optional
IDD7A		3,440	3,200	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

9.3 M381L6523BT(U) [(64M x 8) * 9, 512MB ECC Module]

(V_{DD}=2.7V, T = 10°C)

Symbol		CC(DDR400@CL=3)	B0(DDR333@CL=2.5)	Unit	Notes
IDD0		1,485	1,130	mA	
IDD1		1,665	1,350	mA	
IDD2P		45	45	mA	
IDD2F		270	270	mA	
IDD2Q		225	230	mA	
IDD3P		500	270	mA	
IDD3N		855	450	mA	
IDD4R		1,800	1,490	mA	
IDD4W		2,160	1,710	mA	
IDD5		2,385	2,250	mA	
IDD6	Normal	45	45	mA	
	Low power	27	27	mA	Optional
IDD7A		3,870	3,600	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

9.4 M368L2923BT(U) [(64M x 8) * 16, 1GB Non ECC Module]

(V_{DD}=2.7V, T = 10°C)

Symbol		CC(DDR400@CL=3)	B0(DDR333@CL=2.5)	Unit	Notes
IDD0		2,080	1,400	mA	
IDD1		2,240	1,600	mA	
IDD2P		80	80	mA	
IDD2F		480	480	mA	
IDD2Q		400	400	mA	
IDD3P		880	480	mA	
IDD3N		1,520	800	mA	
IDD4R		2,360	1,720	mA	
IDD4W		2,680	1,920	mA	
IDD5		2,880	2,400	mA	
IDD6	Normal	80	80	mA	
	Low power	48	48	mA	Optional
IDD7A		4,200	3,600	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

9.5 M381L2923BT(U) [(64M x 8) * 18, 1GB ECC Module]

(V_{DD}=2.7V, T = 10°C)

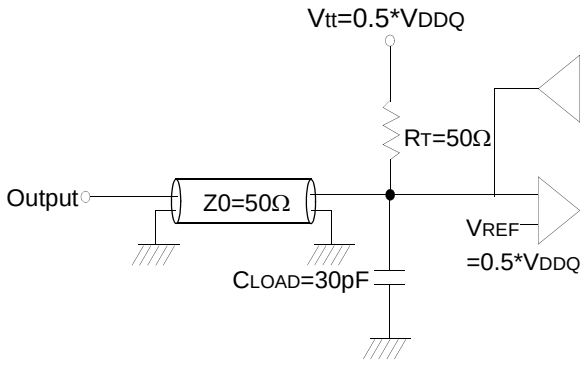
Symbol		CC (DDR400@CL=3)	B3 (DDR333@CL=2.5)	Unit	Notes
IDD0		2,340	1,580	mA	
IDD1		2,520	1,800	mA	
IDD2P		90	90	mA	
IDD2F		540	540	mA	
IDD2Q		450	450	mA	
IDD3P		990	540	mA	
IDD3N		1,710	900	mA	
IDD4R		2,655	1,940	mA	
IDD4W		3,015	2,160	mA	
IDD5		3,240	2,700	mA	
IDD6	Normal	90	90	mA	
	Low power	54	54	mA	Optional
IDD7A		4,725	4,050	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

10.0 AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note :
1. VID is the magnitude of the difference between the input level on CK and the input on $\overline{CK}$.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pim on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specificatims are refation to a Vref envelope that has been bandwidth limited 20MHz.



Output Load Circuit (SSTL_2)

11.0 Input/Output Capacitance

(VDD=2.5V, VDDQ=2.5V, TA= 25°C, f=1MHz)

Parameter	Symbol	M368L3324BT(U)		M368L6523BT(U)		M381L6523BT(U)		Unit
		Min	Max	Min	Max	Min	Max	
Input capacitance(A0 ~ A12, BA0 ~ BA1,$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$)	CIN1	41	45	49	57	51	60	pF
Input capacitance(CKE0)	CIN2	34	38	42	50	44	53	pF
Input capacitance($\overline{CS0}$)	CIN3	34	38	42	50	44	53	pF
Input capacitance(CLK0, CLK1,CLK2)	CIN4	25	30	25	30	25	30	pF
Input capacitance(DM0~DM7, DM8(for ECC))	CIN5	6	7	6	7	6	7	pF
Data & DQS input/output capacitance(DQ0~DQ63)	Cout1	6	7	6	7	6	7	pF
Data input/output capacitance (CB0~CB7)	Cout2	-	-	-	-	6	7	pF

Parameter	Symbol	M368L2923BT(U)		M381L2923BT(U)		Unit
		Min	Max	Min	Max	
Input capacitance(A0 ~ A12, BA0 ~ BA1,$\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$)	CIN1	65	81	69	87	pF
Input capacitance(CKE0,CKE1)	CIN2	42	50	44	53	pF
Input capacitance($\overline{CS0}$, $\overline{CS1}$)	CIN3	42	50	44	53	pF
Input capacitance(CLK0, CLK1,CLK2)	CIN4	28	34	28	34	pF
Input capacitance(DM0~DM7, DM8(for ECC))	CIN5	10	12	10	12	pF
Data & DQS input/output capacitance(DQ0~DQ63)	Cout1	10	12	10	12	pF
Data input/output capacitance (CB0~CB7)	Cout2	-	-	10	12	pF

12.0 AC Timming Parameters & Specifications

Parameter		Symbol	CC (DDR400@CL=3.0)		B3 (DDR333@CL=2.5)		Unit	Note
			Min	Max	Min	Max		
Row cycle time		tRC	55		60		ns	
Refresh row cycle time		tRFC	70		72		ns	
Row active time		tRAS	40	70K	42	70K	ns	
RAS to CAS delay		tRCD	15		18		ns	
Row precharge time		tRP	15		18		ns	
Row active to Row active delay		tRRD	10		12		ns	
Write recovery time		tWR	15		15		ns	
Last data in to Read command		tWTR	2		1		tCK	
Clock cycle time	CL=2.0	tCK	-	-	7.5	12	ns	
	CL=2.5		6	12	6	12	ns	
	CL=3.0		5	10	-	-		
Clock high level width		tCH	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/$\overline{CK}$		tDQSCK	-0.55	+0.55	-0.6	+0.6	ns	
Output data access time from CK/$\overline{CK}$		tAC	-0.65	+0.65	-0.7	+0.7	ns	
Data strobe edge to ouput data edge		tDQSQ	-	0.4	-	0.45	ns	22
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.72	1.28	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		ns	13
DQS-in hold time		tWPRE	0.25		0.25		tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		0.2		tCK	
DQS-in high level width		tDQSH	0.35		0.35		tCK	
DQS-in low level width		tDQSL	0.35		0.35		tCK	
Address and Control Input setup time(fast)		tIS	0.6		0.75		ns	15, 17~19
Address and Control Input hold time(fast)		tIH	0.6		0.75		ns	15, 17~19
Address and Control Input setup time(slow)		tIS	0.7		0.8		ns	16~19
Address and Control Input hold time(slow)		tIH	0.7		0.8		ns	16~19
Data-out high impedence time from CK/$\overline{CK}$		tHZ	-0.65	+0.65	-0.7	+0.7	ns	11
Data-out low impedence time from CK/$\overline{CK}$		tLZ	-0.65	+0.65	-0.7	+0.7	ns	11
Mode register set cycle time		tMRD	10		12		ns	
DQ & DM setup time to DQS		tDS	0.4		0.45		ns	j, k
DQ & DM hold time to DQS		tDH	0.4		0.45		ns	j, k
Control & Address input pulse width		tIPW	2.2		2.2		ns	18
DQ & DM input pulse width		tDIPW	1.75		1.75		ns	18
Exit self refresh to non-Read command		tXSNR	75		75		ns	
Exit self refresh to read command		tXSRD	200		200		tCK	
Refresh interval time		tREFI		7.8		7.8	us	14
Output DQS valid window		tQH	tHP -tQHS	-	tHP -tQHS	-	ns	21
Clock half period		tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	20, 21
Data hold skew factor		tQHS		0.5		0.55	ns	21
DQS write postamble time		tWPST	0.4	0.6	0.4	0.6	tCK	12
Active to Read with Auto precharge command		tRAP	15		18			
Autoprecharge write recovery + Precharge time		tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	23

13.0 System Characteristics for DDR SDRAM

The following specification parameters are required in systems using DDR333 devices to ensure proper system performance. these characteristics are for system simulation purposes and are guaranteed by design.

Table 1 : Input Slew Rate for DQ, DQS, and DM

AC CHARACTERISTICS		DDR400		DDR333			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	Units	Notes
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	TBD	TBD	TBD	TBD	V/ns	a, m

Table 2 : Input Setup & Hold Time Derating for Slew Rate

Input Slew Rate	ΔtIS	ΔtIH	Units	Notes
0.5 V/ns	0	0	ps	i
0.4 V/ns	+50	0	ps	i
0.3 V/ns	+100	0	ps	i

Table 3 : Input/Output Setup & Hold Time Derating for Slew Rate

Input Slew Rate	ΔtDS	ΔtDH	Units	Notes
0.5 V/ns	0	0	ps	k
0.4 V/ns	+75	+75	ps	k
0.3 V/ns	+150	+150	ps	k

Table 4 : Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate

Delta Slew Rate	ΔtDS	ΔtDH	Units	Notes
+/- 0.0 V/ns	0	0	ps	j
+/- 0.25 V/ns	+50	+50	ps	j
+/- 0.5 V/ns	+100	+100	ps	j

Table 5 : Output Slew Rate Characteristice (X4, X8 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	1.0	4.5	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	1.0	4.5	b,c,d,f,g,h

Table 6 : Output Slew Rate Characteristice (X16 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	0.7	5.0	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	0.7	5.0	b,c,d,f,g,h

Table 7 : Output Slew Rate Matching Ratio Characteristics

AC CHARACTERISTICS	DDR400		DDR333		
PARAMETER	MIN	MAX	MIN	MAX	Notes
Output Slew Rate Matching Ratio (Pullup to Pulldown)	TBD	TBD	TBD	TBD	e,m

14.0 Component Notes

1. All voltages referenced to Vss.
2. Tests for ac timing, IDD, and electrical, ac and dc characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Figure 1 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

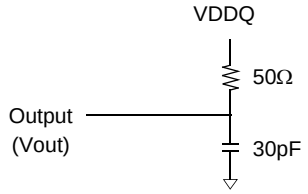


Figure 1 : Timing Reference Load

4. AC timing and IDD tests may use a VIL to VIH swing of up to 1.5 V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/CK), and parameter specifications are guaranteed for the specified ac input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between VIL(ac) and VIH(ac).
5. The ac and dc input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the ac input level and will remain in that state as long as the signal does not ring back above (below) the dc input LOW (HIGH) level.
6. Inputs are not recognized as valid until VREF stabilizes. Exception: during the period before VREF stabilizes, CKE ≤ 0.2VDDQ is recognized as LOW.
7. Enables on.chip refresh and address counters.
8. IDD specifications are tested after the device is properly initialized.
9. The CK/$\overline{CK}$ input reference level (for timing referenced to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK/$\overline{CK}$, is VREF.
10. The output timing reference voltage level is VTT.
11. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
12. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but sys tem performance (bus turnaround) will degrade accordingly.
13. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. when no writes were previ ously in progress on the bus, DQS will be tran sitioning from High- Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
14. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
15. For command/address input slew rate ≥ 1.0 V/ns
16. For command/address input slew rate ≥ 0.5 V/ns and < 1.0 V/ns
17. For CK & $\overline{CK}$ slew rate ≥ 1.0 V/ns
18. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
19. Slew Rate is measured between VOH(ac) and VOL(ac).
20. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.
21. tQH = tHP - tQHS, where:
    tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one tansition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p channel to n-channel variation of the output drivers.
22. tDQSQ - Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
23. tDAL = (tWR/tCK) + (tRP/tCK)
    For each of the terms above, if not already an integer, round to the next highest integer. Example: For DDR266B at CL=2.5 and tCK=7.5ns tDAL = (15 ns / 7.5 ns) + (20 ns/ 7.5ns) = (2) + (3) tDAL = 5 clocks

15.0 System Notes:

a. Pullup slew rate is characteristized under the test conditions as shown in Figure 2.

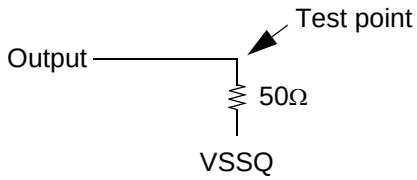


Figure 2 : Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 3.

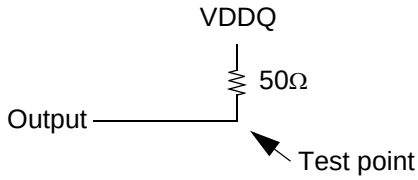


Figure 3 : Pulldown slew rate test load

c. Pullup slew rate is measured between (VDDQ/2 - 320 mV +/- 250 mV)
Pulldown slew rate is measured between (VDDQ/2 + 320 mV +/- 250 mV)
Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.
Example : For typical slew rate, DQ0 is switching
For minmum slew rate, all DQ bits are switching from either high to low, or low to high.
The remaining DQ bits remain the same as for previous state.

d. Evaluation conditions
Typical : 25 °C (T Ambient), VDDQ = 2.5V(for DDR266/333) and 2.6V(for DDR400), typical process
Minimum : 70 °C (T Ambient), VDDQ = 2.3V(for DDR266/333) and 2.5V(for DDR400), slow - slow process
Maximum : 0 °C (T Ambient), VDDQ = 2.7V(for DDR266/333) and 2.7V(for DDR400), fast - fast process

e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOPII package divices only.

h. Only intended for operation up to 266 Mbps per pin.

i. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5V/ns as shown in Table 2. The Input slew rate is based on the lesser of the slew rates detemined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

j. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 3 & 4. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions. The delta rise/fall rate is calculated as: {1/(Slew Rate1)} - {1/(Slew Rate2)}

For example : If Slew Rate 1 is 0.5 V/ns and slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is - 0.5ns/V . Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps.

k. Table 3 is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser on the lesser of the AC - AC slew rate and the DC- DC slew rate. The inut slew rate is based on the lesser of the slew rates deter mined by either VIH(ac) to VIL(ac) or VIH(DC) to VIL(DC), and similarly for rising transitions.

m. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transi tions through the DC region must be monotonic.

16.0 Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A0 ~ A9 A11, A12	Note
Register	Extended MRS		H	X	L	L	L	L	OP CODE			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address (A0~A9, A11,A12)		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

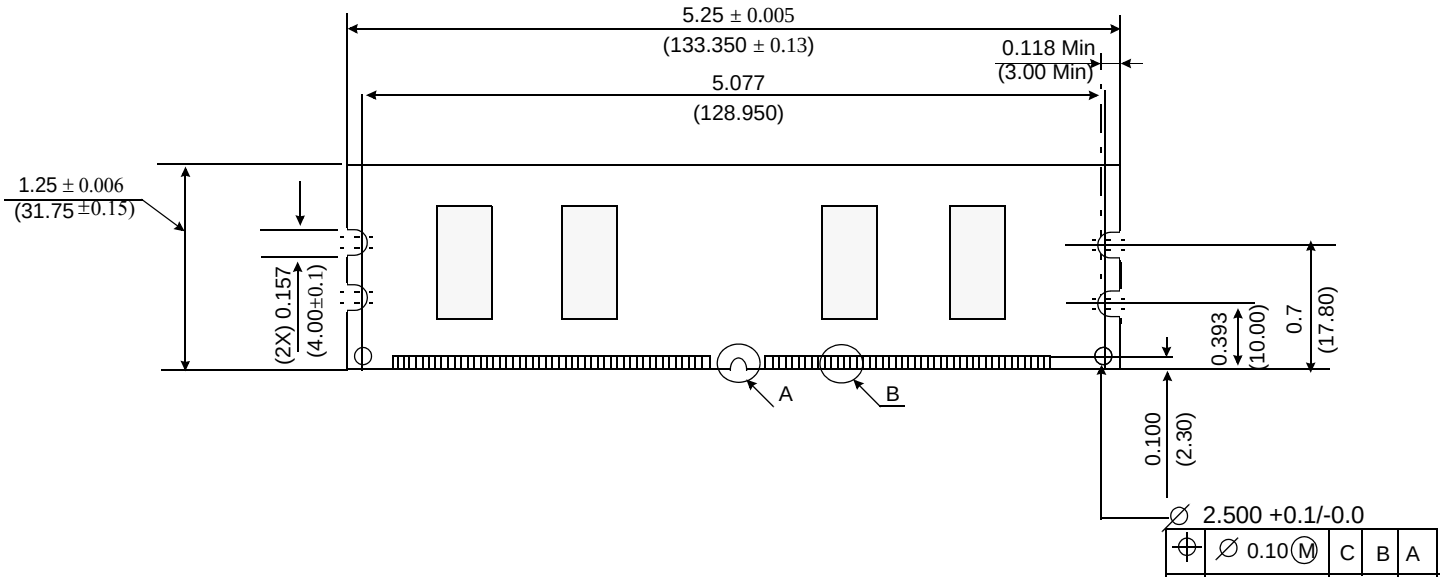
Note :

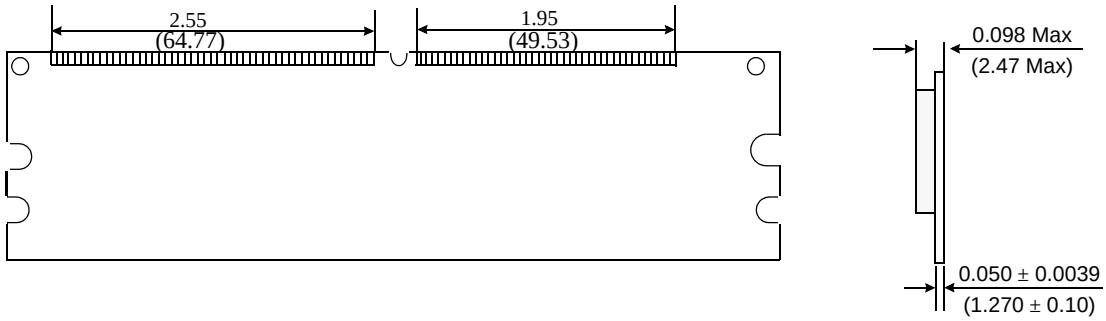
1. OP Code : Operand Code. A_0 ~ A_{12} & BA_0 ~ BA_1 : Program keys. (@EMRS/MRS)
2. EMRS/ MRS can be issued only at all banks precharge state. A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

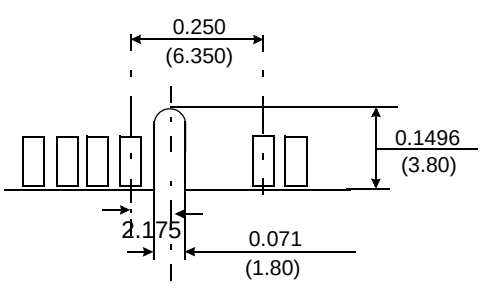
17.0 Physical Dimensions

17.1 32M x 64 (M368L3324BT(U))

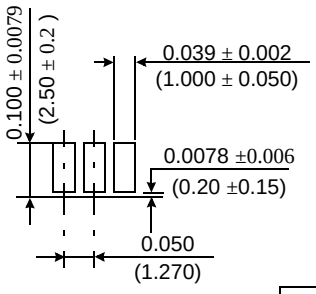
Units : Inches (Millimeters)



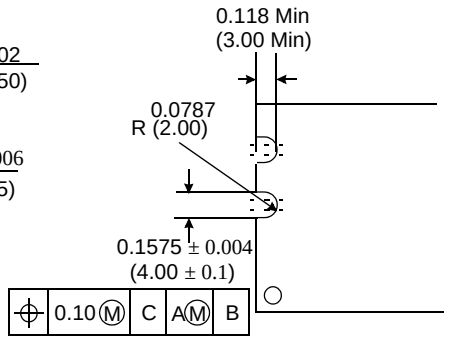




Detail A



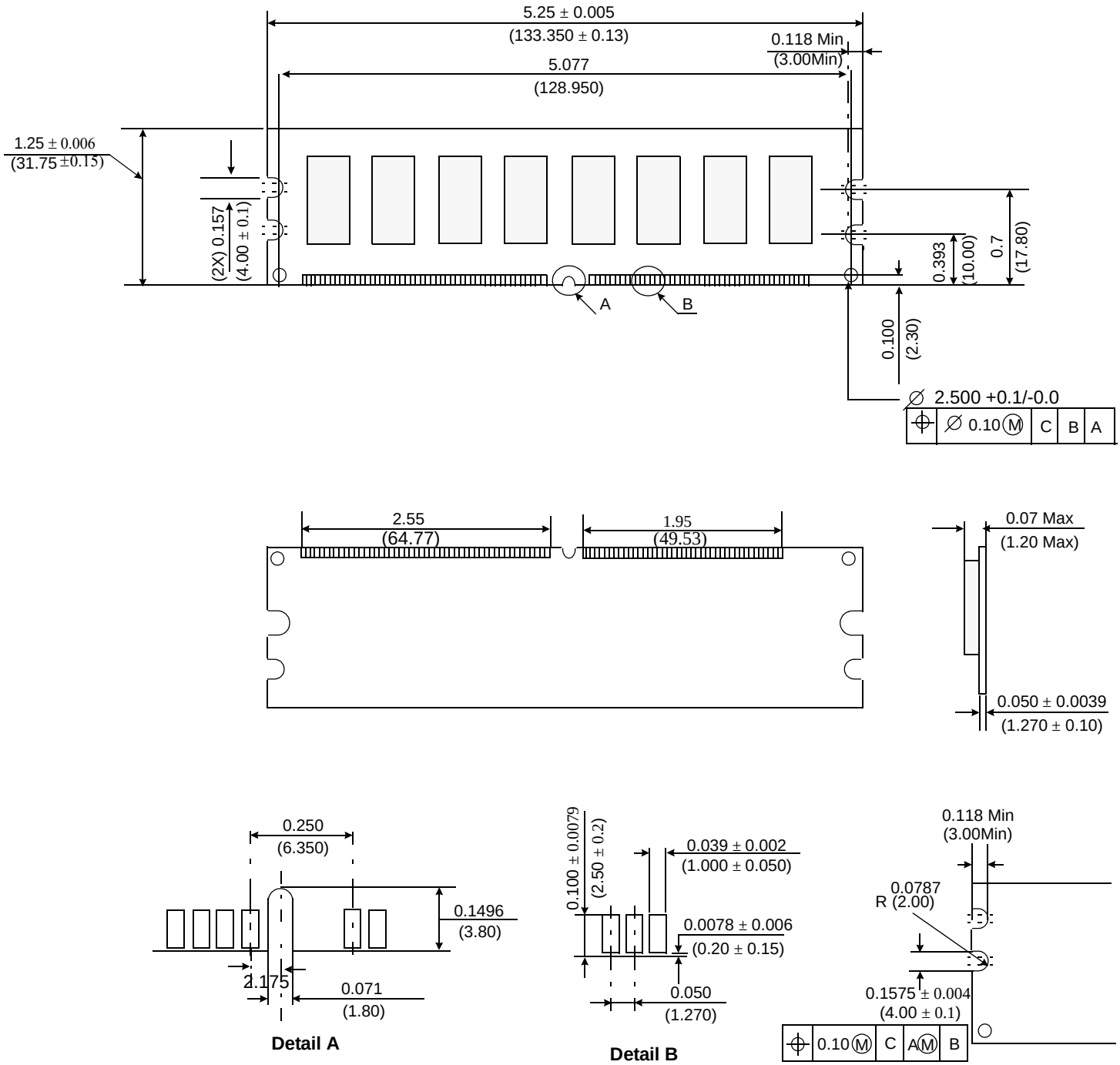
Detail B



Tolerances : ± 0.005(.13) unless otherwise specified.
The used device is 32Mx16 DDR SDRAM, TSOPII.
DDR SDRAM Part No : K4H511638B

17.2 64Mx64 (M368L6523BT(U))

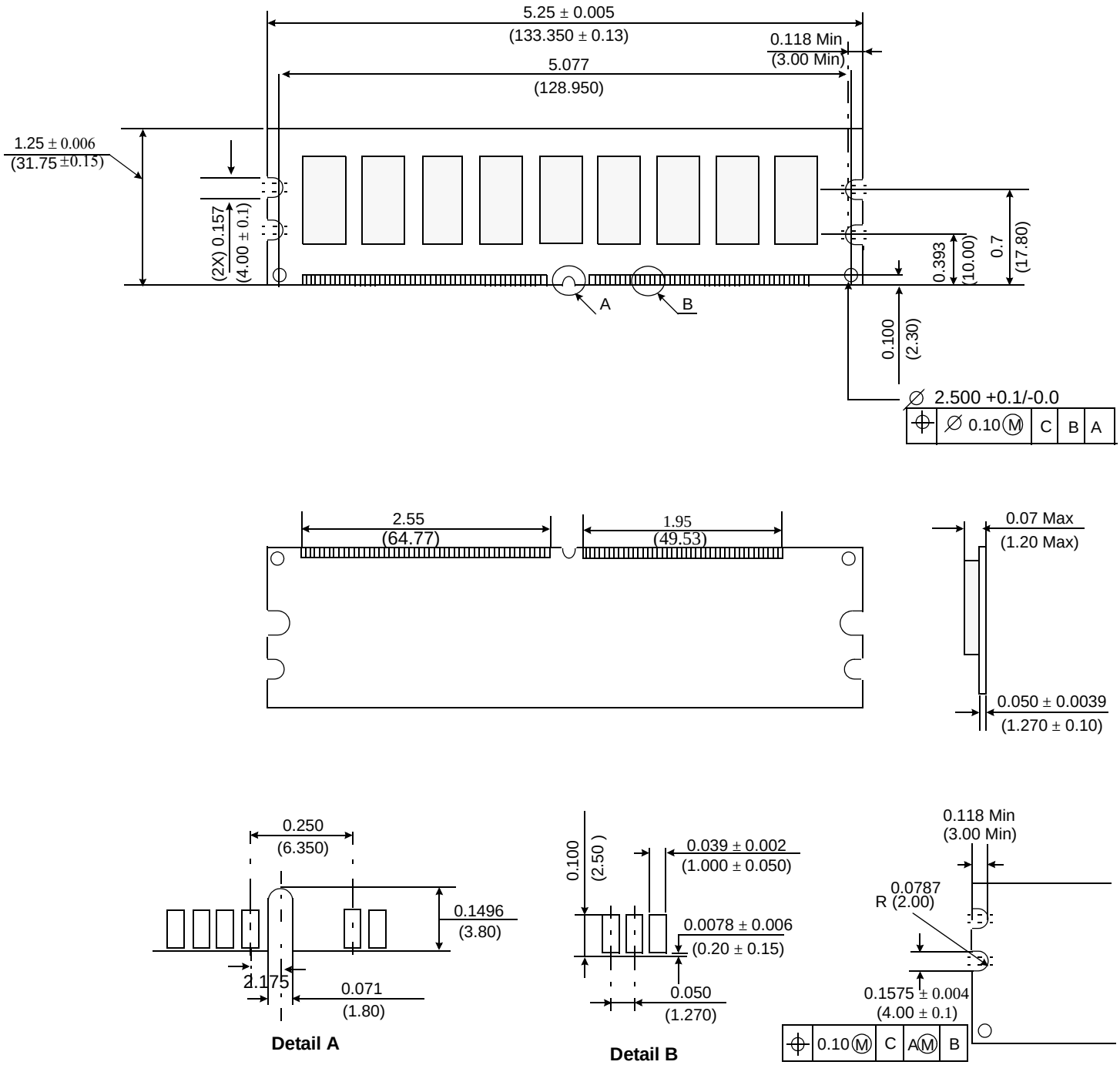
Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified.
The used device is 64Mx8 DDR SDRAM, TSOPII.
DDR SDRAM Part No : K4H510838B

17.3 64Mx72 (M381L6523BT(U))

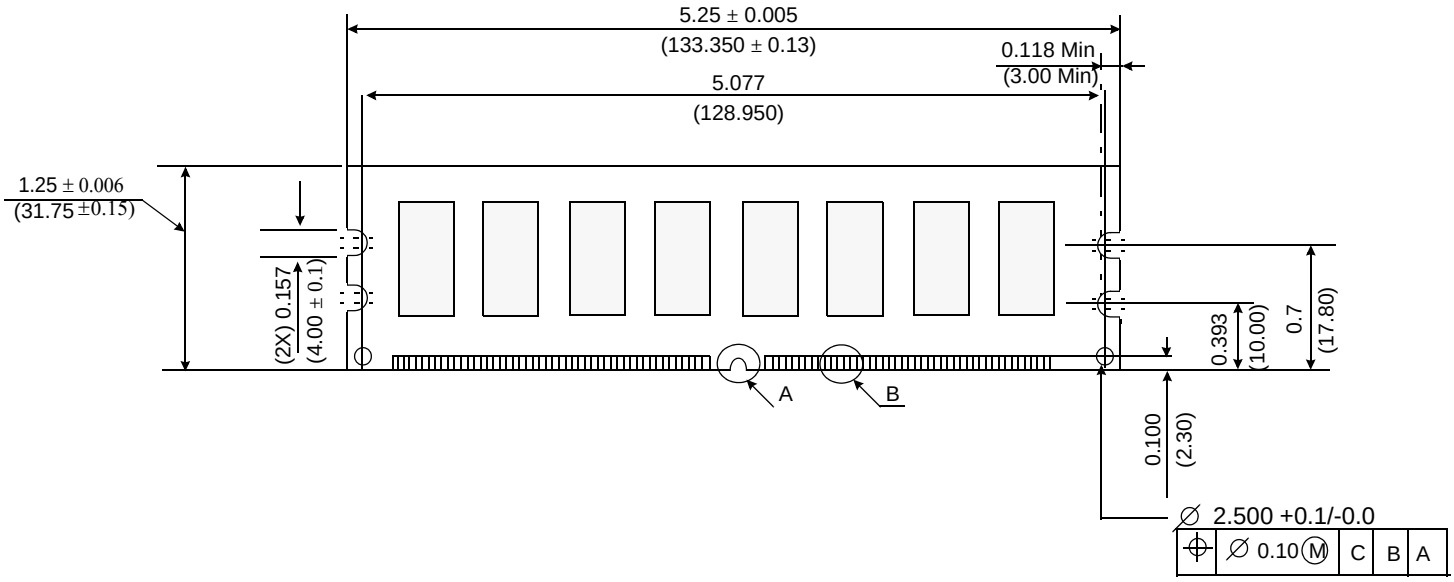
Units : Inches (Millimeters)

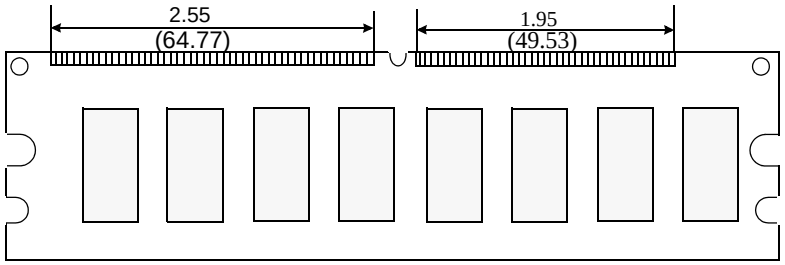


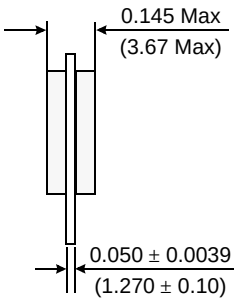
Tolerances : ± 0.005(.13) unless otherwise specified.
The used device is 64Mx8 DDR SDRAM, TSOPII.
DDR SDRAM Part No : K4H510838B

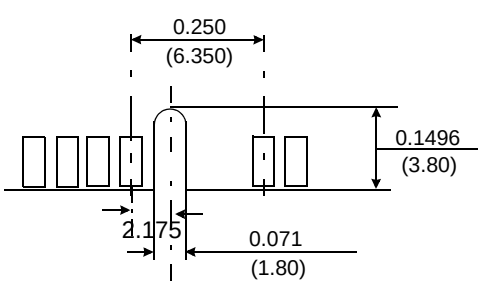
17.4 128Mx64 (M368L2923BT(U))

Units : Inches (Millimeters)

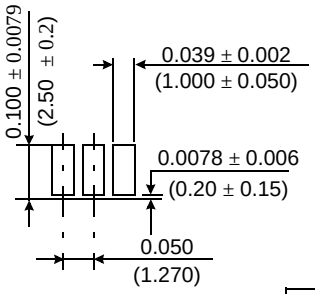




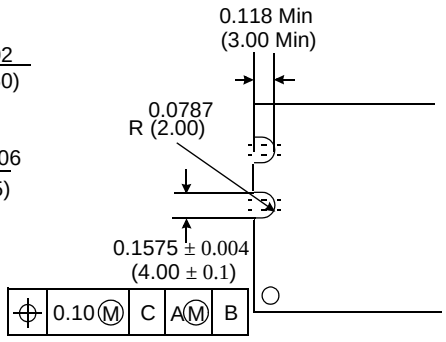




Detail A



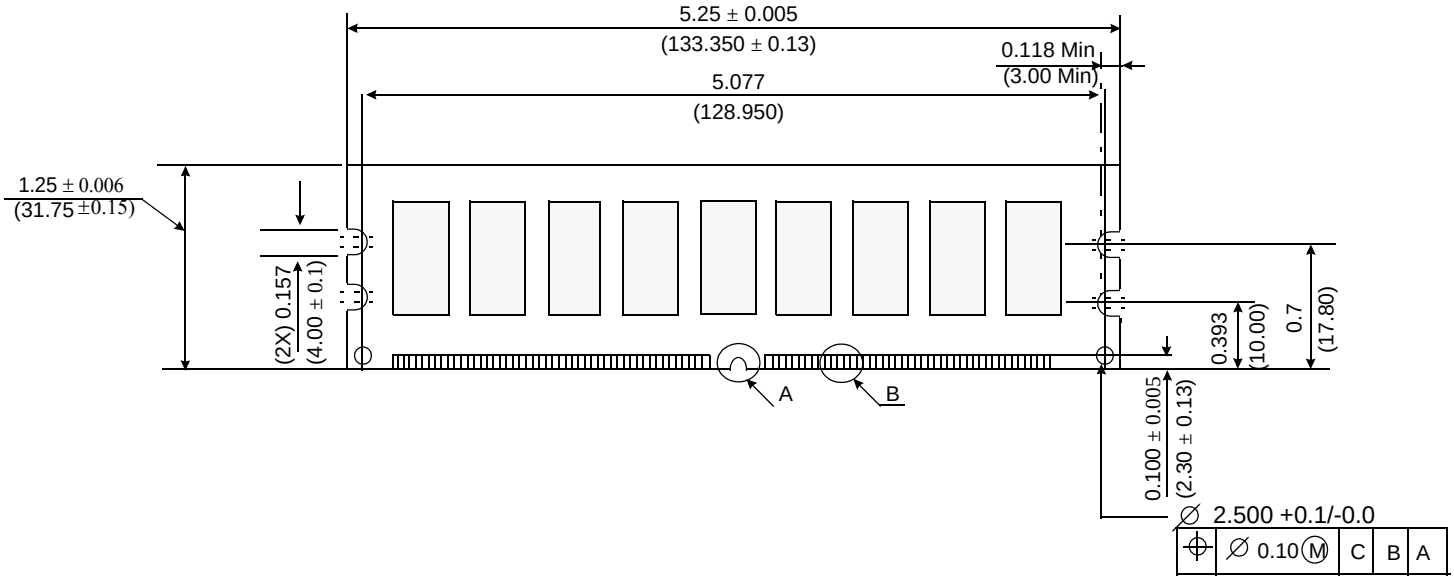
Detail B

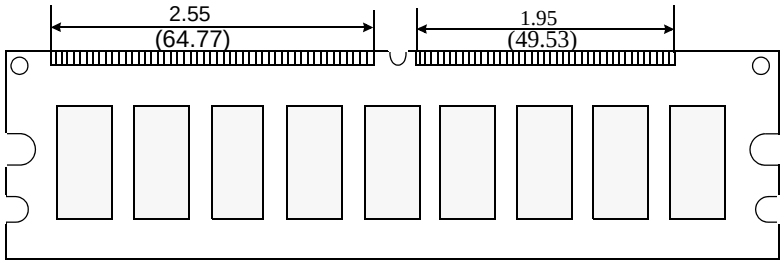


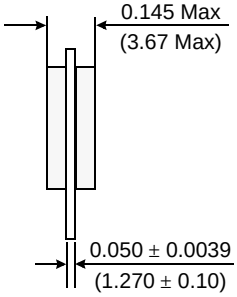
Tolerances : ± 0.005(.13) unless otherwise specified.
The used device is 64Mx8 DDR SDRAM, TSOPII.
DDR SDRAM Part No : K4H510838B

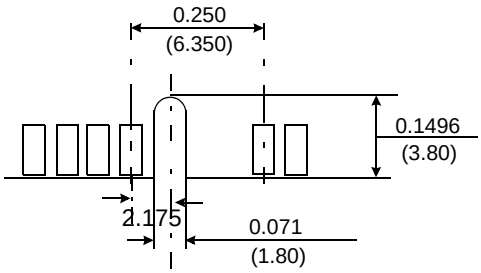
17.5 128Mx72 (M381L2923BT(U))

Units : Inches (Millimeters)

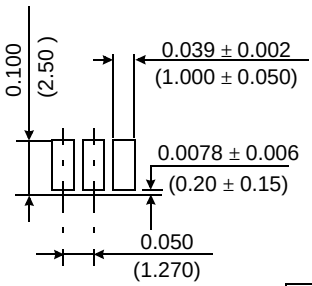




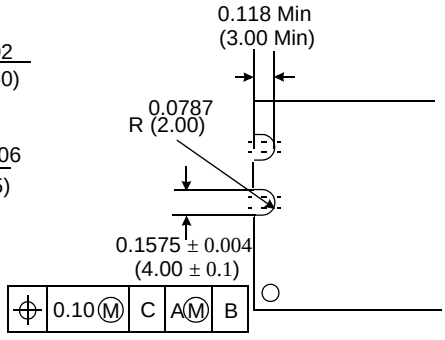




Detail A



Detail B



Tolerances : ± 0.005(.13) unless otherwise specified.
The used device is 64Mx8 DDR SDRAM, TSOPII.
DDR SDRAM Part No : K4H510838B