

# 1

## PRODUCT OVERVIEW

### SAM88RCRI PRODUCT FAMILY

Samsung's SAM88RCRI family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes.

A address/data bus architecture and a large number of bit-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counters with selectable operating modes are included to support real-time operations.

### S3C9442/C9444/C9452/C9454 MICROCONTROLLER

The S3C9442/C9444/C9452/C9454 single-chip 8-bit microcontroller is designed for useful A/D converter, SIO application field. The S3C9442/C9444/C9452/C9454 uses powerful SAM88RCRI CPU and S3C9442/C9444/C9452/C9454 architecture. The internal register file is logically expanded to increase the on-chip register space.

The S3C9442/C9444/C9452/C9454 has 2K/4K bytes of on-chip program ROM and 208 bytes of RAM. The S3C9442/C9444/C9452/C9454 is a versatile general-purpose microcontroller that is ideal for use in a wide range of electronics applications requiring simple timer/counter, PWM. In addition, the S3C9442/C9444/C9452/C9454's advanced CMOS technology provides for low power consumption and wide operating voltage range.

Using the SAM88RCRI design approach, the following peripherals were integrated with the SAM88RCRI core:

- Three configurable I/O ports (18 pins)
- Four interrupt sources with one vector and one interrupt level
- One 8-bit timer/counter with time interval mode
- Analog to digital converter with nine input channels and 10-bit resolution
- One 8-bit PWM output

The S3C9442/C9444/C9452/C9454 microcontroller is ideal for use in a wide range of electronic applications requiring simple timer/counter, PWM, ADC. S3C9452/C9454 is available in a 20/16-pin DIP and a 20-pin SOP package. S3C9452/C9454 is available in a 8-pin and a 8-pin SOP package.

### MTP

The S3F9444/F9454 is an MTP (Multi Time Programmable) version of the S3C9442/C9444/C9452/C9454 microcontroller. The S3F9444/F9454 has on-chip 4-Kbyte multi-time programmable flash ROM instead of masked ROM. The S3F9444/F9454 is fully compatible with the S3C9442/C9444/C9452/C9454, in function, in D.C. electrical characteristics and in pin configuration.

## FEATURES

### CPU

- SAM88RCRI CPU core
- The SAM88RCRI core is low-end version of the current SAM87 core.

### Memory

- 2/4-Kbyte internal program memory
- 208-byte general purpose register area

### Instruction Set

- 41 instructions
- The SAM88RCRI core provides all the SAM87 core instruction except the word-oriented instruction, multiplication, division, and some one-byte instruction.

### Instruction Execution Time

- 400 ns at 10 MHz  $f_{OSC}$  (minimum)

### Interrupts

- 4 interrupt sources with one vector
- One interrupt level

### General I/O

- Three I/O ports (Max 18 pins)
- Bit programmable ports

### 8-bit High-speed PWM

- 8-bit PWM 1-ch (Max: 156 kHz)
- 6-bit base + 2-bit extension

### Built-in reset Circuit

- Low voltage detector for safe reset

### Timer/Counters

- One 8-bit basic timer for watchdog function
- One 8-bit timer/counter with time interval modes

### A/D Converter

- Nine analog input pins
- 10-bit conversion resolution

### Oscillation Frequency

- 1 MHz to 10 MHz external crystal oscillator
- Maximum 10 MHz CPU clock
- Internal RC: 3.2 MHz (typ.), 0.5 MHz (typ.) in  $V_{DD} = 5\text{ V}$

### Operating Temperature Range

- $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

### Operating Voltage Range

- 2.0 V (LVR Level) to 5.5 V

### Smart Option

### Package Types

- S3C9452/C9454:
  - 20-DIP-300A
  - 20-SOP-375
  - 16-DIP-300A
- S3C9442/C9444
  - 8-DIP-300
  - 8-SOP-225

## BLOCK DIAGRAM

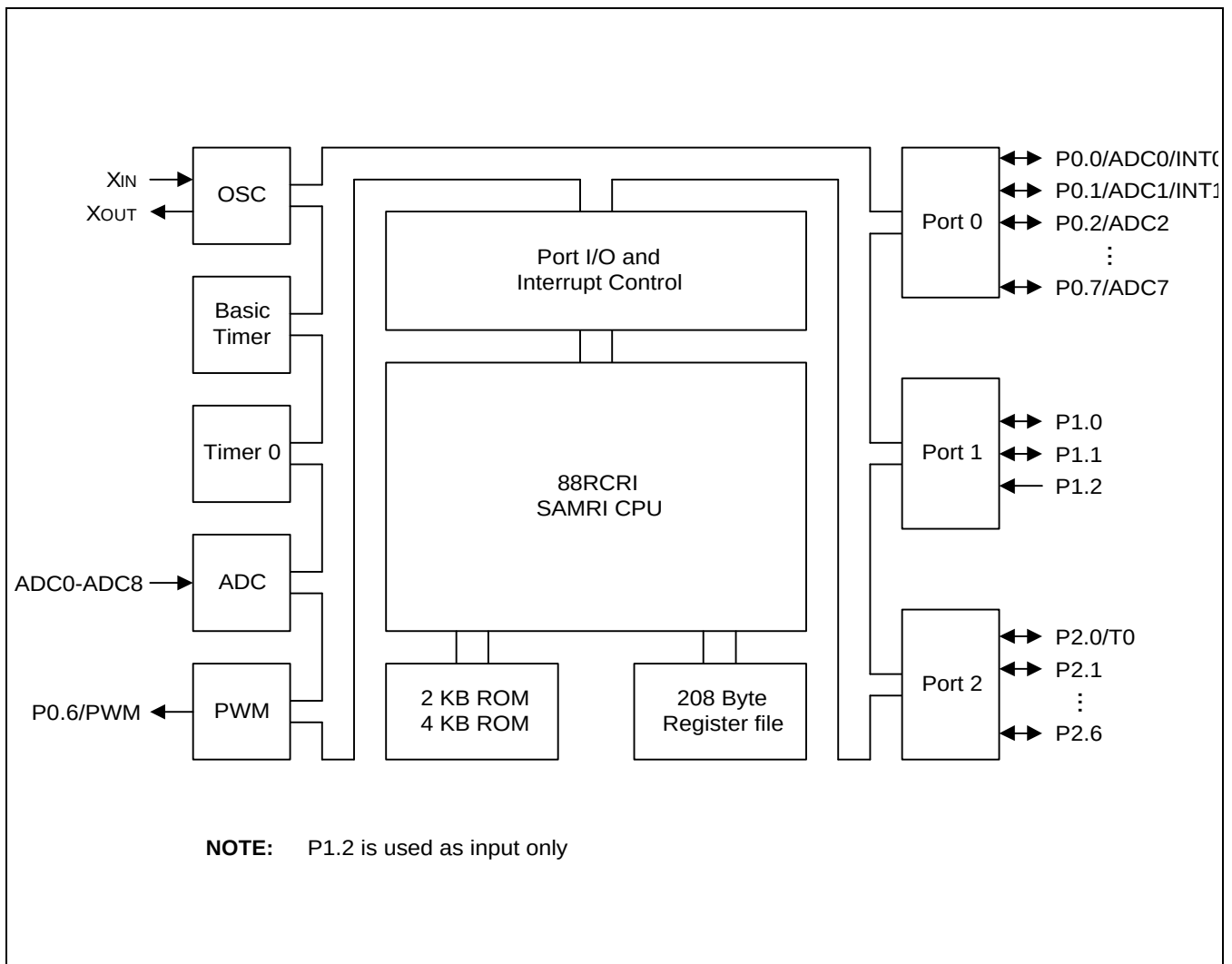


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

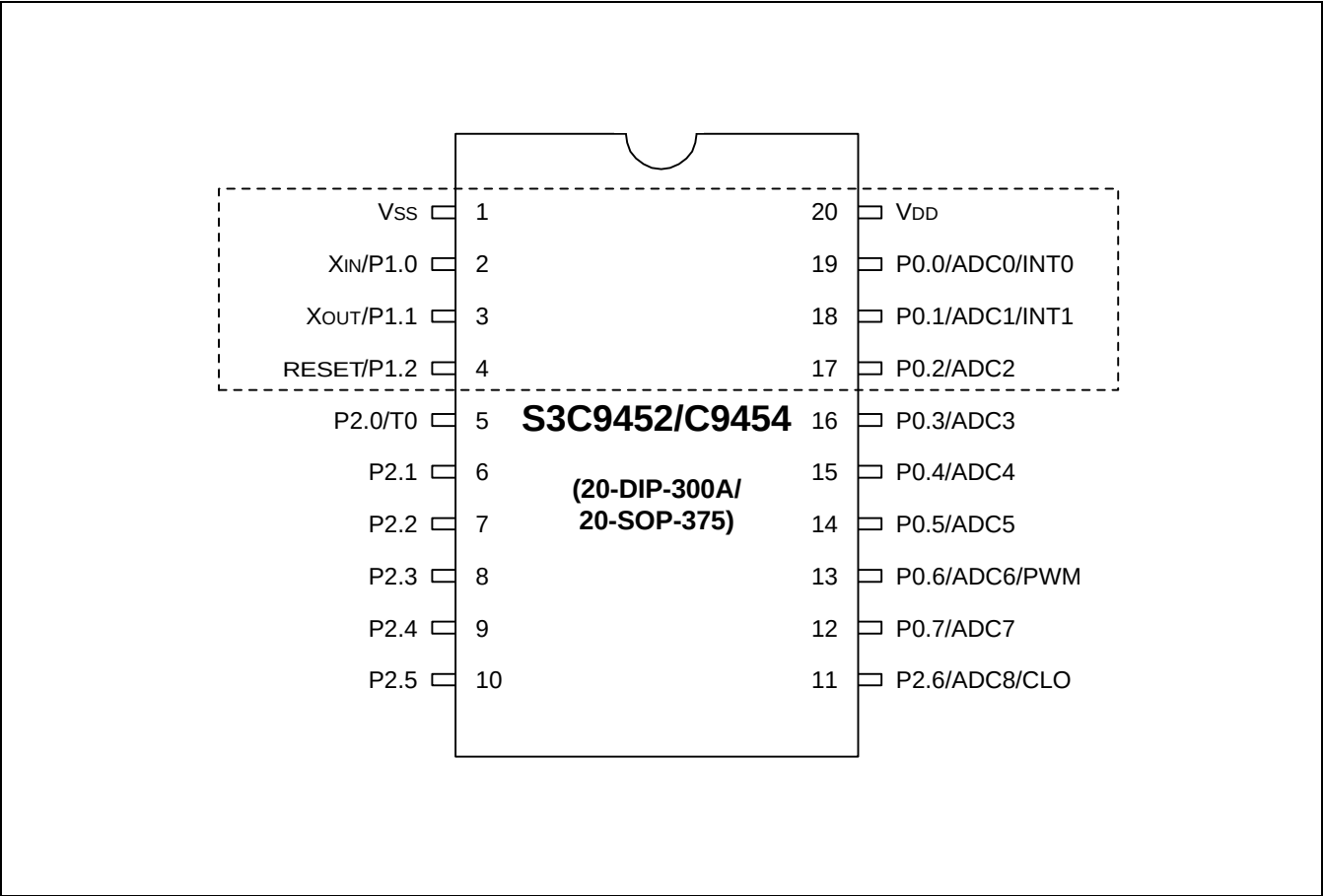


Figure 1-2. Pin Assignment Diagram (20-Pin DIP/SOP Package)

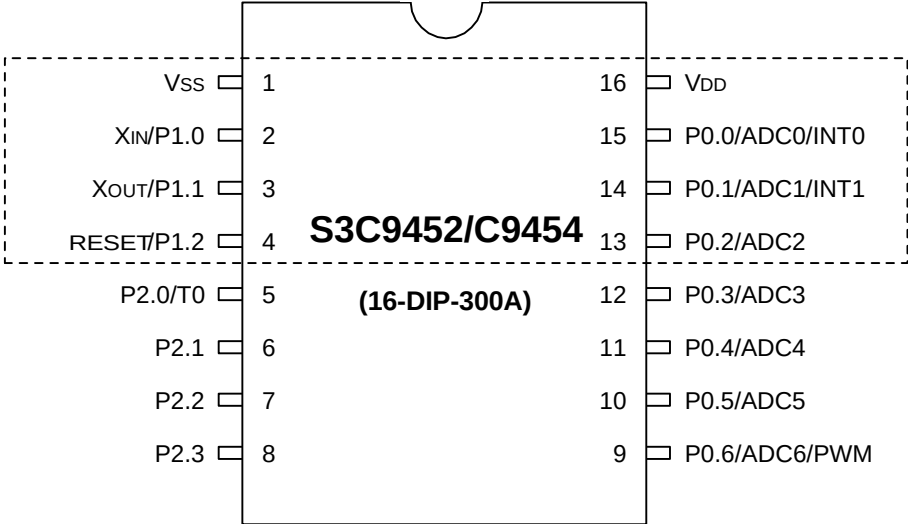


Figure 1-3. Pin Assignment Diagram (16-Pin DIP Package)

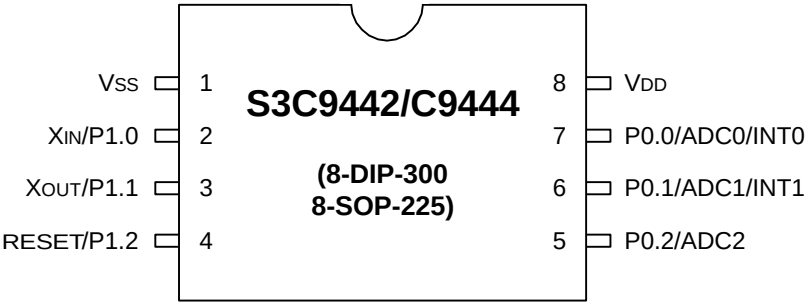


Figure 1-4. Pin Assignment Diagram (8-Pin DIP/SOP Package)

## PIN DESCRIPTIONS

Table 1-1. S3C9452/C9454 Pin Descriptions

| Pin Name             | In/Out | Pin Description                                                                                                                                                                                                    | Pin Type | Share Pins                    |
|----------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-------------------------------|
| P0.0–P0.7            | I/O    | Bit-programmable I/O port for Schmitt trigger input or push-pull output. Pull-up resistors are assignable by software. Port0 pins can also be used as A/D converter input, PWM output or external interrupt input. | E-1      | ADC0–ADC7<br>INT0/INT1<br>PWM |
| P1.0–P1.1            | I/O    | Bit-programmable I/O port for Schmitt trigger input or push-pull, open-drain output. Pull-up resistors or pull-down resistors are assignable by software.                                                          | E-2      | $X_{IN}$ , $X_{OUT}$          |
| P1.2                 | I      | Schmitt trigger input port                                                                                                                                                                                         | B        | RESET                         |
| P2.0–P2.6            | I/O    | Bit-programmable I/O port for Schmitt trigger input or push-pull, open-drain output. Pull-up resistors are assignable by software.                                                                                 | E<br>E-1 | –<br>ADC8/CLO<br>T0           |
| $X_{IN}$ , $X_{OUT}$ | –      | Crystal/Ceramic, or RC oscillator signal for system clock.                                                                                                                                                         |          | P1.0–P1.1                     |
| RESET                | I      | Internal LVR or External RESET                                                                                                                                                                                     | B        | P1.2                          |
| $V_{DD}$ , $V_{SS}$  | –      | Voltage input pin and ground                                                                                                                                                                                       |          | –                             |
| CLO                  | O      | System clock output port                                                                                                                                                                                           | E-1      | P2.6                          |
| INT0–INT1            | I      | External interrupt input port                                                                                                                                                                                      | E-1      | P0.0, P0.1                    |
| PWM                  | O      | 8-Bit high speed PWM output                                                                                                                                                                                        | E-1      | P0.6                          |
| T0                   | O      | Timer0 match output                                                                                                                                                                                                | E-1      | P2.0                          |
| ADC0–ADC8            | I      | A/D converter input                                                                                                                                                                                                | E-1<br>E | P0.0–P0.7<br>P2.6             |

## PIN CIRCUITS

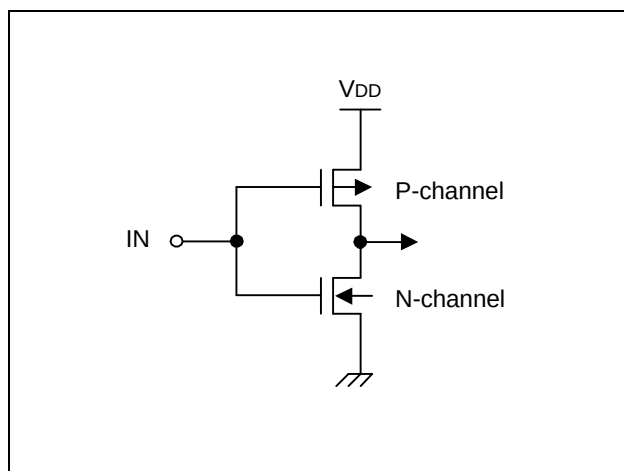


Figure 1-5. Pin Circuit Type A

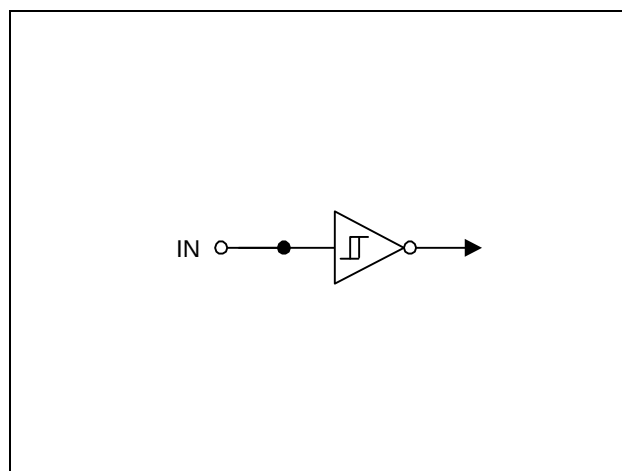


Figure 1-6. Pin Circuit Type B

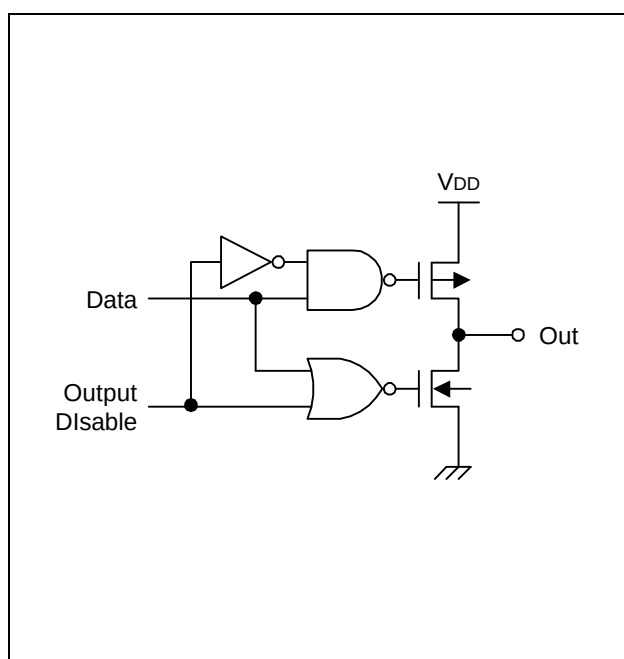


Figure 1-7. Pin Circuit Type C

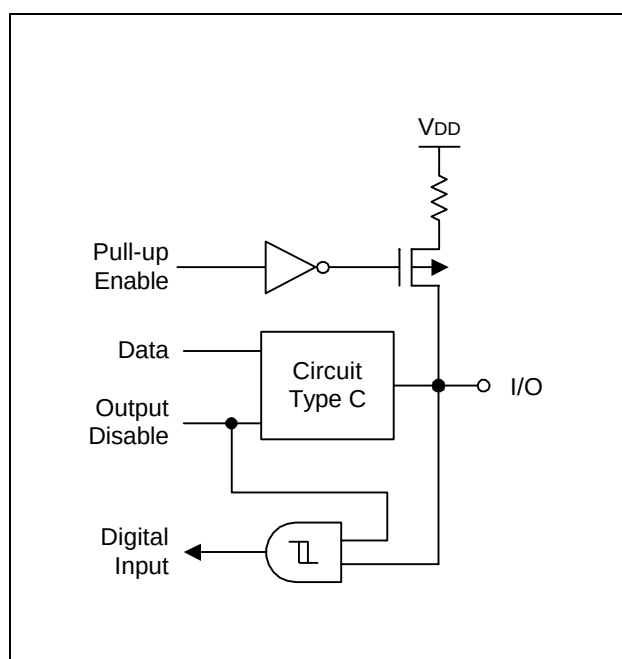


Figure 1-8. Pin Circuit Type D

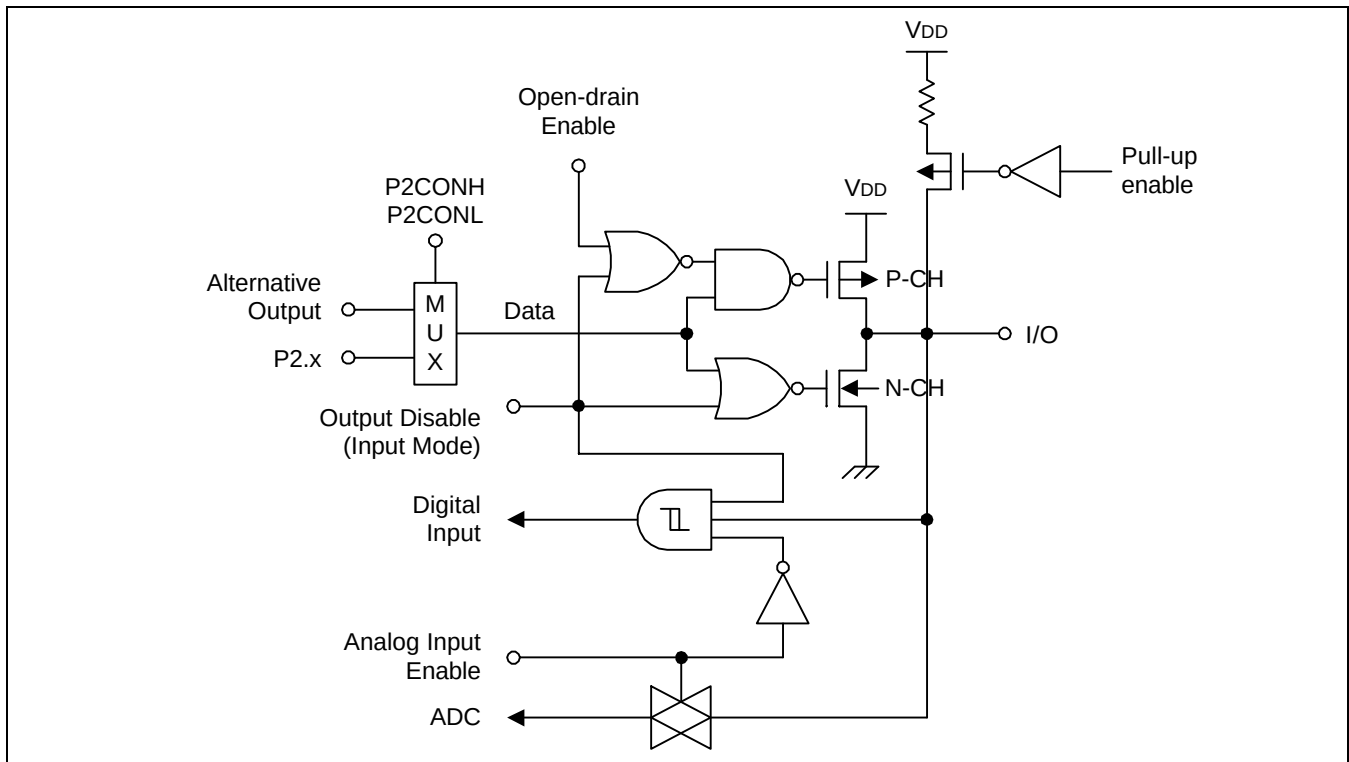


Figure 1-9. Pin Circuit Type E

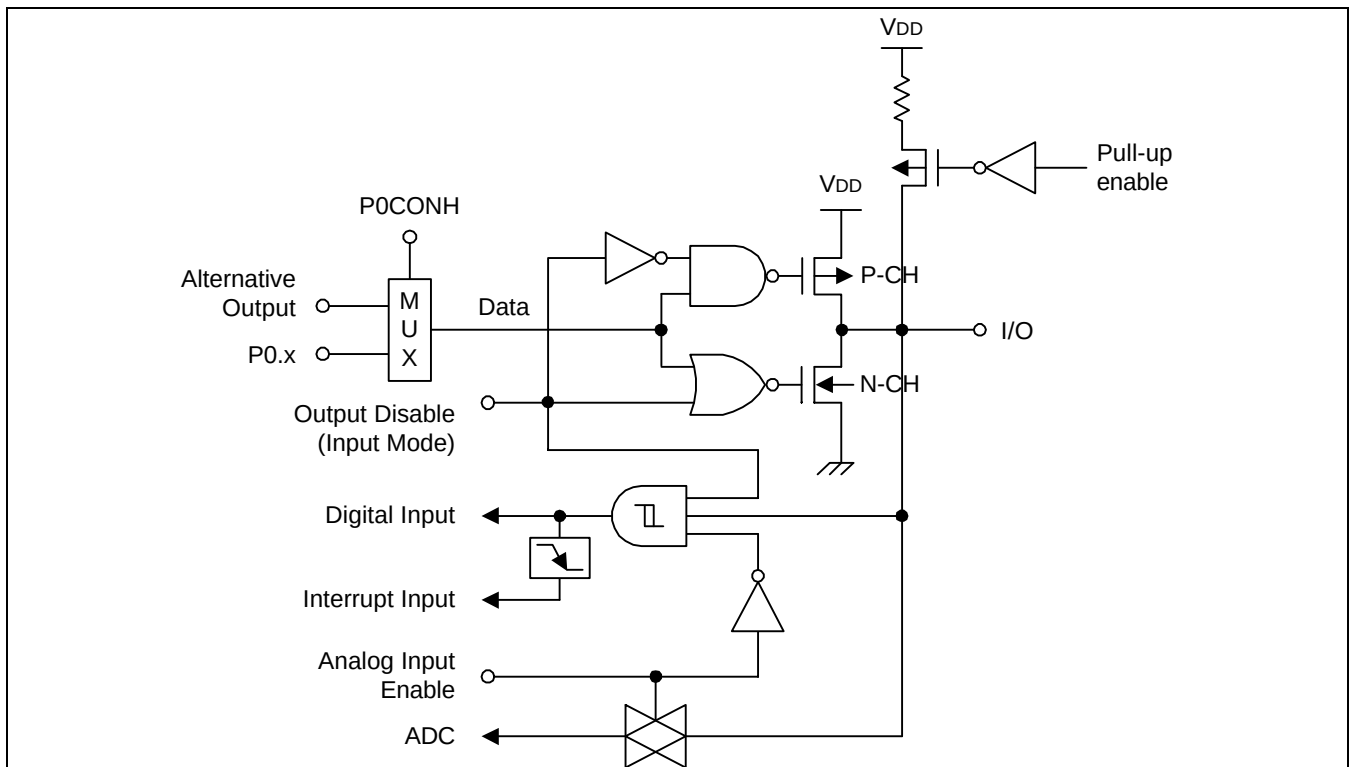


Figure 1-10. Pin Circuit Type E-1



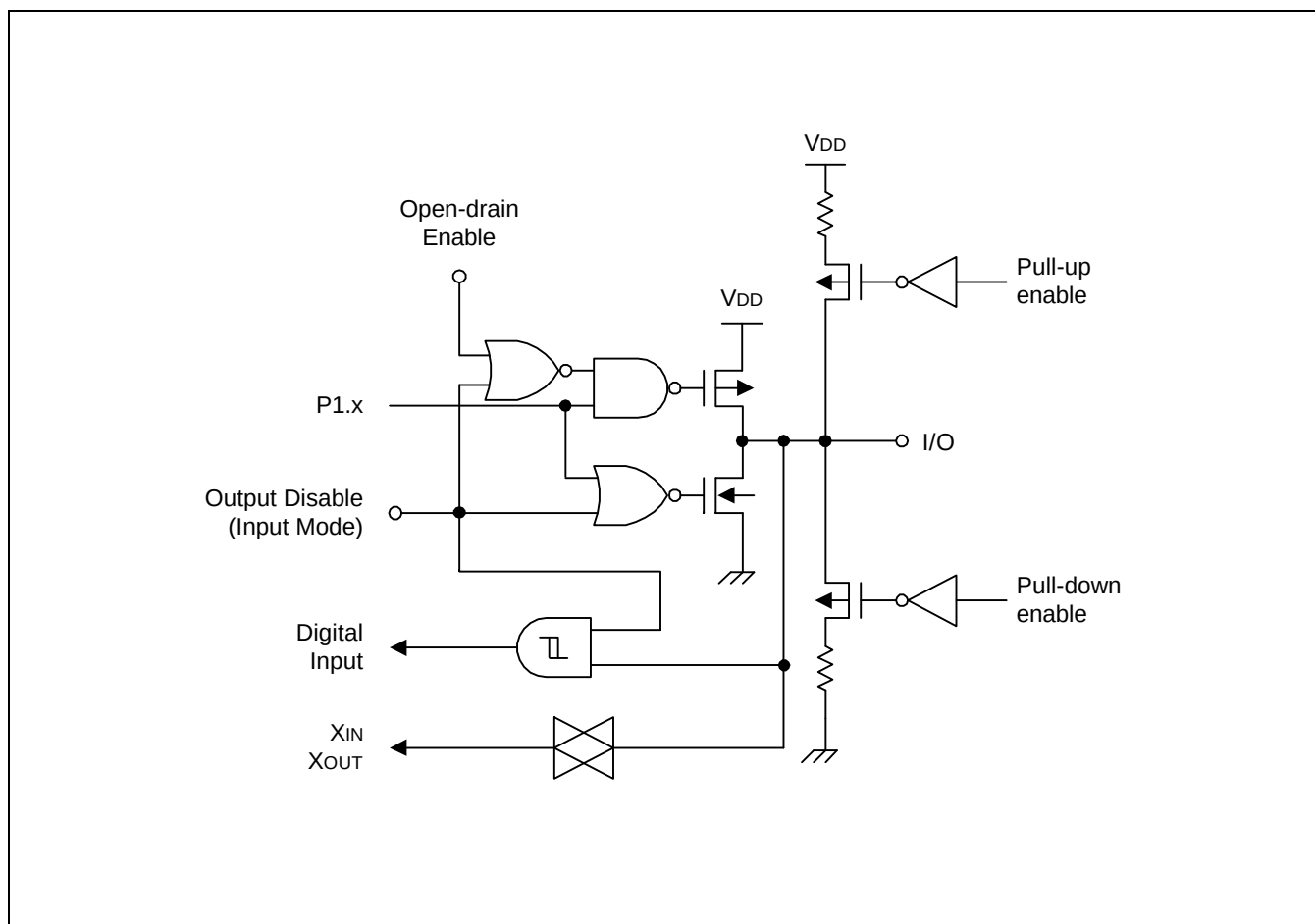


Figure 1-11. Pin Circuit Type E-2

# 13

## ELECTRICAL DATA

### OVERVIEW

In this section, the following S3C9442/C9444/C9452/C9454 electrical characteristics are presented in tables and graphs:

- Absolute maximum ratings
- D.C. electrical characteristics
- A.C. electrical characteristics
- Input Timing Measurement Points
- Oscillator characteristics
- Oscillation stabilization time
- Operating Voltage Range
- Schmitt trigger input characteristics
- Data retention supply voltage in Stop mode
- Stop mode release timing when initiated by a RESET
- A/D converter electrical characteristics
- LVR circuit characteristics
- LVR reset Timing

Table 13-1. Absolute Maximum Ratings

(T<sub>A</sub> = 25 °C)

| Parameter             | Symbol           | Conditions          | Rating                         | Unit |
|-----------------------|------------------|---------------------|--------------------------------|------|
| Supply voltage        | V <sub>DD</sub>  | –                   | – 0.3 to + 6.5                 | V    |
| Input voltage         | V <sub>I</sub>   | All ports           | – 0.3 to V <sub>DD</sub> + 0.3 | V    |
| Output voltage        | V <sub>O</sub>   | All output ports    | – 0.3 to V <sub>DD</sub> + 0.3 | V    |
| Output current high   | I <sub>OH</sub>  | One I/O pin active  | – 25                           | mA   |
|                       |                  | All I/O pins active | – 80                           |      |
| Output current low    | I <sub>OL</sub>  | One I/O pin active  | + 30                           | mA   |
|                       |                  | All I/O pins active | + 150                          |      |
| Operating temperature | T <sub>A</sub>   | –                   | – 40 to + 85                   | °C   |
| Storage temperature   | T <sub>STG</sub> | –                   | – 65 to + 150                  | °C   |

Table 13-2. DC Electrical Characteristics

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 2.0 V to 5.5 V)

| Parameter                   | Symbol            | Conditions                                   | Min                                             | Typ                   | Max                   | Unit |
|-----------------------------|-------------------|----------------------------------------------|-------------------------------------------------|-----------------------|-----------------------|------|
| Input high voltage          | V <sub>IH1</sub>  | Ports 0, 1, 2 and RESET                      | 0.8 V <sub>DD</sub><br>V <sub>DD</sub> - 0.1    | —                     | V <sub>DD</sub>       | V    |
|                             | V <sub>IH2</sub>  | X <sub>IN</sub> and X <sub>OUT</sub>         |                                                 |                       |                       |      |
| Input low voltage           | V <sub>IL1</sub>  | Ports 0, 1, 2 and RESET                      | —                                               | —                     | 0.2 V <sub>DD</sub>   | V    |
|                             | V <sub>IL2</sub>  | X <sub>IN</sub> and X <sub>OUT</sub>         |                                                 |                       | 0.1                   |      |
| Output high voltage         | V <sub>OH</sub>   | I <sub>OH</sub> = -10 mA<br>ports 0, 1, 2    | V <sub>DD</sub> = 4.5 to 5.5 V                  | V <sub>DD</sub> - 1.5 | V <sub>DD</sub> - 0.4 | V    |
| Output low voltage          | V <sub>OL</sub>   | I <sub>OL</sub> = 25 mA<br>port 0, 1, and 2  | V <sub>DD</sub> = 4.5 to 5.5 V                  | —                     | 0.4                   | 2.0  |
| Input high leakage current  | I <sub>LIH1</sub> | All input except I <sub>LIH2</sub>           | V <sub>IN</sub> = V <sub>DD</sub>               | —                     | —                     | 1    |
|                             | I <sub>LIH2</sub> | X <sub>IN</sub> , X <sub>OUT</sub>           | V <sub>IN</sub> = V <sub>DD</sub>               |                       |                       | 20   |
| Input low leakage current   | I <sub>LIL1</sub> | All input except I <sub>LIL2</sub> and RESET | V <sub>IN</sub> = 0 V                           | —                     | —                     | -1   |
|                             | I <sub>LIL2</sub> | X <sub>IN</sub> , X <sub>OUT</sub>           | V <sub>IN</sub> = 0 V                           |                       |                       | -20  |
| Output high leakage current | I <sub>LOH</sub>  | All output pins                              | V <sub>OUT</sub> = V <sub>DD</sub>              | —                     | —                     | 2    |
| Output low leakage current  | I <sub>LOL</sub>  | All output pins                              | V <sub>OUT</sub> = 0 V                          | —                     | —                     | -2   |
| Pull-up resistors           | R <sub>P</sub>    | V <sub>IN</sub> = 0 V<br>Ports 0, 1, 2       | V <sub>DD</sub> = 5 V                           | 25                    | 50                    | 100  |
| Pull-down resistors         | R <sub>P</sub>    | V <sub>IN</sub> = 0 V<br>Ports 1             | V <sub>DD</sub> = 5 V                           | 25                    | 50                    | 100  |
| Supply current              | I <sub>DD1</sub>  | Run mode<br>10 MHz CPU clock                 | V <sub>DD</sub> = 4.5 to 5.5 V                  | —                     | 5                     | 10   |
|                             |                   | 3 MHz CPU clock                              | V <sub>DD</sub> = 2.0 V                         |                       | 2                     | 5    |
|                             | I <sub>DD2</sub>  | Idle mode<br>10 MHz CPU clock                | V <sub>DD</sub> = 4.5 to 5.5 V                  | —                     | 2                     | 4    |
|                             |                   | 3 MHz CPU clock                              | V <sub>DD</sub> = 2.0 V                         |                       | 0.5                   | 1.5  |
|                             | I <sub>DD3</sub>  | Stop mode                                    | V <sub>DD</sub> = 4.5 to 5.5 V<br>(LVR disable) | —                     | 0.1                   | 5    |
|                             |                   |                                              | V <sub>DD</sub> = 4.5 to 5.5 V<br>(LVR enable)  |                       | 100                   | 200  |
|                             |                   |                                              | V <sub>DD</sub> = 2.6 V<br>(LVR enable)         |                       | 30                    | 60   |

**NOTE:** In STOP (I<sub>DD3</sub>), IDLE (I<sub>DD2</sub>) current, current by ADC module is not included.

Table 13-3. AC Electrical Characteristics

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 2.0 V to 5.5 V)

| Parameter                 | Symbol            | Conditions                                 | Min | Typ | Max | Unit |
|---------------------------|-------------------|--------------------------------------------|-----|-----|-----|------|
| Interrupt input low width | t <sub>INTL</sub> | INT0, INT1<br>V <sub>DD</sub> = 5 V ± 10 % | —   | 200 | —   | ns   |
| RESET input low width     | t <sub>RSL</sub>  | Input<br>V <sub>DD</sub> = 5 V ± 10 %      | —   | 1   | —   | us   |

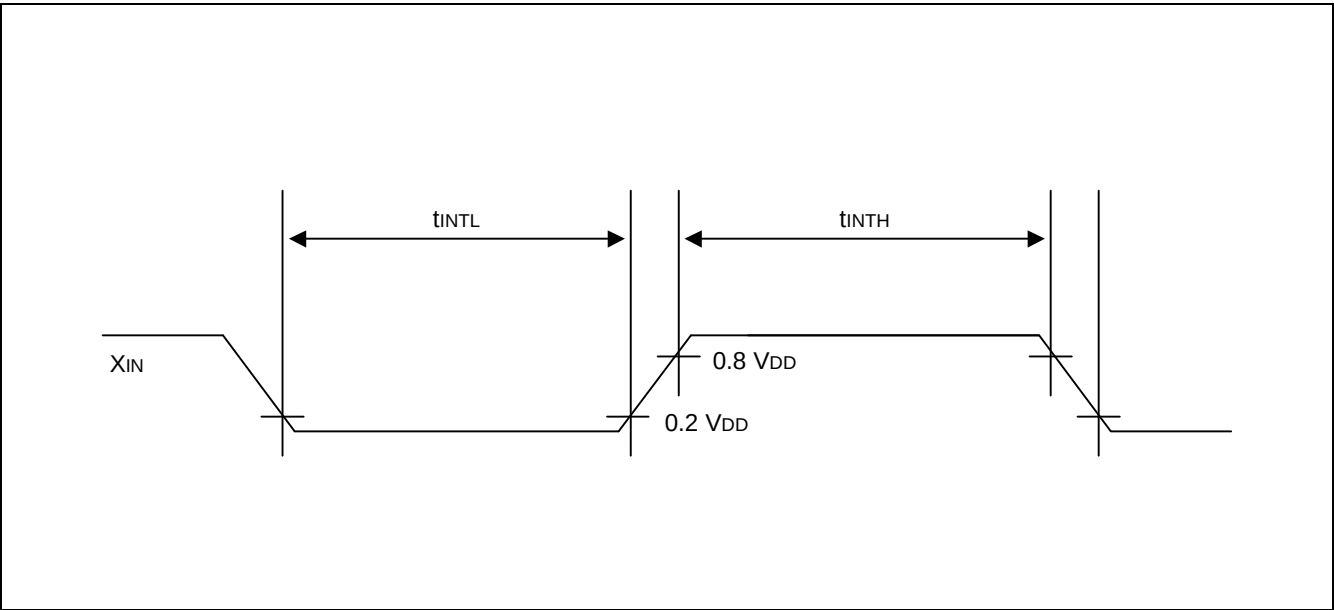


Figure 13-1. Input Timing Measurement Points

Table 13-4. Oscillator Characteristics

(T<sub>A</sub> = -40°C to +85°C)

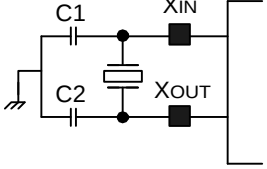
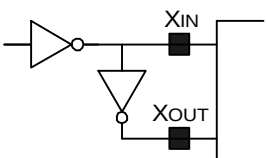
| Oscillator                   | Clock Circuit                                                                     | Test Condition                                      | Min | Typ | Max | Unit |
|------------------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------|-----|-----|-----|------|
| Main crystal or ceramic      |  | V <sub>DD</sub> = 4.5 to 5.5 V                      | 1   | —   | 10  | MHz  |
|                              |                                                                                   | V <sub>DD</sub> = 2.7 to 4.5 V                      | 1   | —   | 6   | MHz  |
|                              |                                                                                   | V <sub>DD</sub> = 2.0 to 2.7 V                      | 1   | —   | 3   | MHz  |
| External clock (Main System) |  | V <sub>DD</sub> = 4.5 to 5.5 V                      | 1   | —   | 10  | MHz  |
|                              |                                                                                   | V <sub>DD</sub> = 2.7 to 4.5 V                      | 1   | —   | 6   | MHz  |
|                              |                                                                                   | V <sub>DD</sub> = 2.0 to 2.7 V                      | 1   | —   | 3   | MHz  |
| External RC oscillator       | —                                                                                 | V <sub>DD</sub> = 4.75 to 5.25 V<br>Tolerance: 10 % | —   | 4   | —   | MHz  |
| Internal RC                  |                                                                                   | V <sub>DD</sub> = 4.75 to 5.25 V                    |     | 3.2 |     |      |
| Oscillator                   |                                                                                   | V <sub>DD</sub> = 4.75 to 5.25 V                    |     | 0.5 |     |      |

Table 13-5. Oscillation Stabilization Time

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 3.0 V to 5.5 V)

| Oscillator                   | Test Condition                                                                                          | Min | Typ                               | Max | Unit |
|------------------------------|---------------------------------------------------------------------------------------------------------|-----|-----------------------------------|-----|------|
| Main crystal                 | f <sub>OSC</sub> > 1.0 MHz                                                                              | —   | —                                 | 20  | ms   |
| Main ceramic                 | Oscillation stabilization occurs when V <sub>DD</sub> is equal to the minimum oscillator voltage range. | —   | —                                 | 10  | ms   |
| External clock (main system) | X <sub>IN</sub> input high and low width (t <sub>XH</sub> , t <sub>XL</sub> )                           | 25  | —                                 | 500 | ns   |
| Oscillator stabilization     | t <sub>WAIT</sub> when released by a reset <sup>(1)</sup>                                               | —   | 2 <sup>16</sup> /f <sub>OSC</sub> | —   | ms   |
| wait time                    | t <sub>WAIT</sub> when released by an interrupt <sup>(2)</sup>                                          | —   | —                                 | —   | ms   |

**NOTES:**

- f<sub>OSC</sub> is the oscillator frequency.
- The duration of the oscillator stabilization wait time, t<sub>WAIT</sub>, when it is released by an interrupt is determined by the settings in the basic timer control register, BTCON.

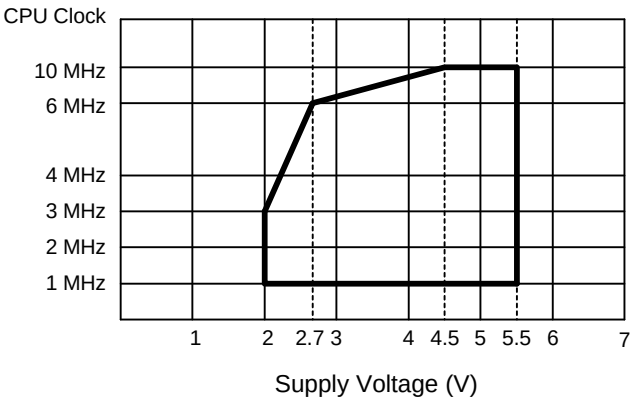


Figure 13-2. Operating Voltage Range

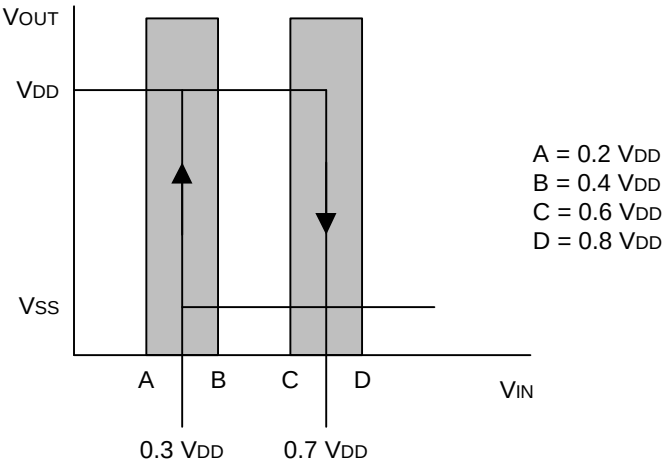


Figure 13-3. Schmitt Trigger Input Characteristics Diagram

**Table 13-6. Data Retention Supply Voltage in Stop Mode**(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 2.0 V to 5.5 V)

| Parameter                     | Symbol            | Conditions                           | Min | Typ | Max | Unit |
|-------------------------------|-------------------|--------------------------------------|-----|-----|-----|------|
| Data retention supply voltage | V <sub>DDDR</sub> | Stop mode                            | 2.0 | –   | 5.5 | V    |
| Data retention supply current | I <sub>DDDR</sub> | Stop mode; V <sub>DDDR</sub> = 2.0 V | –   | 0.1 | 5   | uA   |

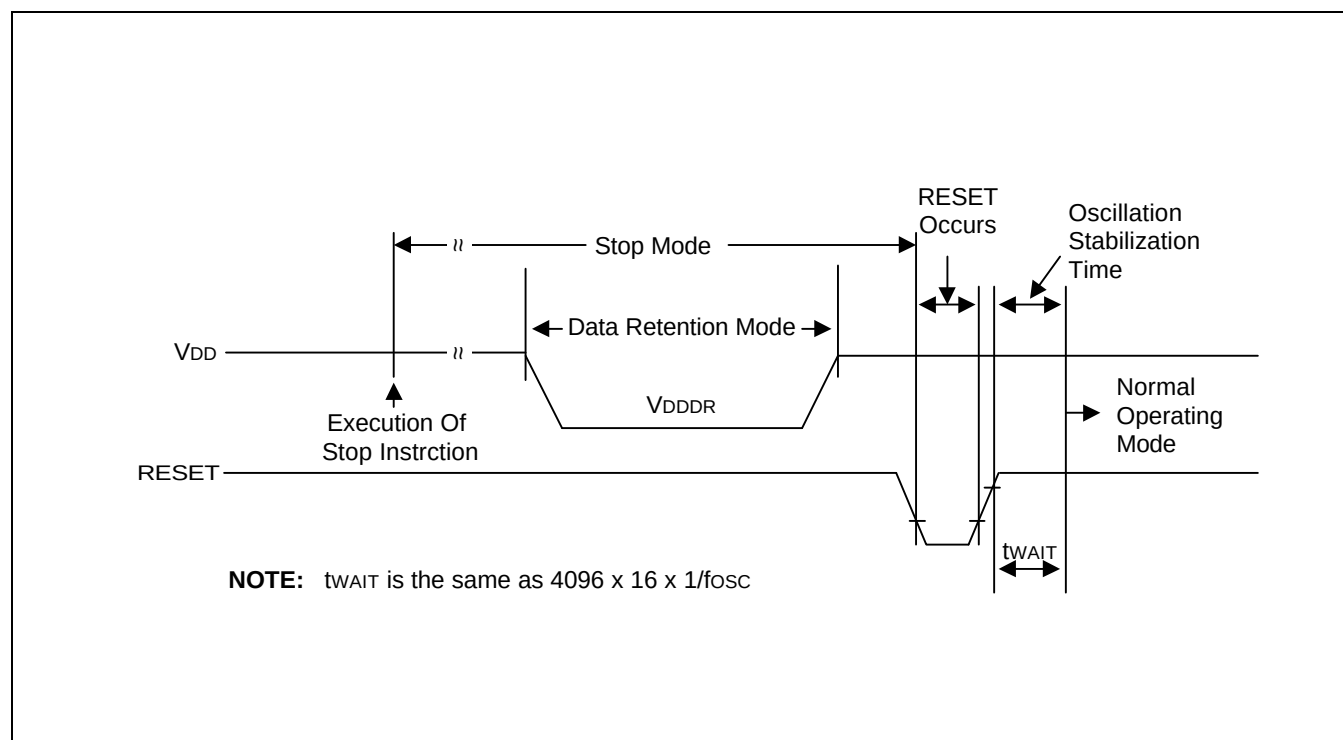
**NOTE:** Supply current does not include current drawn through internal pull-up resistors or external output current loads.**Figure 13-4. Stop Mode Release Timing When Initiated by a RESET**



Table 13-7. A/D Converter Electrical Characteristics

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

| Parameter                           | Symbol            | Test Conditions                                                         | Min             | Typ | Max             | Unit |
|-------------------------------------|-------------------|-------------------------------------------------------------------------|-----------------|-----|-----------------|------|
| Total accuracy                      | —                 | V <sub>DD</sub> = 5.12 V<br>CPU clock = 10 MHz<br>V <sub>SS</sub> = 0 V | —               | —   | ± 3             | LSB  |
| Integral linearity error            | ILE               | "                                                                       | —               | —   | ± 2             |      |
| Differential linearity error        | DLE               | "                                                                       | —               | —   | ± 1             |      |
| Offset error of top                 | EOT               | "                                                                       | —               | ± 1 | ± 3             |      |
| Offset error of bottom              | EOB               | "                                                                       | —               | ± 1 | ± 2             |      |
| Conversion time <sup>(1)</sup>      | t <sub>CON</sub>  | f <sub>OSC</sub> = 10 MHz                                               | —               | 20  | —               | μs   |
| Analog input voltage                | V <sub>IAN</sub>  | —                                                                       | V <sub>SS</sub> | —   | V <sub>DD</sub> | V    |
| Analog input impedance              | R <sub>AN</sub>   | —                                                                       | 2               | —   | —               | MΩ   |
| Analog input current                | I <sub>ADIN</sub> | V <sub>DD</sub> = 5 V                                                   | —               | —   | 10              | μA   |
| Analog block current <sup>(2)</sup> | I <sub>ADC</sub>  | V <sub>DD</sub> = 5 V                                                   | —               | 1   | 3               | mA   |
|                                     |                   | V <sub>DD</sub> = 3 V                                                   |                 | 0.5 | 1.5             |      |
|                                     |                   | V <sub>DD</sub> = 5 V<br>power down mode                                | —               | 100 | 500             | nA   |

**NOTES:**

1. "Conversion time" is the time required from the moment a conversion operation starts until it ends.
2. I<sub>ADC</sub> is operating current during A/D conversion.

Table 13-8. LVR Circuit Characteristics

(T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 2.0 V to 5.5 V)

| Parameter                      | Symbol           | Conditions | Min | Typ               | Max    | Unit |
|--------------------------------|------------------|------------|-----|-------------------|--------|------|
| Low voltage reset              | V <sub>LVR</sub> | —          | —   | 2.3<br>3.0<br>3.9 |        | V    |
| LVR hysteresis voltage         | V <sub>HYS</sub> |            | —   | 0.3               | —      | V    |
| Power supply voltage rise time | t <sub>R</sub>   |            | 10  |                   | (note) | us   |
| Power supply voltage off time  | t <sub>OFF</sub> |            | 0.5 |                   |        | s    |

**NOTE:** 2<sup>16</sup>/f<sub>x</sub> ( = 6.55 ms at f<sub>x</sub> = 10 MHz)

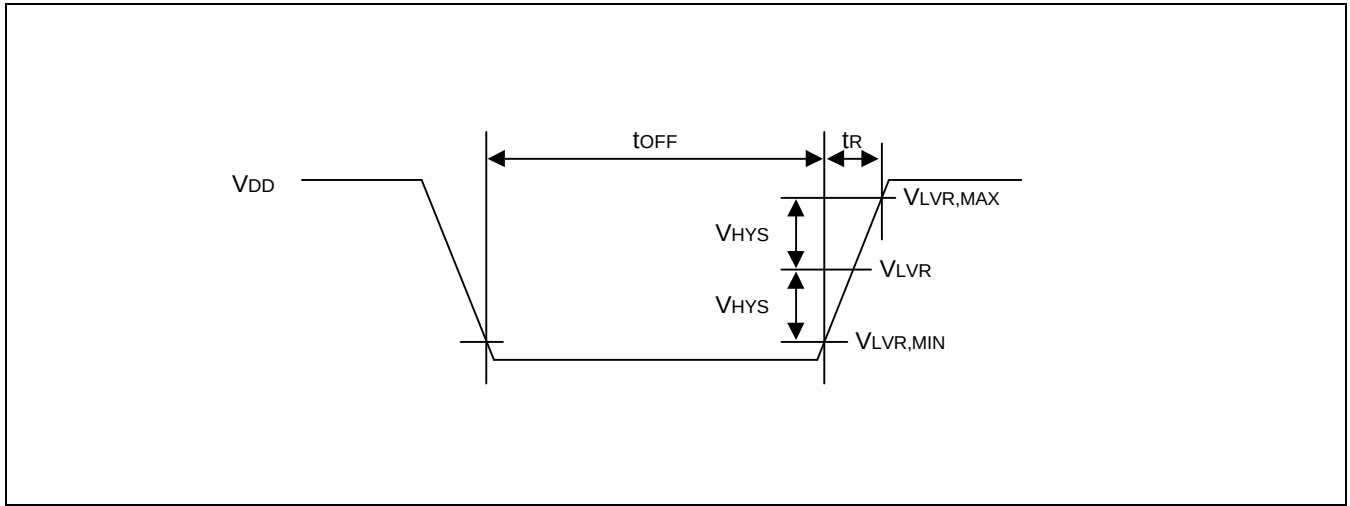


Figure 13-5. LVR Reset Timing

# 14

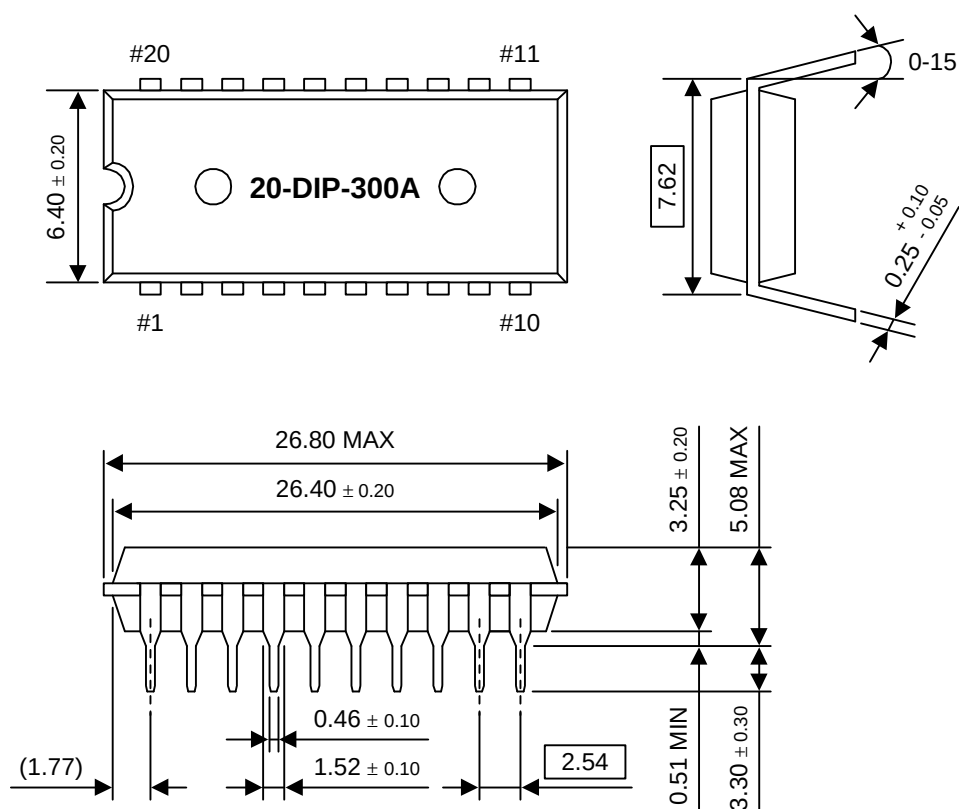
## MECHANICAL DATA

### OVERVIEW

The S3C9452/C9454 is available in a 20-pin DIP package (Samsung: 20-DIP-300A), a 20-pin SOP package (Samsung: 20-SOP-375), a 16-pin DIP package (Samsung: 16-DIP-300A). Package dimensions are shown in Figure 15-1, 15-2, and 15-3.

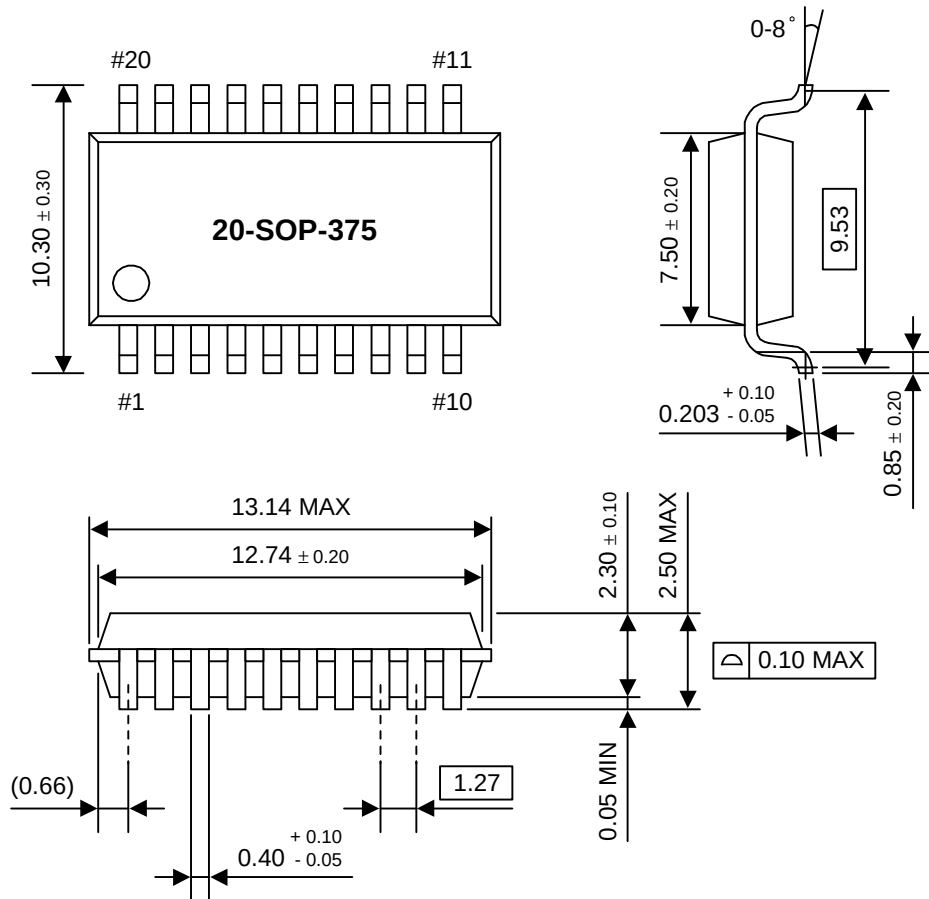
The S3C9442/C9444 is available in a 8-pin DIP package (SAMSUNG 8-DIP-300A), a 8-pin SOP package (SAMSUNG 8-SOP-225).

Package dimensions are shown in figure 14-4 and 14-5.



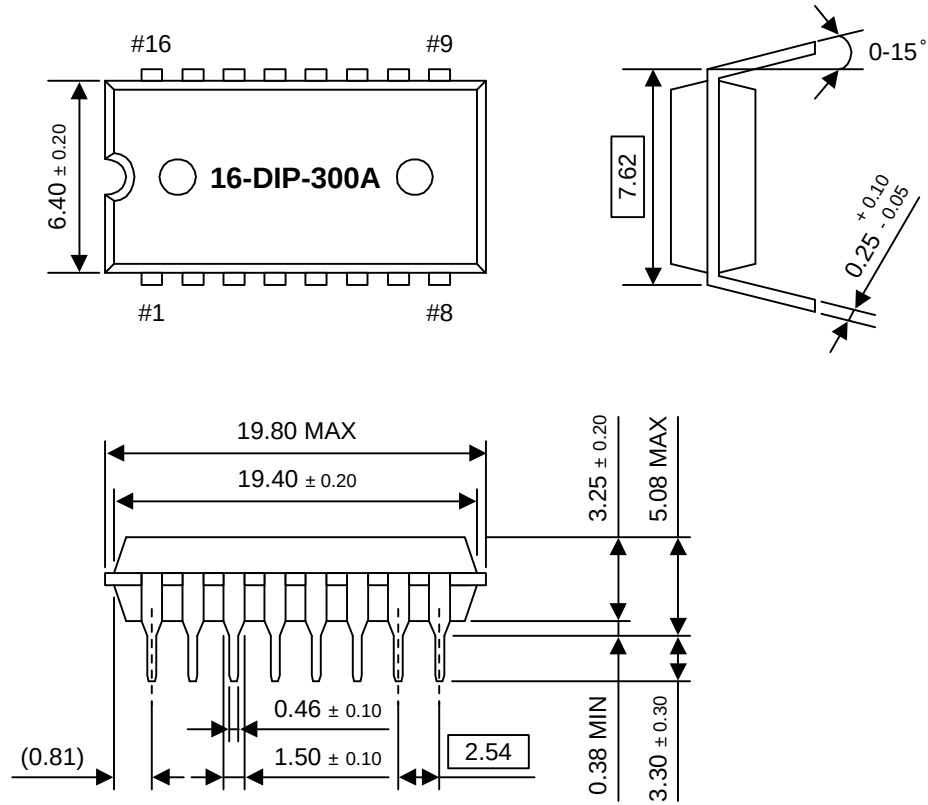
**NOTE:** Dimensions are in millimeters.

Figure 14-1. 20-DIP-300A Package Dimensions



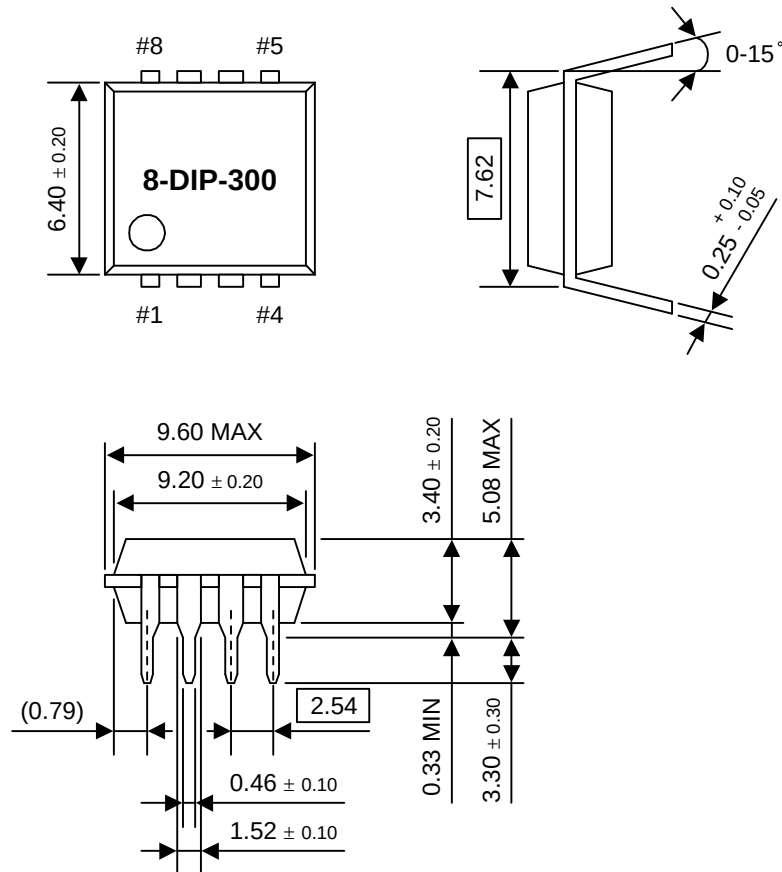
**NOTE:** Dimensions are in millimeters.

**Figure 14-2. 20-SOP-375 Package Dimensions**



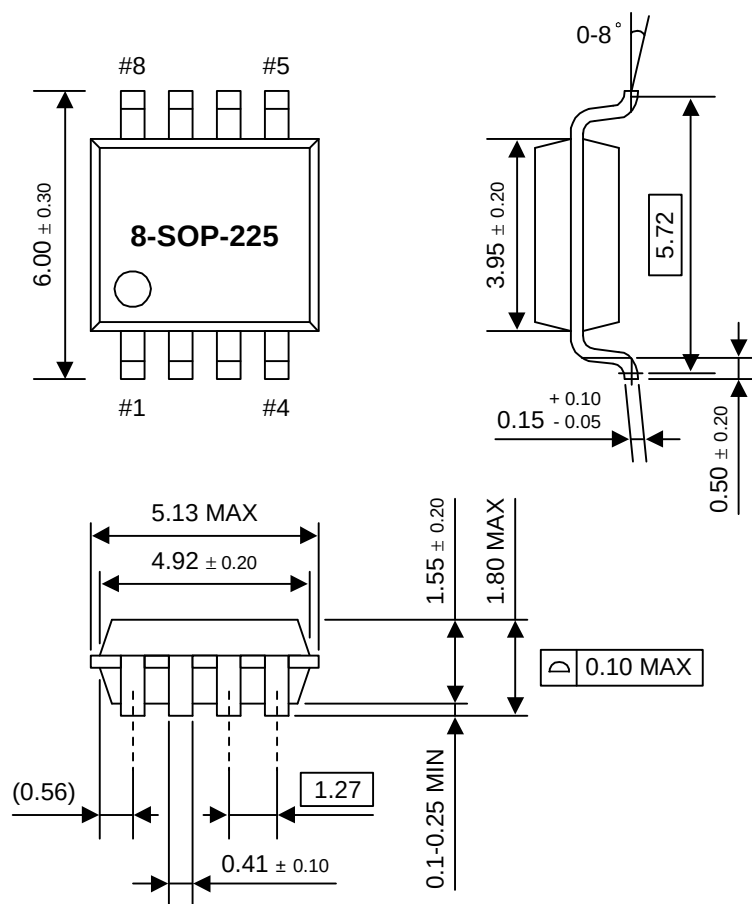
**NOTE:** Dimensions are in millimeters.

**Figure 14-3. 16-DIP-300A Package Dimensions**



**NOTE:** Dimensions are in millimeters.

**Figure 14-4. 8-DIP-300 Package Dimensions**



**NOTE:** Dimensions are in millimeters.

**Figure 14-5. 8-SOP-225 Package Dimensions**

15

S3F9444/F9454 MTP

OVERVIEW

The S3F9444/F9454 single-chip CMOS microcontroller is the MTP (Multi Time Programmable) version of the S3C9442/C9444/C9452/C9454 microcontroller. It has an on-chip Flash ROM instead of masked ROM. The Flash ROM is accessed by serial data format.

The S3F9444/F9454 is fully compatible with the S3C9442/C9444/C9452/C9454, in function, in D.C. electrical characteristics, and in pin configuration. Because of its simple programming requirements, the S3F9444/F9454 is ideal for use as an evaluation chip for the S3C9442/C9444/C9452/C9454.

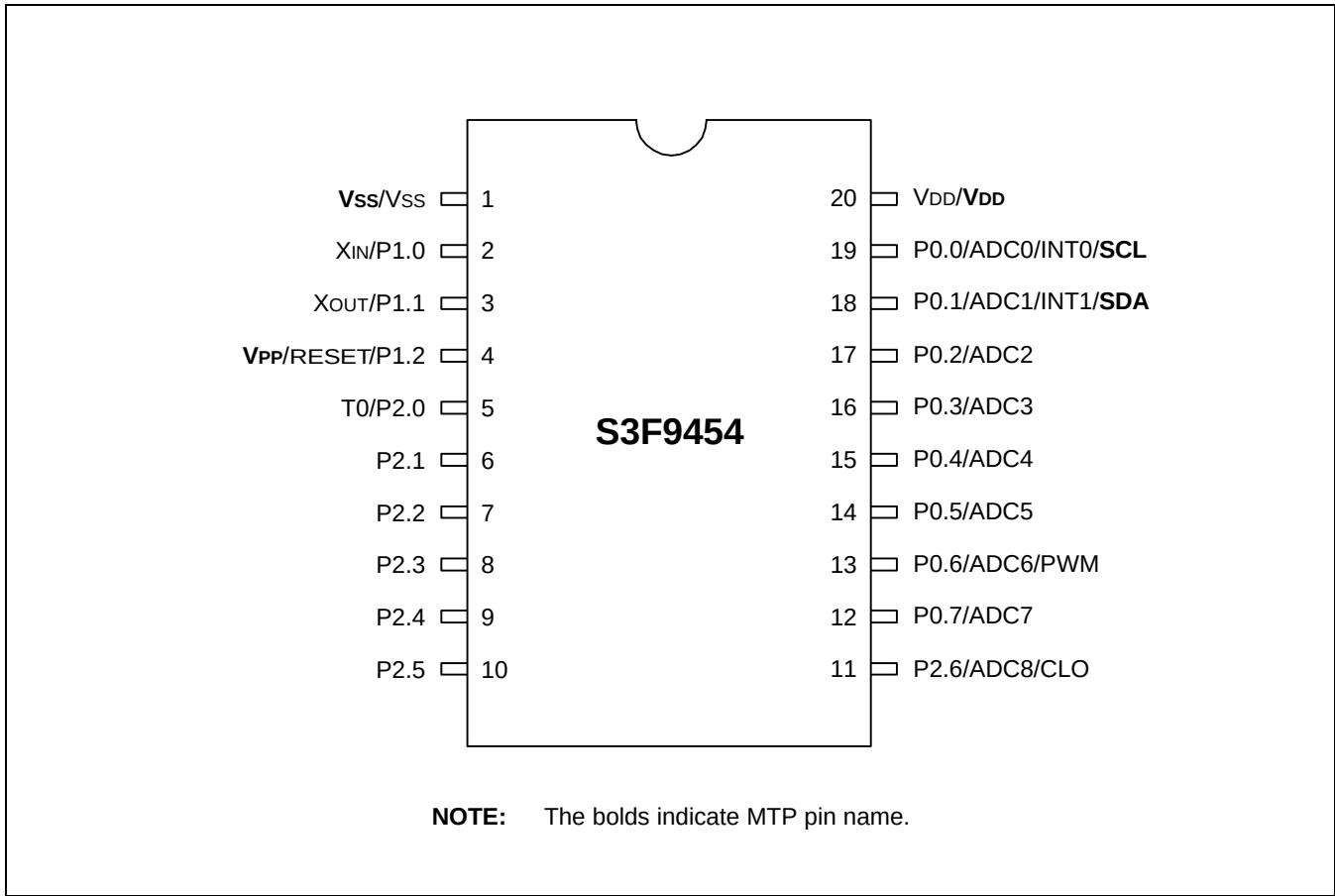
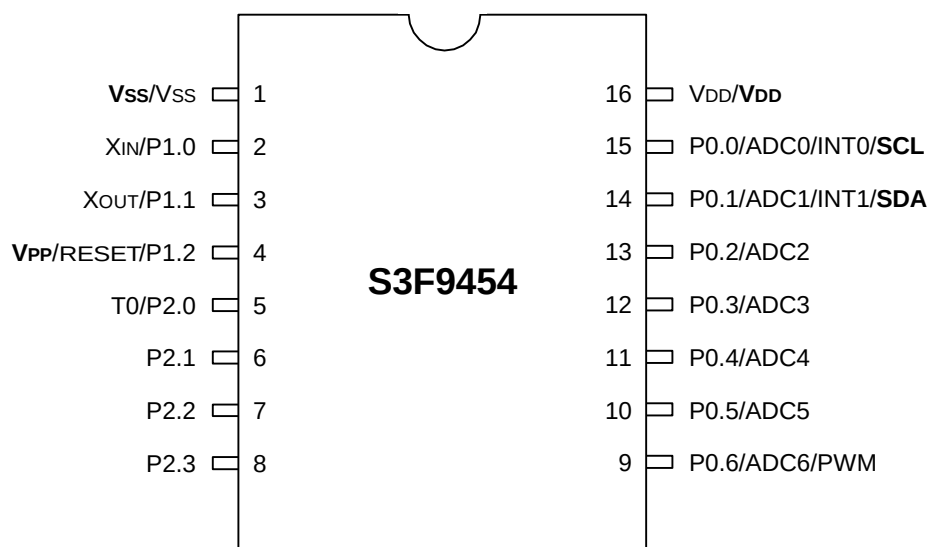


Figure 15-1. Pin Assignment Diagram (20-Pin Package)





**NOTE:** The bolds indicate MTP pin name.

**Figure 15-2. Pin Assignment Diagram (16-Pin Package)**



**NOTE:** The bolds indicate MTP pin name.

**Figure 15-3. Pin Assignment Diagram (8-Pin Package)**

Table 15-1. Descriptions of Pins Used to Read/Write the Flash ROM

| Main Chip<br>Pin Name            | During Programming               |                                                    |     |                                                                                                                                                                                                         |
|----------------------------------|----------------------------------|----------------------------------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                  | Pin Name                         | Pin No.                                            | I/O | Function                                                                                                                                                                                                |
| P0.1                             | SDA                              | 18 (20-pin)<br>14 (16-pin)                         | I/O | Serial data pin (output when reading, Input when writing) Input and push-pull output port can be assigned                                                                                               |
| P0.0                             | SCL                              | 19 (20-pin)<br>15 (16-pin)                         | I   | Serial clock pin (input only pin)                                                                                                                                                                       |
| RESET, P1.2                      | V <sub>PP</sub>                  | 4                                                  | I   | Power supply pin for flash ROM cell writing (indicates that MTP enters into the writing mode). When 12.5 V is applied, MTP is in writing mode and when 5 V is applied, MTP is in reading mode. (Option) |
| V <sub>DD</sub> /V <sub>SS</sub> | V <sub>DD</sub> /V <sub>SS</sub> | 20 (20-pin), 16 (16-pin)<br>1 (20-pin), 1 (16-pin) | I   | Logic power supply pin.                                                                                                                                                                                 |

Table 15-2. Comparison of S3F9444/F9454 and S3C9442/C9444/C9452/C9454 Features

| Characteristic                       | S3F9444/F9454                                   | S3C9442/C9444/C9452/C9454 |
|--------------------------------------|-------------------------------------------------|---------------------------|
| Program Memory                       | 4 Kbyte Flash ROM                               | 2K/4K byte mask ROM       |
| Operating Voltage (V <sub>DD</sub> ) | 2.0 V to 5.5 V                                  | 2.0 V to 5.5 V            |
| OTP Programming Mode                 | V <sub>DD</sub> = 5 V, V <sub>PP</sub> = 12.5 V |                           |
| Pin Configuration                    | 20 DIP/20 SOP/16 DIP/8 DIP/8 SOP                |                           |
| EPROM Programmability                | User Program multi time                         | Programmed at the factory |

## OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V<sub>PP</sub> pin of the S3F9444/F9454 Flash ROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 15-3 below.

Table 15-3. Operating Mode Selection Criteria

| V <sub>DD</sub> | V <sub>PP</sub> | REG/MEM | Address (A15-A0) | R/W | Mode                      |
|-----------------|-----------------|---------|------------------|-----|---------------------------|
| 5 V             | 5 V             | 0       | 0000H            | 1   | Flash ROM read            |
|                 | 12.5 V          | 0       | 0000H            | 0   | Flash ROM program         |
|                 | 12.5 V          | 0       | 0000H            | 1   | Flash ROM verify          |
|                 | 12.5 V          | 1       | 0E3FH            | 0   | Flash ROM read protection |

**NOTE:** "0" means Low level; "1" means High level.