

# 1

## PRODUCT OVERVIEW

### S3C8-SERIES MICROCONTROLLERS

Samsung's S3C8 series of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Among the major CPU features are:

- Efficient register-oriented architecture
- Selectable CPU clock sources
- Idle and Stop power-down mode release by interrupt
- Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum of six CPU clocks) can be assigned to specific interrupt levels.

### S3C821A/P821A MICROCONTROLLER

The S3C821A/P821A single-chip CMOS microcontroller is fabricated using the highly advanced CMOS process, based on Samsung's newest CPU architecture.

The S3C821A is a microcontroller with a 48-Kbyte mask-programmable ROM embedded.

The S3P821A is a microcontroller with a 48-Kbyte one-time-programmable ROM embedded.

Using a proven modular design approach, Samsung engineers have successfully developed the S3C821A/P821A by integrating the following peripheral modules with the powerful SAM8 core:

- Six programmable I/O ports, including five 8-bit

ports and one 7-bit port, for a total of 47 pins.

- Twelve bit-programmable pins for external interrupts.
- One 8-bit basic timer for oscillation stabilization and watchdog functions (system reset).
- One 8-bit timer/counter and one 16-bit timer/counter with selectable operating modes.
- Watch timer for real time.
- 4-input A/D converter
- Serial I/O interface

The S3C821A/P821A is versatile microcontroller for cordless phone, pager, etc. They are currently available in 80-pin TQFP and 80-pin QFP package.

### OTP

The S3P821A is an OTP (One Time Programmable) version of the S3C821A microcontroller. The S3P821A microcontroller has an on-chip 48-Kbyte one-time-programmable EPROM instead of a masked ROM. The S3P821A is comparable to the S3C821A, both in function and in pin configuration.

## FEATURES

### CPU

- SAM8 CPU core

### Memory

- Data memory: 1040-byte of internal register file (Excluding LCD RAM)
- Program memory: 48-Kbyte internal program memory (ROM)

### External Interface

- 64-Kbyte external data memory area

### Instruction Execution Time

- 750 ns at 8 MHz (minimum, Main oscillator)
- 183  $\mu$ s at 32,768 Hz (minimum, Sub oscillator)

### Interrupts

- 7 interrupt levels and 19 interrupt sources
- 19 vectors
- Fast interrupt processing feature (for one selected interrupt level)

### I/O Ports

- Five 8-bit I/O ports (P0–P4) and one 7-bit I/O port (P5) for a total of 47 bit-programmable pins

### 8-Bit Basic Timer

- One programmable 8-bit basic timer (BT) for oscillation stabilization control or watchdog timer (software reset) function

### Watch Timer

- Time interval generation: 3.91 ms, 0.5 s at 32,768 Hz
- Four frequency outputs to BUZ pin
- Clock source generation for LCD

### Timers and Timer/Counters

- One 8-bit timer/counter (Timer 0) with three operating modes: Interval, Capture, and PWM
- One 16-bit timer/counter (Timer 1) with two 8-bit timer/counter modes

### LCD Controller/Driver

- Up to 32 segment pins
- 3, 4, and 8 common selectable
- Choice of duty cycle
- All dots can be switched on/off
- Internal resistor circuit for LCD bias

### Serial Port

- One synchronous SIO

### A/D Converter

- 8-bit conversion resolution  $\times$  4 channel
- 34  $\mu$ s conversion time (4 MHz CPU clock, fxx/4)

### Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal or external oscillator for subsystem clock
- Main system clock frequency: 8 MHz
- Subsystem clock frequency: 32.768 kHz

### Power-down Modes

- Main idle mode (only CPU clock stops)
- Sub idle mode
- Stop mode (main/sub system oscillation stops)

### Operating Temperature Range

- $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

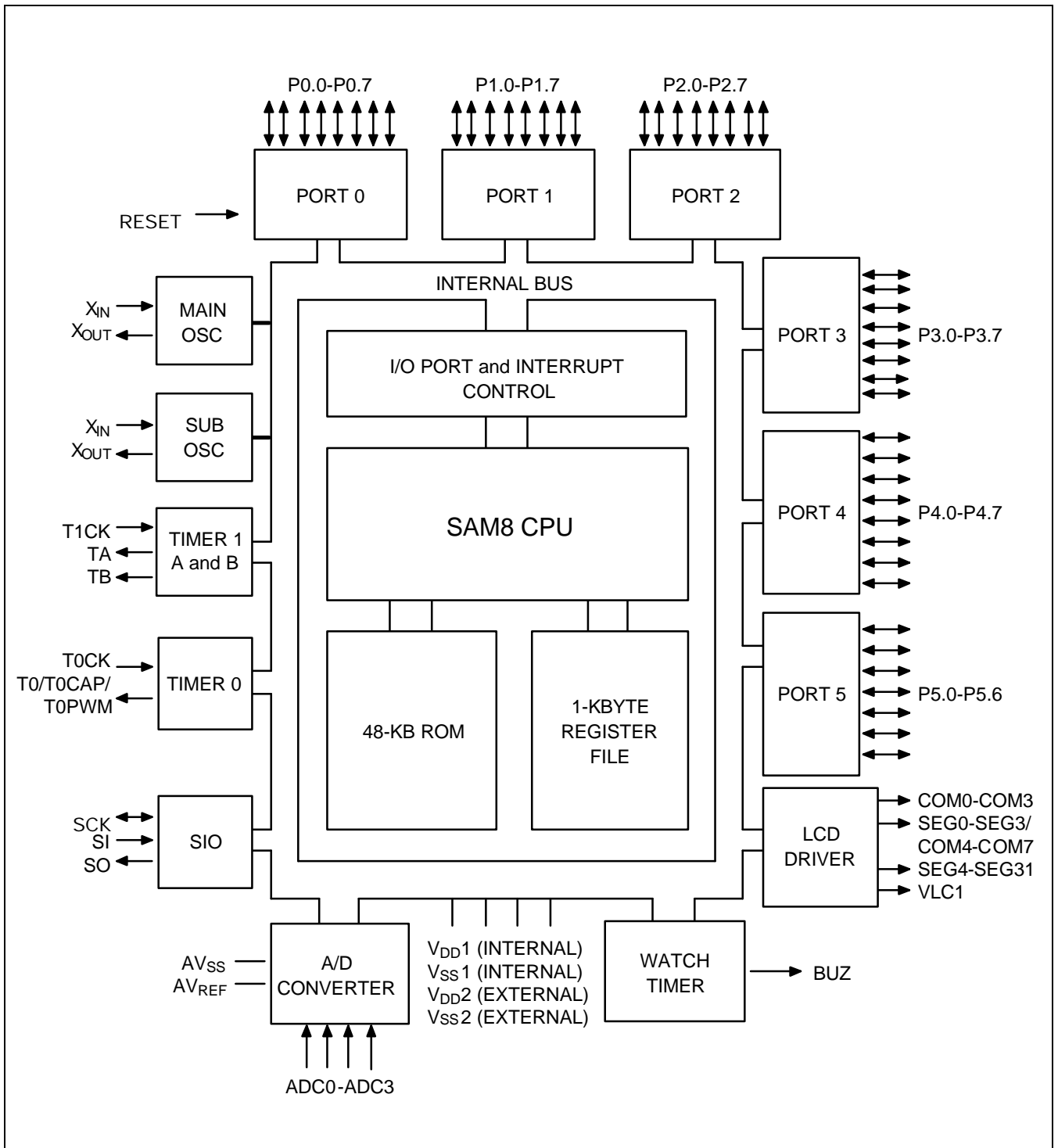
### Operating Voltage Range

- 2.0 V to 5.5 V at 32 kHz (sub clock)-6 MHz (main clock)
- 2.2 V to 5.5 V at 8 MHz

### Package Type

- 80-pin TQFP, 80-pin QFP

**BLOCK DIAGRAM**



**Figure 1-1. S3C821A Simplified Block Diagram**

PIN ASSIGNMENTS

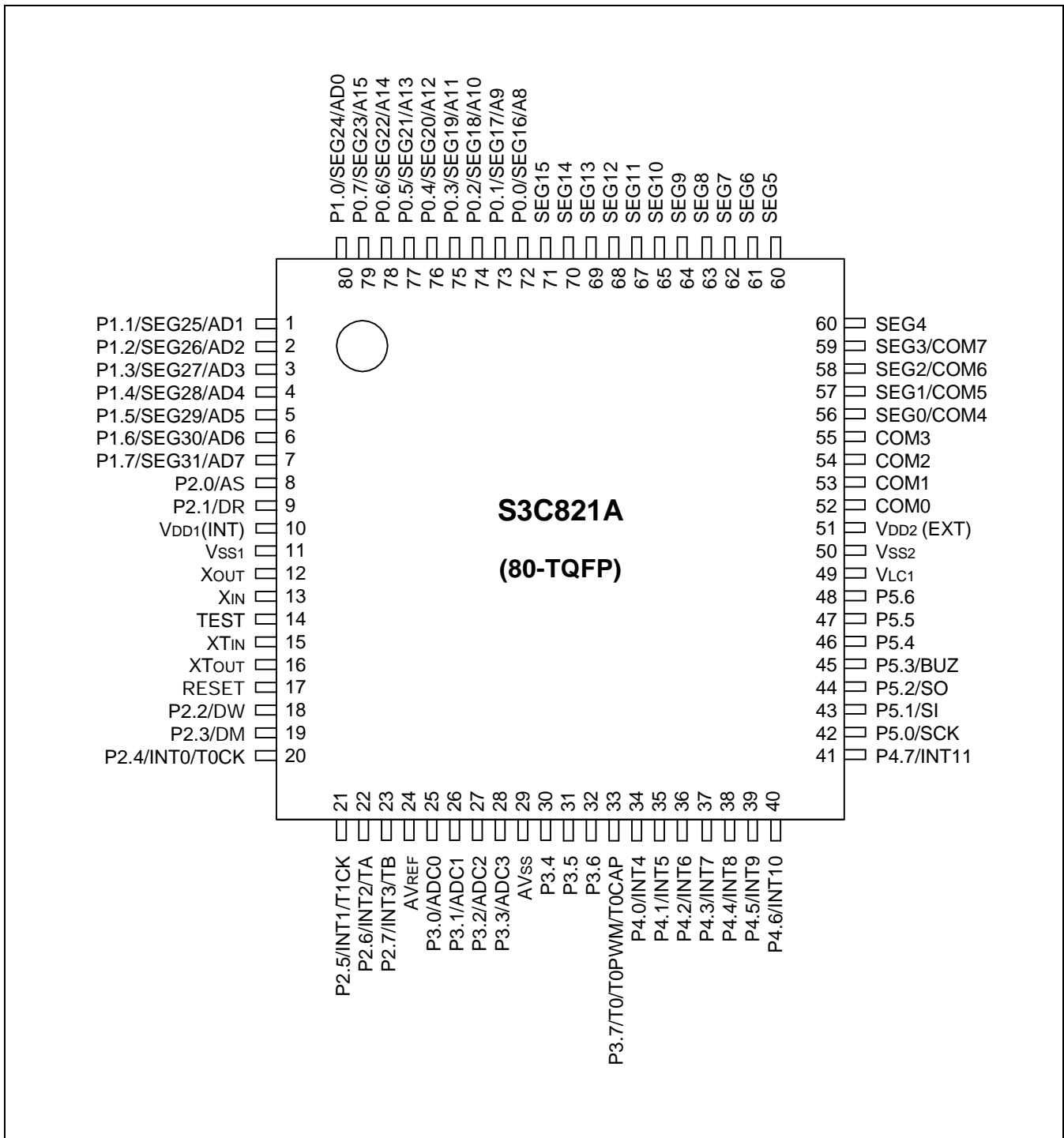


Figure 1-2. S3C821A Pin Assignments (80-TQFP-1212)

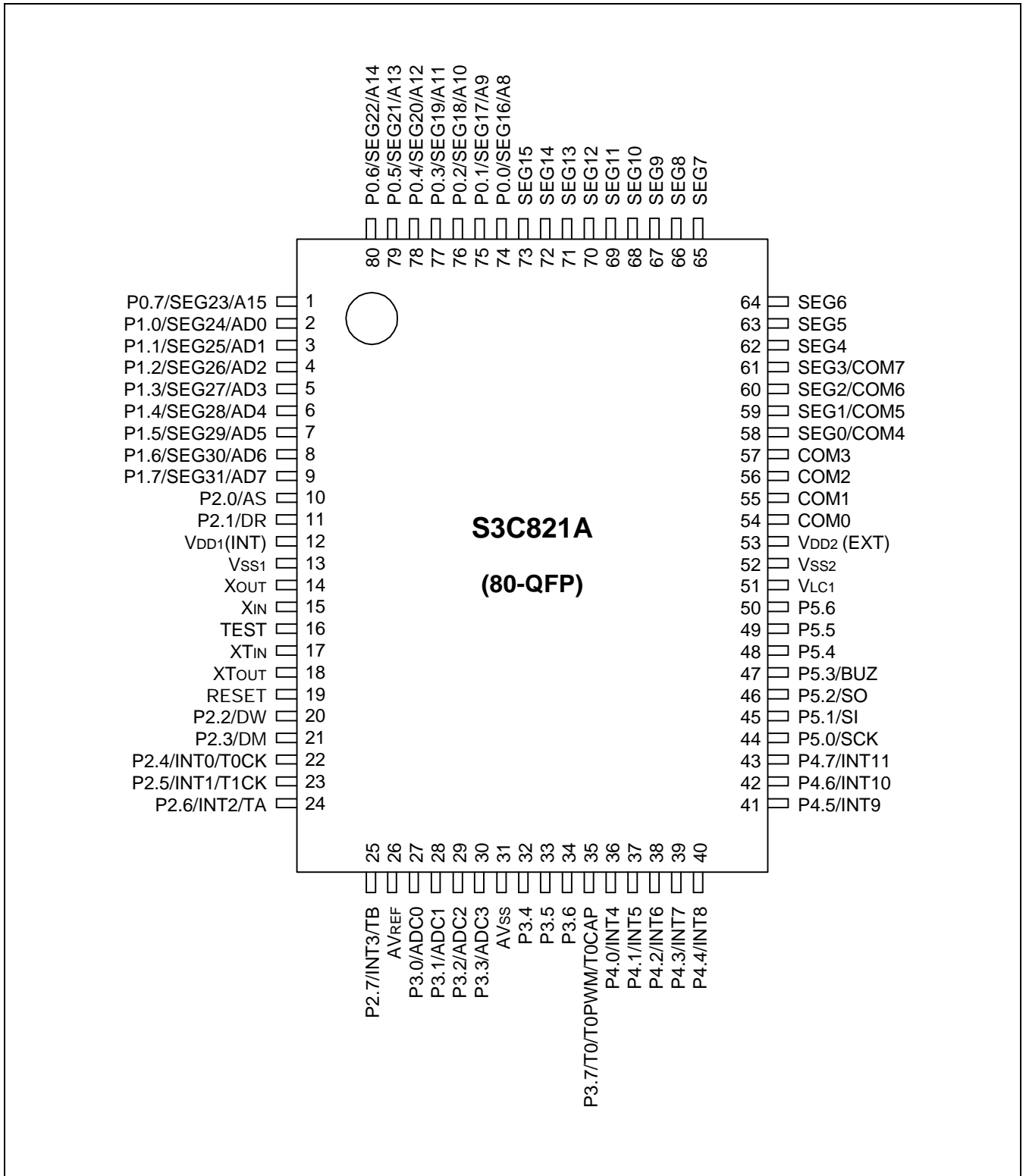


Figure 1-3. S3C821A Pin Assignments (80-QFP-1420C)

**PIN DESCRIPTIONS**

**Table 1-1. S3C821A Pin Descriptions**

Pin Names	Pin Type	Pin Description	Circuit Type	Pin Numbers (note)	Share Pins
P0.0–P0.7	I/O	4-bit-programmable I/O port. Pull-up resistors and open-drain outputs are software assignable. Pull-up resistors are automatically disabled for output pins. Configurable as LCD segments/ external interface address and data lines	H-32	72–79 (74-80, 1)	SEG16/A8 – SEG23/A15
P1.0–1.7	I/O	4-bit-programmable I/O port. Pull-up resistors and open-drain outputs are software assignable. Pull-up resistors are automatically disabled for output pins. Configurable as LCD segments/ external interface address and data lines	H-32	80, 1–7 (2-9)	SEG24/AD0 – SEG31/AD7
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6 P2.7	I/O	1-bit-programmable I/O port. Pull-up resistors are software assignable, and automatically disabled for output pins. P2.0–P2.3 can alternately be used as external interface lines. P2.4–P2.7 are configurable as alternate functions or external interrupts at falling edge with noise filters.	D-4	8 (10) 9 (11) 18 (20) 19 (21) 20 (22) 21 (23) 22 (24) 23 (25)	AS DR DW DM INT0/T0CK INT1/T1CK INT2/TA INT3/TB
P3.0–P3.3  P3.4–P3.6  P3.7	I/O	1-bit-programmable I/O port. Pull-up resistors are software assignable, and automatically disabled for output pins. P3.0–P3.3 can alternately be used as ADC. P3.7 is configurable as an alternate function.	F-16  D-4  D-4	25–28 (27–30)  30–32 (32–34)  33 (35)	ADC0–ADC3    T0/T0PWM/ T0CAP
P4.0–P4.7	I/O	1-bit-programmable I/O port. Pull-up resistors and open-drain outputs are software assignable. Pull-up resistors are automatically disabled for output pins. P4.0–P4.7 are configurable as external interrupts at a selectable edge with noise filters.	E-4	34–41 (36–43)	INT4–INT11
P5.0 P5.1 P5.2 P5.3 P5.4–P5.6	I/O	1-bit-programmable I/O port. Pull-up resistors are software assignable, and automatically disabled for output pins. P5.0–P5.3 are configurable as alternate functions. If SCK and SI are used as input, these pins have noise filters.	D-4	42 (44) 43 (45) 44 (46) 45 (47) 46–48 (48–50)	SCK SI SO BUZ

**NOTE:** Parentheses indicate pin number for 80-QFP package.

Table 1-1. S3C821A Pin Descriptions (Continued)

Pin Names	Pin Type	Pin Description	Circuit Type	Pin Numbers <sup>(note)</sup>	Share Pins
$V_{SS1}$ , $V_{DD1}$	–	Power input pins for internal power block	–	10, 11 (12, 13)	–
$X_{OUT}$ , $X_{IN}$	–	Main oscillator pins	–	12, 13 (14, 15)	–
TEST	–	Chip test input pin Hold GND when the device is operating	–	14 (16)	–
$XT_{IN}$ , $XT_{OUT}$	–	Sub oscillator pins for sub-system clock	–	15, 16 (17,18)	–
RESET	I	RESET signal input pin. Schmitt trigger input with internal pull-up resistor.	B	17 (19)	–
INT0–INT3	I/O	External interrupts input with noise filter.	D-4	20–23 (22–25)	P2.4–P2.7
T0CK	I/O	8Bit Timer 0 external clock input.	D-4	20 (22)	P2.4
T1CK	I/O	Timer 1/A external clock input.	D-4	21 (23)	P2.5
TA	I/O	Timer 1/A clock output	D-4	22 (24)	P2.6
TB	I/O	Timer B clock output	D-4	23 (25)	P2.7
T0	I/O	Timer 0 clock output	D-4	33 (35)	P3.7
T0PWM	I/O	Timer 0 PWM output	D-4	33 (35)	P3.7
T0CAP	I/O	Timer 0 capture input	D-4	33 (35)	P3.7
ADC0–ADC3	I/O	Analog input pins for A/D converts module	F-16	25–28 (27–30)	P3.0–P3.3
$AV_{REF}$ , $AV_{SS}$	–	A/D converter reference voltage and ground	–	24, 29 (26, 31)	–
INT4–INT11	I/O	External interrupts input with noise filter.	E-4	34–41 (36–43)	P4.0–P4.7
BUZ	I/O	Buzzer signal output	D-4	45 (47)	P5.3
SCK, SI, SO	I/O	Serial clock, serial data input, serial data output	D-4	42–44 (44–46)	P5.0–P5.2
$V_{LC1}$	–	LCD bias voltage input pins	–	49 (51)	–
$V_{SS2}$ , $V_{DD2}$	–	Power input pins for external power block	–	50, 51 (52, 53)	–
COM0–COM3	O	LCD Common signal output	H-30	52–55 (54–57)	–
SEG0–SEG3 (COM4–COM7)	O	LCD Common or Segment signal output	H-31	56–59 (58–61)	–
SEG4–SEG15	O	LCD segment signal output	H-29	60–71 (62–73)	–

**NOTE:** Parentheses indicate pin number for 80-QFP package.

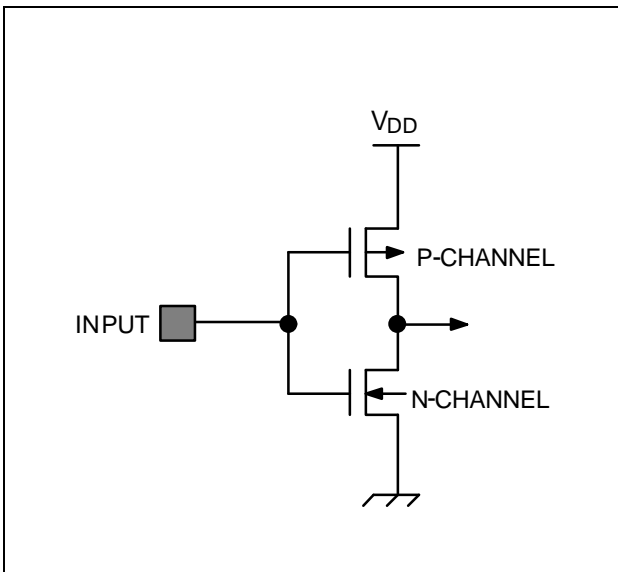
Table 1-1. S3C821A Pin Descriptions (Continued)

Pin Names	Pin Type	Pin Description	Circuit Type	Pin Numbers	Share Pins
SEG16–SEG23	I/O	LCD segment signal output	H-32	72–79 (74–80, 1)	P0.0–P0.7
SEG24–SEG31	I/O	LCD segment signal output	H-32	80, 1–7 (2–9)	P1.0–P1.7
A8–A15	I/O	External interface address lines	H-32	72–79 (74–80, 1)	P0.0–P0.7
AD0–AD7	I/O	External interface address/data lines	H-32	80, 1–7 (2–9)	P1.0–P1.7
AS	I/O	Address strobe	D-4	8 (10)	P2.0
DR	I/O	Data read	D-4	9 (11)	P2.1
DW	I/O	Data write	D-4	18 (20)	P2.2
DM	I/O	Data memory select	D-4	19 (21)	P2.3

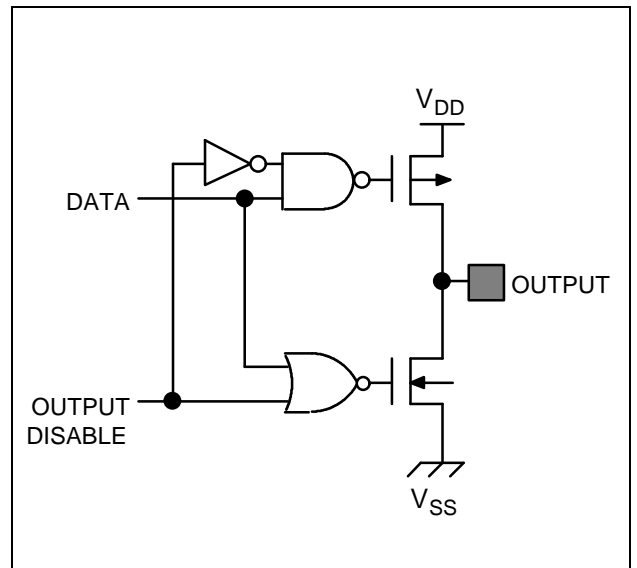
**NOTE:** Parentheses indicate pin number for 80-QFP package.



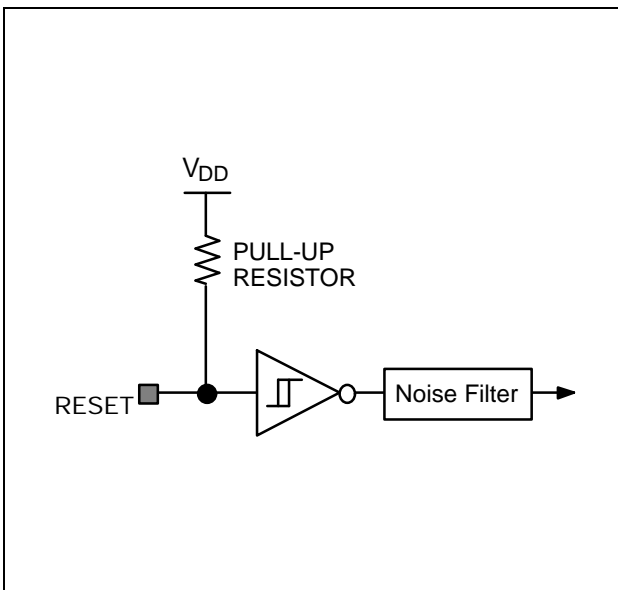
**PIN CIRCUITS**



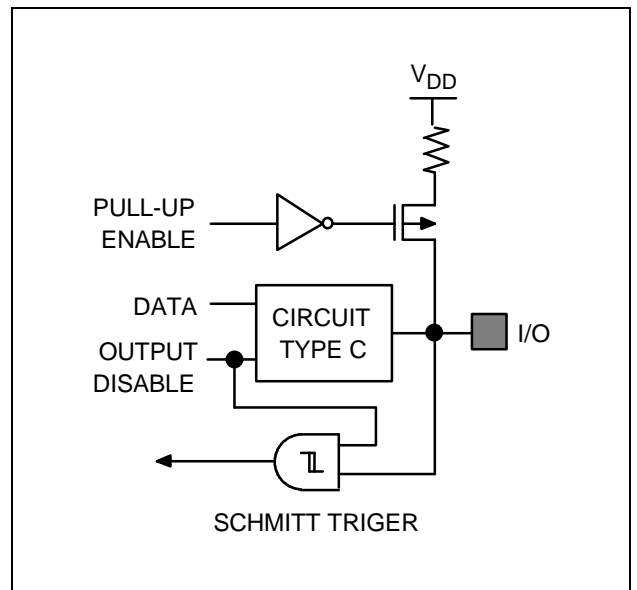
**Figure 1-4. Pin Circuit Type A**



**Figure 1-6. Pin Circuit Type C**



**Figure 1-5. Pin Circuit Type B**



**Figure 1-7. Pin Circuit Type D-4**

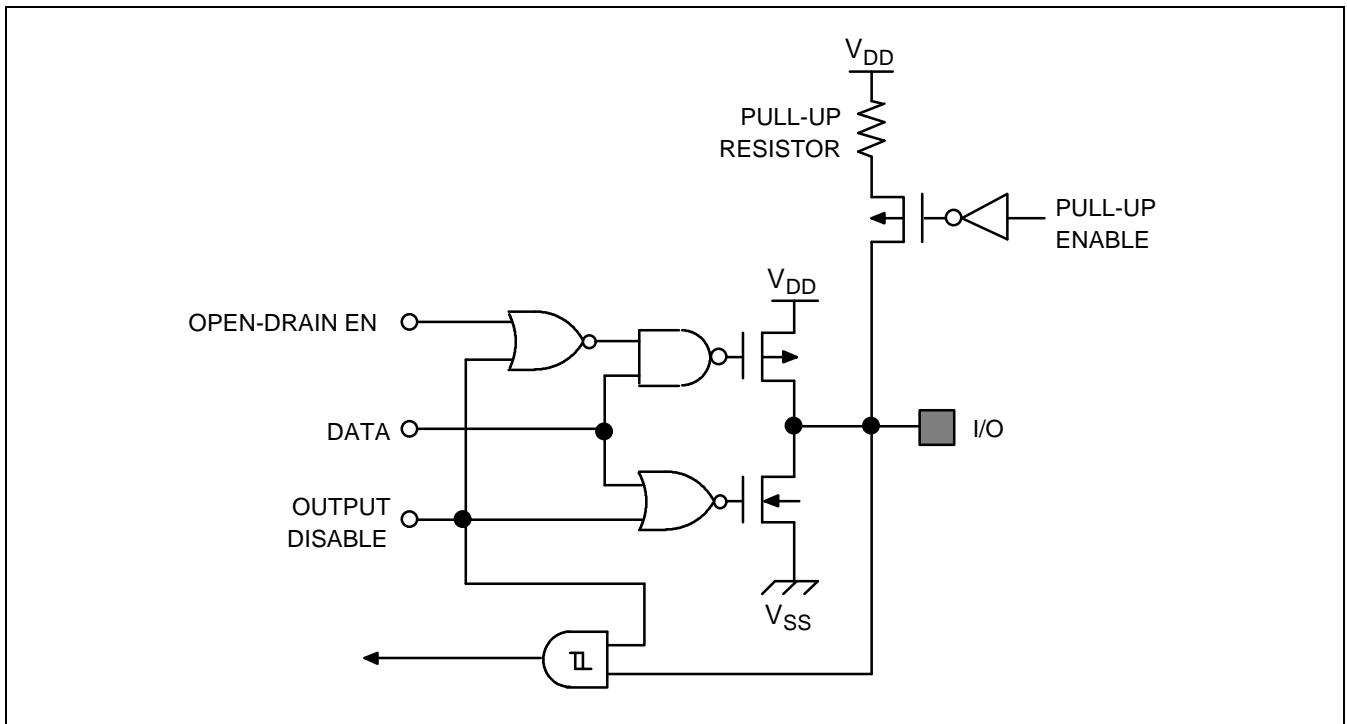


Figure 1-8. Pin Circuit Type E-4

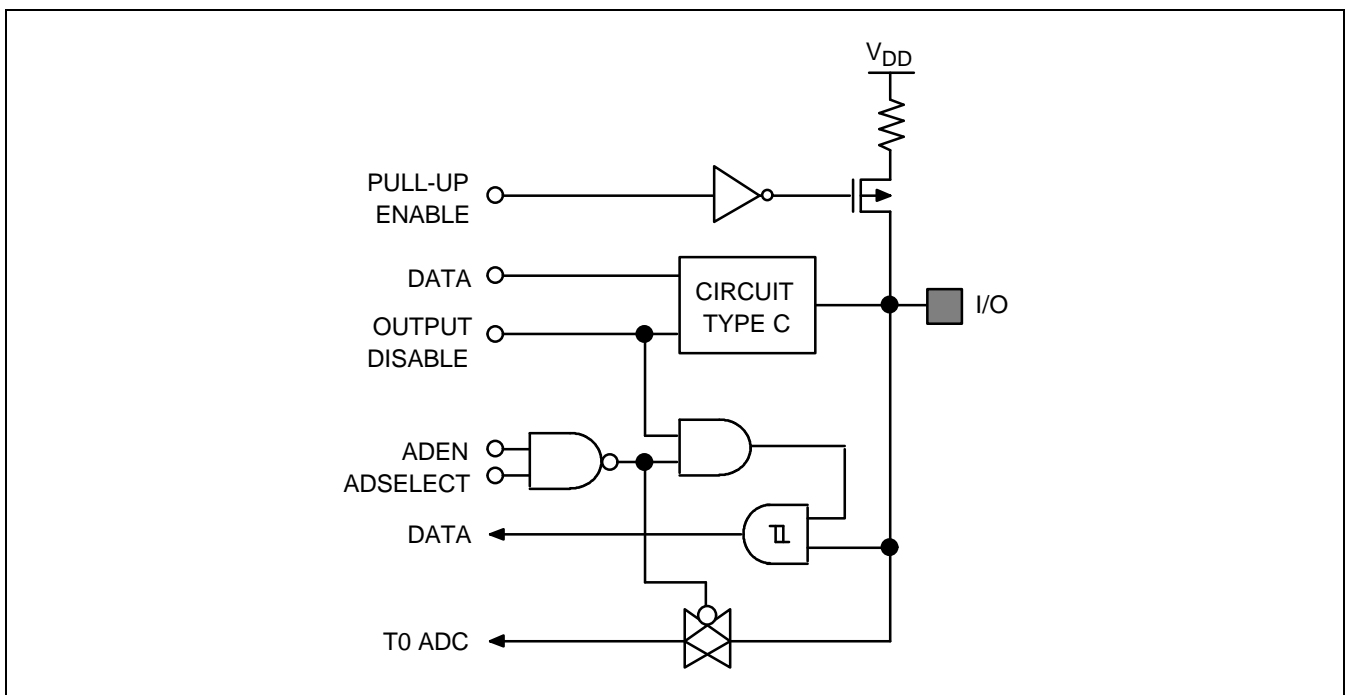


Figure 1-9. Pin Circuit Type F-16

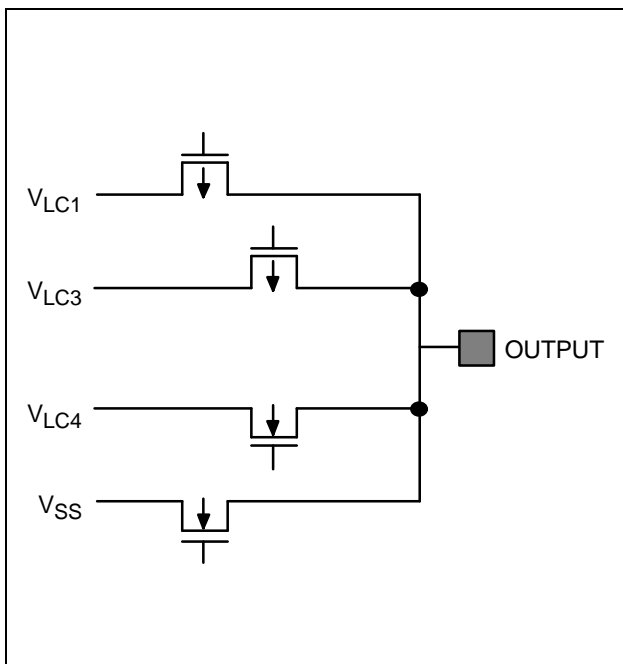


Figure 1-10. Pin Circuit Type H-29

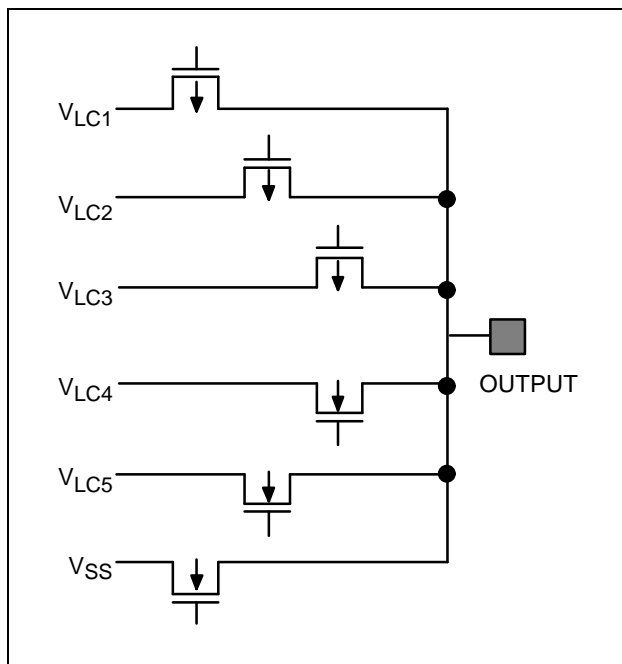


Figure 1-12. Pin Circuit Type H-31

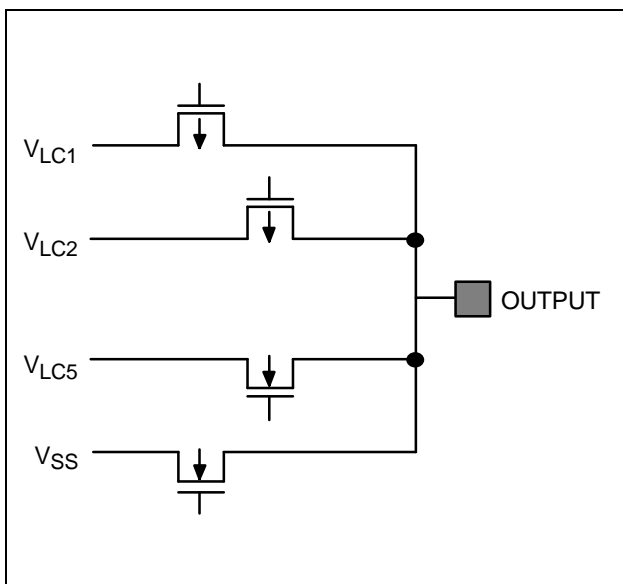


Figure 1-11. Pin Circuit Type H-30

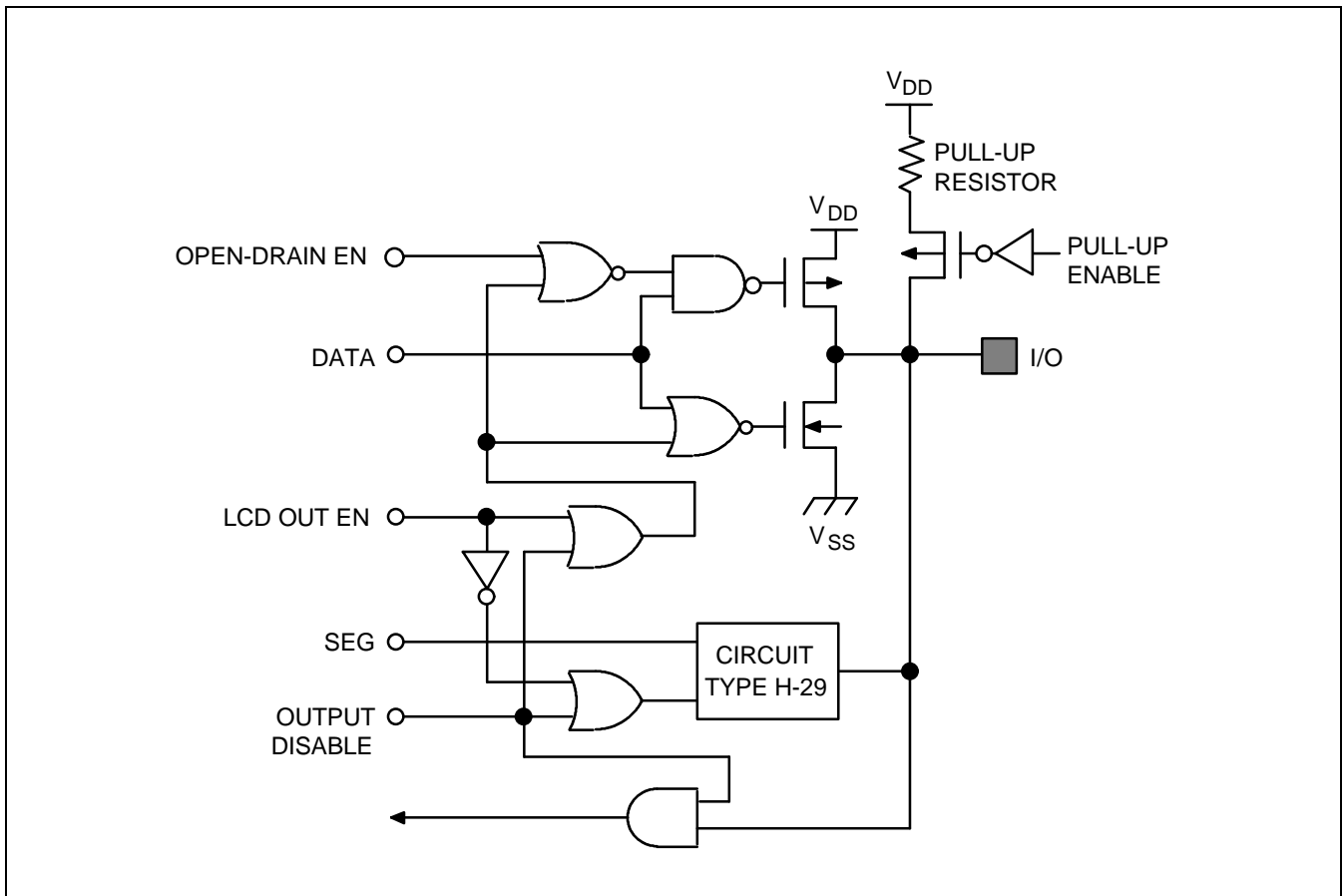


Figure 1-13. Pin Circuit Type H-32

# 17 ELECTRICAL DATA

## OVERVIEW

In this section, S3C821A electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

- Absolute maximum ratings
- D.C. electrical characteristics
- Data retention supply voltage in Stop mode
- Stop mode release timing when initiated by an external interrupt
- Stop mode release timing when initiated by a Reset
- I/O capacitance
- A.C. electrical characteristics
- A/D converter electrical characteristics
- Input timing for external interrupts (P4, P2.4–P2.7)
- Input timing for RESET
- Serial data transfer timing
- Oscillation characteristics
- Oscillation stabilization time
- Operating voltage range

Table 17-1. Absolute Maximum Ratings

 $(T_A = 25\text{ }^\circ\text{C})$ 

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	$V_{DD}$	–	– 0.3 to + 6.5	V
Input voltage	$V_{IN}$	All I/O ports	– 0.3 to $V_{DD} + 0.3$	V
Output voltage	$V_O$	–	– 0.3 to $V_{DD} + 0.3$	V
Output current High	$I_{OH}$	One I/O port active	– 18	mA
		All I/O ports active	– 60	
Output current Low	$I_{OL}$	One I/O port active	+ 30 (peak value)	mA
			+ 15 (note)	
		Ports 0, 1, 2, and 3	+ 100 (peak value)	
			+ 60 (note)	
		Ports 4 and 5	+ 100 (peak value)	
			+ 60 (note)	
Operating temperature	$T_A$	–	– 40 to + 85	$^\circ\text{C}$
Storage temperature	$T_{STG}$	–	– 65 to + 150	$^\circ\text{C}$

**NOTE:** The values for Output Current Low ( $I_{OL}$ ) are calculated as Peak Value  $\times \sqrt{\text{Duty}}$ .

Table 17-2. D.C. Electrical Characteristics

 $(T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C, } V_{DD} = 2.0\text{ V to } 5.5\text{ V})$ 

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	$V_{DD}$	$f_{OSC} = 8\text{ MHz}$ (Instruction clock = 1.33 MHz)	2.2	–	5.5	V
		$f_{OSC} = 6\text{ MHz}$ (Instruction clock = 1 MHz)	2.0			
Input High voltage	$V_{IH1}$	P0 and P1	$0.7 V_{DD}$	–	$V_{DD}$	V
	$V_{IH2}$	RESET, P2, P3, P4, and P5	$0.8 V_{DD}$		$V_{DD}$	
	$V_{IH3}$	$X_{IN}, XT_{IN}$	$V_{DD} - 0.1$		$V_{DD}$	
Input Low voltage	$V_{IL1}$	P0 and P1	0	–	$0.3 V_{DD}$	
	$V_{IL2}$	RESET, P2, P3, P4, and P5			$0.2 V_{DD}$	
	$V_{IL3}$	$X_{IN}, XT_{IN}$			0.1	
Output High voltage	$V_{OH}$	$V_{DD} = 3\text{ V}; I_{OH} = -200\text{ }\mu\text{A}$ All output pins	$V_{DD} - 1.0$	–	–	
Output Low voltage	$V_{OL}$	$V_{DD} = 3\text{ V}; I_{OL} = 1\text{ mA}$ All output pins	–	0.4	1.0	
Input High leakage current	$I_{LIH1}$	$V_{IN} = V_{DD}$ All input pins except those specified below for $I_{LIH2}$	–	–	1	$\mu\text{A}$
	$I_{LIH2}$	$V_{IN} = V_{DD}$ $X_{IN}, X_{OUT}, XT_{IN}, \text{ and } XT_{OUT}$			20	
Input Low leakage current	$I_{LIL1}$	$V_{IN} = 0\text{ V}$ All input pins except those specified below for $I_{LIL2}$ and RESET	–	–	–1	
	$I_{LIL2}$	$V_{IN} = 0\text{ V}$ $X_{IN}, X_{OUT}, XT_{IN}, \text{ and } XT_{OUT}$			–20	
Output High leakage current	$I_{LOH}$	$V_{OUT} = V_{DD}$ All output pins	–	–	1	
Output Low leakage current	$I_{LOL}$	$V_{OUT} = 0\text{ V}$ All output pins	–	–	–1	
$ V_{DD-COMi} $ voltage drop ( $i = 0-7$ )	$V_{DC}$	$V_{DD} = 2.7\text{ V to } 5.5\text{ V}$ – $15\text{ }\mu\text{A}$ per common pin	–	–	120	mV
$ V_{DD-SEGx} $ voltage drop ( $x = 0-31$ )	$V_{DS}$	$V_{LCD} = 2.7\text{ V to } 5.5\text{ V}$ – $15\text{ }\mu\text{A}$ per segment pin	–	–	120	

Table 17-2. D.C. Electrical Characteristics (Continued)

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit		
V <sub>LC2</sub> output voltage	V <sub>LC2</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V LCD clock = 0 Hz	0.8 V <sub>DD</sub> - 0.15	0.8 V <sub>DD</sub>	0.8 V <sub>DD</sub> + 0.15	V		
V <sub>LC3</sub> output voltage	V <sub>LC3</sub>	V <sub>LC1</sub> = V <sub>DD</sub>	0.6 V <sub>DD</sub> - 0.15	0.6 V <sub>DD</sub>	0.6 V <sub>DD</sub> + 0.15			
V <sub>LC4</sub> output voltage	V <sub>LC4</sub>		0.4 V <sub>DD</sub> - 0.15	0.4 V <sub>DD</sub>	0.4 V <sub>DD</sub> + 0.15			
V <sub>LC5</sub> output voltage	V <sub>LC5</sub>		0.2 V <sub>DD</sub> - 0.15	0.2 V <sub>DD</sub>	0.2 V <sub>DD</sub> + 0.15			
Pull-up resistors	R <sub>L1</sub>		V <sub>IN</sub> = 0 V; T <sub>A</sub> = 25 °C V <sub>DD</sub> = 3.0 ± 10 %; Ports 0-5	30	80		200	kΩ
	R <sub>L2</sub>	V <sub>IN</sub> = 0 V; T <sub>A</sub> = 25 °C V <sub>DD</sub> = 3.0 ± 10 % RESET only	200	450	800			
LCD voltage dividing resistor	R <sub>LCD</sub>	V <sub>LCD</sub> = 2.7 V to 5.5 V T <sub>A</sub> = 25 °C	45	65	80	kΩ		
Supply current (note)	I <sub>DD1</sub>	Run mode; V <sub>DD</sub> = 5.0 V ± 10 % Crystal oscillator C1 = C2 = 22 pF	6.0 MHz	-	6.0	12	mA	
			4.19 MHz		4.5	9.0		
		V <sub>DD</sub> = 3.0 V ± 10 %	6.0 MHz		2.9	5.8		
			4.19 MHz		2.0	4.0		
	I <sub>DD2</sub>	Idle mode; V <sub>DD</sub> = 5.0 V ± 0 % Crystal oscillator C1 = C2 = 22 pF	6.0 MHz		1.3	2.6		
			4.19 MHz		1.2	2.4		
		V <sub>DD</sub> = 3.0 V ± 10 %	6.0 MHz		0.6	1.2		
			4.19 MHz		0.4	0.8		
	I <sub>DD3</sub>	Run mode; V <sub>DD</sub> = 3.0 V ± 10 % 32 kHz crystal oscillator			20	40		μA
	I <sub>DD4</sub>	Idle mode; V <sub>DD</sub> = 3.0 V ± 10 % 32 kHz crystal oscillator			7	14		
I <sub>DD5</sub>	Stop mode; V <sub>DD</sub> = 5.0 V ± 10 %		0.5	3				
	Stop mode; V <sub>DD</sub> = 3.0 V ± 10 %		0.3	2				

**NOTES:**

- Supply current does not include current drawn through internal pull-up resistors, LCD voltage dividing resistors, and ADC.
- I<sub>DD1</sub> and I<sub>DD2</sub> include power consumption for subsystem clock oscillation.
- I<sub>DD3</sub> and I<sub>DD4</sub> are current when main system clock oscillation stops and the subsystem clock is used.
- I<sub>DD5</sub> is current when main system clock and subsystem clock oscillation stops.



Table 17-3. Data Retention Supply Voltage in Stop Mode

( $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	$V_{DDDR}$	–	2.2	–	3.4	V
Data retention supply current	$I_{DDDR}$	$V_{DDDR} = 1.0\text{ V}$ Stop mode	–	–	1	$\mu\text{A}$
Oscillator stabilization wait time	$t_{\text{WAIT}}$	Released by RESET	–	$2^{16}/f_x$ (1)	–	ms
		Released by interrupt	–	(2)	–	

**NOTES:**

1.  $f_x$  is the main oscillator frequency.
2. The duration of the oscillation stabilization time ( $t_{\text{WAIT}}$ ) when it is released by an interrupt is determined by the setting in the basic timer control register, BTCON.

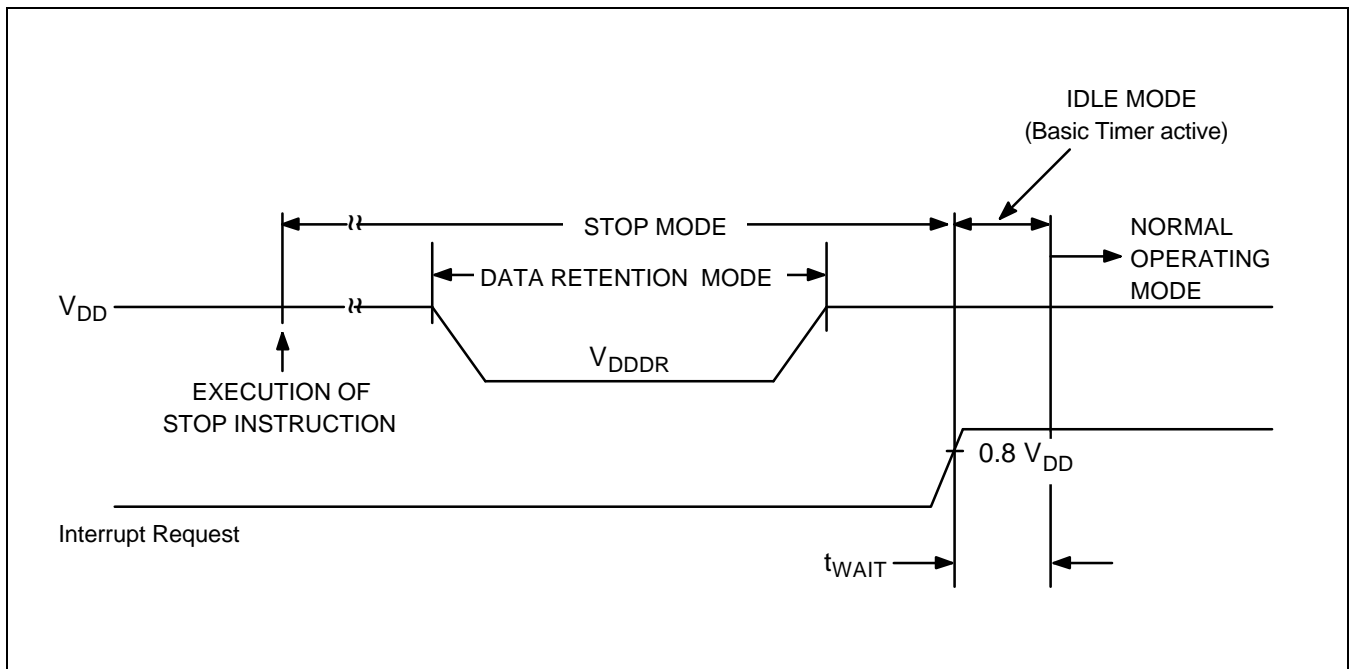


Figure 17-1. Stop Mode Release Timing When Initiated by an External Interrupt

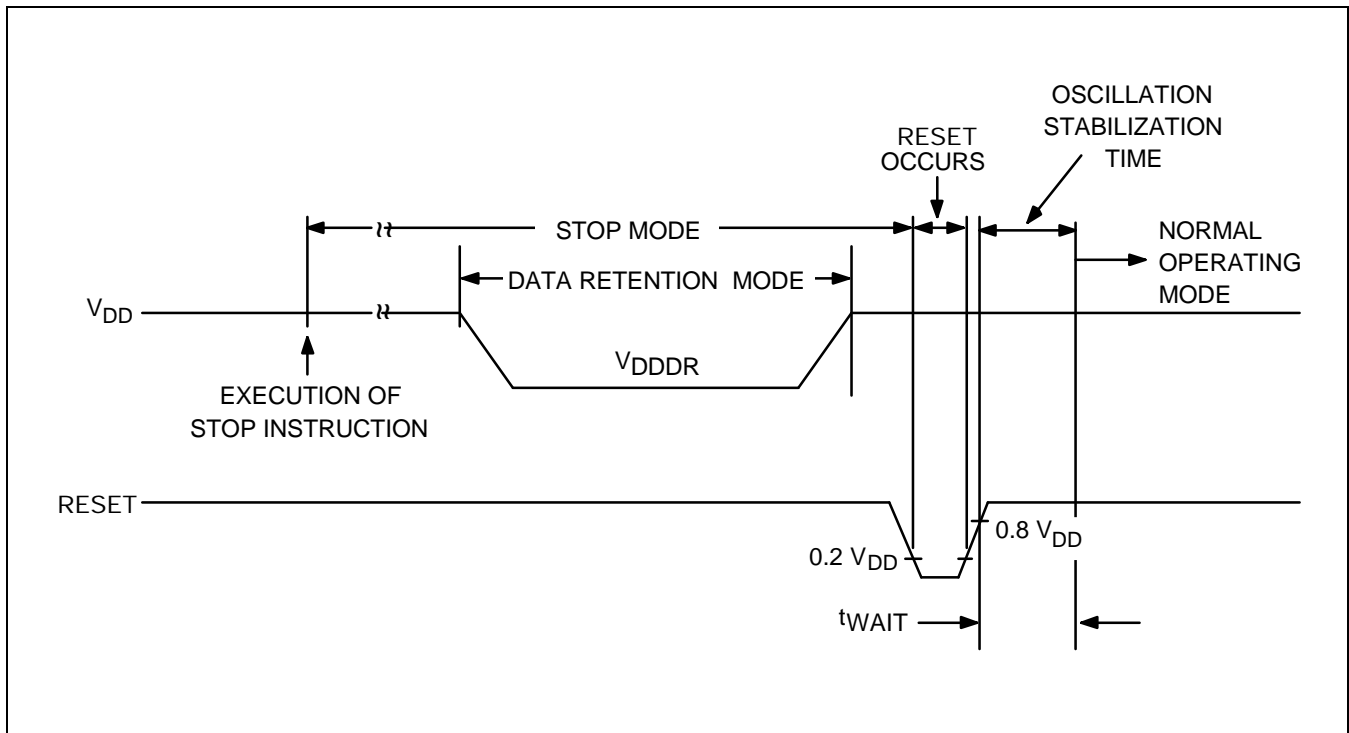


Figure 17-2. Stop Mode Release Timing When Initiated by a RESET

Table 17-4. Input/output Capacitance

(T<sub>A</sub> = -25 °C, V<sub>DD</sub> = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C <sub>IN</sub>	f = 1 MHz; unmeasured pins are connected to V <sub>SS</sub>	-	-	10	pF
Output capacitance	C <sub>OUT</sub>					
I/O capacitance	C <sub>IO</sub>					

Table 17-5. A.C. Electrical Characteristics

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SCK cycle time	t <sub>KCY</sub>	External SCK source	1,000	-	-	ns
		Internal SCK source	1,000			
SCK high, low width	t <sub>KH</sub> , t <sub>KL</sub>	External SCK source	500	-	-	-
		Internal SCK source	t <sub>KCY</sub> /2-50			
SI setup time to SCK high	t <sub>SIK</sub>	External SCK source	250	-	-	-
		Internal SCK source	250			
SI hold time to SCK high	t <sub>KSI</sub>	External SCK source	400	-	-	-
		Internal SCK source	400			
Output delay for SCK to SO	t <sub>KSO</sub>	External SCK source	-	-	300	ns
		Internal SCK source			250	
Interrupt input, high, low width	t <sub>INTH</sub> , t <sub>INTL</sub>	All interrupt V <sub>DD</sub> = 3 V	500	700	-	ns
RESET input low width	t <sub>RSL</sub>	Input V <sub>DD</sub> = 3 V	2,000	-	-	

Table 17-6. A/D Converter Electrical Characteristics

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution			–	8	–	bit
Total accuracy		V <sub>DD</sub> = 5.12 V AV <sub>REF</sub> = 5.12 V AV <sub>SS</sub> = 0 V	–	–	± 2	LSB
Conversion time <sup>(1)</sup>	t <sub>CON</sub>	8 bit conversion 34 x n/f <sub>XX</sub> <sup>(2)</sup> , n=1,4,8,16	17	–	170	μs
Analog input voltage	V <sub>IAN</sub>	–	AV <sub>SS</sub>	–	AV <sub>REF</sub>	V
Analog input impedance	R <sub>AN</sub>	–	2	1,000	–	MΩ
Analog reference voltage	AV <sub>REF</sub>	–	2.5	–	V <sub>DD</sub>	V
Analog ground	AV <sub>SS</sub>	–	V <sub>SS</sub>	–	V <sub>SS</sub> + 0.3	V
Analog input current	I <sub>ADIN</sub>	AV <sub>REF</sub> = V <sub>DD</sub> = 5V	–	–	10	μA

**NOTES:**

- "Conversion time" is the time required from the moment a conversion operation starts until it ends.
- f<sub>XX</sub> is a selected system clock for peripheral hardware.

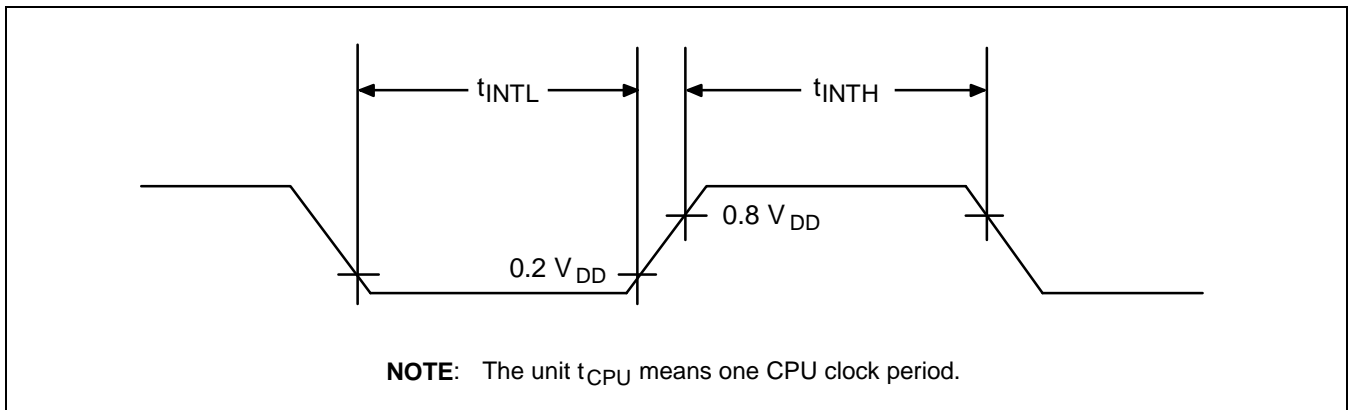


Figure 17-3. Input Timing for External Interrupts

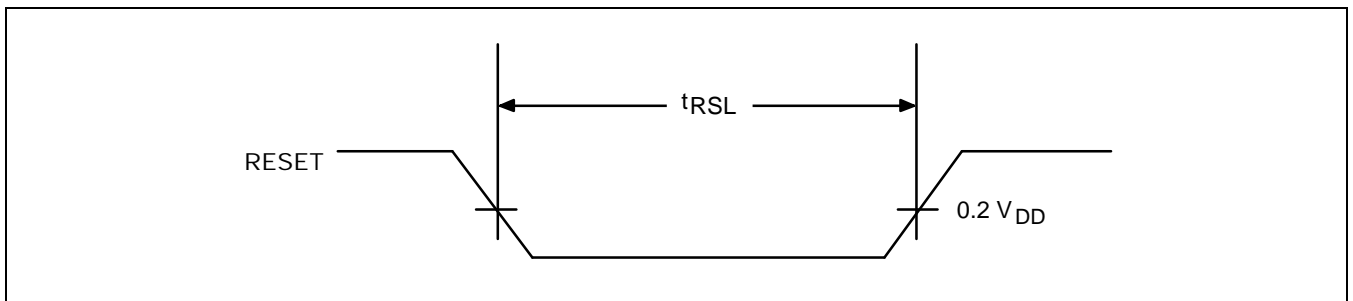


Figure 17-4. Input Timing for RESET

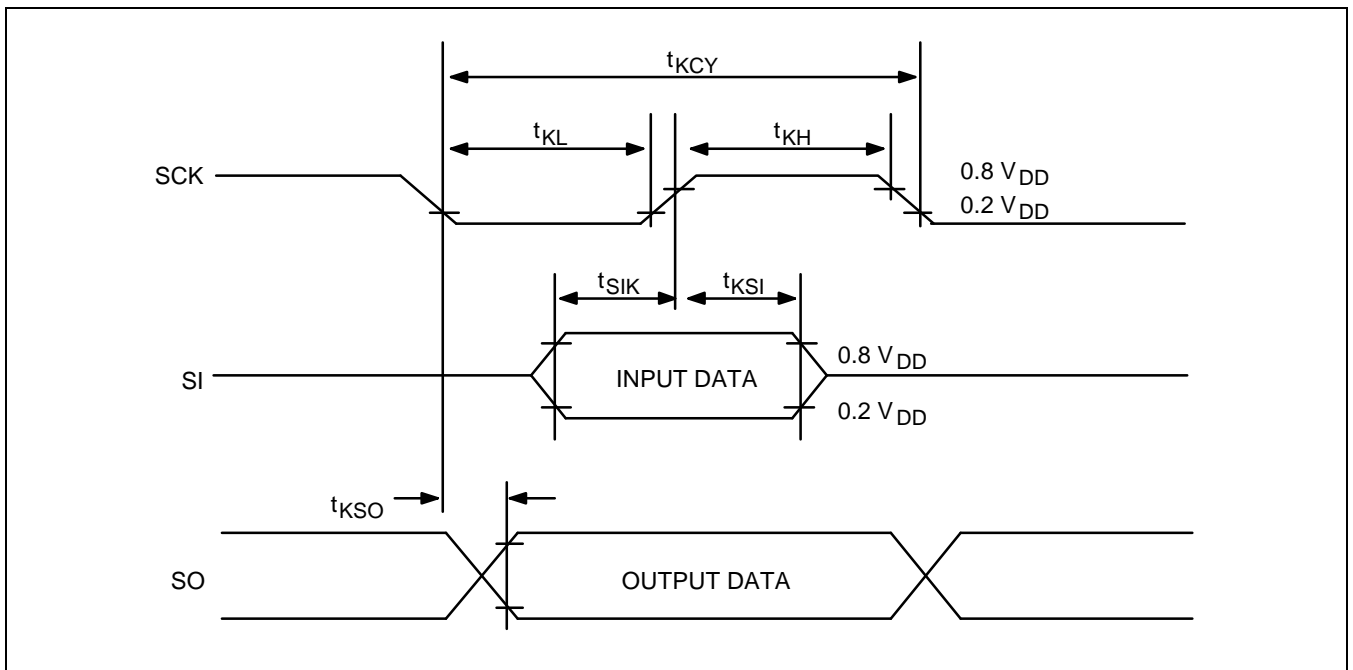


Figure 17-5. Serial Data Transfer Timing

Table 17-7. Main System Oscillation Characteristics

 $(T_A = -40\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C})$ 

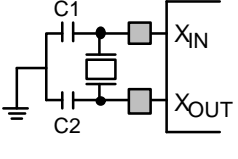
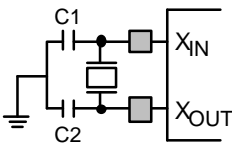
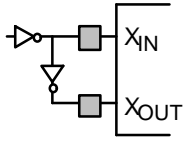
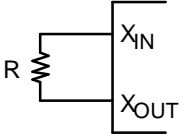
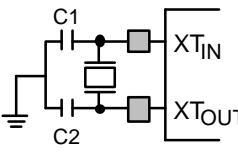
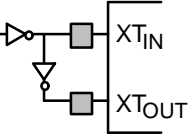
Oscillator	Clock Circuit	Parameter	Condition ( $V_{DD}$ )	Min	Typ	Max	Unit
Crystal		Main oscillation frequency	2.2 V–5.5 V	0.4	–	8	MHz
			2.0 V–5.5 V	0.4	–	6	
Ceramic		Main oscillation frequency	2.2 V–5.5 V	0.4	–	8	
			2.0 V–5.5 V	0.4	–	6	
External clock		$X_{1IN}$ input frequency	2.2 V–5.5 V	0.4	–	8	
			2.0 V–5.5 V	0.4	–	6	
RC		Frequency	3.0 V	0.4	–	2	

Table 17-8. Subsystem Oscillation Characteristics

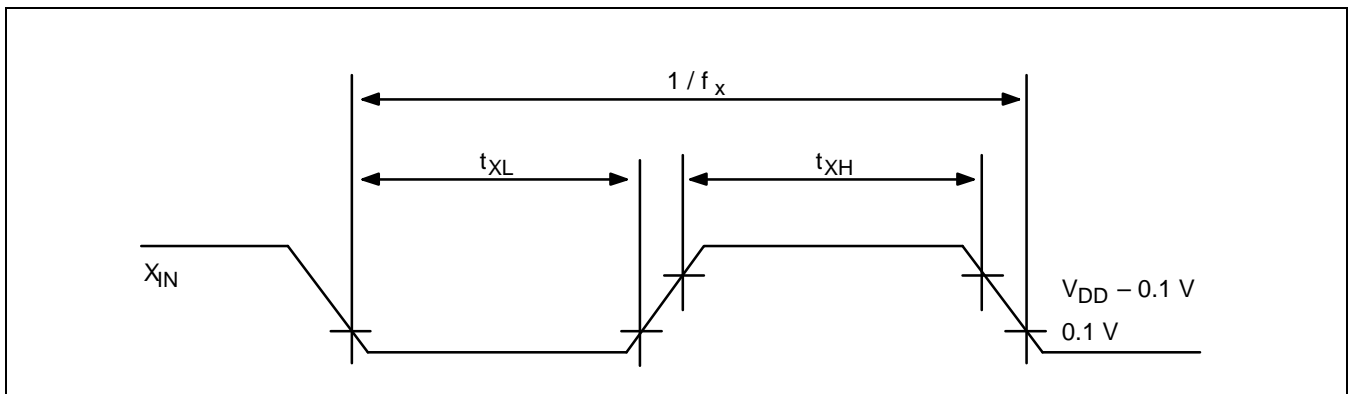
 $(T_A = -40\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C})$ 

Oscillator	Clock Circuit	Parameter	Condition ( $V_{DD}$ )	Min	Typ	Max	Unit
Crystal		Sub oscillation frequency	2.0 V–5.5 V	32	32.768	35	kHz
External clock		$XT_{1IN}$ input frequency	2.0 V–5.5 V	32	–	500	kHz

**Table 17-9. Main Oscillation Stabilization Time**

( $T_A = -40\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 2.0\text{ V to } 5.5\text{ V}$ )

Oscillator	Test Condition	Min	Typ	Max	Unit
Crystal	$f_x > 400\text{ kHz}$	–	–	20	ms
Ceramic	Oscillation stabilization occurs when $V_{DD}$ is equal to the minimum oscillator voltage range.	–	–	10	ms
External clock	$X_{IN}$ input High and Low width ( $t_{XH}$ , $t_{XL}$ )	25	–	500	ns

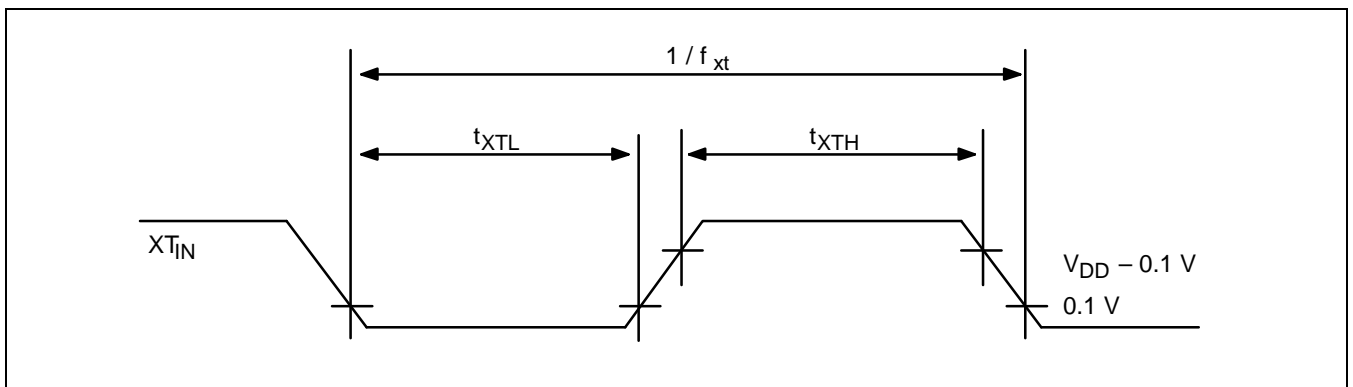


**Figure 17-6. Clock Timing Measurement at  $X_{IN}$**

**Table 17-10. Sub Oscillation Stabilization Time**

( $T_A = -40\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C}$ ,  $V_{DD} = 2.0\text{ V to } 5.5\text{ V}$ )

Oscillator	Test Condition	Min	Typ	Max	Unit
Crystal	–	–	–	10	s
External clock	$XT_{IN}$ input High and Low width ( $t_{XTH}$ , $t_{XTL}$ )	1	–	18	$\mu\text{s}$



**Figure 17-7. Clock Timing Measurement at  $XT_{IN}$**

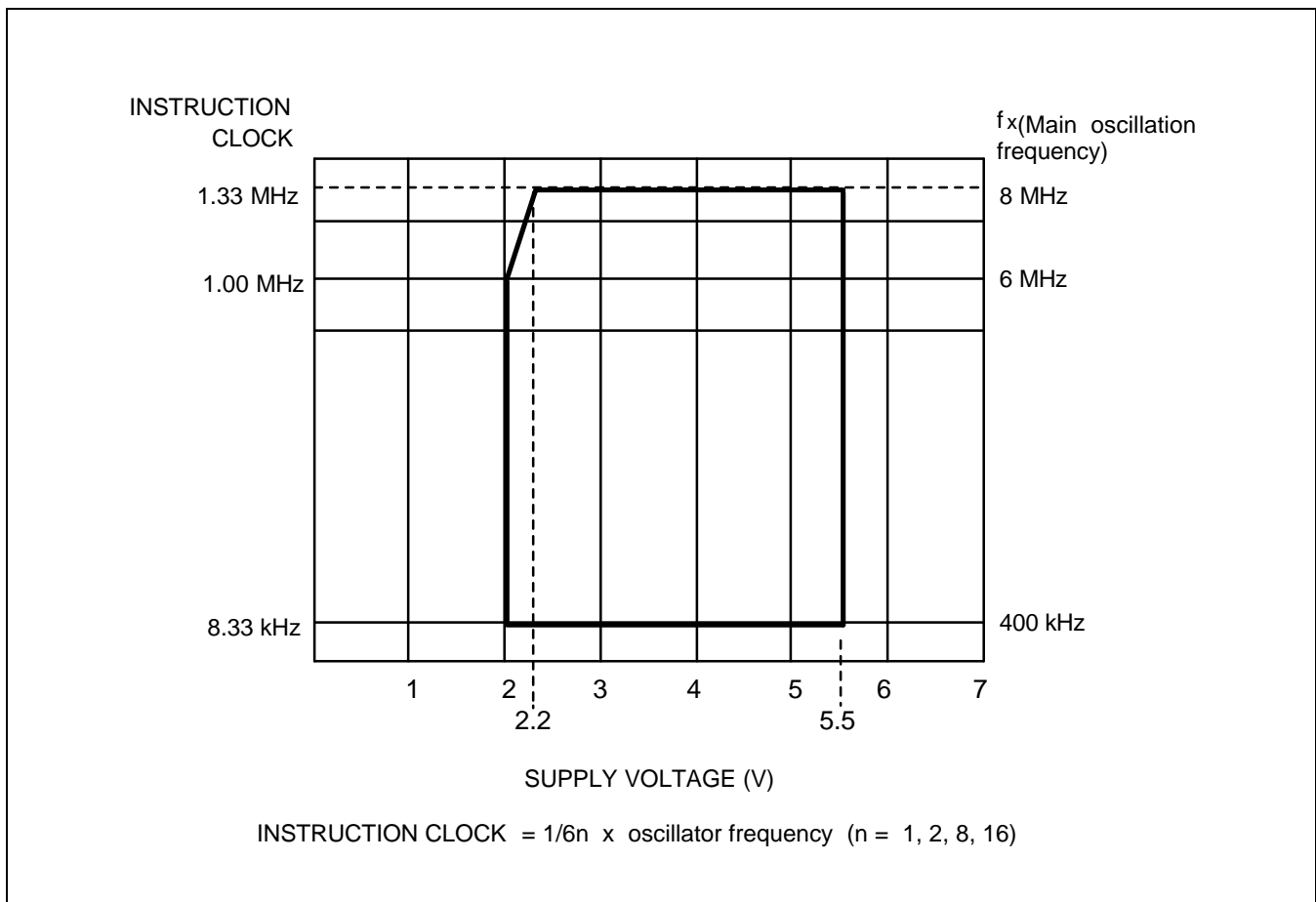


Figure 17-8. Operating Voltage Range



# 18 MECHANICAL DATA

## OVERVIEW

The S3C821A microcontroller is currently available in 80-pin QFP and TQFP package.

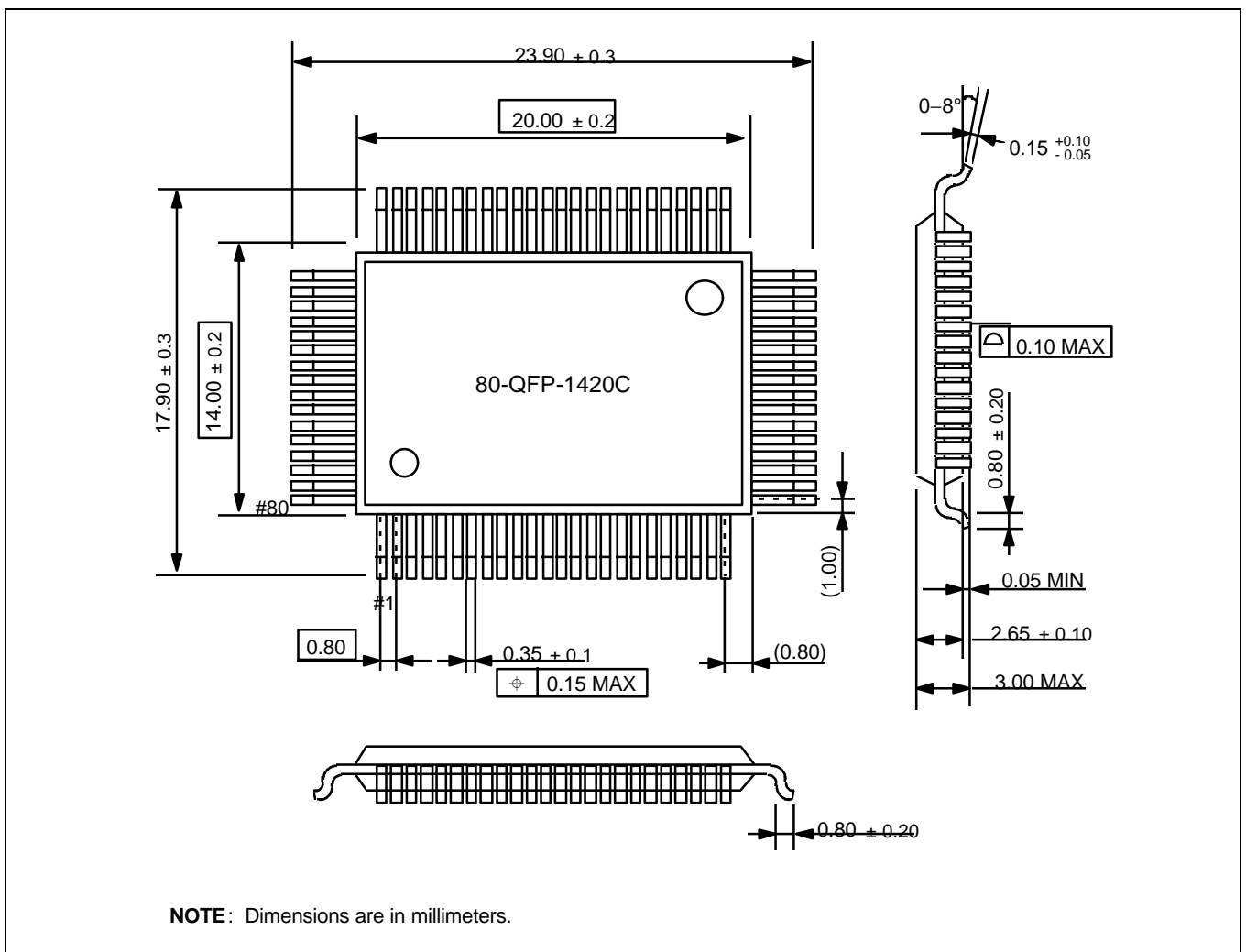


Figure 18-1. 80-Pin QFP Package Dimensions

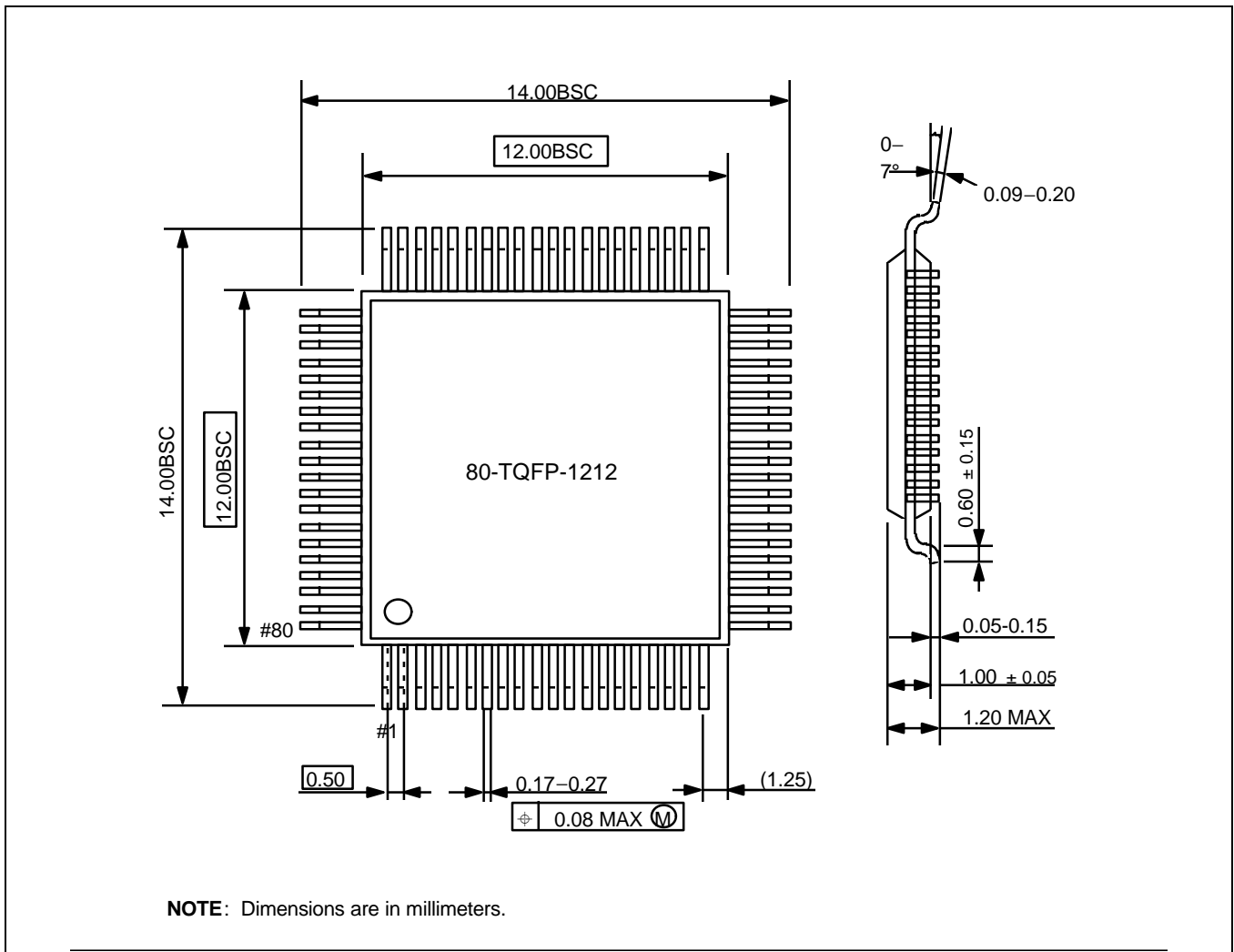


Figure 18-2. 80-Pin TQFP Package Dimensions

# 20

## S3P821A OTP

### OVERVIEW

The S3P821A single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C821A microcontroller. It has an on-chip OTP ROM instead of a masked ROM. The EPROM is accessed by serial data format.

The S3P821A is fully compatible with the S3C821A, both in function and in pin configuration. Because of its simple programming requirements, the S3P821A is ideal as an evaluation chip for the S3C821A.

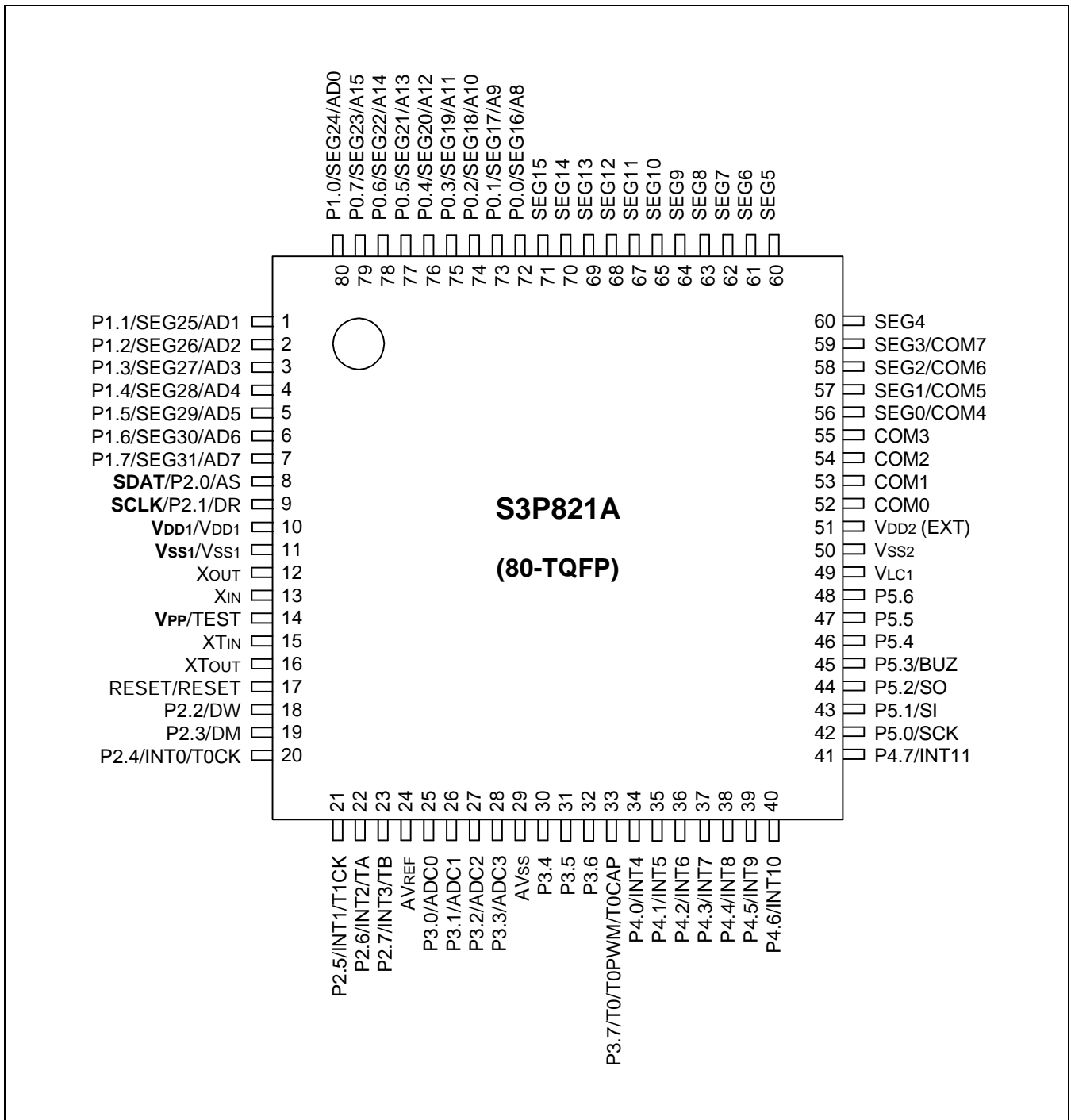


Figure 20-1. S3P821A Pin Assignments (80-TQFP-1212 Package)

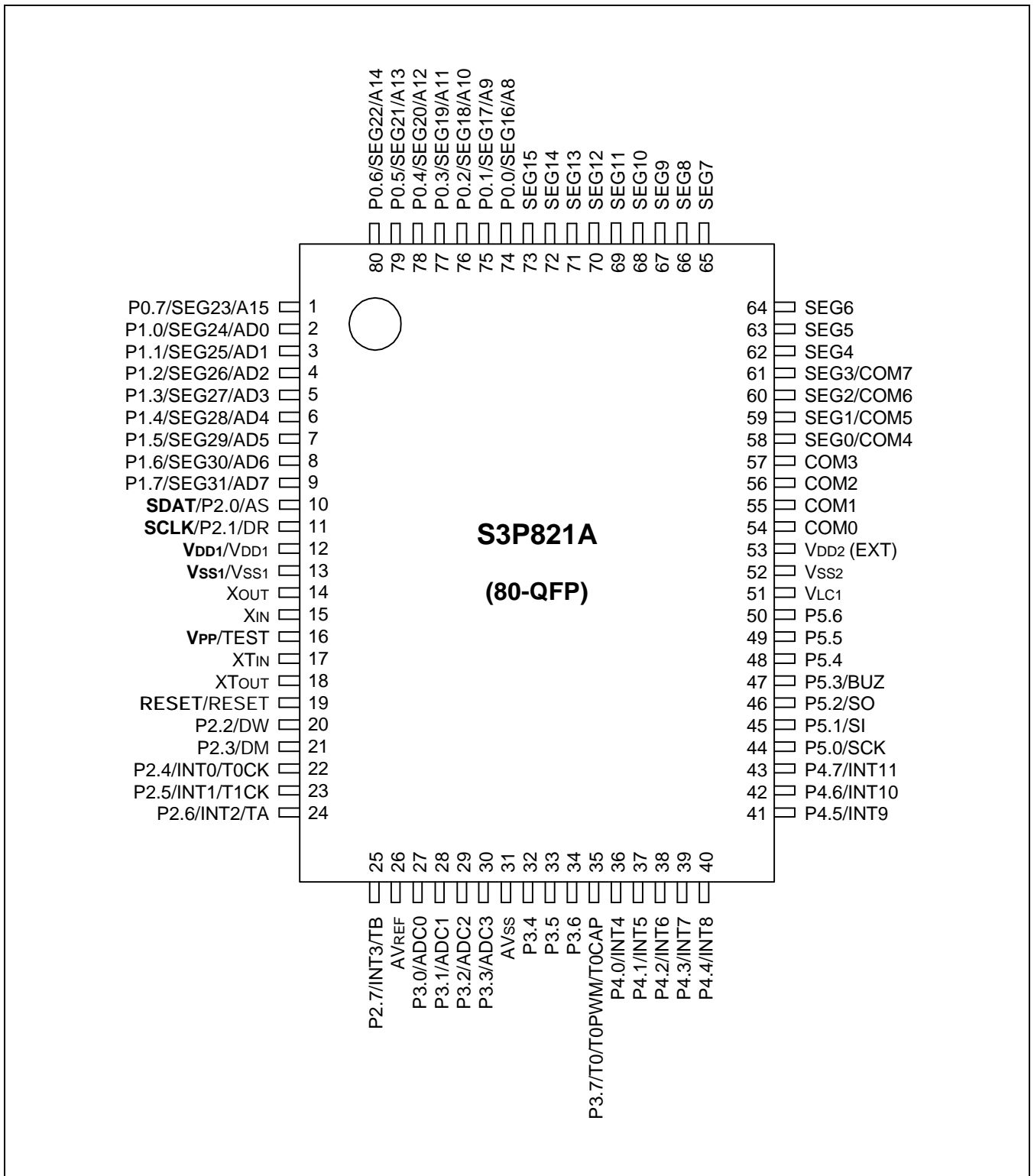


Figure 20-2. S3P821A Pin Assignments (80-QFP-1420C Package)

Table 20-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P2.0	SDAT	8 (10)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P2.1	SCLK	9 (11)	I/O	Serial clock pin. Input only pin.
V <sub>PP</sub>	TEST	14 (16)	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	17 (19)	I	Chip Initialization
V <sub>DD1</sub> /V <sub>SS1</sub>	V <sub>DD1</sub> /V <sub>SS1</sub>	10 (12)/11 (13)	–	Logic power supply pin. V <sub>DD</sub> should be tied to + 5 V during programming.

NOTE: ( ) means 80 QFP package.

Table 20-2. Comparison of S3P821A and S3C821A Features

Characteristic	S3P821A	S3C821A
Program Memory	48-K byte EPROM	48-K byte mask ROM
Operating Voltage (V <sub>DD</sub> )	2.0 V to 5.5 V	2.0 V to 5.5 V
OTP Programming Mode	V <sub>DD</sub> = 5 V, V <sub>PP</sub> (TEST) = 12.5 V	
Pin Configuration	80 QFP/80 TQFP	80 QFP/80 TQFP
EPROM Programmability	User Program 1 time	Programmed at the factory

### OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V<sub>PP</sub> (TEST) pin of the S3P821A, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 20-3 below.

Table 20-3. Operating Mode Selection Criteria

V <sub>DD</sub>	V <sub>PP</sub> (TEST)	REG/ MEM	ADDRESS (A15–A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

Table 20-4. D.C. Electrical Characteristics

(T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V <sub>DD</sub>	f <sub>OSC</sub> = 8 MHz (Instruction clock = 1.33 MHz)	2.2	–	5.5	V
		f <sub>OSC</sub> = 6 MHz (Instruction clock = 1 MHz)	2.0			
Input High voltage	V <sub>IH1</sub>	P0 and P1	0.7 V <sub>DD</sub>	–	V <sub>DD</sub>	V
	V <sub>IH2</sub>	RESET, P2, P3, P4, and P5	0.8 V <sub>DD</sub>		V <sub>DD</sub>	
	V <sub>IH3</sub>	X <sub>IN</sub> , XT <sub>IN</sub>	V <sub>DD</sub> - 0.1		V <sub>DD</sub>	
Input Low voltage	V <sub>IL1</sub>	P0 and P1	0	–	0.3 V <sub>DD</sub>	
	V <sub>IL2</sub>	RESET, P2, P3, P4, and P5			0.2 V <sub>DD</sub>	
	V <sub>IL3</sub>	X <sub>IN</sub> , XT <sub>IN</sub>			0.1	
Output High voltage	V <sub>OH</sub>	V <sub>DD</sub> = 3 V; I <sub>OH</sub> = -200 μA All output pins	V <sub>DD</sub> - 1.0	–	–	
Output Low voltage	V <sub>OL</sub>	V <sub>DD</sub> = 3 V; I <sub>OL</sub> = 1 mA All output pins	–	0.4	1.0	
Input High leakage current	I <sub>LIH1</sub>	V <sub>IN</sub> = V <sub>DD</sub> All input pins except those specified below for I <sub>LIH2</sub>	–	–	1	μA
	I <sub>LIH2</sub>	V <sub>IN</sub> = V <sub>DD</sub> X <sub>IN</sub> , X <sub>OUT</sub> , XT <sub>IN</sub> , and XT <sub>OUT</sub>			20	
Input Low leakage current	I <sub>LIL1</sub>	V <sub>IN</sub> = 0 V All input pins except those specified below for I <sub>LIL2</sub> and RESET	–	–	-1	
	I <sub>LIL2</sub>	V <sub>IN</sub> = 0 V X <sub>IN</sub> , X <sub>OUT</sub> , XT <sub>IN</sub> , and XT <sub>OUT</sub>			-20	
Output High leakage current	I <sub>LOH</sub>	V <sub>OUT</sub> = V <sub>DD</sub> All output pins	–	–	1	
Output Low leakage current	I <sub>LOL</sub>	V <sub>OUT</sub> = 0 V All output pins	–	–	-1	
V <sub>DD-COMi</sub>   voltage drop (i = 0-7)	V <sub>DC</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V – 15 μA per common pin	–	–	120	mV
V <sub>DD-SEGx</sub>   voltage drop (x = 0-31)	V <sub>DS</sub>	V <sub>LCD</sub> = 2.7 V to 5.5 V – 15 μA per segment pin	–	–	120	

Table 20-4. D.C. Electrical Characteristics (Continued)

 $(T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}, V_{DD} = 2.0\text{ V to } 5.5\text{ V})$ 

Parameter	Symbol	Conditions	Min	Typ	Max	Unit		
V <sub>LC2</sub> output voltage	V <sub>LC2</sub>	V <sub>DD</sub> = 2.7 V to 5.5 V LCD clock = 0 Hz V <sub>LC1</sub> = V <sub>DD</sub>	0.8 V <sub>DD</sub> – 0.15	0.8 V <sub>DD</sub>	0.8 V <sub>DD</sub> + 0.15	V		
V <sub>LC3</sub> output voltage	V <sub>LC3</sub>		0.6 V <sub>DD</sub> – 0.15	0.6 V <sub>DD</sub>	0.6 V <sub>DD</sub> + 0.15			
V <sub>LC4</sub> output voltage	V <sub>LC4</sub>		0.4 V <sub>DD</sub> – 0.15	0.4 V <sub>DD</sub>	0.4 V <sub>DD</sub> + 0.15			
V <sub>LC5</sub> output voltage	V <sub>LC5</sub>		0.2 V <sub>DD</sub> – 0.15	0.2 V <sub>DD</sub>	0.2 V <sub>DD</sub> + 0.15			
Pull-up resistors	R <sub>L1</sub>	V <sub>IN</sub> = 0 V; T <sub>A</sub> = 25 °C V <sub>DD</sub> = 3.0 ± 10%; Ports 0–5	30	80	200	kΩ		
	R <sub>L2</sub>	V <sub>IN</sub> = 0 V; T <sub>A</sub> = 25 °C V <sub>DD</sub> = 3.0 ± 10 % RESET only	300	500	800			
LCD voltage dividing resistor	R <sub>LCD</sub>	V <sub>LCD</sub> = 2.7 V to 5.5 V T <sub>A</sub> = 25 °C	45	65	80	kΩ		
Supply current (note)	I <sub>DD1</sub>	Run mode; V <sub>DD</sub> =5.0V±10% Crystal oscillator C1 = C2 = 22 pF	6.0 MHz	–	6.0	12	mA	
			4.19 MHz		4.5	9.0		
		V <sub>DD</sub> = 3.0 V ± 10 %	6.0 MHz		2.9	5.8		
			4.19 MHz		2.0	4.0		
	I <sub>DD2</sub>	Idle mode; V <sub>DD</sub> =5.0 V± 0% Crystal oscillator C1 = C2 = 22 pF	6.0 MHz		1.3	2.6		
			4.19 MHz		1.2	2.4		
		V <sub>DD</sub> = 3.0 V ± 10 %	6.0 MHz		0.6	1.2		
			4.19 MHz		0.4	0.8		
	I <sub>DD3</sub>	Run mode; V <sub>DD</sub> = 3.0 V ± 10 % 32 kHz crystal oscillator			20	40		μA
	I <sub>DD4</sub>	Idle mode; V <sub>DD</sub> = 3.0 V ± 10 % 32 kHz crystal oscillator			7	14		
I <sub>DD5</sub>	Stop mode; V <sub>DD</sub> = 5.0 V ± 10 %		0.5	3				
	Stop mode; V <sub>DD</sub> = 3.0 V ± 10 %		0.3	2				

**NOTES:**

- Supply current does not include current drawn through internal pull-up resistors, LCD voltage dividing resistors, and ADC.
- I<sub>DD1</sub> and I<sub>DD2</sub> include power consumption for subsystem clock oscillation.
- I<sub>DD3</sub> and I<sub>DD4</sub> are current when main system clock oscillation stops and the subsystem clock is used.
- I<sub>DD5</sub> is current when main system clock and subsystem clock oscillation stops.



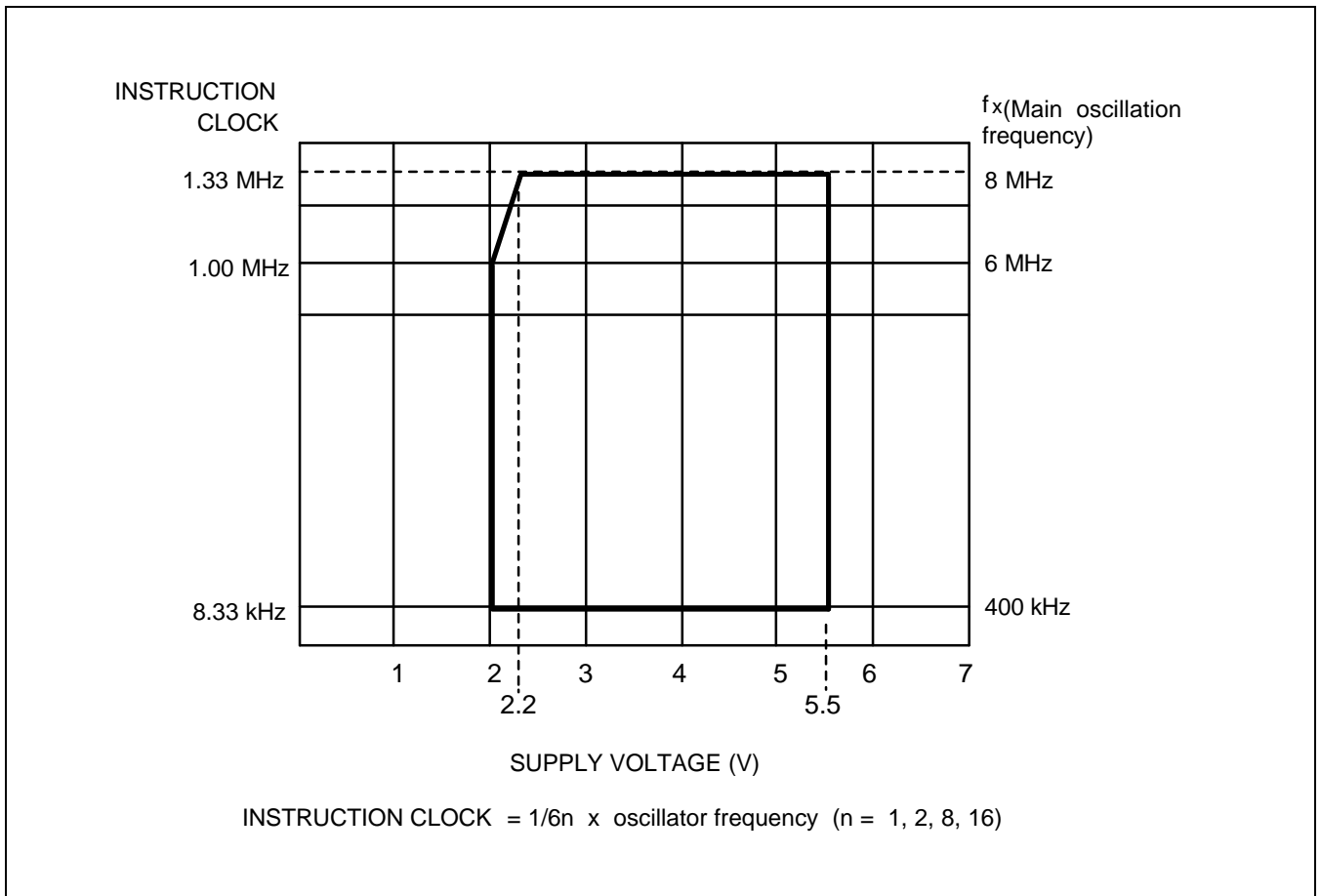


Figure 20-3. Operating Voltage Range