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STDL80

0.5μm 3.3V Standard Cell Library

April 1997

SAMSUNG

SAMSUNG ASIC

STDL80
0.5μm 3.3V Standard Cell Library
Data Book

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Introduction

This databook contains information about STDL80, 0.5 μm 3.3V DLM/TLM standard cell library developed by SEC (Samsung Electronics Corporation).

The “library” basically contains various kinds of internal and I/O cells and soft-macros which are used for developing ASIC (Application Specific Integrated Circuit). It also includes a design kit helping designers to work in a workstation platform, and all sorts of design environments needed for an automatic chip design.

There are seven chapters in this databook:

In this databook each cell is followed by its AC electrical characteristics, and these characteristic values are almost equal when the corresponding cell is operated in a real chip.

The purpose of this databook is to prevent any misuse or misapplication of STDL80 cell library by providing precise information about the cell list, electrical data, directions for use, and matters demanding special attention.

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Introduction to STDL80 1

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LIBRARY DESCRIPTION

STDL80 is a 0.5µm 3.3V CMOS standard cell library supporting double-layer or triple-layer metal interconnection options. This process is optimized for a 3.3V operation. Because of a process optimization for 3.3V, there are some limitations on the interface with 5V. Therefore, SEC supports 5V tolerant I/O which can receive 5V signal but cannot drive 5 volt as output voltage.

Various kinds of macrofunctions, megafunctions, memory compilers, datapath compilers may satisfy the complicated design requirements for your convenience.

Moreover, core & megafunction cells such as MPU and DSP, and analog cells are under development.

We ensure the product reliability by preventing any possible noise, ESD and latch-up efficiently.

Every work operation in a design flow has been systematized and automated, and each stage is designed to go through enough reviews and verifications. It makes the design work easier and faster, and prevents any errors or mistakes possible through a design flow.

FEATURES

- ❑ 3.3V standard cell library
- ❑ 5V tolerant I/O
- ❑ 0.5µm 3.3V HCMOS technology
  – Double and Triple layer metal options
- ❑ High basic cell usages
  – Up to 700,000 total number of gates
  – Maximum usage: 70% for triple layer metal
  – Maximum usage: 40% for double layer metal
- ❑ High speed
  – 0.2 ns delay of 2-input NAND with fanout = 2
- ❑ Fully configurable RAM,ROM and DPRAM
  – Up to 512K-bit ROM available
  – Up to 128K-bit RAM available
  – Up to 64K-bit DPRAM available
- ❑ Configurable Datapath elements available
  – 4 ~ 128-bit bus width
- ❑ Operating Temperature (T_A)
  – Commercial range: 0˚C to +70˚C
  – Industrial range: –40˚C to +85˚C
- ❑ ESD and latch-up protection
  – ESD: 2000V (Min.)
  – Latch-up: 300mA (Min.)
- ❑ Selectable output current drive capability
  – 1/2/4/8/12/16/20/24mA available
- ❑ TTL, CMOS, LVTTL, LVCMOS and Schmitt trigger I/Os
- ❑ X-tal oscillators
- ❑ PCI buffers
- ❑ GTL, NTL, CardBus, PECL, USB under-developed
- ❑ Various package options
- ❑ Fully integrated CAD software support
  – Verilog, Viewlogic, Mentor and Synopsys

CAE SUPPORT

STDL80 supports popular design platforms and environments such as Verilog, Viewlogic, Mentor and Synopsys for front-end logic design capture and simulation, and ArcCell for back-end placement and routing.

For a high simulation accuracy, STDL80 uses a proprietary delay calculator. Cell delay calculations are based on a matrix of delay parameters for each macrocell, and signal interconnection delay is based on the RC tree analysis.

PRODUCT FAMILY

STDL80 library include the following design elements:

(a) Internal Macrocells
(b) Input/Output Cells
(c) Macrofunctions
(d) Megafunctions
(e) Memory Compilers
(f) Datapath Compilers
(g) JTAG Boundary Scans.

< Internal Macrocells >

Macrocells are the lowest level of logic functions such as NAND, NOR and flip-flop used for logic designs. There are about 300 different types of internal macrocells. They usually come in two levels of drive strength (1X and 2X).

These macrocells have many levels of representations—logic symbol, logic model, timing model, transistor schematic, HSPICE netlist, physical layout, and placement and routing model.

< Macrofunctions >

Macrofunctions are netlists of logic function which have the complexity of a standard MSI circuit. Macrofunctions are logic building blocks. There are 44 kinds of 74XX (TTL) compatible functions in this library.

< Megafunctions >

Megafunctions are also netlists of logic function, but with a high logic complexity of a standard LSI circuit. Multipliers, barrel shifters, 82XX Intel functions, etc. are supported in this library.

< Memory Compilers>

Memory compilers of STDL80 consist of two ROMs (synchronous contact programmable and synchronous diffusion programmable), three single-port RAMs (synchronous and asynchronous) and three dual-port RAMs (synchronous and asynchronous).

In addition, a Register File and a FIFO are under-developed.

< Datapath Compilers >

Datapath compilers of STDL80 consist of 16 macro cells (Adder, ALU, Multiplier, etc.) and 14 primitive cells (NAND, NOR, DFF, LATCH, MUX, etc.)

< Input/Output Cells >

There are about 400 different I/O buffers. Each I/O cell is implemented solely on the basic I/O cell architecture which forms the periphery of the masterslice.

A test logic is provided to enable the efficient parametric (threshold voltage) testing on input buffers including CMOS and TTL level converters, Schmitt trigger input buffers, clock drivers and oscillator buffers. Pull-up and pull-down resistors are optional features.

Three basic types of output buffers (non-inverting, tri-state and open drain) are available in a range of driving capabilities from 1mA to 24mA. The slew rate control is provided for each buffer type (except 1mA and 2mA buffers) to reduce output power/ground bus noise and signal ringing, especially in simultaneous switching outputs.

Bi-directional buffers are combinations of input buffers and output buffers (tri-state or open drain) in a single unit. The bi-directional output drive capability of 5V tolerant I/O is in the range of 1mA to 6mA. The I/O structure has been fully characterized for ESD protection and latch-up resistance.

For user's convenience, STDL80 library provides with three options of pull-down and pull-up resistances respectively. They are 50KΩ, 100KΩ, and 200KΩ (The default value is 100KΩ).

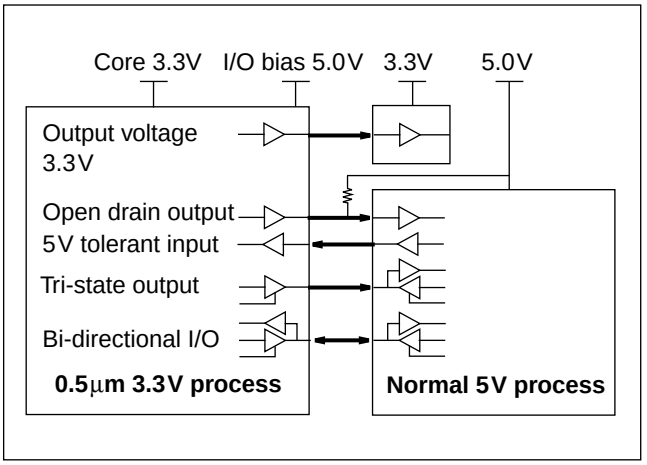
I/O Cell Drive Options

To provide designers with the greater flexibility, each I/O buffer can be selected among various current levels (e.g., 1mA, 2mA, ..., 24mA). The choice of current-level for I/O buffers affects their propagation delay and current noise.

The slew rate control helps decrease the system noise and output signal overshoot/undershoot caused by the switching of output buffers. The output edge rate can be slowed down by selecting the high slew rate control cells. STDL80 provides three different sets of output slew rate controls. Only one I/O slot is required for any slew rate control options.

5V Tolerant I/O Buffers

STDL80 library is a process which has the most optimum performance in 3.3V. In this process, voltages more than 3.6V are not allowed at the gate oxide because of a reliability problem. And a special circuit is adopted in order to make pin voltage tolerable up to 5.25V and to offer TTL interface driving up to 6mA. Obviously, this circuit is constructed not to permit more than 3.6 voltages at the gate oxide. The external circuit diagram is as follows.



The maximum external tolerance voltage of this buffer is 5.5V. And the leakage current of tri-state input pin and output pin is less than 10nA in 0 ~ 5V and less than 70μA in 5.5V. When the output is tri-state and the output pin voltage is 5V, 5V of bulk bias voltage is required to prevent current from flowing through a chip, however, almost no current flows. If the bulk bias is 3.3V, it operates as a 3.3V normal buffer.

PCI Buffers

In addition to input, output, bi-directional, slew rate controlled and Schmitt trigger I/O buffers, SEC ASIC now offers PCI (Peripheral Component Interconnect) I/O buffers. PCI is expected to be better suited to the more complex and feature-rich design than the existing local bus standards. 5V tolerant and 3.3V PCI buffers are included in this library.

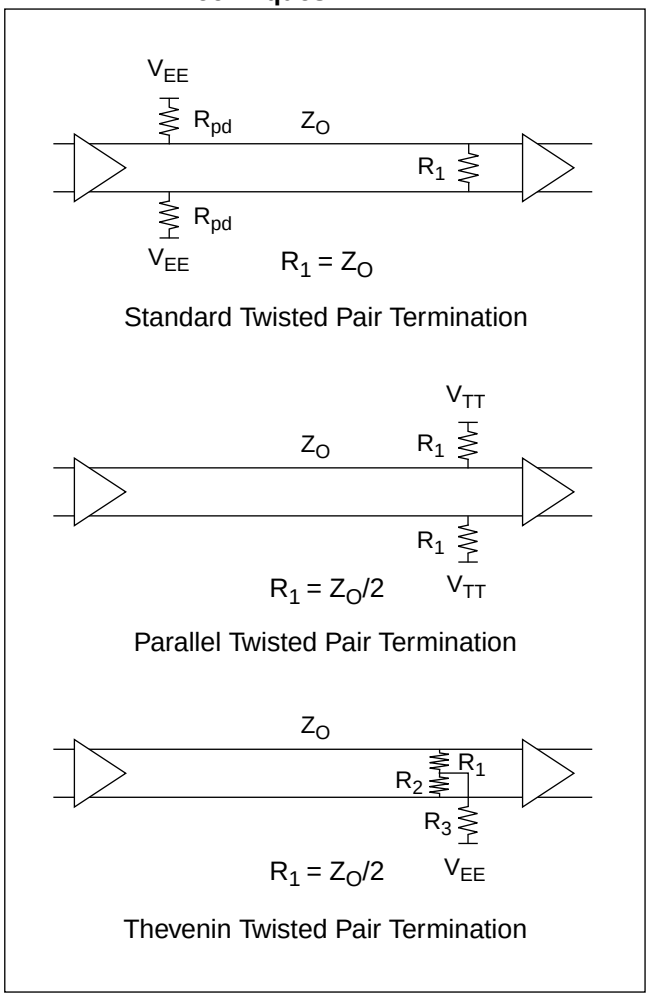
PECL

SEC ASIC's PECL (Positive Emitter Coupled Logic) buffer having 155MHz operating frequency is suited to ATM interface.

The voltage swing level is about 0.8V, being similar to that of ECL, and the external terminator is needed. Its main features are the same as ECL; low noise, high speed and single ended/differential function.

In case of differential transmission, the external terminator is shown in the following figure.

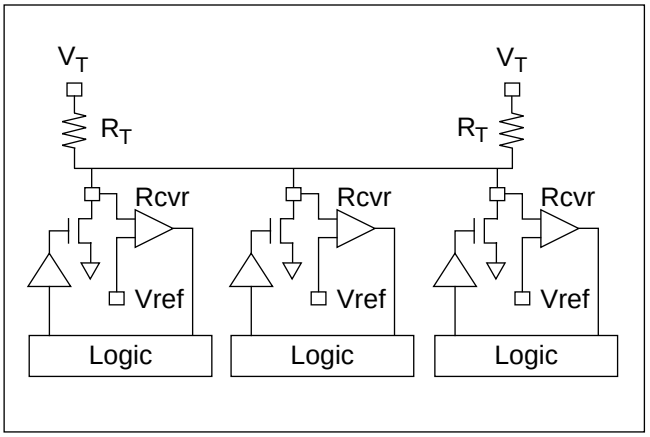
Figure 1-1. Twisted Pair Termination Techniques



GTL (Gunning Transceiver Logic)

GTL and GTL+ interface I/Os are useful for implementing highly reliable system, satisfying fast and low-powered signal transfers and reducing noise in a switching circuitry.

In all 0.5μm cell libraries in SEC ASIC, GTL interface is fully supported.

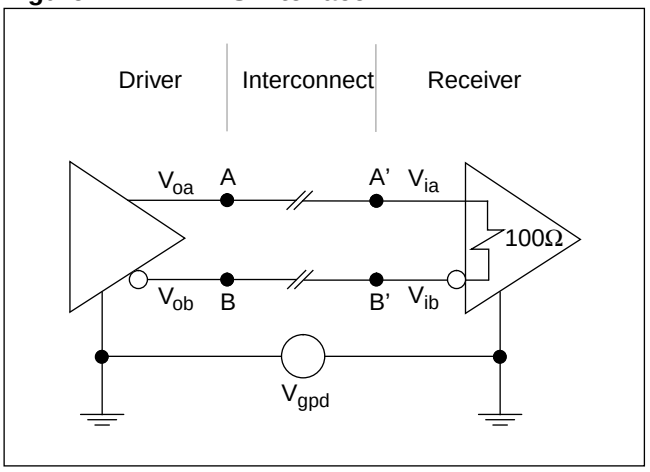


LVDS

LVDS (Low Voltage Differential Signals) buffer for SCI (Scalable Coherent Interface) system, shown in the following figure, enables high speed I/O interface with SEC ASIC's high frequency PLL.

This structure is designed for high speed point-to-point unidirectional interface. Its main characteristics are much the same as ECL's differential mode; low noise generation, high noise immunity and low level signalling.

Figure 1-2. LVDS Interface



USB (Universal Serial Bus)

Various kinds of peripheral equipments such as mouse, joy stick, keyboard, modem, scanner and printer improve the power of a computer. However, it is not easy to connect and use them properly in the computer.

USB specification established late in 1995 is a good solution for this problem, providing facile method of an expansion. SEC ASIC offers USB interfaced buffers in the 0.5μm technology.

USB is applicable only in STD cells.

Figure 1-3. Full Speed Device Cable and Resistor Connections

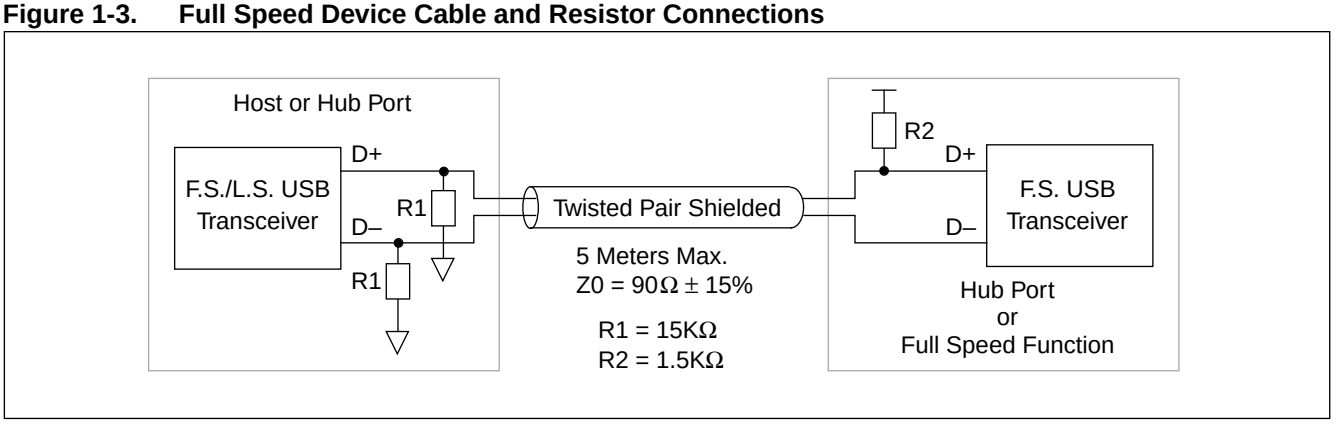
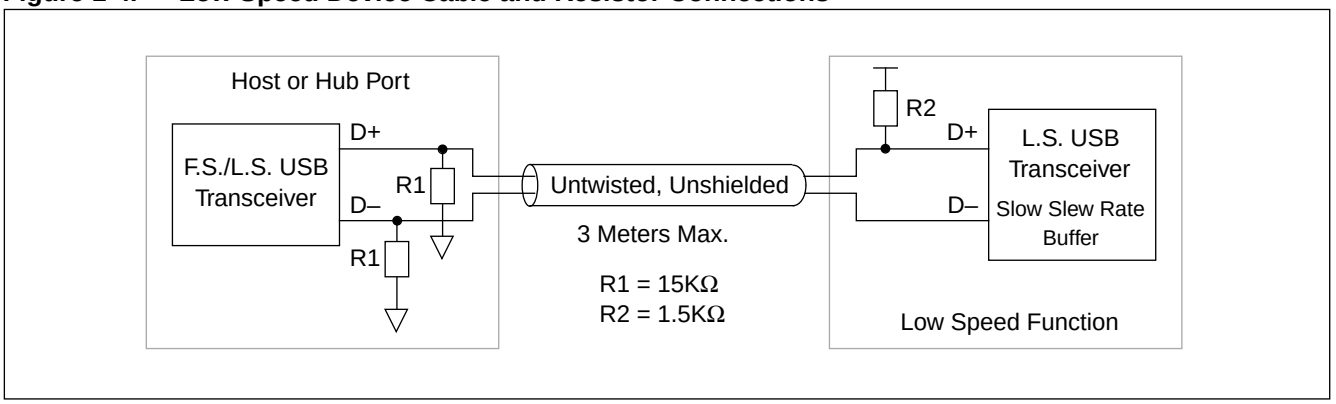


Figure 1-4. Low Speed Device Cable and Resistor Connections



LVTTL/LVCMOS

Low Voltage TTL and Low Voltage CMOS I/O buffers have various kinds of applications as normal TTL and CMOS I/O sets. Their key features are low voltage swing and low noise.

Input voltage level is 5V compatible. Output high voltage is 2.4V ~ 2.8V in LVTTL and VDD–0.2V in LVCMOS.

In a STDL80 library, they employ 5V tolerant I/O.

CardBus Buffers

CardBus I/O buffers have 3.3V 32-bit bus width and 33MHz of transmission speed. They are for external CardBus type of extension card of notebook PC.

V_{DD}/V_{SS} RULES AND GUIDELINES

There are three types of V_{DD} and V_{SS} in STDL80, each with its related bus and pad cells. To support the use of mixed voltage, two different V_{DD} types are needed for 3.3V and 5V respectively.

(1) Core logic
– VSSI, VDD3I (for 3.3V)
(2) Input buffers (usable when requested)
– VSSP, VDD3P (for 3.3V), VDD5P (for 5V)
(3) Output buffers
– VSSO, VDD3O (for 3.3V), VDD5O (for 5V)

The number of V_{DD} and V_{SS} pads required for a specific design depends on the following factors:

- Number of input and output buffers
- Number of simultaneous switching inputs
- Number of simultaneous switching outputs
- Number of used gates and simultaneous switching gates
- Operating frequency of the design.

Input Buffer V_{DD}/V_{SS} Pad Allocation Guidelines

These guidelines ensure that an adequate input threshold voltage margin is maintained during a switching.

- One VSSP is required to support 32 input buffers, and one input buffer V_{DD} can support up to 64 inputs.
- For simultaneous switching inputs, one VSSP pad is required for every 20 inputs, and one input buffer V_{DD} pad for every 40 inputs.
- Input buffer V_{SS}/V_{DD} pads should be placed in such a way that they equally divide the input buffers on either side.

Output Buffer V_{DD}/V_{SS} Pad Allocation Guidelines

The number of VSSO pads required for a device can be calculated from the following expression:

$$\Sigma (I_{OL\ Simultaneous\ switching\ outputs}) / 40 + \Sigma (I_{OL\ Normal\ outputs}) / 64.$$

- The total number of output buffer V_{DD} pads required is half of VSSO.
- Output buffer V_{SS}/V_{DD} pads should be placed in such a way that output buffers are equally divided on either side.

Core Logic V_{SS} Bus and VSSI Pad Allocation Guidelines

The purpose of these guidelines is to ensure that V_{DD}/V_{SS} bounce caused by a simultaneous gate switching is kept to minimum. The voltage bounce on the power bus can have a negative impact on a gate-switching speed and even on the functionality of macrocells like flip-flops and latches in an extreme case.

Because of variations in package inductance, the number of V_{DD}/V_{SS} pads required for a specific design is the function of the operating frequency of a chip, i.e., designs operating at high frequency should use more V_{DD}/V_{SS} pads.

- V_{DD} bus width and pad requirements are half of V_{SS}.
- V_{DD}/V_{SS} buses and pads should be distributed evenly in the core and on all sides of the chip.
- Whenever possible, at least one VSSI pad should be used on each side of the chip.
- The total number of core logic V_{DD} pads required is half of VSSI.

The number of VSSI pads required for a design can be calculated from the following expression:

$$G \times S \times F \times 2.00e{-}5$$

,where
G = Total number of used gates,
S = % of simultaneous switching gates,
F = Switching frequency in MHz.

POWER DISSIPATION

Estimation of Power Dissipation in CMOS Circuit

CMOS circuits have been traditionally considered to consume low power since they draw very small amount of current in a steady state. However, the recent revolution in a CMOS technology that allows very high gate density has changed the way the power dissipation should be understood. The power dissipation in a CMOS circuit is affected by various factors such as the number of gates, a switching frequency, the loading on the output of a gate, and so on.

Power dissipation is important when designers decide the amount of necessary power supply current for the device to operate in safety. Propagation delays and a reliability of the device also depend on the power dissipation which determines the temperature at which the die operates. To obtain a high speed and a reliability, designers must estimate the power dissipation of the device accurately and determine the appropriate environments including packages and system cooling methods.

This section describes the concept of two types of power dissipation (static and dynamic) in a CMOS circuit, the method of calculating them in the SEC STDL80 library, and finally their relationship with a temperature.

Static (DC) Power Dissipation

There are two types of static or DC current contributing to the total static power dissipation in CMOS circuits.

One is the leakage current of the gates resulted by a reverse bias between a well and a substrate region. There is no DC current path from power to ground in a CMOS because one of the transistor pair is always off, therefore, no static current except the leakage current flows through the internal gates of the device. The amount of this leakage current is, however, in the range of tens of nano amperes, which is negligible.

The other is DC current that flows through the input and output buffers when the circuit is interfaced with other devices, especially TTL. The current of pull-up/ pull-down transistor included in the input buffers is about 50μA typically, which is also negligible. Therefore, only DC current that the output buffers source or sink has to be counted to estimate the total static power dissipation.

DC power dissipation of TTL output and bi-directional buffers is determined by the following formula:

$$P_{DC\_TTL\_OUTPUT} = \Sigma(V_{OL} \times I_{OL} \times t_L) + \Sigma((V_{DD} - V_{OH}) \times I_{OH} \times t_H)$$

,where

$t_H = T_{HIGH} / T$,

$t_L + t_H = 1$.

Dynamic (AC) Power Dissipation

When a CMOS gate changes its state, it draws switching current as a result of charging or discharging of a node capacitance, C_L. The energy associated with the switching current for a node capacitance, C_L, is

$$1 / 2 \times (C_L \times V_{DD}^2)$$

,where V_{DD} is a power supply voltage.

The switching occurs twice per cycle for periodic signals: once for charging a capacitance and once for discharging it. Hence, the dynamic power dissipation due to the switching current is the energy divided by the clock period and multiplied by the factor of two, or

$$C_L \times V_{DD} \times V_{DD} / T$$

,where T is a clock period.

As shown above, it is quite straight forward to calculate the dynamic power dissipation for a single gate. The dynamic power dissipation for an entire chip is, however, much more complicated to estimate since it depends on the degree of switching activity of the circuit. SEC has found that the degree of switching activity is 20% on the average and recommends to use this number to estimate the total dynamic power dissipation.

Power Dissipation in STDL80

This section describes the equations on how to estimate the power dissipation in STDL80. As explained in the previous section, the total power dissipation (P_{TOTAL}) consists of static power dissipation (P_{DC}) and dynamic power dissipation (P_{AC}).

$$P_{TOTAL} = P_{DC} + P_{AC}$$

Since only output buffers contribute to the static power dissipation,

$$P_{DC} = P_{DC\_OUTPUT}$$

,where P_{DC} output is the static power dissipated when output buffers source or sink.

The dynamic power dissipation is caused by three components: input buffers (P_{AC_INPUT}), output buffers (P_{AC_OUTPUT}), and internal cells ($P_{AC\_INTERNAL}$).

$$P_{AC} = P_{AC\_INPUT} + P_{AC\_OUTPUT} + P_{AC\_INTERNAL}$$

Each term mentioned above is characterized by the following equations:

$P_{DC\_OUTPUT} = 150 \times I_{OL} \times N\_output$ [µW]
$P_{AC\_INPUT} = 10.8 \times N\_input \times F \times S$ [µW]
$P_{AC\_OUTPUT} = 11 \times N\_output \times F \times S \times C$ [µW]
$P_{AC\_INTERNAL} = 1.3 \times N\_internal \times F \times S$ [µW]

,where
I_{OL} is source and sink current of output buffers in mA,
N_output is the number of output buffers used,
N_input is the number of input buffers used,
N_internal is the number of internal cells used,
F is the maximum operation frequency in MHz,
S is the estimated degree of a switching activity (typically 0.2),
C is the output load capacitance in pF.

Temperature and Power Dissipation

The total power dissipation, P_{TOTAL} can be used to find out the device temperature by the following equation:

$$\theta_{JA} = (T_J - T_A) / P_{TOTAL}$$

,where
θ_{JA} is the thermal impedance,
T_J is the junction temperature of the device,
T_A is the ambient temperature.

Thermal impedances of the SEC packages are given in the following table. The junction temperature, obtained by multiplying P_{TOTAL} by the appropriate θ_{JA} and adding T_A, determines the derating factor for the propagation delays and also indicates the reliability measures.

Hence, designers can achieve the desired derating factor and reliability targets by choosing appropriate packages and system cooling methods.

Table 1-1. Thermal Impedances of SEC Packages

	QFP						
Pin Number	**64**	**80**	**100**	**120**	**160**	**208**	**240**
θ_{JA} [°C/W]	60	60	60	50	50	40	40

Maximum Junction Temperature (T_J)

The allowable maximum junction temperatures for plastic and ceramic packages are as follows:

Junction temperature for plastic package ≤ 125°C
Junction temperature for ceramic package ≤ 150°C.

PROPAGATION DELAYS

Interconnection wire length, temperature and supply voltage are the chief factors affecting propagation delays.

Wire Length Load

The loading due to interconnection wire length can be estimated with the following expression. The result is given in terms of number of equivalent standard loads.

$$C_{WL} = C_{FO} \times (0.049 \times \sqrt{A} + 0.48) + 0.079 \times \sqrt{A} + 0.33$$

,where

C_{FO} = Number of fanouts in a standard load,

A = Area of block size in mm^2,

C_{WL} = Number of equivalent standard loads due to an interconnection,

e.g.,

C_{FO} = 7 (standard load),

A = 25mm^2,

C_{WL} = 5.8 (standard load).

Best and Worst Case Conditions

A circuit should be designed to operate properly within a given specification level, either commercial or industrial. It is recommended that circuits be simulated for best case, normal case, and worst case conditions at each specification level.

The following expressions also allow for the effect of process variation on circuit performance.

Best case:

$$T_{BC} = K_{PBC} \times K_T \times K_V \times T_{NOM} = K_{BC} \times T_{NOM}$$

Worst case:

$$T_{WC} = K_{PWC} \times K_T \times K_V \times T_{NOM} = K_{WC} \times T_{NOM}$$

,where

T_{BC} = Best case propagation delay

T_{WC} = Worst case propagation delay

T_{NOM} = Normal propagation delay

(T_J = 25^oC, V_{DD} = 3.3V and typical process)

K_{PWC} = Worst case process correction factor

K_{PBC} = Best case process correction factor

With above equations, we can calculate the multipliers of K_{WC} and K_{BC} as follows.

Table 1-2. Best case delay

Application	Best case delay			
	Parameter			K_{BC}
	V_{DD}	T_J	Proc.	
Industrial	3.6V	–40^oC	Min.	0.49
Commercial	3.6V	0^oC	Min.	0.54

Table 1-3. Worst case delay

Application	Worst case delay			
	Parameter			K_{WC}
	V_{DD}	T_J	Proc.	
Industrial	2.7V	125^oC	Max.	2.03
Commercial	3.0V	115^oC	Max.	1.82

Derating factors

The multipliers can be applied to nominal delay data in order to estimate the effects of supply voltage, temperature and process. Nominal data are provided for conditions of V_{DD} = 3.3V, T_A = 25°C and typical process.

The derating factors of STDL80 are as follows.

Table 1-4. Process derating factor

Process Factor (K_P)	Slow	Typ.	Fast
	1.40	1.00	0.60

Table 1-5. Temperature derating factor

Temp. (^oC)	125	85	70	25	0	–40
K_T	1.21	1.13	1.10	1.00	0.95	0.86

Table 1-6. Voltage derating factor (K_V)

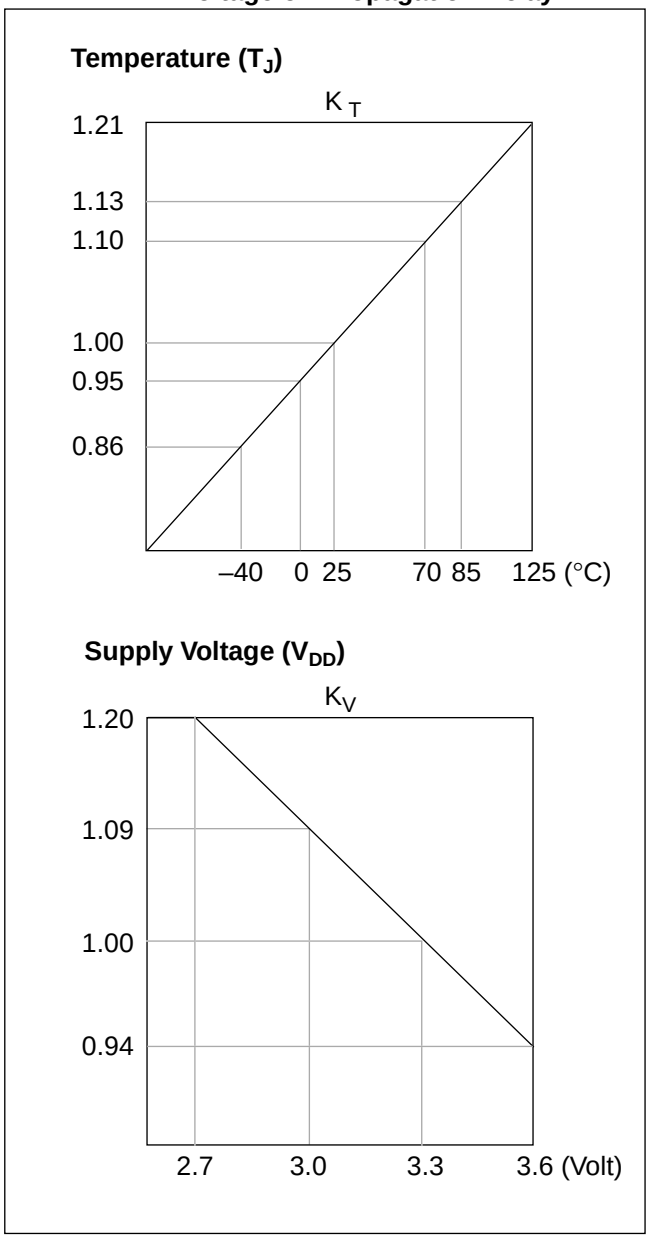
Voltage (V)	3.6	3.3	3.0	2.7
K_V	0.94	1.00	1.09	1.20

Temperature and Supply Voltage

The next figure describes propagation delay correction factors (K_T, K_V) as a function of on-chip junction temperature (T_J) as well as supply voltage (V_{DD}). As a result of increasing CMOS power dissipation, ambient and junction temperature are generally not the same.

The temperature of the die inside the package (junction temperature, T_J), is calculated using chip power dissipation and the thermal resistance to ambient temperature (θ_{JA}) of the package. Information on package thermal performance can be obtained from SEC application engineers.

Figure 1-5. Effect of Temperature and Supply Voltage on Propagation Delay



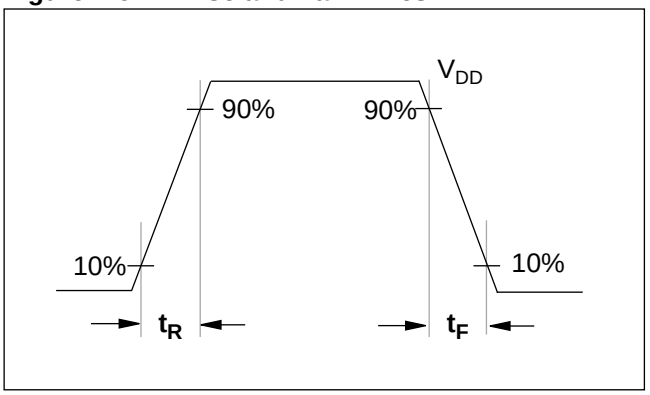
Timing Parameters

This section discusses issues involving timing parameters for primitive cells.

RISE / FALL TIMES

The definition of rise time (t_R) and fall time (t_F) is shown in the following figure.

Figure 1-6. Rise and Fall Times

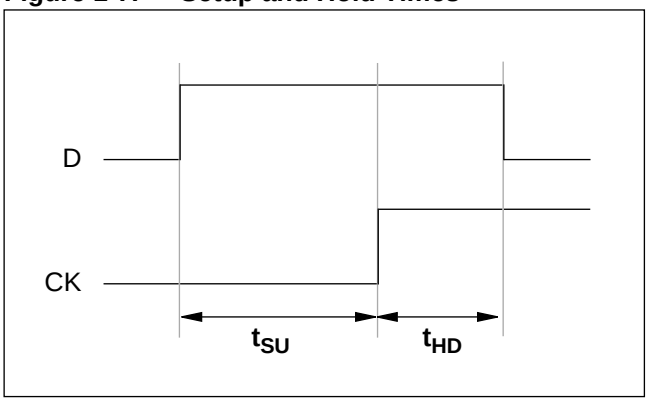


SETUP / HOLD TIMES

Setup time (t_{SU}) is a minimum period in which the input data to a flip-flop or a latch must be stable before the active edge of the clock occurs. Hold time (t_{HD}) is a minimum period in which the input data to a flip-flop or a latch must remain stable after the active edge of the clock has occurred.

The next figure shows the relationship between setup and hold times for a standard flip-flop triggered on the rising edge of the clock.

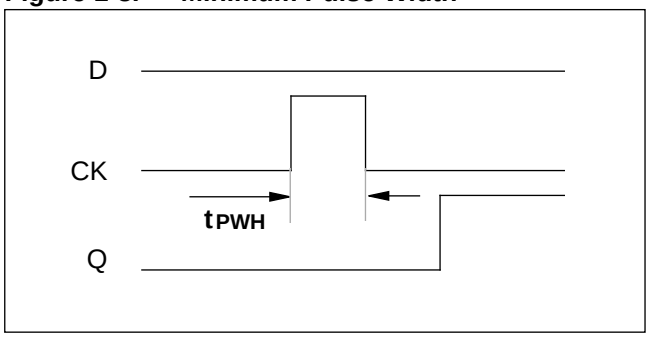
Figure 1-7. Setup and Hold Times



MINIMUM PULSE WIDTHS

Minimum clock pulse widths (t_{PWH}, t_{PWL}) are the time intervals during a clock signal is high or low, so that it ensures proper operation of a flip-flop or a latch.

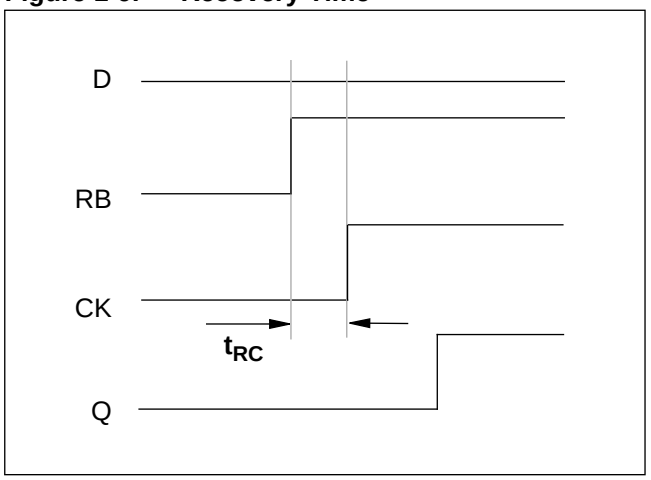
Figure 1-8. Minimum Pulse Width



RECOVERY TIMES

Recovery time (t_{RC}) is the minimum time after an asynchronous pin is disabled that an active clock edge will propagate data from input to output. If the active edge or clock occurs before the specified recovery time, the input data will not propagate.

Figure 1-9. Recovery Time

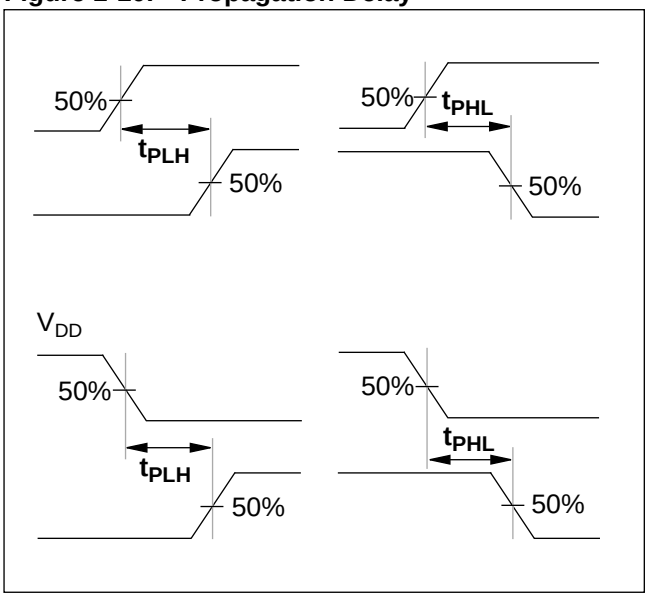


PROPAGATION DELAYS

A delay for a macrocell is considered to be a rising delay (t_{PLH}) if the signal on the output pin is rising. For a rising input and a rising output, the rising delay is the interval between the times the input becomes 50% of supply voltage (V_{DD}) and the output becomes 50% of V_{DD}.

If the input is falling and the output is rising, the rising delay is the interval between the times the input falls to 50% of V_{DD} and the output rises to 50% of V_{DD}. The converse is true for a falling delay (t_{PHL}).

Figure 1-10. Propagation Delay

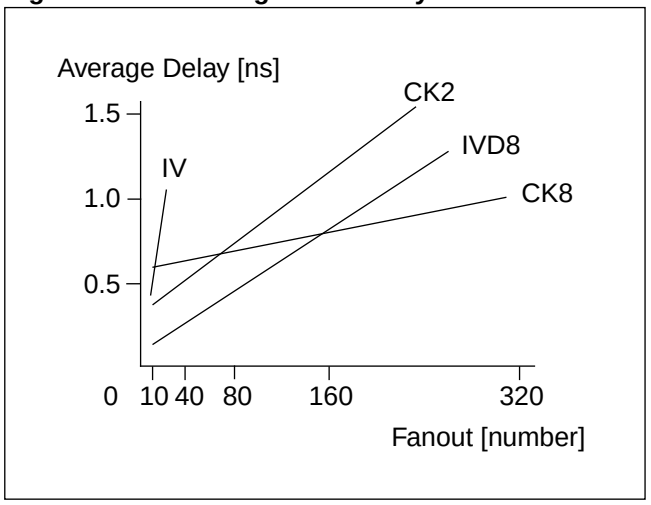


Proper Use of Buffers

Figure 1-11. Average Gate Delay in STDL80 shows the average propagation delays of an internal inverter (IV), an 8X inverter (IVD8), a normal clock driver (CK2), and a high clock driver (CK8).

Note that transistors uses in I/O slots are larger and have ON channel resistance about one order of magnitude lower than those of the N and P channel transistors in primitive cells. This makes them likely candidates for use as buffers for high fanout signals. For example, CK2 and CK8 buffers require one I/O slot location. Both can be used as high fanout internal buffers.

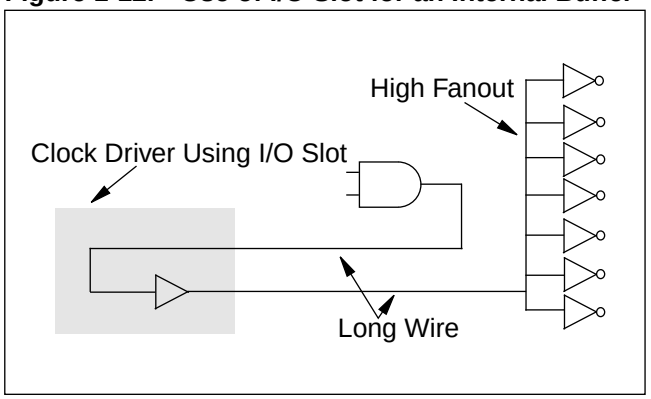
Figure 1-11. Average Gate Delay in STDL80



One caution, emphasized in Figure 1-12. Use of I/O Slot for an Internal Buffer, shows that if you route to a buffer that uses an I/O slot from an internal element and back into internal logic, the additional wiring needed could increase propagation delays materially. Higher drive strength internal cells may be more appropriate than I/O slot buffers.

Realize also that using I/O slot cells for internal buffering removes those locations for use as external I/Os and uses two wiring channels, thereby increasing routability congestion on masterslice products.

Figure 1-12. Use of I/O Slot for an Internal Buffer



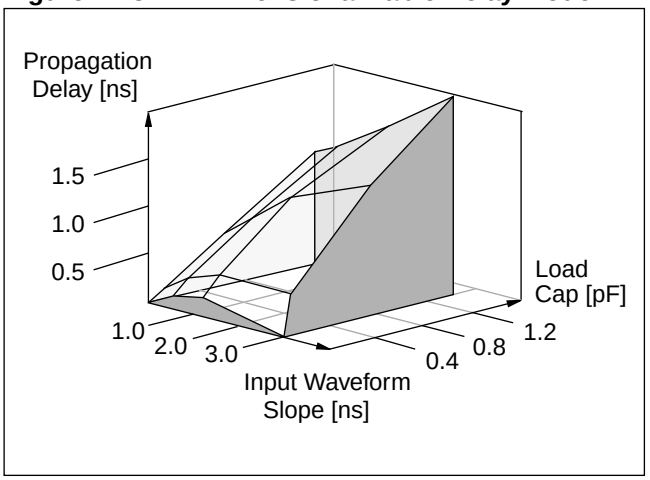
DELAY MODEL

The ASIC timing characteristics consist of the following components:

- Cell propagation delay from input to output transitions based on input waveform slope, fanout loads and distributed interconnection wire resistance and capacitance.
- Interconnection wire delay across the metal lines.
- Timing requirement parameters such as setup time, hold time, recovery time, skew time, minimum pulse width, etc.
- Derating factors for junction temperature, power supply voltage, and process variations.

Timing model for STDL80 focuses on how to characterize cell propagation delay time accurately. To accomplish this goal, 2-dimensional table look-up delay model has been adopted. The index variables of this table are input waveform slope and output load capacitance. See the figure below. SEC ASIC design automation system supports an n-dimensional table model even though we adopted 2-dimensional model for our 0.5μm cell-based products.

Figure 1-13. 2-Dimensional Table Delay Model



The Table 1-7. Table Delay Model Example shows an example of this model for 2-input NAND cell. The data in this table are high-to-low transition delay times from one of the two input pins to output pin. The number of points and values of the index variables can differ for each cell.

Table 1-7. Table Delay Model Example

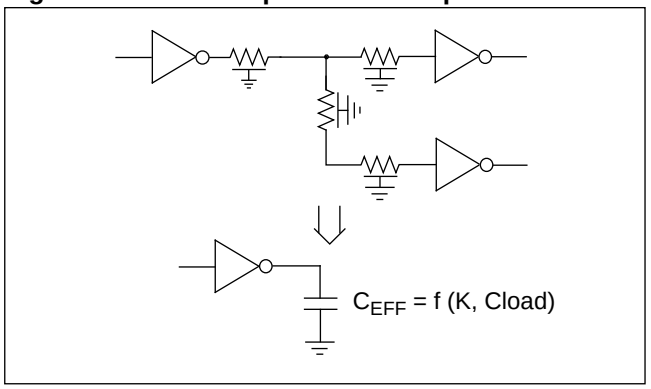
Slope \ Cap.	0.03	0.13	0.53	1.32
0.10	0.07	0.14	0.42	0.97
0.30	0.08	0.17	0.45	1.02
0.80	0.06	0.18	0.51	1.07
1.60	0.01	0.18	0.60	1.18

Notice that 4-by-4 table is used. Delay values between grid points and beyond this table are determined by linear interpolation and extrapolation methods. This general table delay model provides great flexibility as well as high accuracy since extensive software revisions are not required when a cell library is updated. The other timing components such as interconnection wire delay, timing requirement parameters and derating factors are characterized in a commonly-accepted way in industry.

The delay time due to the interconnection wire can be separated into two components. One is the signal propagation delay time across the metal lines. This delay time component is computed through conventional RC analysis based on Π-model. The other is an additional delay on the driving cell due to the wire load. The traditional way to compute this is based on the lumped capacitance model, ignoring wire resistance.

For sub-micron technology, this approximation cannot be accepted any more. The wire resistance has a shielding effect on the driving cell from load capacitances. An effective capacitance C_{EFF}, a single capacitance approximating distributed interconnection wire resistance and capacitance, is derived, as illustrated in the following figure. The compensation factor K, extracted for each cell, is a function of the length of interconnection wires and the layout topology. All these effects are merged to determine the effective capacitance and this value is used as an index of the table delay model.

Figure 1-14. Concept of Effect Capacitance



The figure below summarizes the features of SEC ASIC's delay model.

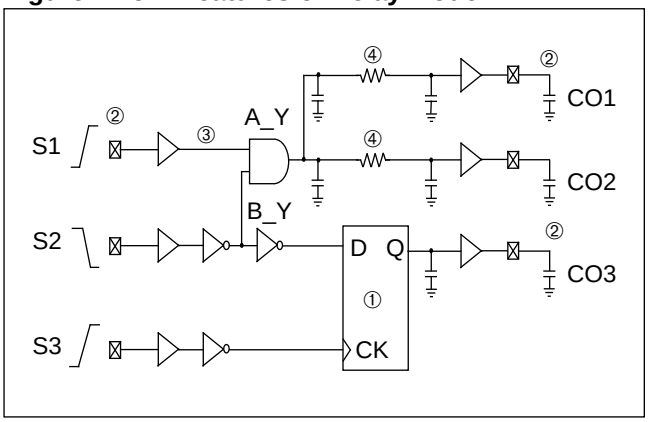
① 2-dimensional table delay model for output loading and input waveform slope effects is used. The slopes (t_R, t_F) and delay times (t_{PLH}, t_{PHL}) of all cell instances are calculated recursively.

② The input waveform slope of each primary input pad and the loading capacitance of each primary output pad can be assigned individually or by default.

③ Pin to pin delays of cells and interconnection wires are supported.

④ The effect of distributed interconnection wire resistance and capacitance on cell delay is analysed using the effective capacitance concept.

Figure 1-15. Features of Delay Model



MAXIMUM FANOUTS

Internal Macrocells

The maximum fanouts for STDL80 primitive cells are as follows. Note that these fanout limitation values are calculated when the rise and fall times of the input signal is 0.35ns. Depending on the rise and fall times, the maximum fanout limitations can be varied case by case.

In the following table the maximum fanout values for all pins of STDL80 internal macrocells are listed.

Table 1-8. Maximum Fanouts of Internal Macrocells (When t_R/t_F = 0.35ns)

Cell Name	Output Pin	Maximum Fanout
Logic Cells		
AD2	Y	59
AD2D2	Y	121
AD3	Y	60
AD3D3	Y	181
AD4	Y	60
AD4D2	Y	121
AD5	Y	35
AD5D2	Y	71
ND2	Y	48
ND2D2	Y	103
ND3	Y	32
ND3D2	Y	66
ND4	Y	24
ND4D2	Y	48
ND5	Y	18
ND5D2	Y	37
ND6	Y	59
ND6D2	Y	119
ND8	Y	59
ND8D2	Y	120
NR2	Y	36
NR2D2	Y	76
NR3	Y	23
NR3D2	Y	47
NR4	Y	16
NR4D2	Y	34
NR5	Y	59
NR5D2	Y	122
NR6	Y	59
NR6D2	Y	120
NR8	Y	59
NR8D2	Y	121
OR2	Y	60
OR2D2	Y	119
OR3	Y	58
OR3D3	Y	172
OR4	Y	47
OR4D2	Y	95
OR5	Y	45
OR5D2	Y	96
XN2	Y	59
XN2D2	Y	116
XN3	Y	55
XN3D3	Y	148
XO2	Y	58
XO2D2	Y	114
XO3	Y	55
XO3D3	Y	149
AO21	Y	31
AO21D2	Y	67
AO211	Y	20
AO211D2	Y	41
AO22	Y	31
AO22D2	Y	65
AO22A	Y	31
AO22D2A	Y	64
AO222	Y	19
AO222D2	Y	122
AO222A	Y	23
AO222D2A	Y	49
AO33	Y	20
AO33D2	Y	123
AO333	Y	17
AO333D2	Y	124
OA21	Y	32
OA21D2	Y	65
OA211	Y	21
OA211D2	Y	44
OA22	Y	30
OA22D2	Y	63
OA22A	Y	32

Cell Name	Output Pin	Maximum Fanout
OA22D2A	Y	66
OA2222	Y	59
OA2222D2	Y	119
DL1D2	Y	122
DL1D4	Y	257
DL2D2	Y	123
DL2D4	Y	258
DL3D2	Y	126
DL3D4	Y	260
DL4D2	Y	127
DL4D4	Y	256
DL5D2	Y	129
DL5D4	Y	271
DL10D2	Y	129
DL10D4	Y	270
IV	Y	62
IVD2	Y	134
IVD3	Y	206
IVD4	Y	268
IVD6	Y	376
IVD8	Y	525
IVA	Y	62
IVD2A	Y	134
IVD3A	Y	206
IVD4A	Y	268
IVCD11	Y	61
	YN	62
IVCD13	Y	57
	YN	206
IVCD22	All Pins	134
IVCD26	Y	116
	YN	376
IVCD44	Y	301
	YN	227
IVT	Y	47
IVTD2	Y	102
IVTD4	Y	195
IVTD8	Y	525
IVTN	Y	47
IVTND2	Y	95
IVTND4	Y	195
IVTND8	Y	373
NID	Y	59

Cell Name	Output Pin	Maximum Fanout
NID2	Y	121
NID3	Y	187
NID4	Y	242
NID6	Y	371
NID8	Y	511
NIT	Y	47
NITD2	Y	100
NITD4	Y	201
NITD8	Y	373
NITN	Y	47
NITND2	Y	96
NITND4	Y	183
NITND8	Y	351
Flip-Flops		
FD1	Q	60
	QN	59
FD1D2	Q	121
	QN	123
FD1CS	All Pins	59
FD1CSD2	All Pins	120
FD1S	Q	60
	QN	59
FD1SD2	Q	121
	QN	123
FD1Q	Q	60
FD1QD2	Q	123
FD1X2	Q(0/1)	60
	QN(0/1)	59
FD1X4	Q(0/1/2/3)	60
	QN(0/1/2/3)	59
YFD1	Q	58
	QN	50
YFD1D2	Q	116
	QN	102
FD2	Q	59
	QN	60
FD2D2	Q	121
	QN	126
FD2CS	All Pins	59
FD2CSD2	Q	121
	QN	122
FD2S	Q	59
	QN	60

Cell Name	Output Pin	Maximum Fanout
FD2SD2	Q	121
	QN	123
FD2Q	Q	60
FD2QD2	Q	123
FD2X2	All Pins	59
FD2X4	Q(0/1/2/3)	59
	QN(0/1/2/3)	60
YFD2	Q	57
	QN	44
YFD2D2	Q	113
	QN	87
FD2T	Q	59
	Z	33
FD2TD2	Q	123
	Z	61
FD2TCS	Q	59
	Z	33
FD2TCSD2	Q	120
	Z	59
FD2TS	Q	59
	Z	33
FD2TSD2	Q	122
	Z	61
FD3	Q	60
	QN	59
FD3D2	Q	124
	QN	121
FD3CS	All Pins	59
FD3CSD2	Q	122
	QN	120
FD3S	Q	60
	QN	59
FD3SD2	All Pins	122
FD3Q	Q	60
FD3QD2	Q	123
FD3X2	Q(0/1)	60
	QN(0/1)	59
FD3X4	Q(0/1/2/3)	60
	QN(0/1/2/3)	59
YFD3	Q	47
	QN	50
YFD3D2	Q	93
	QN	101

Cell Name	Output Pin	Maximum Fanout
FD4	All Pins	59
FD4D2	Q	121
	QN	120
FD4CS	All Pins	59
FD4CSD2	Q	121
	QN	120
FD4S	All Pins	59
FD4SD2	Q	121
	QN	120
FD4Q	Q	59
FD4QD2	Q	121
FD4X2	All Pins	59
FD4X4	All Pins	59
YFD4	Q	47
	QN	43
YFD4D2	Q	92
	QN	89
FD5	Q	60
	QN	59
FD5D2	Q	121
	QN	123
FD5S	Q	60
	QN	59
FD5SD2	Q	121
	QN	123
FD5X4	Q(0/1/2/3)	60
	QN(0/1/2/3)	59
FD6	Q	59
	QN	60
FD6D2	Q	120
	QN	125
FD6S	Q	59
	QN	60
FD6SD2	Q	121
	QN	124
FD7	Q	60
	QN	59
FD7D2	Q	122
	QN	121
FD7S	Q	60
	QN	59
FD7SD2	All Pins	122
FD8	All Pins	59

Cell Name	Output Pin	Maximum Fanout
FD8D2	Q	121
	QN	122
FD8S	All Pins	59
FD8SD2	All Pins	120
FDS2	Q	60
	QN	59
FDS2D2	Q	121
	QN	123
FDS2CS	All Pins	59
FDS2CSD2	All Pins	120
FDS2S	Q	59
	QN	60
FDS2SD2	Q	123
	QN	121
FDS3	Q	59
	QN	60
FDS3D2	Q	123
	QN	121
FG1	Q	60
	QN	59
FG1X4	Q(0/1/2/3)	60
	QN(0/1/2/3)	59
FG2	Q	59
	QN	60
FG2X4	All Pins	59
FJ1	Q	60
	QN	59
FJ1D2	All Pins	120
FJ1S	All Pins	60
FJ1SD2	Q	120
	QN	124
FJ2	All Pins	60
FJ2D2	Q	121
	QN	124
FJ2S	All Pins	60
FJ2SD2	Q	120
	QN	125
FJ4	Q	60
	QN	59
FJ4D2	Q	120
	QN	121
FJ4S	Q	60
	QN	59

Cell Name	Output Pin	Maximum Fanout
FJ4SD2	Q	120
	QN	121
FT2	All Pins	60
FT2D2	Q	121
	QN	122
FT3	Q	60
	QN	59
FT3D2	Q	123
	QN	120
Latches		
LD1	Q	59
	QN	60
LD1D2	Q	123
	QN	120
LD1S	Q	59
	QN	60
LD1SD2	Q	123
	QN	122
LD1Q	Q	59
LD1QD2	Q	122
LD1X4	Q(0/1/2/3)	59
	QN(0/1/2/3)	60
LD1X4D2	Q(0/1/2/3)	124
	QN(0/1/2/3)	122
YLD1	Q	50
	QN	61
YLD1D2	Q	102
	QN	126
LD1A	Q	47
LD1B	QN	11
	ZN	47
LD2	All Pins	60
LD2D2	Q	121
	QN	124
LD2Q	Q	60
LD2QD2	Q	124
YLD2	Q	49
	QN	48
YLD2D2	Q	54
	QN	101
LD3	All Pins	60
LD3D2	Q	124
	QN	121

Cell Name	Output Pin	Maximum Fanout
LD4	Q	60
	QN	59
LD4D2	Q	123
	QN	122
LD5	Q	59
	QN	60
LD5D2	Q	122
	QN	121
LD5S	Q	59
	QN	60
LD5SD2	Q	123
	QN	122
LD5X4	Q(0/1/2/3)	59
	QN(0/1/2/3)	60
LD5X4D2	Q(0/1/2/3)	123
	QN(0/1/2/3)	122
LD6	All Pins	60
LD6D2	Q	121
	QN	124
LD7	All Pins	60
LD7D2	Q	124
	QN	121
LD8	Q	60
	QN	59
LD8D2	Q	123
	QN	121
LDS2	Q	59
	QN	60
LDS6	Q	59
	QN	60
LS0	All Pins	43
LS0D2	All Pins	86
LS1	All Pins	20
LS2	All Pins	43
Bus Holder		
BUSHOLDER	Y	10,000
Internal Clock Drivers		
CK2	Y	Fig 1-16 (a)
CK4	Y	Fig 1-16 (b)
CK6	Y	Fig 1-16 (c)
CK8	Y	Fig 1-16 (d)
Decoders		

Cell Name	Output Pin	Maximum Fanout
DC4	Y0	59
	Y(1/2/3)	60
DC4I	YN(0/2)	48
	YN(1/3)	49
DC8I	All Pins	32
Adders		
FA	All Pins	59
FAD2	S	117
	CO	115
HA	All Pins	59
HAD2	S	114
	CO	123
Multiplexers		
MX2	Y	59
MX2D3	Y	170
MX2X4	Y(0/1/3)	60
	Y2	59
YMX2	Y	59
YMX2D2	Y	121
MX2I	YN	31
MX2ID2	YN	122
MX2IA	YN	31
MX2ID2A	YN	122
MX2IX4	YN0	31
	YN(1/2/3)	32
MX3I	YN	59
MX3ID2	YN	122
MX4	Y	56
MX4D2	Y	107
YMX4	Y	59
YMX4D2	Y	114
MX5	Y	59
MX5D2	Y	116
MX8	Y	51
MX8D2	Y	94
YMX8	Y	59
YMX8D2	Y	112

I/O Cells

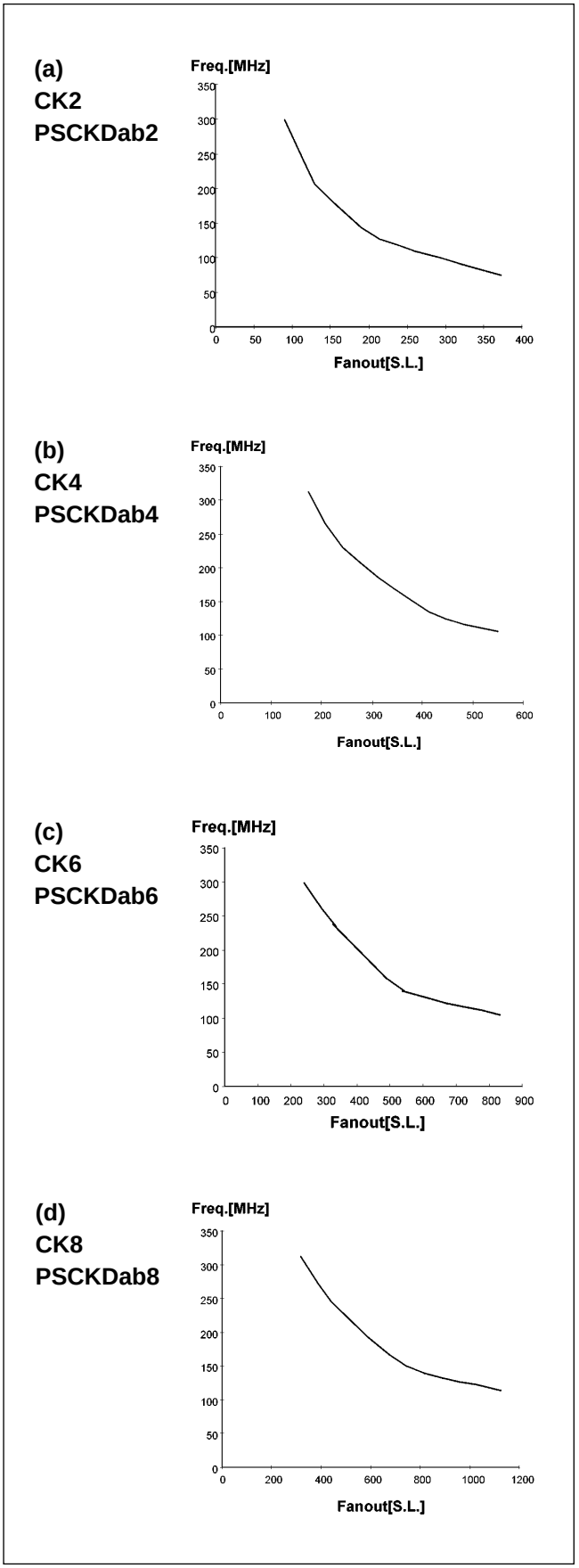
The maximum fanouts for 3.3V and 5V I/O cells are as follows when the rise and fall times of the input signal is 0.40ns.

The graphs for fanout vs. frequency curve of STDL80 internal/input clock drivers are shown below.

Table 1-9. Maximum Fanouts of I/O Cells (When t_R/t_F = 0.40ns)

Cell Name	Output Pin	Maximum Fanouts
PIC	PO	172
	Y	350
PICD	PO	174
	Y	405
PICU	PO	178
	Y	350
PIS	PO	181
	Y	716
PISD	PO	181
	Y	659
PISU	PO	181
	Y	658
PSCKDab2	Y	Fig 1-14 (a)
PSCKDab4	Y	Fig 1-14 (b)
PSCKDab6	Y	Fig 1-14 (c)
PSCKDab8	Y	Fig 1-14 (d)
PSOSCK(1/16)	PADY	10
	YN	38
PSOSCK(2/26)	PADY	102
	YN	339
PSOSCM(1/16) PSOSCM(2/26)	PADY	1163
	YN	940
PSOSCM(3/36)	PADY	2328
	YN	1689
PSOSCM(4/46)	PADY	4650
	YN	2529
PSOSCM(5/56)	PADY	7058
	YN	1330
PSOSCM(6/66)	PADY	9577
	YN	5032

Figure 1-16. Fanout (SL) vs. Frequency Curve of STDL80 Clock Drivers



PRODUCT LINE-UP

Table 1-10. Optimum Gates vs. Pad Numbers on STD80/STDM80

Ref. No	Estimated Gates	Total Pads		Maximum I/O Pads	
		TLM (70%)	DLM (40%)	TLM	DLM
01	10,000	57	75	41	59
02	15,000	70	93	54	77
03	20,000	81	107	65	91
04	30,000	99	131	83	115
05	40,000	114	151	98	135
06	50,000	128	169	112	153
07	60,000	140	186	124	170
08	70,000	151	201	135	185
09	80,000	162	214	146	198
10	90,000	172	227	156	211
11	100,000	181	240	175	224
12	120,000	198	263	182	247
13	140,000	214	284	198	268
14	160,000	229	303	213	287
15	180,000	243	322	227	306
16	200,000	256	339	240	323
17	250,000	287	379	271	363
18	300,000	314	416	298	400
19	350,000	339	449	323	433
20	400,000	363	480	347	464
21	450,000	385	509	369	493
22	500,000	406	537	390	521

NOTE: Chip size can be changed depending on the circuit design.

PACKAGES

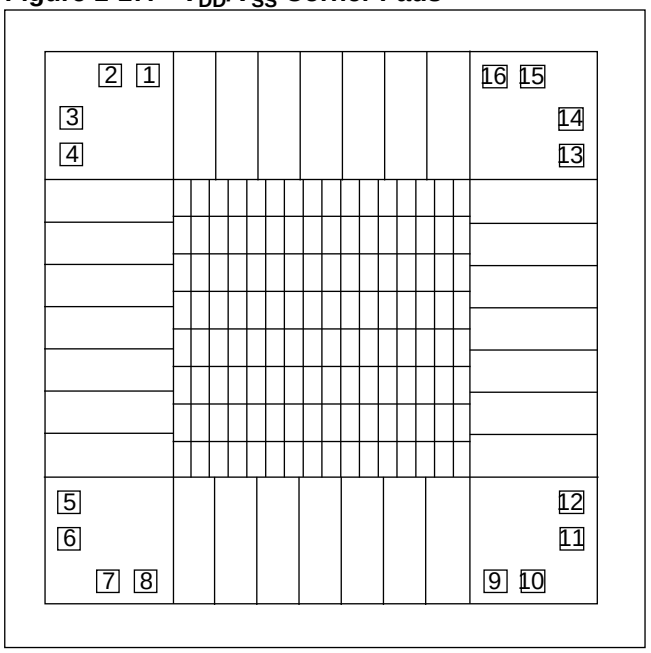
Type	DIP	SDIP	SOP	PLCC	QFP
Pin Count	24	24	28	28	44
	28	28	32	32	48
	40	30		44	60
	42	32		68	64
		40		84	80
		42			100
		48			128
		54			132
		56			160
		64			208
					240

NOTE: The selection of a package type and pin count is dependent on the size of a chip.

DEDICATED CORNER V_{DD}/V_{SS} PADS

The corner pads shown in the following figure are well-suited for double bonding purposes. Pad 1 and pad 2 can be bonded to the same package pin. Unlike normal I/O pads, these pads can only be used for V_{DD}/V_{SS} listed in Table 1-11. Use of Corner Pads.

Figure 1-17. V_{DD}/V_{SS} Corner Pads



NOTES:

1. There is no dedicated corner VSSI pad. Therefore, internal V_{SS} must be supplied using I/O pad type cell.
2. Corner pads are used to reduce the power/ground noise when some parts of the design cause noise problem especially while the other parts keep quiet.

Table 1-11. Use of Corner Pads

1	VSSO	9	VDD3O
2	VSSO	10	VDD3O
3	VSSI	11	VSSI
4	VSSI	12	VSSI
5	VDDI	13	VDDI
6	VDDI	14	VDDI
7	VDD5O	15	VSSO
8	VDD5O	16	VSSO

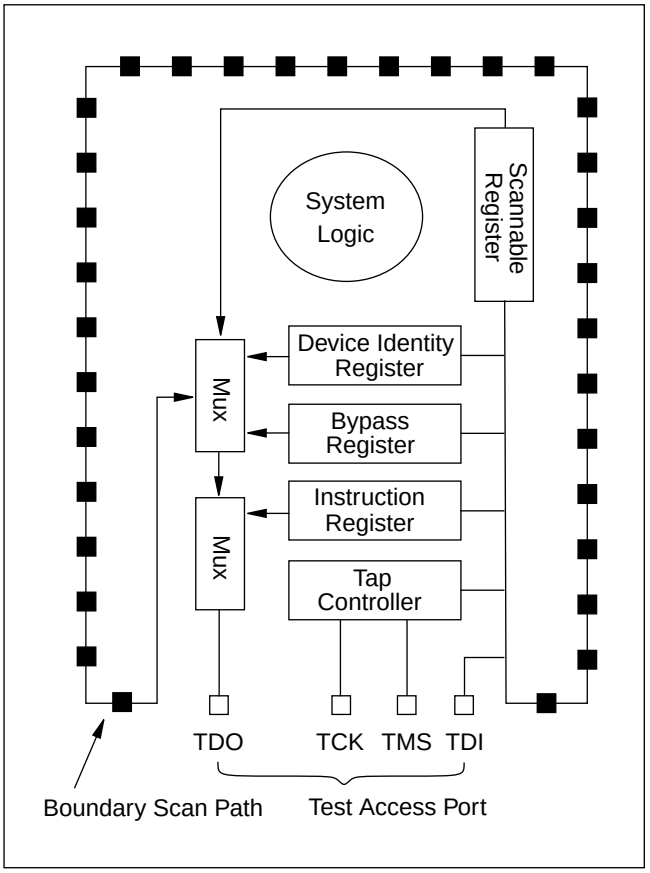
TESTABILITY DESIGN METHODOLOGY

Scan Design

- Multiplexed scan flip-flop that minimizes the area or delay overhead needed to implement scan design
- Automated design rules checking, scan insertion, and test pattern generation
- High fault coverage on synchronous designs

Boundary-Scan

- IEEE Std 1149.1
- 5 types of JTAG boundary-scan cells
- Boundary-Scan Description Language (BSDL) description for board testing
- Combination with internal scan design



EXTERNAL DESIGN INTERFACE CONSIDERATIONS

This section briefly describes what you should consider when chips interface with outside world especially for a noise protection.

Input Buffer

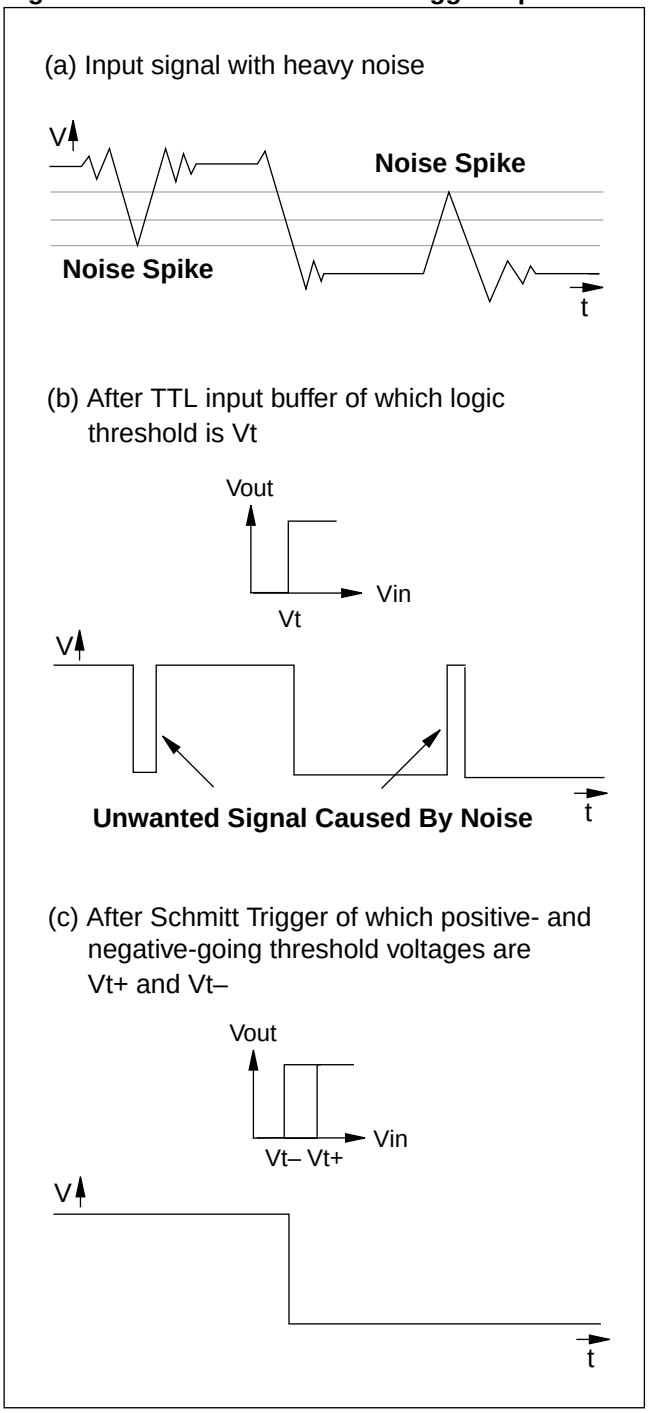
Usually there are three types of input receivers in ASIC libraries; TTL input buffer, CMOS input buffer, and various Schmitt trigger input buffers.

TTL input buffer has relatively poor noise characteristics because of its shifted logic threshold voltage. CMOS input buffer is better than TTL against a noise because the logic threshold voltage is near 2.5volt. If an input signal has relatively large noise spikes, it could cause an unwanted input signal.

When an input signal is very noisy, the noise can be filtered by using a Schmitt trigger input buffer. As shown in Figure 1-18. Effect of Schmitt Trigger Input Buffer, Schmitt trigger input buffers have two different input thresholds for positive- and negative-going signals. This hysteresis between positive- and negative-going voltage signals can filter a noisy signal to a wanted one.

According to applications, the most suitable one can be chosen among the various Schmitt trigger input buffers having different levels of threshold voltage.

Figure 1-18. Effect of Schmitt Trigger Input Buffer



Output Pad Cell

As incoming signals to a chip have a noise, the noise can also be induced by the operation of the chip itself. There are several sources of a noise, but the greatest singular source of a noise is the switching of an output with high capacitive load.

Figure 1-19. Simple Model of Output Pad Cell

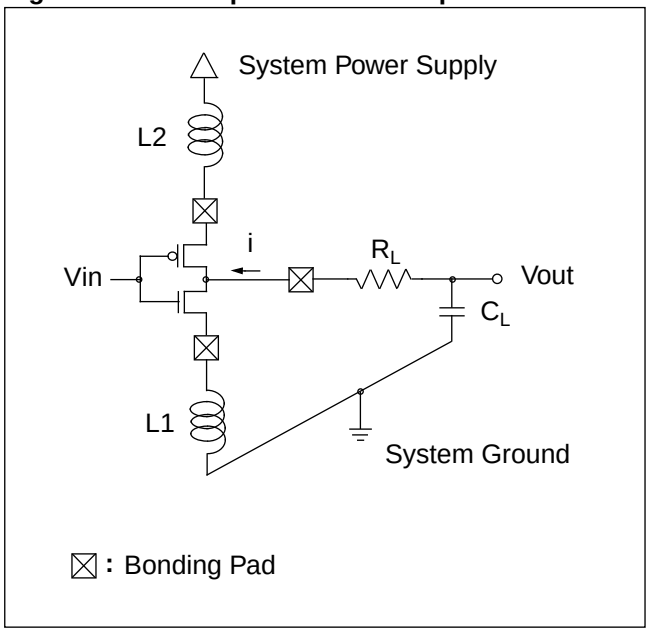


Figure 1-19. Simple Model of Output Pad Cell shows the simple model of an output driver considering the external interface. L1 and L2 are parasitic inductances of the package and C_L is an output load. Vout will fall as Vin rises and the current i flows through n-transistor discharging the loaded charge ($V_{DD} \times C_L$).

The details of this operations are described in Figure 1-20. Ground Bounce Phenomenon.

The important phenomenon which can be observed in this figure is that the voltage level Vn shifts relative to the system ground. Vn is the ground of the chip.

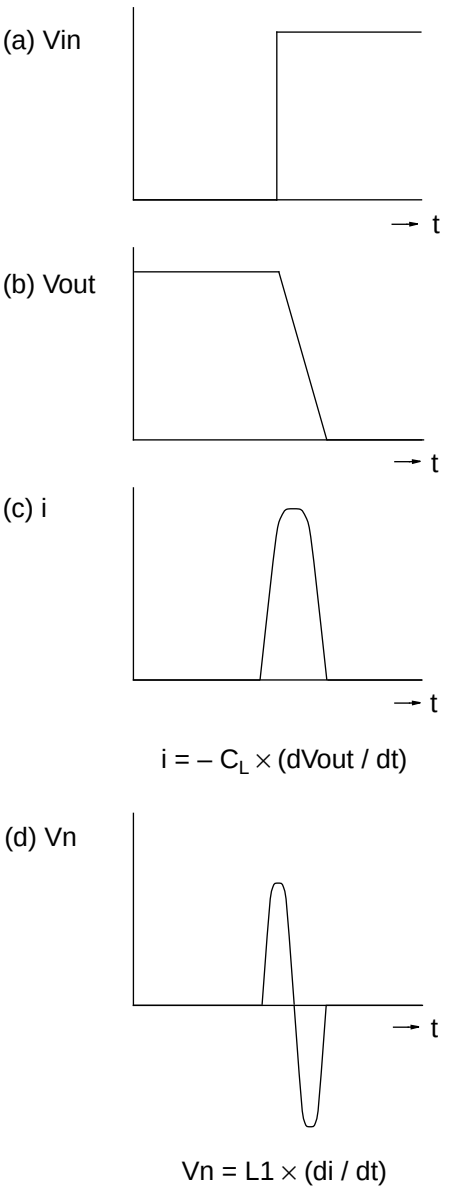
This phenomenon is called as a “ground bounce” that is the chip reference shift caused by the external inductance and the transient current flow to the ground.

The amount of voltage level shifted by the ground bounce is

$$Vn = -L \times (di / dt)$$

When the output driver makes a low-to-high transition, the similar noise problem is generated on the power.

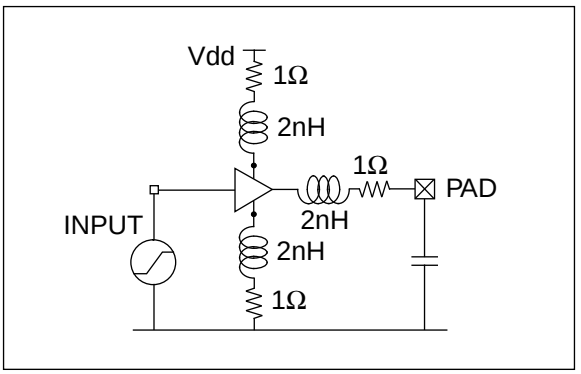
Figure 1-20. Ground Bounce Phenomenon



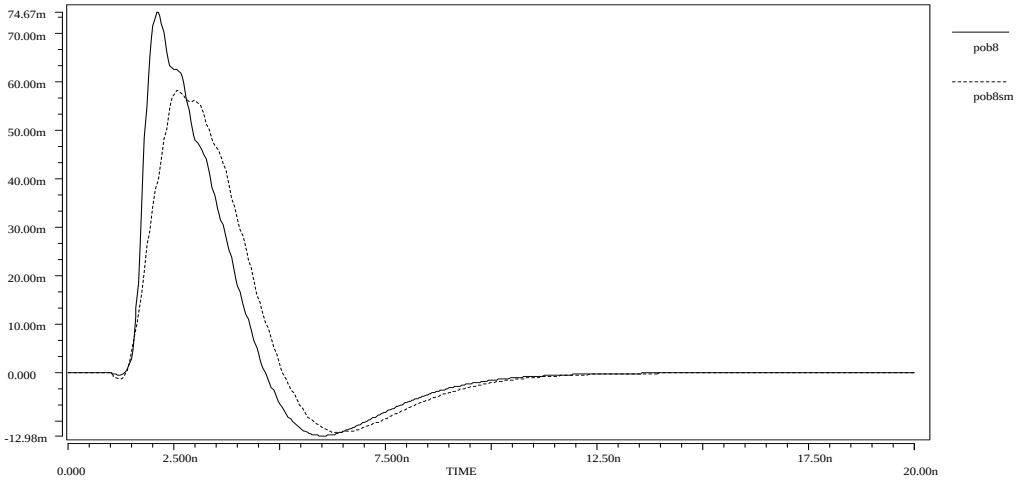
The following graphs “AC Characteristics of Non-Slew and Slew Rate Output Drives” show typical AC characteristics of non-slew and slew-rate output drives in STDL80. Using the slew-rate control, you can reduce the switching noise.

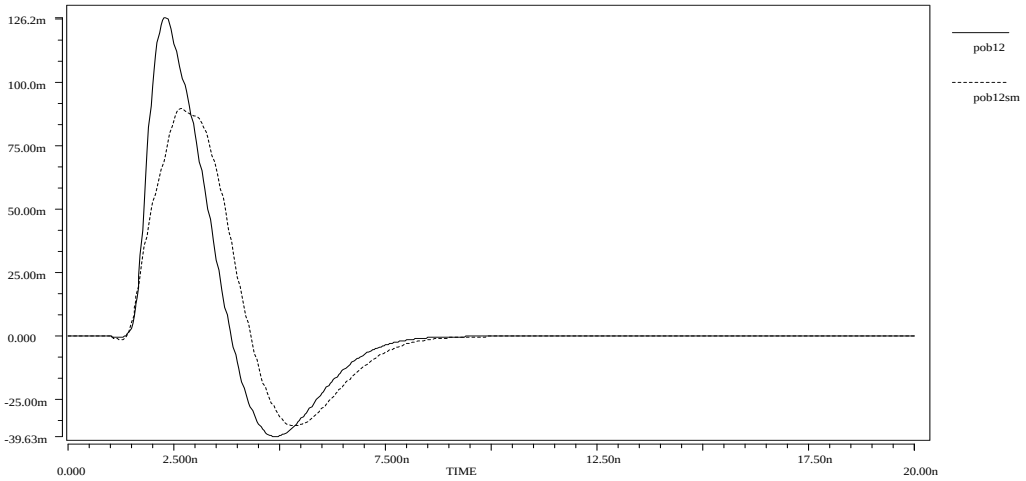
Figure 1-21. AC Characteristics of Non-Slew and Slew Rate Output Drives

< Test Condition >

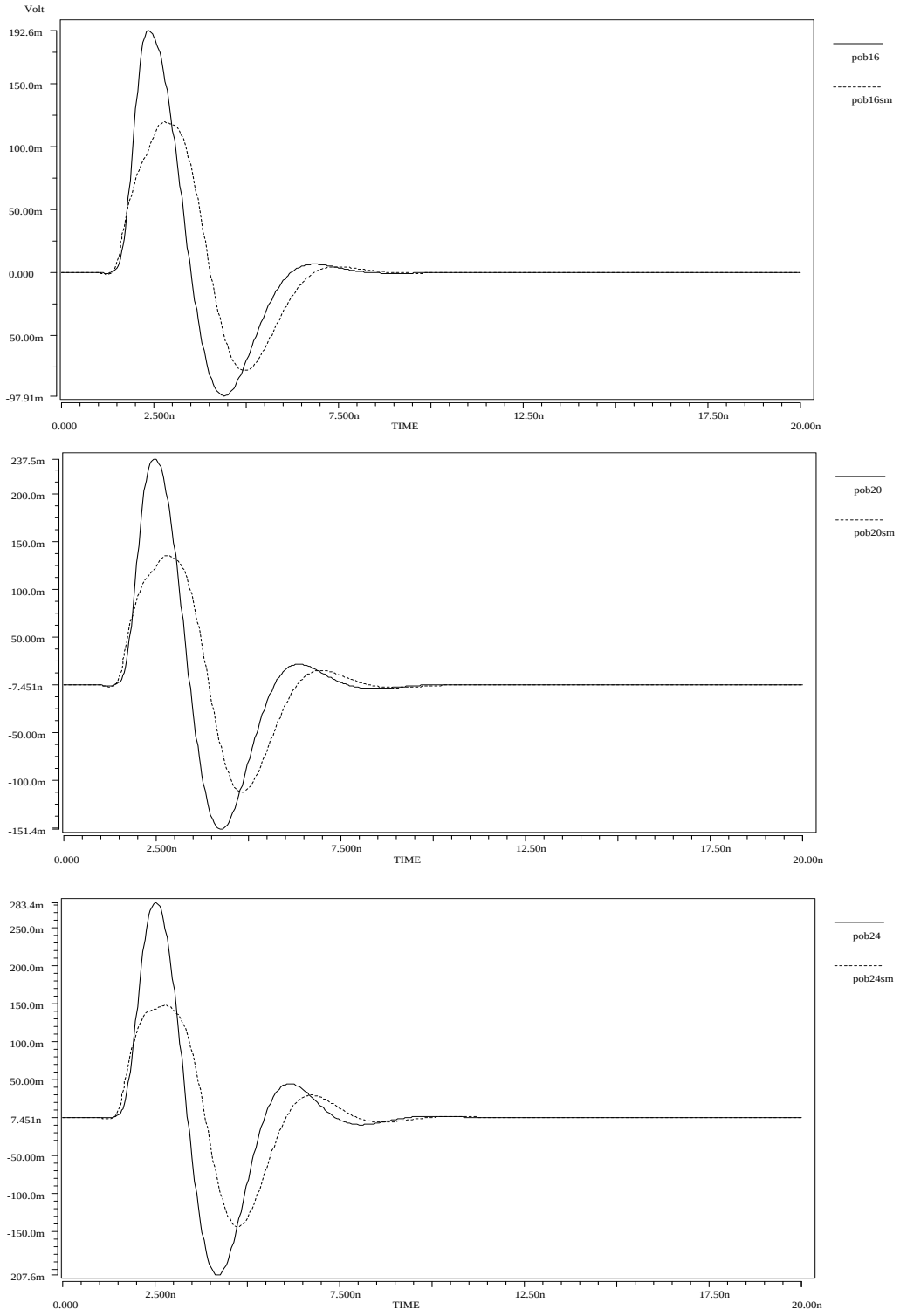


Ground Bouncing Voltage vs. Time





Ground Bouncing Voltage vs. Time



Simultaneous Switching Outputs (SSOs)

If several output drivers switch from high to low simultaneously, the ground bouncing level becomes quite large because the current flowing through the inductance L is the total sum of the transient current of each output driver. The amount of total current and the level of ground bounce are proportional to the number of SSOs.

This ground bounce can cause two types of problems, a noise margin reduction and a generation of noise spike on the output pad.

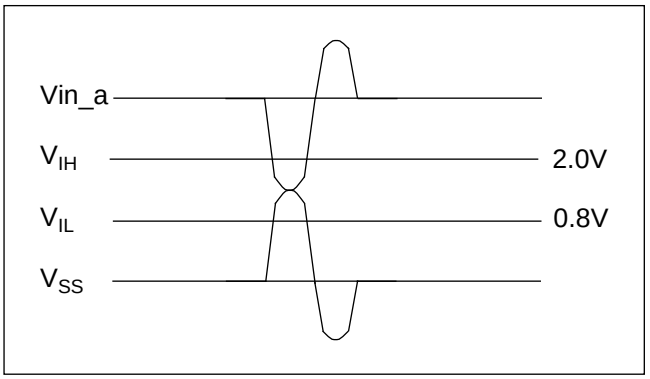
NOISE MARGIN REDUCTION

The ground bounce can cause a noise margin reduction when the same ground bus is used for both input buffers and output drivers as shown in Figure 1-23. The Figure of SSOs. The noise margin reduction can be explained using the circuit in the same figure.

As you can see, if outputs switch from high to low simultaneously, it results in a ground bounce or the rise of the chip ground level relative to system ground. The rise appears as the input voltage Vin_a is below V_{IH} causing false triggering of the input buffer. Vin is, in this case, not the same as Vin_a. Note that Vin is measured relative to the system ground, while Vin_a is measured relative to the local device ground.

This phenomenon is shown in Figure 1-22. Noise Margin Reduction due to SSOs. For a low-to-high transition, it is the low input levels (V_{IL}) that are affected.

Figure 1-22. Noise Margin Reduction due to SSOs

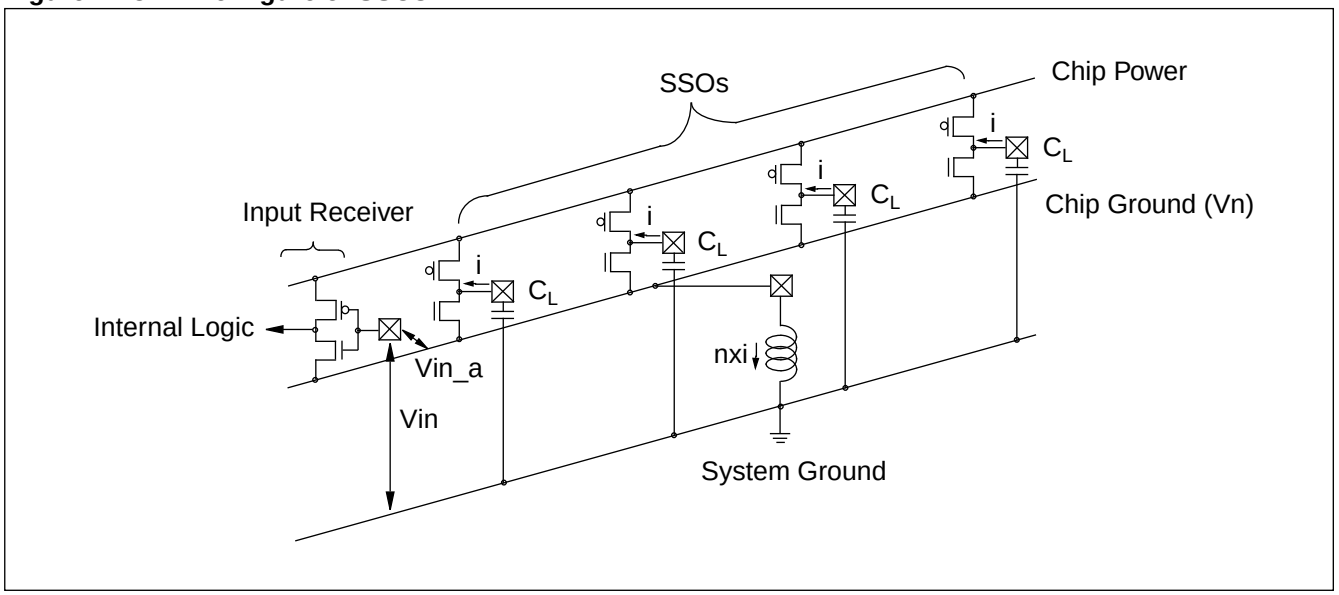


NOISE SPIKE GENERATION ON STABLE OUTPUT

If input and output power buses are separated, the problem of a noise margin reduction in the input buffer can be solved. However, ground bounce can cause another problem in spite of using separated power and ground bus.

The Figure 1-24. Noise Spike Induced by Ground Bounce shows a common octal driver application where ground bounce spikes will be observable on the one stable output. If the spike is considered as high by another chip, this ground bounce may upset that operation of interfacing device or cause system logic errors.

Figure 1-23. The Figure of SSOs



For example, suppose C_L = 100pF, V_{DD} = 3.3Volt, t_F = 5ns. From Figure 1-20. Ground Bounce Phenomenon, the maximum current flow occurs at time $0.5 \times t_F$. Then approximately,

$i = C_L \times (dv / dt) \cong C_L \times (\Delta V / \Delta t)$,
and

$i\ (max) = 100 \times 10^{-12} \times \{5 / (2.5 \times 10^{-9})\} = 200$ [mA].

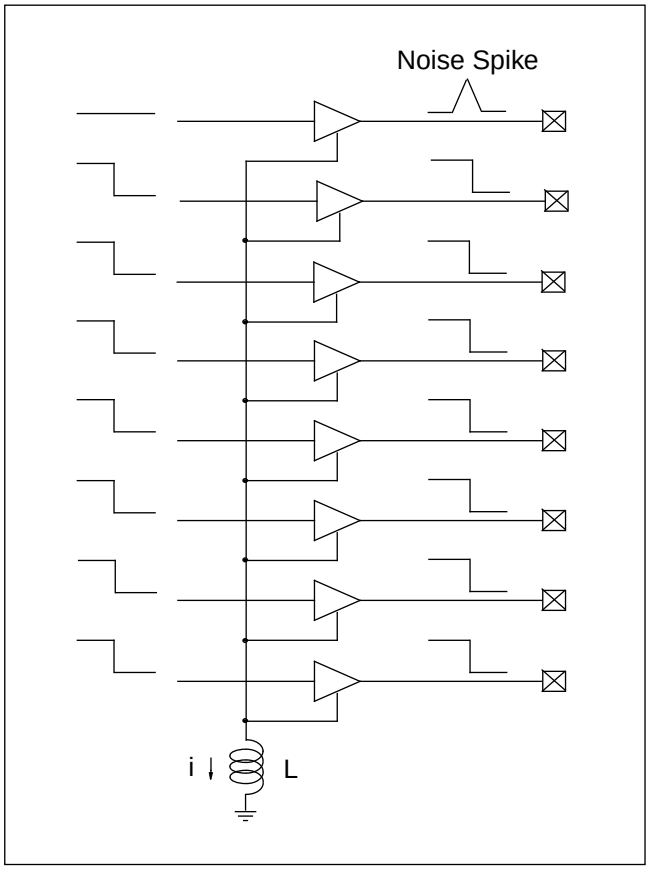
If the number of SSOs is 5, and L is 4nH,

$Vn = L \times (di / dt) \times N \cong L \times (\Delta i / \Delta t) \times N$ by approximation,

$Vn\ (max) = 4 \times 10^{-9} \times \{0.200 / (2.5 \times 10^{-9})\} \times 5 = 1.60$ [Volt].

From this calculation, 1.60V of noise spike is expected. This is about logic threshold voltage of TTL. This numerical estimate clearly shows that power bus noise control is one of the fundamental problems in a high-speed CMOS VLSI design. It is an important design consideration to prevent the noise from affecting the integrity of the logic operation of a chip.

Figure 1-24. Noise Spike Induced by Ground Bounce



How to Protect Ground Bounce?

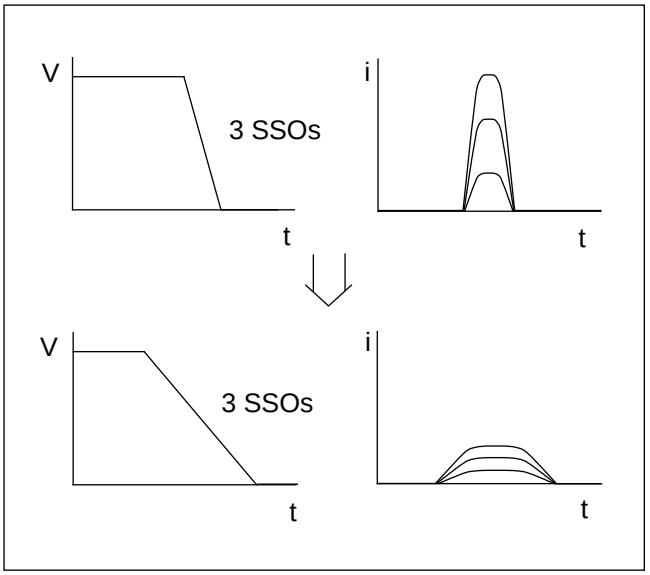
The fundamental solution to the ground bounce problem is to reduce the inductance of the package. However, in the boundary of a given packaging technology, the following guidelines can be used for reducing ground bounce:

(1) If possible, use separate power and ground buses for input buffers and output drivers.

(2) The number of ground and power pads should not be less than the required number of pads.

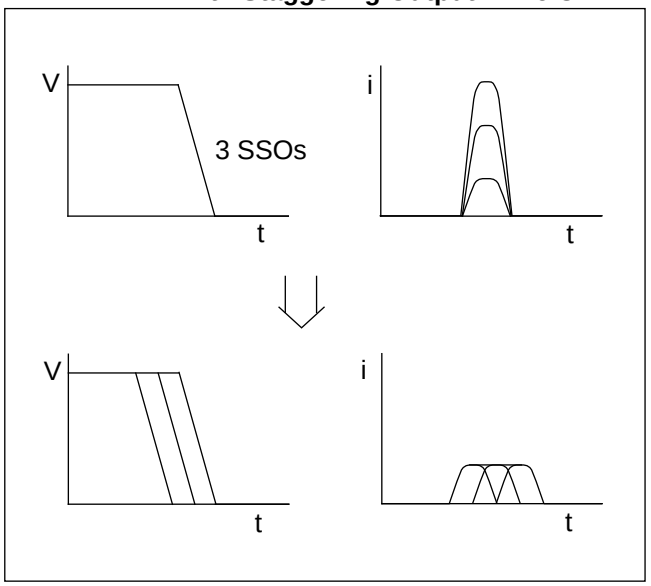
(3) If the design is not so much sensitive to speed, use slew rate control, i.e., increase switching time, to reduce the value of di / dt of an output driver. SEC supports two levels of slew rate controlled output buffers, SM and SH. You can see this effect in the following figure.

Figure 1-25. Effect on Reducing Peak Current with Slew-Rate Control



(4) If you cannot use a slew rate cell because of the speed requirement, you can stagger the output driver as shown in Figure 1-26. Effect on Reducing Peak Current with Staggering Output Drivers. This is not a general-purpose solution. It makes sense only when special relief in timing requirements exists from a system architecture.

Figure 1-26. Effect on Reducing Peak Current with Staggering Output Drivers



(5) High-drive outputs should be close to V_{SS} pins. SSOs should be placed particularly close to V_{SS} pins.

(6) SSOs should be appropriately placed in groups belonging to given V_{SS} pins.

(7) Noise-sensitive signals such as clock, asynchronous clear and preset should be located away from SSOs and high-drive outputs. Also, assign them to pins with low inductance and resistance, preferably near V_{SS}, if one is available away from SSOs or high-drive outputs.

(8) Place SSOs on low inductance pins, such as those located on the inner rows or middle positions of PGAs.

(9) Clock, preset and clear inputs must not be placed on the corners of a package, especially when the array is packaged in DIP.

(10) Output signals to be used as clock, preset or clear for other devices must be kept away from SSOs and close to V_{SS} pin.

These guidelines assist you in choosing the best package(s) for the application. Furthermore, the recommendations about pinout results in reliable and predictable devices that minimizes harmful DC and AC effects on the system.

CRYSTAL OSCILLATOR CONSIDERATIONS

Overview

STDL80 contains a circuit commonly referred to as an “on-chip oscillator.” The on-chip circuit itself is not an oscillator but an amplifier which is suitable for being used as the amplifier part of a feedback oscillator. With proper selection of off-chip components, this oscillator circuit performs better than any other types of clock oscillators.

It is very important to select suitable off-chip components to work with the on-chip oscillator circuitry. It should be noted, however, that SEC cannot assume the responsibility of writing specifications for the off-chip components of the complete oscillator circuit, nor of guaranteeing the performance of the finished design in production, anymore than a transistor manufacturer, whose data sheets show a number of suggested amplifier circuits, can assume responsibility for the operation, in production, of any of them.

We are often asked why we don’t publish a list of required crystal or ceramic resonator specifications, and recommend values for the other off-chip components. This has been done in the past, but sometimes with consequences that were not intended.

Suppose we suggest a maximum crystal resistance of 30 ohms for some given frequency. Then your crystal supplier tells you the 30 ohm crystals are going to cost twice as much as 50 ohm crystals. Fearing that SEC will not “guarantee operation” with 50 ohm crystals, you order the expensive ones.

In fact, SEC guarantees only what is embodied within an SEC product. Besides, there is no reason why 50 ohm crystals couldn’t be used, if the other off-chip components are suitably adjusted.

Should we recommend values for the other off-chip components? Should we do for 50 ohm crystals or 30 ohm crystals? With respect to what should we optimize their selection? Should we minimize start-up time or maximize frequency stability?

In many applications, neither start-up time nor frequency stability is particularly critical, and our “recommendations” are only restricting your system to unnecessary tolerances. It all depends on the application.

Oscillator Design Considerations

ASIC designers have a number of options for clocking the system. The main decision is whether to use the “on-chip” oscillator or an external oscillator. If the choice is to use the on-chip oscillator, what kinds of external components are to use an external oscillator, what type of oscillator would it be?

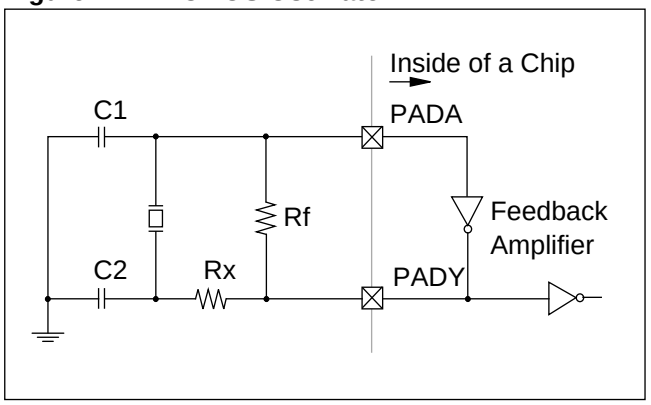
The decisions have to be based on both economic and technical requirements. In this section we will discuss some of the factors that should be considered.

ON-CHIP OSCILLATOR

In most cases, the on-chip amplifier with the appropriate external components provides the most economical solution to the clocking problem. Exceptions may arise in server environments when frequency tolerances are tighter than about 0.01%.

The external components that commonly used for CMOS gate oscillator are a positive reactance (normal crystal oscillator), two capacitors, C1 and C2, and two resistor Rf and Rx as shown in the figure below.

Figure 1-27. CMOS Oscillator



CRYSTAL SPECIFICATIONS

Specifications for an appropriate crystal are not very critical, unless the frequency is. Any fundamental-mode crystal of medium or better quality can be used.

We are often asked what maximum crystal resistance should be specified. The best answer to that question is the lower the better, but use what is available.

The crystal resistance will have some effect on start-up time and steady-state amplitude, but not so much that it can’t be compensated for by appropriate selection of the capacitances, C1 and C2.

Similar questions are asked about specifications of load capacitance and shunt capacitance. The best advice we can give is to understand what these parameters mean and how they affect the operation of the circuit (that being the purpose of this application note), and then to decide for yourself if such specifications are meaningful in your frequency tolerances are tighter than about 0.1%.

Part of the problem is that crystal manufacturers are accustomed to talking “ppm” tolerances with radio engineers and simply won’t take your order until you’ve filled out their list of frequency tolerance requirements, both for yourself and to the crystal manufacturer. Don’t pay for 0.003% crystals if your actual frequency tolerance is 1%.

OSCILLATION FREQUENCY

The oscillation frequency is determined 99.5% by the crystal and up to about 0.5% by the circuit external to the crystal.

The on-chip amplifier has little effect on the frequency, which is as it should be, since the amplifier parameterizes temperature and process dependent.

The influence of the on-chip amplifier on the frequency is by means of its input and output (pin-to-ground) capacitances, which parallel C1 and C2, and the PADA-to-PADY (pin-to-pin) capacitance, which parallels the crystal. The input and pin-to-pin capacitances are about 7 pF each.

Internal phase deviations capacitance of 25 to 30 pF. These deviations from the ideal have less effect in the positive reactance oscillator (with the inverting amplifier) than in a comparable series resonant oscillator (with the non-inverting amplifier) for two reasons: first, the effect of the output capacitor; second, the positive reactance oscillator is less sensitive, frequency-wise, to such phase errors.

C1 / C2 SELECTION

Optimal values for the capacitors C1 and C2 depend on whether a quartz crystal or ceramic resonator is being used, and also on application-specific requirements on start-up time and frequency tolerance.

Start-up time is sometimes more critical in microcontroller systems than frequency stability, because of various reset and initialization requirements.

Less commonly, accuracy of the oscillator frequency is also critical, for example, when the oscillator is being used as a time base. As a general rule, fast start-up and stable frequency tend to pull the oscillator design in opposite directions.

Considerations of both start-up time and frequency stability over temperature suggest that C1 and C2 should be about equal and at least 20pF. (But they don't have to be either.)

Increasing the value of these capacitances above some 40 or 50pF improves frequency stability. It also tends to increase the start-up time. These is a maximum value (several hundred pH, depending on the value of R1 of the quartz or ceramic resonator) above which the oscillator won't start up at all.

If the on-chip amplifier is a simple inverter, the user can select values for C1 and C2 between some 20 and 100pF, depending on whether start-up time or frequency stability is the more critical parameter in a specific application.

RF / RX SELECTION

A CMOS inverter might work better in this application since a large Rf (1mega-ohm) can be used to hold the inverter in its linear region.

Logic gates tend to have a fairly low output resistance, which testabilizes the oscillator. For that reason a resistor Rx (several k-ohm) is often added to the feedback network, as shown in Figure 1-27. CMOS Oscillator.

At higher frequencies a 20 or 30pF capacitor is sometimes used in the Rx position, to compensate for some of the internal propagation delay.

PIN CAPACITANCE

Internal pin-to-ground and pin-to-pin capacitances, and PADA and PADY have some effect on the oscillator. These capacitances are normally taken to be in the range of 5 to 10pF, but they are extremely difficult to evaluate. Any measurement of one such capacitance necessarily include effects from the others.

One advantage of the positive reactance oscillator is that the pin-to ground cap. is paralleled by an external bulk capacitance, so a precise determination of their value is unnecessary.

We would suggest that there is little justification for more precision than to assign them a value of 7pF (PADA-to-ground and PADA-to-PADY). This value is probably not in error by more than 3 or 4pF.

The PADY-to-ground cap. is not entirely a "pin capacitance", but more like an "equivalent output capacitance" of some 25 to 30pF, having to include the effect of internal phase delays. This value varies to some extent with temperature, process, and frequency.

PLACEMENT OF COMPONENTS

Noise glitches arising at PADA or PADY pins at the wrong time can cause a miscount in the internal clock-generating circuitry. These kinds of glitches can be produced through capacitive coupling between the oscillator components and PCB traces carrying digital signals with fast rise and fall times.

For this reason, the oscillator components should be mounted close to the chip and have short, direct traces to the PADA, PADY, and V_{SS} pins.

If possible, use dedicated V_{SS} and V_{DD} pin for only crystal feedback amplifier.

Troubleshooting Oscillator Problems

The first thing to consider in case of difficulty is that there may be significant differences in stray caps between the test jig and the actual application, particularly if the actual application is on a multi-layer board.

Noise glitches, that are not present in the test jig but are in the application board, are another possibility. Capacitive coupling between the oscillator circuitry and other signal has already been mentioned as a source of miscounts in the internal clocking circuitry. Inductive coupling is also doubtful, if there is strong current nearby. These problems are a function of the PCB layout.

Surrounding oscillator components with “quit” traces (for example, VCC and ground) will alleviate capacitive coupling to signals having fast transition time. To minimize inductive coupling, the PCB layout should minimize the areas of the loops formed by oscillator components.

The loops demanding to be checked are as follows:

PADA through the resonator to PADY;
PADA through C1 to the V_{SS} pin;
PADY through C2 to the V_{SS} pin.

It is not unusual to find that the ground ends of C1 and C2 eventually connect up to the V_{SS} pin only after looping around the farthest ends of the board. Not good.

Finally, it should not be overlooked that software problems sometimes imitate the symptoms of a slow-starting oscillator or incorrect frequency. Never underestimate the perversity of a software problem.

Electrical Characteristics 2

Contents

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V ± 10%, T_A = 0 to 70°C (Normal 3.3V I/O)

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	High level input voltage				V
	CMOS interface		$0.7V_{DD}$		
	CMOS schmitt trigger			2.1	
V_{IL}	Low level input voltage				V
	CMOS interface			$0.3V_{DD}$	
	CMOS schmitt trigger		0.8		
I_{IH}	High level input current				µA
	Input buffer	$V_{IN} = V_{DD}$	–10	10	
	Input buffer with pull-down		10	200	
I_{IL}	Low level input current				µA
	Input buffer	$V_{IN} = V_{SS}$	–10	10	
	Input buffer with pull-up		–200	–10	
V_{OH}	High level output voltage				V
	Type B1 to B24[Note1]	I_{OH} = –1µA	V_{DD} – 0.05		
	Type B1	I_{OH} = –1mA	2.4		
	Type B2	I_{OH} = –2mA			
	Type B4	I_{OH} = –4mA			
	Type B8	I_{OH} = –8mA			
	Type B12	I_{OH} = –12mA			
	Type B16	I_{OH} = –16mA			
	Type B20	I_{OH} = –20mA			
	Type B24	I_{OH} = –24mA			
V_{OL}	Low level output voltage				V
	Type B1 to B24	I_{OL} = 1µA		0.05	
	Type B1	I_{OL} = 1mA		0.4	
	Type B2	I_{OL} = 2mA			
	Type B4	I_{OL} = 4mA			
	Type B8	I_{OL} = 8mA			
	Type B12	I_{OL} = 12mA			
	Type B16	I_{OL} = 16mA			
	Type B20	I_{OL} = 20mA			
	Type B24	I_{OL} = 24mA			
I_{OZ}	Tri-state output leakage current	$V_{OUT} = V_{SS}$ or V_{DD}	–10	10	µA
I_{DD}	Quiescent supply current	$V_{IN} = V_{SS}$ or V_{DD}		100[Note2]	µA

NOTES:

1. Type B1 means 1mA output driver cells, and Type B24 means 24mA output driver cells.
2. This value depends on the customer design.

V_{DD} = 3.3V ± 10%, V_{BB} = 5V ± 5%, T_A = 0 to 70°C (5V Tolerant I/O)

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	High level input voltage				V
	CMOS interface		0.7V_{DD}		
	CMOS schmitt trigger			2.1	
V_{IL}	Low level input voltage				V
	CMOS interface			0.3V_{DD}	
	CMOS schmitt trigger		0.8		
I_{IH}	High level input current				µA
	Input buffer	V_{IN} = 5V	–10	10	
	Input buffer with pull-down		10	200	
I_{IL}	Low level input current				µA
	Input buffer	V_{IN} = V_{SS}	–10	10	
	Input buffer with pull-up		–200	–10	
V_{OH}	High level output voltage				V
	Type B1 to B6	I_{OH} = –1µA	V_{DD} – 0.05		
	Type B1	I_{OH} = –1mA	2.4		
	Type B2	I_{OH} = –2mA			
	Type B4	I_{OH} = –4mA			
	Type B6	I_{OH} = –6mA			
V_{OL}	Low level output voltage				V
	Type B1 to B6	I_{OL} = 1µA		0.05	
	Type B1	I_{OL} = 1mA		0.4	
	Type B2	I_{OL} = 2mA			
	Type B4	I_{OL} = 4mA			
	Type B6	I_{OL} = 6mA			

Absolute Maximum Ratings

Symbol	Parameter		Rating	Unit
V_{DD}	DC supply voltage		–0.3 to 4.6	V
V_{BB}	PMOS bulk bias		–0.3 to 6	
V_{IN}	DC input voltage	5V	–0.3 to V_{DD}+0.3	
		3.3V	–0.3 to V_{BB}+0.3	
I_{IN}	DC input current		±10	mA
T_{STG}	Storage temperature		–40 to 125	°C

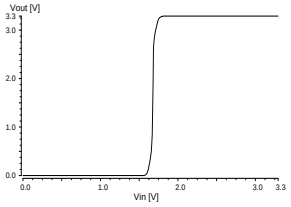
Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	3.0 to 3.6	V
V_{BB}	PMOS bulk bias	5 ± 0.25	
T_A	Commercial temperature	0 to 70	°C
	Industrial temperature	–40 to 85	

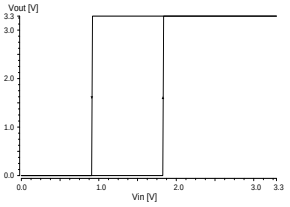
INPUT BUFFER DC CURVES

Input Buffer Transfer Curves

V_{DD} = 3.3V, T_A = 25°C, Typical Process

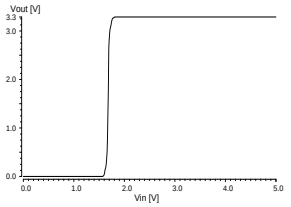


CMOS

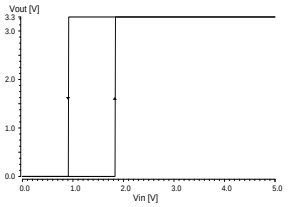


CMOS Schmitt Trigger

V_{DD} = 3.3V, V_{BB} = 5V, T_A = 25°C, Typical Process



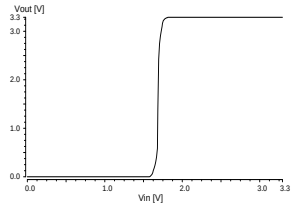
CMOS



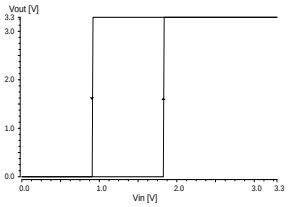
CMOS Schmitt Trigger

Input Clock Drivers Transfer Curves

V_{DD} = 3.3V, T_A = 25°C, Typical Process

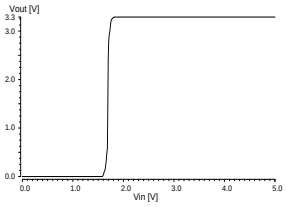


CMOS

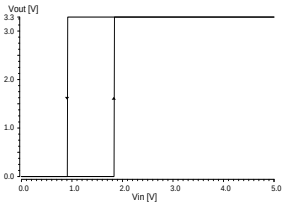


CMOS Schmitt Trigger

V_{DD} = 3.3V, V_{BB} = 5V, T_A = 25°C, Typical Process



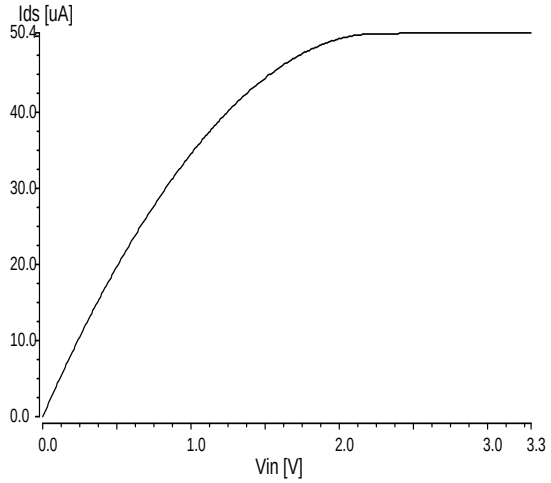
CMOS



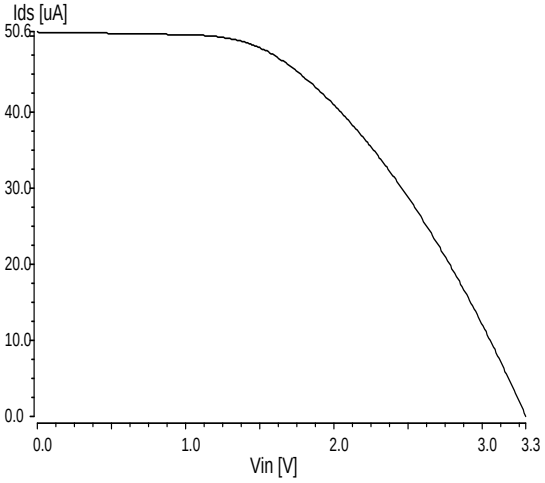
CMOS Schmitt Trigger

Input Buffer Pull-Down/Pull-Up Characteristics

V_{DD} = 3.3V, T_A = 25°C, Typical Process



Pull-Down

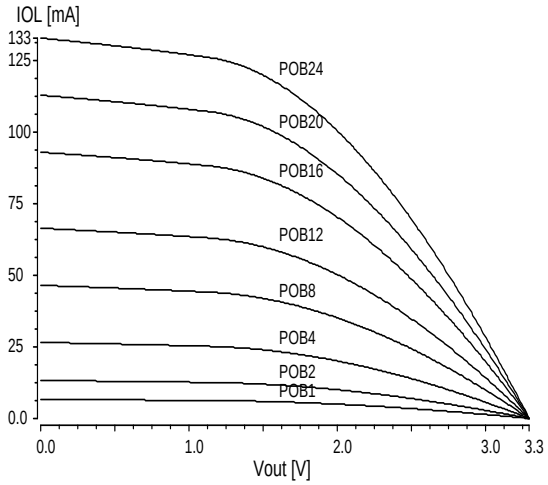


Pull-Up

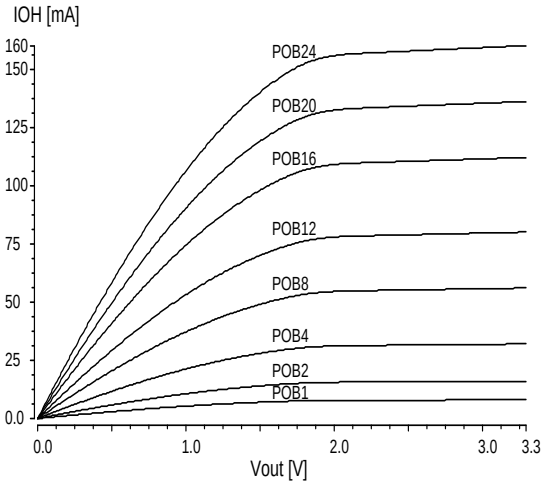
OUTPUT DRIVE CAPABILITIES

IV Characteristics

V_{DD} = 3.3V, T_A = 25°C, Typical Process

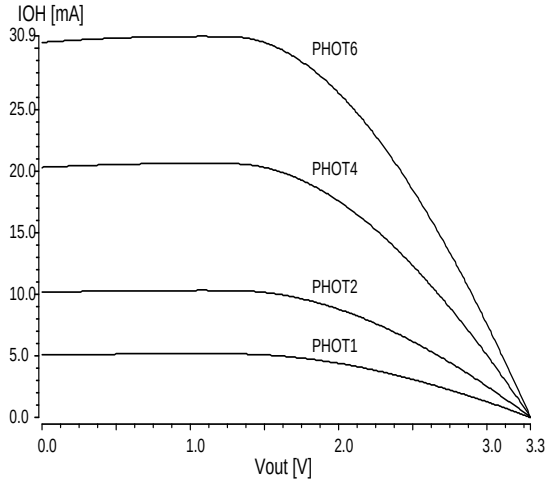


P-TR Characteristics

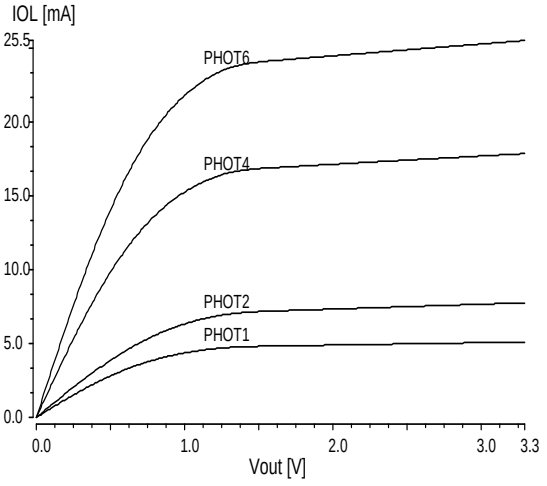


N-TR Characteristics

V_{DD} = 3.3V, V_{BB} = 5V, T_A = 25°C, Typical Process



P-TR Characteristics



N-TR Characteristics

Internal Macrocells 3

Contents

OVERVIEW

This chapter contains data sheets of logic cells, flip-flops, latches, bus holder, internal clock drivers, decoders, adders and multiplexers.

The electrical characteristics of each cell follows its basic cell data.

Summary tables in the following pages list the whole STDL80 internal macrocells by the type and show their reference page numbers for your convenience. Moreover, you can find the more detailed description tables on the leading pages of each category.

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Cell Names & Function Descriptions

Cell Name	Function Description
AD2	2-Input AND
AD2D2	2-Input AND with 2X Drive
AD3	3-Input AND
AD3D3	3-Input AND with 3X Drive
AD4	4-Input AND
AD4D2	4-Input AND with 2X Drive
AD5	5-Input AND
AD5D2	5-Input AND with 2X Drive
ND2	2-Input NAND
ND2D2	2-Input NAND with 2X Drive
ND3	3-Input NAND
ND3D2	3-Input NAND with 2X Drive
ND4	4-Input NAND
ND4D2	4-Input NAND with 2X Drive
ND5	5-Input NAND
ND5D2	5-Input NAND with 2X Drive
ND6	6-Input NAND
ND6D2	6-Input NAND with 2X Drive
ND8	8-Input NAND
ND8D2	8-Input NAND with 2X Drive
NR2	2-Input NOR
NR2D2	2-Input NOR with 2X Drive
NR3	3-Input NOR
NR3D2	3-Input NOR with 2X Drive
NR4	4-Input NOR
NR4D2	4-Input NOR with 2X Drive
NR5	5-Input NOR
NR5D2	5-Input NOR with 2X Drive
NR6	6-Input NOR
NR6D2	6-Input NOR with 2X Drive
NR8	8-Input NOR
NR8D2	8-Input NOR with 2X Drive
OR2	2-Input OR
OR2D2	2-Input OR with 2X Drive

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
OR3	3-Input OR
OR3D3	3-Input OR with 3X Drive
OR4	4-Input OR
OR4D2	4-Input OR with 2X Drive
OR5	5-Input OR
OR5D2	5-Input OR with 2X Drive
XN2	2-Input Exclusive-NOR
XN2D2	2-Input Exclusive-NOR with 2X Drive
XN3	3-Input Exclusive-NOR
XN3D3	3-Input Exclusive-NOR with 3X Drive
XO2	2-Input Exclusive-OR
XO2D2	2-Input Exclusive-OR with 2X Drive
XO3	3-Input Exclusive-OR
XO3D3	3-Input Exclusive-OR with 3X Drive
AO21	2-AND into 2-NOR
AO21D2	2-AND into 2-NOR with 2X Drive
AO211	2-AND into 3-NOR
AO211D2	2-AND into 3-NOR with 2X Drive
AO22	Two 2-ANDs into 2-NOR
AO22D2	Two 2-ANDs into 2-NOR with 2X Drive
AO22A	2-AND and 2-NOR into 2-NOR
AO22D2A	2-AND and 2-NOR into 2-NOR with 2X Drive
AO222	Three 2-ANDs into 3-NOR
AO222D2	Three 2-ANDs into 3-NOR with 2X Drive
AO222A	Inverting 2-of-3 Majority
AO222D2A	Inverting 2-of-3 Majority with 2X Drive
AO33	Two 3-ANDs into 2-NOR
AO33D2	Two 3-ANDs into 2-NOR with 2X Drive
AO333	Three 3-ANDs into 3-NOR
AO333D2	Three 3-ANDs into 3-NOR with 2X Drive
OA21	2-OR into 2-NAND
OA21D2	2-OR into 2-NAND with 2X Drive
OA211	2-OR into 3-NAND
OA211D2	2-OR into 3-NAND with 2X Drive

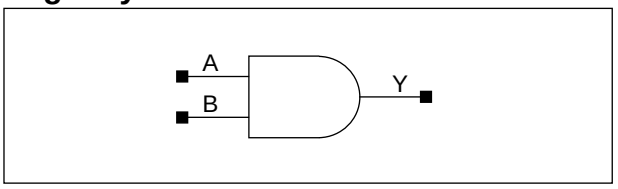
Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
OA22	Two 2-ORs into 2-NAND
OA22D2	Two 2-ORs into 2-NAND with 2X Drive
OA22A	2-OR and 2-NAND into 2-NAND
OA22D2A	2-OR and 2-NAND into 2-NAND with 2X Drive
OA2222	Four 2-ORs into 4-NAND
OA2222D2	Four 2-ORs into 4-NAND with 2X Drive
DL1D2	1ns Delay Cell with 2X Drive
DL1D4	1ns Delay Cell with 4X Drive
DL2D2	2ns Delay Cell with 2X Drive
DL2D4	2ns Delay Cell with 4X Drive
DL3D2	3ns Delay Cell with 2X Drive
DL3D4	3ns Delay Cell with 4X Drive
DL4D2	4ns Delay Cell with 2X Drive
DL4D4	4ns Delay Cell with 4X Drive
DL5D2	5ns Delay Cell with 2X Drive
DL5D4	5ns Delay Cell with 4X Drive
DL10D2	10ns Delay Cell with 2X Drive
DL10D4	10ns Delay Cell with 4X Drive
IV	Inverter
IVD2	Inverter with 2X Drive
IVD3	Inverter with 3X Drive
IVD4	Inverter with 4X Drive
IVD6	Inverter with 6X Drive
IVD8	Inverter with 8X Drive
IVA	Inverter with 2X P-Transistor, 1X N-Transistor
IVD2A	Inverter with 4X P-Transistor, 2X N-Transistor
IVD3A	Inverter with 6X P-Transistor, 3X N-Transistor
IVD4A	Inverter with 8X P-Transistor, 4X N-Transistor
IVCD11	1X Inverter into 1X Inverter
IVCD13	1X Inverter into 3X Inverter
IVCD22	2X Inverter into 2X Inverter
IVCD26	2X Inverter into 6X Inverter
IVCD44	4X Inverter into 4X Inverter
IVT	Inverting Tri-State Buffer with Enable High

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
IVTD2	Inverting Tri-State Buffer with Enable High, 2X Drive
IVTD4	Inverting Tri-State Buffer with Enable High, 4X Drive
IVTD8	Inverting Tri-State Buffer with Enable High, 8X Drive
IVTN	Inverting Tri-State Buffer with Enable Low
IVTND2	Inverting Tri-State Buffer with Enable Low, 2X Drive
IVTND4	Inverting Tri-State Buffer with Enable Low, 4X Drive
IVTND8	Inverting Tri-State Buffer with Enable Low, 8X Drive
NID	Non-Inverting Buffer
NID2	Non-Inverting Buffer with 2X Drive
NID3	Non-Inverting Buffer with 3X Drive
NID4	Non-Inverting Buffer with 4X Drive
NID6	Non-Inverting Buffer with 6X Drive
NID8	Non-Inverting Buffer with 8X Drive
NIT	Non-Inverting Tri-State Buffer with Enable High
NITD2	Non-Inverting Tri-State Buffer with Enable High, 2X Drive
NITD4	Non-Inverting Tri-State Buffer with Enable High, 4X Drive
NITD8	Non-Inverting Tri-State Buffer with Enable High, 8X Drive
NITN	Non-Inverting Tri-State Buffer with Enable Low
NITND2	Non-Inverting Tri-State Buffer with Enable Low, 2X Drive
NITND4	Non-Inverting Tri-State Buffer with Enable Low, 4X Drive
NITND8	Non-Inverting Tri-State Buffer with Enable Low, 8X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Cell Data

Input Load (SL)				Gate Count	
AD2		*AD2D2*		*AD2*	*AD2D2*
A	B	A	B		
0.7	0.8	0.7	0.8	1.3	1.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.22 + 0.031*SL	0.22 + 0.028*SL	0.23 + 0.027*SL
	t_{PHL}	0.32	0.24 + 0.037*SL	0.25 + 0.033*SL	0.26 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
B to Y	t_{PLH}	0.26	0.20 + 0.032*SL	0.21 + 0.028*SL	0.22 + 0.027*SL
	t_{PHL}	0.34	0.26 + 0.037*SL	0.27 + 0.034*SL	0.28 + 0.033*SL
	t_R	0.23	0.11 + 0.056*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.22	0.09 + 0.063*SL	0.09 + 0.063*SL	0.07 + 0.066*SL

AD2D2

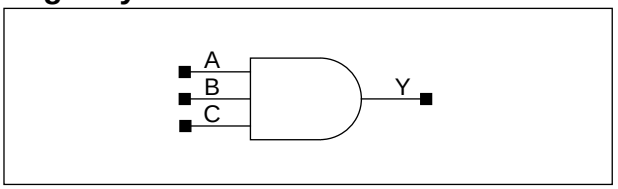
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.30	0.26 + 0.019*SL	0.27 + 0.015*SL	0.29 + 0.013*SL
	t_{PHL}	0.32	0.28 + 0.022*SL	0.29 + 0.018*SL	0.31 + 0.017*SL
	t_R	0.18	0.13 + 0.024*SL	0.12 + 0.027*SL	0.11 + 0.029*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
B to Y	t_{PLH}	0.27	0.24 + 0.020*SL	0.25 + 0.015*SL	0.27 + 0.013*SL
	t_{PHL}	0.34	0.30 + 0.022*SL	0.31 + 0.018*SL	0.33 + 0.017*SL
	t_R	0.18	0.14 + 0.020*SL	0.12 + 0.027*SL	0.11 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

AD3/AD3D3

3-Input AND with 1X/3X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

Cell Data

Input Load (SL)						Gate Count	
AD3			*AD3D3*			*AD3*	*AD3D3*
A	B	C	A	B	C		
0.7	0.8	0.8	0.8	0.8	0.8	1.7	2.3

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AD3

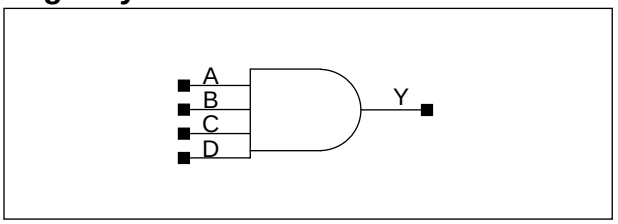
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.37	0.30 + 0.035*SL	0.31 + 0.030*SL	0.34 + 0.027*SL
	t_{PHL}	0.34	0.26 + 0.038*SL	0.27 + 0.034*SL	0.28 + 0.033*SL
	t_R	0.26	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.22	0.10 + 0.064*SL	0.10 + 0.063*SL	0.08 + 0.065*SL
B to Y	t_{PLH}	0.36	0.29 + 0.035*SL	0.31 + 0.030*SL	0.33 + 0.027*SL
	t_{PHL}	0.36	0.28 + 0.038*SL	0.29 + 0.034*SL	0.30 + 0.033*SL
	t_R	0.26	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.23	0.10 + 0.062*SL	0.10 + 0.063*SL	0.08 + 0.065*SL
C to Y	t_{PLH}	0.35	0.28 + 0.035*SL	0.30 + 0.030*SL	0.32 + 0.027*SL
	t_{PHL}	0.38	0.30 + 0.038*SL	0.31 + 0.034*SL	0.32 + 0.033*SL
	t_R	0.26	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.23	0.11 + 0.061*SL	0.11 + 0.063*SL	0.08 + 0.065*SL

AD3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.46	0.42 + 0.017*SL	0.43 + 0.013*SL	0.47 + 0.010*SL
	t_{PHL}	0.39	0.35 + 0.017*SL	0.36 + 0.014*SL	0.38 + 0.011*SL
	t_R	0.26	0.23 + 0.017*SL	0.22 + 0.017*SL	0.21 + 0.018*SL
	t_F	0.18	0.13 + 0.023*SL	0.14 + 0.020*SL	0.13 + 0.021*SL
B to Y	t_{PLH}	0.45	0.42 + 0.017*SL	0.43 + 0.013*SL	0.46 + 0.010*SL
	t_{PHL}	0.40	0.37 + 0.017*SL	0.38 + 0.014*SL	0.40 + 0.011*SL
	t_R	0.26	0.23 + 0.016*SL	0.22 + 0.017*SL	0.21 + 0.018*SL
	t_F	0.19	0.15 + 0.019*SL	0.14 + 0.021*SL	0.14 + 0.021*SL
C to Y	t_{PLH}	0.44	0.41 + 0.017*SL	0.42 + 0.013*SL	0.45 + 0.010*SL
	t_{PHL}	0.42	0.38 + 0.017*SL	0.39 + 0.014*SL	0.42 + 0.011*SL
	t_R	0.26	0.22 + 0.017*SL	0.22 + 0.017*SL	0.21 + 0.018*SL
	t_F	0.19	0.15 + 0.020*SL	0.15 + 0.020*SL	0.14 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Cell Data

Input Load (SL)								Gate Count	
AD4				*AD4D2*				*AD4*	*AD4D2*
A	B	C	D	A	B	C	D		
0.7	0.8	0.8	0.8	0.7	0.8	0.8	0.8	2.0	2.3

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.43	0.35 + 0.039*SL	0.38 + 0.031*SL	0.42 + 0.027*SL
	t_{PHL}	0.34	0.27 + 0.038*SL	0.28 + 0.034*SL	0.29 + 0.033*SL
	t_R	0.29	0.18 + 0.057*SL	0.18 + 0.057*SL	0.16 + 0.059*SL
	t_F	0.23	0.10 + 0.064*SL	0.10 + 0.063*SL	0.08 + 0.065*SL
B to Y	t_{PLH}	0.44	0.36 + 0.039*SL	0.38 + 0.031*SL	0.42 + 0.027*SL
	t_{PHL}	0.36	0.29 + 0.038*SL	0.30 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.29	0.18 + 0.056*SL	0.18 + 0.057*SL	0.16 + 0.059*SL
	t_F	0.23	0.11 + 0.063*SL	0.11 + 0.063*SL	0.08 + 0.065*SL
C to Y	t_{PLH}	0.44	0.37 + 0.039*SL	0.39 + 0.031*SL	0.43 + 0.027*SL
	t_{PHL}	0.38	0.30 + 0.039*SL	0.32 + 0.034*SL	0.33 + 0.033*SL
	t_R	0.29	0.18 + 0.056*SL	0.18 + 0.057*SL	0.16 + 0.059*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.08 + 0.065*SL
D to Y	t_{PLH}	0.44	0.36 + 0.039*SL	0.38 + 0.032*SL	0.42 + 0.027*SL
	t_{PHL}	0.39	0.31 + 0.040*SL	0.33 + 0.034*SL	0.34 + 0.033*SL
	t_R	0.29	0.18 + 0.056*SL	0.18 + 0.057*SL	0.16 + 0.059*SL
	t_F	0.24	0.12 + 0.063*SL	0.12 + 0.062*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

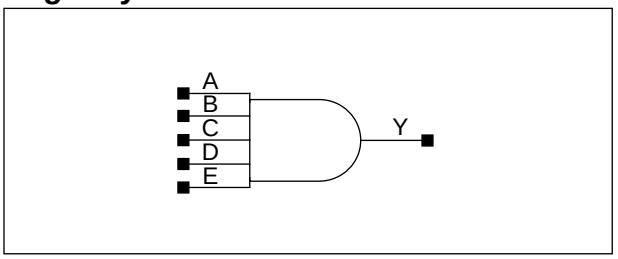
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.47	0.42 + 0.026*SL	0.44 + 0.019*SL	0.49 + 0.014*SL
	t_{PHL}	0.35	0.30 + 0.023*SL	0.31 + 0.019*SL	0.34 + 0.017*SL
	t_R	0.27	0.21 + 0.029*SL	0.22 + 0.027*SL	0.21 + 0.028*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.10 + 0.032*SL
B to Y	t_{PLH}	0.48	0.43 + 0.025*SL	0.45 + 0.019*SL	0.50 + 0.014*SL
	t_{PHL}	0.37	0.32 + 0.023*SL	0.33 + 0.019*SL	0.36 + 0.017*SL
	t_R	0.27	0.22 + 0.025*SL	0.22 + 0.028*SL	0.21 + 0.028*SL
	t_F	0.18	0.11 + 0.031*SL	0.11 + 0.031*SL	0.10 + 0.032*SL
C to Y	t_{PLH}	0.48	0.43 + 0.026*SL	0.45 + 0.019*SL	0.50 + 0.014*SL
	t_{PHL}	0.38	0.33 + 0.024*SL	0.35 + 0.019*SL	0.37 + 0.017*SL
	t_R	0.27	0.22 + 0.027*SL	0.22 + 0.027*SL	0.21 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.030*SL	0.11 + 0.032*SL
D to Y	t_{PLH}	0.48	0.43 + 0.026*SL	0.45 + 0.019*SL	0.50 + 0.014*SL
	t_{PHL}	0.40	0.35 + 0.024*SL	0.36 + 0.019*SL	0.39 + 0.017*SL
	t_R	0.27	0.22 + 0.026*SL	0.22 + 0.027*SL	0.21 + 0.028*SL
	t_F	0.19	0.13 + 0.032*SL	0.13 + 0.030*SL	0.12 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	x	x	x	0
x	0	x	x	x	0
x	x	0	x	x	0
x	x	x	0	x	0
x	x	x	x	0	0
1	1	1	1	1	1

Cell Data

Input Load (SL)										Gate Count	
AD5					*AD5D2*					*AD5*	*AD5D2*
A	B	C	D	E	A	B	C	D	E		
0.7	0.8	0.8	0.8	0.7	0.7	0.8	0.8	0.8	0.7	3.0	3.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.42	0.31 + 0.052*SL	0.33 + 0.047*SL	0.34 + 0.046*SL
	t_{PHL}	0.39	0.31 + 0.038*SL	0.32 + 0.034*SL	0.34 + 0.033*SL
	t_R	0.41	0.21 + 0.101*SL	0.21 + 0.102*SL	0.18 + 0.105*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
B to Y	t_{PLH}	0.43	0.33 + 0.051*SL	0.34 + 0.047*SL	0.35 + 0.046*SL
	t_{PHL}	0.37	0.30 + 0.038*SL	0.31 + 0.034*SL	0.32 + 0.033*SL
	t_R	0.41	0.21 + 0.100*SL	0.21 + 0.102*SL	0.18 + 0.105*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
C to Y	t_{PLH}	0.44	0.33 + 0.051*SL	0.35 + 0.047*SL	0.36 + 0.046*SL
	t_{PHL}	0.35	0.28 + 0.038*SL	0.29 + 0.034*SL	0.30 + 0.033*SL
	t_R	0.41	0.21 + 0.101*SL	0.21 + 0.102*SL	0.18 + 0.105*SL
	t_F	0.23	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.066*SL
D to Y	t_{PLH}	0.35	0.25 + 0.050*SL	0.26 + 0.047*SL	0.27 + 0.046*SL
	t_{PHL}	0.38	0.31 + 0.036*SL	0.32 + 0.034*SL	0.33 + 0.033*SL
	t_R	0.39	0.18 + 0.103*SL	0.18 + 0.104*SL	0.17 + 0.105*SL
	t_F	0.29	0.16 + 0.061*SL	0.16 + 0.063*SL	0.13 + 0.066*SL
E to Y	t_{PLH}	0.37	0.27 + 0.050*SL	0.28 + 0.047*SL	0.29 + 0.046*SL
	t_{PHL}	0.36	0.29 + 0.036*SL	0.30 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.39	0.18 + 0.102*SL	0.18 + 0.104*SL	0.17 + 0.105*SL
	t_F	0.28	0.16 + 0.061*SL	0.16 + 0.063*SL	0.13 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

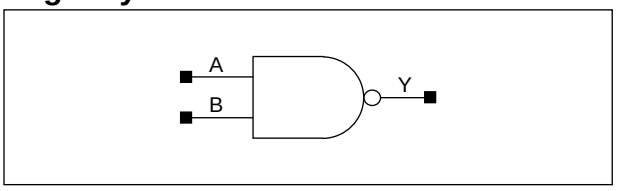
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AD5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.44	0.38 + 0.029*SL	0.39 + 0.025*SL	0.41 + 0.023*SL
	t_{PHL}	0.39	0.35 + 0.024*SL	0.36 + 0.019*SL	0.39 + 0.017*SL
	t_R	0.32	0.22 + 0.047*SL	0.21 + 0.051*SL	0.20 + 0.052*SL
	t_F	0.19	0.13 + 0.032*SL	0.13 + 0.030*SL	0.12 + 0.032*SL
B to Y	t_{PLH}	0.45	0.39 + 0.029*SL	0.40 + 0.026*SL	0.42 + 0.023*SL
	t_{PHL}	0.38	0.33 + 0.023*SL	0.35 + 0.019*SL	0.37 + 0.017*SL
	t_R	0.32	0.22 + 0.048*SL	0.22 + 0.050*SL	0.20 + 0.052*SL
	t_F	0.19	0.12 + 0.033*SL	0.13 + 0.031*SL	0.11 + 0.032*SL
C to Y	t_{PLH}	0.46	0.40 + 0.029*SL	0.41 + 0.026*SL	0.43 + 0.023*SL
	t_{PHL}	0.36	0.32 + 0.023*SL	0.33 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.32	0.22 + 0.049*SL	0.21 + 0.051*SL	0.20 + 0.052*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
D to Y	t_{PLH}	0.36	0.30 + 0.028*SL	0.31 + 0.026*SL	0.33 + 0.023*SL
	t_{PHL}	0.39	0.35 + 0.021*SL	0.36 + 0.018*SL	0.38 + 0.017*SL
	t_R	0.28	0.17 + 0.053*SL	0.18 + 0.052*SL	0.17 + 0.052*SL
	t_F	0.24	0.18 + 0.030*SL	0.18 + 0.030*SL	0.16 + 0.032*SL
E to Y	t_{PLH}	0.38	0.32 + 0.029*SL	0.33 + 0.026*SL	0.35 + 0.023*SL
	t_{PHL}	0.38	0.33 + 0.021*SL	0.34 + 0.018*SL	0.36 + 0.017*SL
	t_R	0.28	0.18 + 0.051*SL	0.18 + 0.052*SL	0.17 + 0.052*SL
	t_F	0.24	0.18 + 0.030*SL	0.18 + 0.030*SL	0.16 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Cell Data

Input Load (SL)				Gate Count	
ND2		*ND2D2*		*ND2*	*ND2D2*
A	B	A	B		
1.1	1.1	2.2	2.2	1.0	1.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

ND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.12 + 0.032*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_{PHL}	0.17	0.08 + 0.040*SL	0.09 + 0.037*SL	0.09 + 0.037*SL
	t_R	0.28	0.18 + 0.050*SL	0.16 + 0.057*SL	0.11 + 0.062*SL
	t_F	0.30	0.16 + 0.068*SL	0.13 + 0.078*SL	0.10 + 0.081*SL
B to Y	t_{PLH}	0.17	0.10 + 0.034*SL	0.12 + 0.028*SL	0.12 + 0.028*SL
	t_{PHL}	0.19	0.10 + 0.043*SL	0.12 + 0.037*SL	0.11 + 0.037*SL
	t_R	0.26	0.16 + 0.051*SL	0.14 + 0.057*SL	0.09 + 0.063*SL
	t_F	0.31	0.17 + 0.069*SL	0.15 + 0.076*SL	0.11 + 0.081*SL

ND2D2

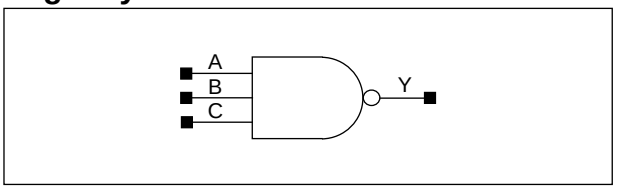
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.14	0.10 + 0.018*SL	0.11 + 0.014*SL	0.12 + 0.013*SL
	t_{PHL}	0.13	0.08 + 0.023*SL	0.09 + 0.019*SL	0.10 + 0.019*SL
	t_R	0.22	0.17 + 0.024*SL	0.17 + 0.025*SL	0.12 + 0.030*SL
	t_F	0.22	0.16 + 0.034*SL	0.15 + 0.036*SL	0.11 + 0.040*SL
B to Y	t_{PLH}	0.14	0.10 + 0.018*SL	0.11 + 0.014*SL	0.12 + 0.013*SL
	t_{PHL}	0.13	0.08 + 0.023*SL	0.09 + 0.019*SL	0.10 + 0.019*SL
	t_R	0.22	0.17 + 0.024*SL	0.17 + 0.025*SL	0.12 + 0.030*SL
	t_F	0.22	0.16 + 0.034*SL	0.15 + 0.036*SL	0.12 + 0.040*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

ND3/ND3D2

3-Input NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

Cell Data

Input Load (SL)						Gate Count	
ND3			*ND3D2*			*ND3*	*ND3D2*
A	B	C	A	B	C		
1.1	1.1	1.1	2.2	1.9	2.3	1.3	2.3

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

ND3

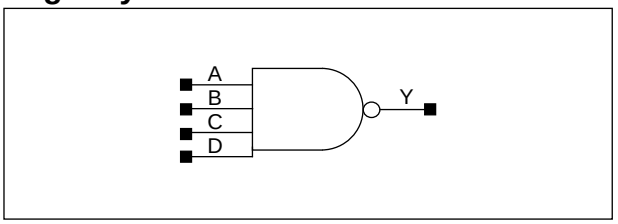
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.21	0.15 + 0.029*SL	0.16 + 0.028*SL	0.15 + 0.028*SL
	t_{PHL}	0.25	0.14 + 0.052*SL	0.14 + 0.051*SL	0.14 + 0.052*SL
	t_R	0.34	0.23 + 0.051*SL	0.22 + 0.057*SL	0.17 + 0.062*SL
	t_F	0.45	0.24 + 0.109*SL	0.22 + 0.114*SL	0.21 + 0.115*SL
B to Y	t_{PLH}	0.19	0.12 + 0.033*SL	0.13 + 0.028*SL	0.13 + 0.028*SL
	t_{PHL}	0.26	0.16 + 0.051*SL	0.16 + 0.051*SL	0.16 + 0.052*SL
	t_R	0.29	0.19 + 0.053*SL	0.17 + 0.058*SL	0.13 + 0.063*SL
	t_F	0.46	0.25 + 0.107*SL	0.23 + 0.112*SL	0.21 + 0.115*SL
C to Y	t_{PLH}	0.20	0.14 + 0.030*SL	0.15 + 0.028*SL	0.14 + 0.028*SL
	t_{PHL}	0.26	0.15 + 0.052*SL	0.16 + 0.051*SL	0.15 + 0.052*SL
	t_R	0.31	0.21 + 0.051*SL	0.19 + 0.058*SL	0.15 + 0.063*SL
	t_F	0.46	0.24 + 0.108*SL	0.23 + 0.113*SL	0.21 + 0.115*SL

ND3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.15	0.11 + 0.018*SL	0.12 + 0.015*SL	0.13 + 0.014*SL
	t_{PHL}	0.21	0.16 + 0.027*SL	0.16 + 0.025*SL	0.16 + 0.026*SL
	t_R	0.23	0.19 + 0.024*SL	0.18 + 0.026*SL	0.15 + 0.030*SL
	t_F	0.35	0.24 + 0.054*SL	0.24 + 0.054*SL	0.21 + 0.057*SL
B to Y	t_{PLH}	0.17	0.14 + 0.016*SL	0.15 + 0.014*SL	0.15 + 0.014*SL
	t_{PHL}	0.19	0.14 + 0.027*SL	0.14 + 0.026*SL	0.14 + 0.026*SL
	t_R	0.28	0.24 + 0.022*SL	0.22 + 0.026*SL	0.19 + 0.030*SL
	t_F	0.34	0.23 + 0.054*SL	0.22 + 0.055*SL	0.20 + 0.057*SL
C to Y	t_{PLH}	0.16	0.13 + 0.017*SL	0.14 + 0.014*SL	0.14 + 0.014*SL
	t_{PHL}	0.20	0.15 + 0.028*SL	0.15 + 0.026*SL	0.15 + 0.026*SL
	t_R	0.26	0.21 + 0.023*SL	0.20 + 0.026*SL	0.16 + 0.030*SL
	t_F	0.34	0.24 + 0.051*SL	0.23 + 0.055*SL	0.21 + 0.057*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Cell Data

Input Load (SL)								Gate Count	
ND4				*ND4D2*				*ND4*	*ND4D2*
A	B	C	D	A	B	C	D		
0.9	1.1	1.1	0.8	2.4	2.2	2.3	2.3	1.7	3.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

ND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.16 + 0.030*SL	0.17 + 0.028*SL	0.17 + 0.028*SL
	t_{PHL}	0.33	0.19 + 0.066*SL	0.19 + 0.066*SL	0.20 + 0.066*SL
	t_R	0.37	0.27 + 0.051*SL	0.25 + 0.057*SL	0.20 + 0.062*SL
	t_F	0.62	0.32 + 0.146*SL	0.32 + 0.149*SL	0.30 + 0.150*SL
B to Y	t_{PLH}	0.20	0.14 + 0.030*SL	0.15 + 0.028*SL	0.15 + 0.028*SL
	t_{PHL}	0.33	0.20 + 0.066*SL	0.20 + 0.066*SL	0.20 + 0.066*SL
	t_R	0.32	0.22 + 0.051*SL	0.20 + 0.058*SL	0.16 + 0.063*SL
	t_F	0.62	0.34 + 0.144*SL	0.32 + 0.148*SL	0.30 + 0.150*SL
C to Y	t_{PLH}	0.22	0.16 + 0.029*SL	0.16 + 0.028*SL	0.16 + 0.028*SL
	t_{PHL}	0.33	0.20 + 0.066*SL	0.20 + 0.066*SL	0.20 + 0.066*SL
	t_R	0.34	0.24 + 0.052*SL	0.22 + 0.058*SL	0.18 + 0.063*SL
	t_F	0.62	0.33 + 0.145*SL	0.32 + 0.148*SL	0.30 + 0.150*SL
D to Y	t_{PLH}	0.19	0.13 + 0.032*SL	0.14 + 0.028*SL	0.14 + 0.028*SL
	t_{PHL}	0.32	0.19 + 0.066*SL	0.19 + 0.066*SL	0.19 + 0.066*SL
	t_R	0.30	0.19 + 0.054*SL	0.18 + 0.058*SL	0.14 + 0.063*SL
	t_F	0.62	0.34 + 0.143*SL	0.32 + 0.148*SL	0.30 + 0.150*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

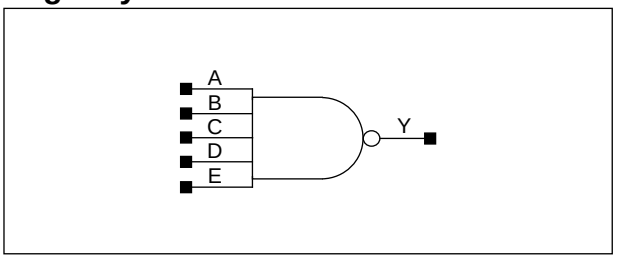
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

ND4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.16 + 0.016*SL	0.16 + 0.014*SL	0.17 + 0.014*SL
	t_{PHL}	0.26	0.19 + 0.034*SL	0.20 + 0.033*SL	0.20 + 0.033*SL
	t_R	0.31	0.26 + 0.024*SL	0.26 + 0.026*SL	0.22 + 0.030*SL
	t_F	0.46	0.32 + 0.072*SL	0.31 + 0.074*SL	0.30 + 0.075*SL
B to Y	t_{PLH}	0.15	0.12 + 0.018*SL	0.13 + 0.014*SL	0.13 + 0.014*SL
	t_{PHL}	0.26	0.19 + 0.032*SL	0.19 + 0.033*SL	0.19 + 0.033*SL
	t_R	0.24	0.20 + 0.023*SL	0.19 + 0.026*SL	0.15 + 0.030*SL
	t_F	0.47	0.33 + 0.070*SL	0.32 + 0.072*SL	0.30 + 0.075*SL
C to Y	t_{PLH}	0.18	0.15 + 0.016*SL	0.15 + 0.014*SL	0.16 + 0.014*SL
	t_{PHL}	0.26	0.20 + 0.034*SL	0.20 + 0.033*SL	0.20 + 0.033*SL
	t_R	0.29	0.24 + 0.023*SL	0.23 + 0.026*SL	0.19 + 0.030*SL
	t_F	0.47	0.33 + 0.070*SL	0.32 + 0.073*SL	0.31 + 0.075*SL
D to Y	t_{PLH}	0.17	0.13 + 0.017*SL	0.14 + 0.014*SL	0.15 + 0.014*SL
	t_{PHL}	0.26	0.20 + 0.033*SL	0.20 + 0.033*SL	0.20 + 0.033*SL
	t_R	0.26	0.22 + 0.024*SL	0.21 + 0.026*SL	0.17 + 0.030*SL
	t_F	0.47	0.33 + 0.070*SL	0.32 + 0.073*SL	0.31 + 0.075*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	x	x	x	x	1
x	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
1	1	1	1	1	0

Cell Data

Input Load (SL)										Gate Count	
ND5					*ND5D2*					*ND5*	*ND5D2*
A	B	C	D	E	A	B	C	D	E		
1.1	0.8	1.1	0.8	1.1	2.4	2.5	1.5	2.3	2.3	2.0	3.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

ND5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.18 + 0.029*SL	0.19 + 0.029*SL	0.19 + 0.028*SL
	t_{PHL}	0.46	0.30 + 0.081*SL	0.30 + 0.081*SL	0.30 + 0.080*SL
	t_R	0.42	0.32 + 0.054*SL	0.31 + 0.057*SL	0.26 + 0.062*SL
	t_F	0.87	0.51 + 0.182*SL	0.50 + 0.184*SL	0.50 + 0.185*SL
B to Y	t_{PLH}	0.24	0.18 + 0.029*SL	0.18 + 0.028*SL	0.18 + 0.028*SL
	t_{PHL}	0.46	0.30 + 0.082*SL	0.30 + 0.081*SL	0.30 + 0.080*SL
	t_R	0.40	0.29 + 0.052*SL	0.28 + 0.058*SL	0.23 + 0.063*SL
	t_F	0.88	0.51 + 0.181*SL	0.51 + 0.184*SL	0.50 + 0.185*SL
C to Y	t_{PLH}	0.23	0.17 + 0.029*SL	0.18 + 0.028*SL	0.18 + 0.028*SL
	t_{PHL}	0.45	0.29 + 0.081*SL	0.29 + 0.081*SL	0.30 + 0.080*SL
	t_R	0.37	0.27 + 0.053*SL	0.25 + 0.058*SL	0.21 + 0.063*SL
	t_F	0.88	0.52 + 0.181*SL	0.51 + 0.183*SL	0.50 + 0.185*SL
D to Y	t_{PLH}	0.22	0.16 + 0.029*SL	0.17 + 0.028*SL	0.16 + 0.028*SL
	t_{PHL}	0.44	0.28 + 0.080*SL	0.28 + 0.081*SL	0.28 + 0.080*SL
	t_R	0.35	0.24 + 0.054*SL	0.23 + 0.059*SL	0.19 + 0.063*SL
	t_F	0.88	0.52 + 0.181*SL	0.51 + 0.183*SL	0.50 + 0.185*SL
E to Y	t_{PLH}	0.21	0.15 + 0.030*SL	0.15 + 0.028*SL	0.15 + 0.028*SL
	t_{PHL}	0.42	0.26 + 0.080*SL	0.26 + 0.080*SL	0.26 + 0.080*SL
	t_R	0.33	0.22 + 0.055*SL	0.21 + 0.059*SL	0.17 + 0.063*SL
	t_F	0.87	0.51 + 0.180*SL	0.50 + 0.184*SL	0.49 + 0.185*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

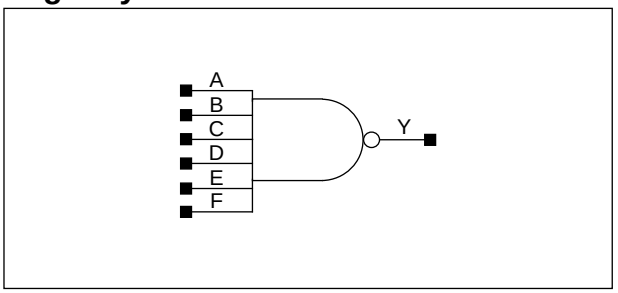
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

ND5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.17 + 0.016*SL	0.17 + 0.014*SL	0.18 + 0.014*SL
	t_{PHL}	0.35	0.27 + 0.040*SL	0.27 + 0.041*SL	0.28 + 0.040*SL
	t_R	0.35	0.30 + 0.024*SL	0.30 + 0.026*SL	0.27 + 0.030*SL
	t_F	0.64	0.46 + 0.090*SL	0.46 + 0.091*SL	0.45 + 0.092*SL
B to Y	t_{PLH}	0.20	0.17 + 0.016*SL	0.17 + 0.014*SL	0.17 + 0.014*SL
	t_{PHL}	0.36	0.28 + 0.041*SL	0.28 + 0.041*SL	0.28 + 0.040*SL
	t_R	0.33	0.28 + 0.024*SL	0.27 + 0.026*SL	0.24 + 0.030*SL
	t_F	0.65	0.47 + 0.090*SL	0.47 + 0.091*SL	0.45 + 0.092*SL
C to Y	t_{PLH}	0.16	0.13 + 0.017*SL	0.14 + 0.014*SL	0.14 + 0.014*SL
	t_{PHL}	0.32	0.24 + 0.040*SL	0.24 + 0.040*SL	0.24 + 0.040*SL
	t_R	0.26	0.21 + 0.026*SL	0.21 + 0.026*SL	0.17 + 0.030*SL
	t_F	0.64	0.47 + 0.089*SL	0.46 + 0.091*SL	0.44 + 0.092*SL
D to Y	t_{PLH}	0.19	0.16 + 0.016*SL	0.16 + 0.014*SL	0.17 + 0.014*SL
	t_{PHL}	0.35	0.27 + 0.040*SL	0.27 + 0.041*SL	0.27 + 0.040*SL
	t_R	0.30	0.25 + 0.025*SL	0.25 + 0.026*SL	0.21 + 0.030*SL
	t_F	0.65	0.47 + 0.089*SL	0.47 + 0.091*SL	0.45 + 0.092*SL
E to Y	t_{PLH}	0.18	0.15 + 0.016*SL	0.15 + 0.014*SL	0.16 + 0.014*SL
	t_{PHL}	0.34	0.26 + 0.040*SL	0.26 + 0.040*SL	0.26 + 0.040*SL
	t_R	0.28	0.23 + 0.024*SL	0.22 + 0.027*SL	0.19 + 0.030*SL
	t_F	0.65	0.47 + 0.090*SL	0.47 + 0.091*SL	0.45 + 0.092*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	x	x	x	x	x	1
x	0	x	x	x	x	1
x	x	0	x	x	x	1
x	x	x	0	x	x	1
x	x	x	x	0	x	1
x	x	x	x	x	0	1
1	1	1	1	1	1	0

Cell Data

Input Load (SL)												Gate Count	
ND6						*ND6D2*						*ND6*	*ND6D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.6	0.5	0.6	0.8	0.7	0.7	0.6	0.5	0.7	0.8	0.7	0.7	4.0	4.3

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

ND6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.41	0.36 + 0.029*SL	0.36 + 0.027*SL	0.36 + 0.027*SL
	t_{PHL}	0.59	0.51 + 0.042*SL	0.53 + 0.036*SL	0.55 + 0.033*SL
	t_R	0.20	0.09 + 0.055*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.26	0.14 + 0.063*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
B to Y	t_{PLH}	0.38	0.32 + 0.028*SL	0.33 + 0.027*SL	0.33 + 0.027*SL
	t_{PHL}	0.61	0.53 + 0.041*SL	0.54 + 0.036*SL	0.57 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.26	0.14 + 0.065*SL	0.14 + 0.062*SL	0.12 + 0.065*SL
C to Y	t_{PLH}	0.40	0.34 + 0.029*SL	0.35 + 0.027*SL	0.35 + 0.027*SL
	t_{PHL}	0.60	0.52 + 0.041*SL	0.54 + 0.036*SL	0.56 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.26	0.13 + 0.064*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
D to Y	t_{PLH}	0.40	0.35 + 0.028*SL	0.35 + 0.027*SL	0.35 + 0.027*SL
	t_{PHL}	0.63	0.55 + 0.041*SL	0.56 + 0.036*SL	0.59 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.26	0.14 + 0.064*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
E to Y	t_{PLH}	0.42	0.36 + 0.029*SL	0.37 + 0.027*SL	0.37 + 0.027*SL
	t_{PHL}	0.62	0.54 + 0.042*SL	0.56 + 0.036*SL	0.58 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.26	0.14 + 0.064*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
F to Y	t_{PLH}	0.44	0.38 + 0.029*SL	0.39 + 0.027*SL	0.39 + 0.027*SL
	t_{PHL}	0.61	0.53 + 0.042*SL	0.55 + 0.036*SL	0.57 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.26	0.14 + 0.064*SL	0.14 + 0.063*SL	0.12 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

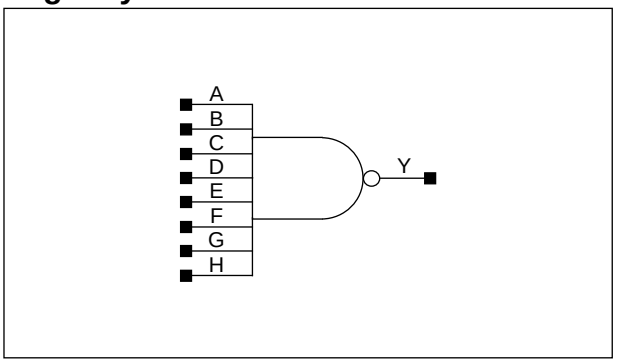
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

ND6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.42	0.38 + 0.016*SL	0.39 + 0.014*SL	0.40 + 0.013*SL
	t_{PHL}	0.64	0.59 + 0.026*SL	0.60 + 0.021*SL	0.64 + 0.017*SL
	t_R	0.14	0.09 + 0.026*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.23	0.17 + 0.030*SL	0.17 + 0.031*SL	0.17 + 0.032*SL
B to Y	t_{PLH}	0.38	0.35 + 0.016*SL	0.36 + 0.014*SL	0.36 + 0.013*SL
	t_{PHL}	0.66	0.61 + 0.026*SL	0.62 + 0.021*SL	0.66 + 0.017*SL
	t_R	0.14	0.09 + 0.026*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.23	0.17 + 0.031*SL	0.17 + 0.031*SL	0.17 + 0.032*SL
C to Y	t_{PLH}	0.40	0.37 + 0.017*SL	0.38 + 0.014*SL	0.38 + 0.013*SL
	t_{PHL}	0.65	0.60 + 0.026*SL	0.61 + 0.021*SL	0.65 + 0.017*SL
	t_R	0.14	0.09 + 0.026*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.23	0.17 + 0.030*SL	0.17 + 0.031*SL	0.16 + 0.032*SL
D to Y	t_{PLH}	0.41	0.37 + 0.017*SL	0.38 + 0.014*SL	0.39 + 0.013*SL
	t_{PHL}	0.68	0.63 + 0.026*SL	0.64 + 0.021*SL	0.68 + 0.017*SL
	t_R	0.15	0.10 + 0.027*SL	0.09 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.23	0.17 + 0.031*SL	0.17 + 0.031*SL	0.17 + 0.032*SL
E to Y	t_{PLH}	0.43	0.39 + 0.017*SL	0.40 + 0.014*SL	0.41 + 0.013*SL
	t_{PHL}	0.67	0.62 + 0.026*SL	0.63 + 0.021*SL	0.67 + 0.017*SL
	t_R	0.15	0.10 + 0.027*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.23	0.17 + 0.030*SL	0.17 + 0.031*SL	0.16 + 0.032*SL
F to Y	t_{PLH}	0.44	0.41 + 0.017*SL	0.42 + 0.014*SL	0.43 + 0.013*SL
	t_{PHL}	0.66	0.61 + 0.026*SL	0.62 + 0.021*SL	0.66 + 0.017*SL
	t_R	0.15	0.10 + 0.027*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.23	0.17 + 0.030*SL	0.17 + 0.031*SL	0.16 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	x	x	x	x	x	x	x	1
x	0	x	x	x	x	x	x	1
x	x	0	x	x	x	x	x	1
x	x	x	0	x	x	x	x	1
x	x	x	x	0	x	x	x	1
x	x	x	x	x	0	x	x	1
x	x	x	x	x	x	0	x	1
x	x	x	x	x	x	x	0	1
1	1	1	1	1	1	1	1	0

Cell Data

Input Load (SL)																Gate Count	
ND8								*ND8D2*								*ND8*	*ND8D2*
A	B	C	D	E	F	G	H	A	B	C	D	E	F	G	H		
0.6	0.5	0.7	0.5	0.5	0.5	0.6	0.6	0.6	0.5	0.6	0.5	0.6	0.6	0.6	0.5	4.7	4.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

ND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.43	0.37 + 0.029*SL	0.38 + 0.027*SL	0.38 + 0.027*SL
	t_{PHL}	0.69	0.60 + 0.042*SL	0.62 + 0.036*SL	0.65 + 0.033*SL
	t_R	0.20	0.10 + 0.054*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.26	0.14 + 0.064*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
B to Y	t_{PLH}	0.40	0.35 + 0.028*SL	0.35 + 0.027*SL	0.35 + 0.027*SL
	t_{PHL}	0.69	0.61 + 0.041*SL	0.62 + 0.036*SL	0.65 + 0.033*SL
	t_R	0.20	0.09 + 0.055*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.27	0.14 + 0.064*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
C to Y	t_{PLH}	0.42	0.36 + 0.028*SL	0.37 + 0.027*SL	0.37 + 0.027*SL
	t_{PHL}	0.69	0.61 + 0.041*SL	0.62 + 0.036*SL	0.65 + 0.033*SL
	t_R	0.20	0.09 + 0.055*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.26	0.14 + 0.064*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
D to Y	t_{PLH}	0.38	0.33 + 0.028*SL	0.33 + 0.027*SL	0.33 + 0.027*SL
	t_{PHL}	0.68	0.60 + 0.042*SL	0.62 + 0.036*SL	0.64 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.27	0.14 + 0.064*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
E to Y	t_{PLH}	0.41	0.35 + 0.029*SL	0.36 + 0.027*SL	0.36 + 0.027*SL
	t_{PHL}	0.70	0.61 + 0.042*SL	0.63 + 0.036*SL	0.66 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.27	0.14 + 0.064*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
F to Y	t_{PLH}	0.43	0.37 + 0.029*SL	0.38 + 0.027*SL	0.38 + 0.027*SL
	t_{PHL}	0.70	0.62 + 0.042*SL	0.64 + 0.036*SL	0.66 + 0.033*SL
	t_R	0.21	0.09 + 0.057*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.27	0.14 + 0.065*SL	0.14 + 0.062*SL	0.12 + 0.065*SL
G to Y	t_{PLH}	0.45	0.39 + 0.029*SL	0.39 + 0.027*SL	0.40 + 0.027*SL
	t_{PHL}	0.71	0.62 + 0.043*SL	0.64 + 0.036*SL	0.67 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.27	0.14 + 0.063*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
H to Y	t_{PLH}	0.46	0.40 + 0.028*SL	0.40 + 0.027*SL	0.41 + 0.027*SL
	t_{PHL}	0.70	0.62 + 0.042*SL	0.63 + 0.036*SL	0.66 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.27	0.14 + 0.064*SL	0.14 + 0.063*SL	0.12 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

ND8D2

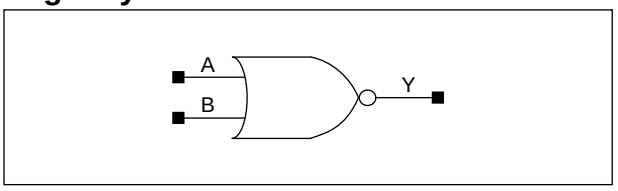
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.43	0.40 + 0.017*SL	0.41 + 0.014*SL	0.42 + 0.013*SL
	t_{PHL}	0.74	0.69 + 0.026*SL	0.70 + 0.021*SL	0.74 + 0.017*SL
	t_R	0.14	0.09 + 0.026*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.24	0.18 + 0.030*SL	0.18 + 0.031*SL	0.17 + 0.032*SL
B to Y	t_{PLH}	0.41	0.37 + 0.016*SL	0.38 + 0.014*SL	0.39 + 0.013*SL
	t_{PHL}	0.74	0.69 + 0.026*SL	0.70 + 0.021*SL	0.74 + 0.017*SL
	t_R	0.14	0.09 + 0.027*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.24	0.18 + 0.030*SL	0.18 + 0.031*SL	0.17 + 0.032*SL
C to Y	t_{PLH}	0.42	0.39 + 0.016*SL	0.40 + 0.014*SL	0.41 + 0.013*SL
	t_{PHL}	0.74	0.69 + 0.026*SL	0.71 + 0.021*SL	0.74 + 0.017*SL
	t_R	0.14	0.09 + 0.026*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.24	0.18 + 0.029*SL	0.17 + 0.031*SL	0.17 + 0.032*SL
D to Y	t_{PLH}	0.39	0.35 + 0.017*SL	0.36 + 0.014*SL	0.37 + 0.013*SL
	t_{PHL}	0.74	0.68 + 0.026*SL	0.70 + 0.021*SL	0.74 + 0.017*SL
	t_R	0.14	0.09 + 0.025*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.24	0.18 + 0.030*SL	0.18 + 0.031*SL	0.17 + 0.032*SL
E to Y	t_{PLH}	0.46	0.43 + 0.017*SL	0.44 + 0.014*SL	0.45 + 0.013*SL
	t_{PHL}	0.76	0.70 + 0.026*SL	0.72 + 0.021*SL	0.76 + 0.017*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.24	0.18 + 0.029*SL	0.18 + 0.031*SL	0.17 + 0.032*SL
F to Y	t_{PLH}	0.44	0.40 + 0.017*SL	0.41 + 0.014*SL	0.42 + 0.013*SL
	t_{PHL}	0.76	0.71 + 0.026*SL	0.72 + 0.021*SL	0.76 + 0.017*SL
	t_R	0.15	0.10 + 0.026*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.24	0.18 + 0.029*SL	0.18 + 0.031*SL	0.17 + 0.032*SL
G to Y	t_{PLH}	0.45	0.42 + 0.017*SL	0.43 + 0.014*SL	0.44 + 0.013*SL
	t_{PHL}	0.76	0.71 + 0.026*SL	0.72 + 0.021*SL	0.76 + 0.017*SL
	t_R	0.15	0.10 + 0.026*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.24	0.18 + 0.030*SL	0.18 + 0.031*SL	0.17 + 0.032*SL
H to Y	t_{PLH}	0.42	0.38 + 0.017*SL	0.39 + 0.014*SL	0.40 + 0.013*SL
	t_{PHL}	0.75	0.70 + 0.026*SL	0.71 + 0.021*SL	0.75 + 0.017*SL
	t_R	0.15	0.10 + 0.026*SL	0.09 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.24	0.18 + 0.031*SL	0.18 + 0.031*SL	0.17 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

NR2/NR2D2

2-Input NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Cell Data

Input Load (SL)				Gate Count	
NR2		*NR2D2*		*NR2*	*NR2D2*
A	B	A	B		
0.9	0.7	1.6	1.6	1.0	1.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NR2

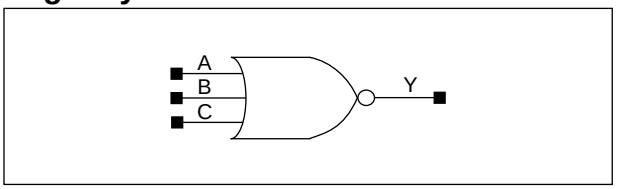
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.13 + 0.048*SL	0.13 + 0.045*SL	0.13 + 0.046*SL
	t_{PHL}	0.21	0.13 + 0.036*SL	0.14 + 0.033*SL	0.14 + 0.033*SL
	t_R	0.38	0.19 + 0.097*SL	0.17 + 0.103*SL	0.15 + 0.105*SL
	t_F	0.31	0.21 + 0.049*SL	0.18 + 0.060*SL	0.13 + 0.065*SL
B to Y	t_{PLH}	0.22	0.13 + 0.048*SL	0.14 + 0.045*SL	0.13 + 0.046*SL
	t_{PHL}	0.18	0.10 + 0.039*SL	0.12 + 0.033*SL	0.12 + 0.033*SL
	t_R	0.40	0.21 + 0.093*SL	0.19 + 0.101*SL	0.14 + 0.105*SL
	t_F	0.25	0.14 + 0.055*SL	0.12 + 0.061*SL	0.08 + 0.066*SL

NR2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.16	0.11 + 0.026*SL	0.12 + 0.023*SL	0.12 + 0.023*SL
	t_{PHL}	0.14	0.09 + 0.023*SL	0.11 + 0.017*SL	0.12 + 0.016*SL
	t_R	0.27	0.18 + 0.043*SL	0.17 + 0.049*SL	0.14 + 0.052*SL
	t_F	0.21	0.15 + 0.029*SL	0.15 + 0.028*SL	0.11 + 0.032*SL
B to Y	t_{PLH}	0.16	0.11 + 0.026*SL	0.12 + 0.023*SL	0.12 + 0.023*SL
	t_{PHL}	0.14	0.09 + 0.023*SL	0.11 + 0.017*SL	0.12 + 0.016*SL
	t_R	0.27	0.18 + 0.043*SL	0.17 + 0.049*SL	0.14 + 0.052*SL
	t_F	0.21	0.15 + 0.029*SL	0.15 + 0.028*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	1
1	x	x	0
x	1	x	0
x	x	1	0

Cell Data

Input Load (SL)						Gate Count	
NR3			*NR3D2*			*NR3*	*NR3D2*
A	B	C	A	B	C		
0.9	0.8	0.7	1.8	1.2	1.8	1.3	2.3

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NR3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.34	0.20 + 0.070*SL	0.20 + 0.069*SL	0.21 + 0.069*SL
	t_{PHL}	0.23	0.16 + 0.036*SL	0.16 + 0.034*SL	0.17 + 0.033*SL
	t_R	0.61	0.31 + 0.151*SL	0.29 + 0.156*SL	0.27 + 0.158*SL
	t_F	0.36	0.24 + 0.059*SL	0.24 + 0.061*SL	0.19 + 0.065*SL
B to Y	t_{PLH}	0.33	0.19 + 0.068*SL	0.19 + 0.069*SL	0.19 + 0.069*SL
	t_{PHL}	0.22	0.15 + 0.035*SL	0.15 + 0.033*SL	0.15 + 0.033*SL
	t_R	0.61	0.31 + 0.151*SL	0.30 + 0.155*SL	0.27 + 0.158*SL
	t_F	0.31	0.19 + 0.057*SL	0.18 + 0.061*SL	0.14 + 0.066*SL
C to Y	t_{PLH}	0.29	0.16 + 0.066*SL	0.16 + 0.068*SL	0.15 + 0.069*SL
	t_{PHL}	0.18	0.11 + 0.038*SL	0.12 + 0.033*SL	0.12 + 0.033*SL
	t_R	0.61	0.31 + 0.148*SL	0.29 + 0.155*SL	0.27 + 0.158*SL
	t_F	0.26	0.15 + 0.054*SL	0.13 + 0.062*SL	0.09 + 0.066*SL

NR3D2

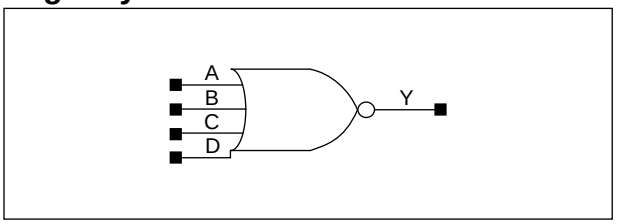
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.17 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.17	0.13 + 0.020*SL	0.14 + 0.017*SL	0.15 + 0.017*SL
	t_R	0.42	0.27 + 0.072*SL	0.26 + 0.076*SL	0.24 + 0.079*SL
	t_F	0.26	0.21 + 0.026*SL	0.20 + 0.029*SL	0.17 + 0.032*SL
B to Y	t_{PLH}	0.21	0.14 + 0.035*SL	0.14 + 0.033*SL	0.13 + 0.034*SL
	t_{PHL}	0.13	0.08 + 0.023*SL	0.10 + 0.018*SL	0.11 + 0.016*SL
	t_R	0.42	0.28 + 0.071*SL	0.26 + 0.075*SL	0.23 + 0.079*SL
	t_F	0.19	0.13 + 0.028*SL	0.13 + 0.029*SL	0.09 + 0.032*SL
C to Y	t_{PLH}	0.25	0.17 + 0.036*SL	0.18 + 0.035*SL	0.18 + 0.035*SL
	t_{PHL}	0.17	0.13 + 0.020*SL	0.14 + 0.017*SL	0.15 + 0.017*SL
	t_R	0.42	0.27 + 0.072*SL	0.26 + 0.077*SL	0.24 + 0.079*SL
	t_F	0.26	0.22 + 0.024*SL	0.20 + 0.029*SL	0.17 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

NR4/NR4D2

4-Input NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	0	1
1	x	x	x	0
x	1	x	x	0
x	x	1	x	0
x	x	x	1	0

Cell Data

Input Load (SL)								Gate Count	
NR4				*NR4D2*				*NR4*	*NR4D2*
A	B	C	D	A	B	C	D		
0.6	0.8	0.9	0.9	1.7	1.4	1.5	1.7	1.7	2.3

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NR4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.35	0.17 + 0.087*SL	0.16 + 0.091*SL	0.16 + 0.092*SL
	t_{PHL}	0.19	0.11 + 0.038*SL	0.13 + 0.033*SL	0.12 + 0.033*SL
	t_R	0.85	0.44 + 0.203*SL	0.42 + 0.210*SL	0.42 + 0.210*SL
	t_F	0.26	0.14 + 0.059*SL	0.13 + 0.061*SL	0.09 + 0.066*SL
B to Y	t_{PLH}	0.41	0.23 + 0.092*SL	0.23 + 0.092*SL	0.23 + 0.092*SL
	t_{PHL}	0.22	0.15 + 0.035*SL	0.16 + 0.033*SL	0.16 + 0.033*SL
	t_R	0.87	0.46 + 0.204*SL	0.45 + 0.208*SL	0.43 + 0.210*SL
	t_F	0.31	0.20 + 0.056*SL	0.18 + 0.061*SL	0.14 + 0.066*SL
C to Y	t_{PLH}	0.46	0.28 + 0.094*SL	0.28 + 0.093*SL	0.29 + 0.092*SL
	t_{PHL}	0.24	0.17 + 0.036*SL	0.17 + 0.034*SL	0.18 + 0.033*SL
	t_R	0.87	0.47 + 0.202*SL	0.45 + 0.208*SL	0.43 + 0.210*SL
	t_F	0.36	0.24 + 0.059*SL	0.23 + 0.061*SL	0.19 + 0.065*SL
D to Y	t_{PLH}	0.48	0.29 + 0.093*SL	0.30 + 0.093*SL	0.30 + 0.092*SL
	t_{PHL}	0.24	0.17 + 0.037*SL	0.17 + 0.036*SL	0.19 + 0.033*SL
	t_R	0.87	0.46 + 0.203*SL	0.45 + 0.209*SL	0.43 + 0.210*SL
	t_F	0.40	0.28 + 0.062*SL	0.28 + 0.063*SL	0.25 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NR4D2

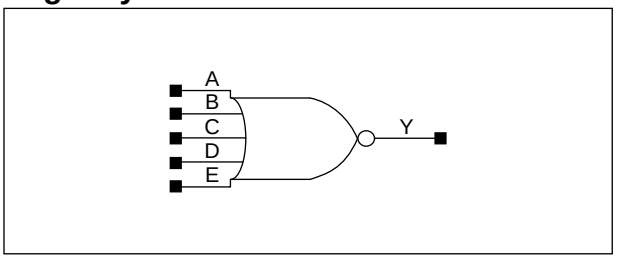
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.33	0.24 + 0.047*SL	0.24 + 0.046*SL	0.25 + 0.046*SL
	t_{PHL}	0.18	0.14 + 0.020*SL	0.15 + 0.018*SL	0.16 + 0.017*SL
	t_R	0.62	0.42 + 0.099*SL	0.42 + 0.102*SL	0.39 + 0.105*SL
	t_F	0.28	0.22 + 0.029*SL	0.22 + 0.030*SL	0.20 + 0.032*SL
B to Y	t_{PLH}	0.29	0.20 + 0.045*SL	0.20 + 0.046*SL	0.20 + 0.046*SL
	t_{PHL}	0.16	0.12 + 0.022*SL	0.13 + 0.018*SL	0.14 + 0.017*SL
	t_R	0.61	0.42 + 0.098*SL	0.40 + 0.103*SL	0.38 + 0.105*SL
	t_F	0.24	0.18 + 0.029*SL	0.18 + 0.029*SL	0.15 + 0.032*SL
C to Y	t_{PLH}	0.30	0.21 + 0.046*SL	0.21 + 0.046*SL	0.20 + 0.046*SL
	t_{PHL}	0.16	0.12 + 0.022*SL	0.13 + 0.017*SL	0.14 + 0.017*SL
	t_R	0.62	0.42 + 0.098*SL	0.41 + 0.102*SL	0.38 + 0.105*SL
	t_F	0.24	0.18 + 0.030*SL	0.18 + 0.029*SL	0.15 + 0.032*SL
D to Y	t_{PLH}	0.34	0.24 + 0.047*SL	0.24 + 0.047*SL	0.25 + 0.046*SL
	t_{PHL}	0.18	0.14 + 0.020*SL	0.15 + 0.018*SL	0.16 + 0.017*SL
	t_R	0.62	0.43 + 0.098*SL	0.42 + 0.102*SL	0.39 + 0.105*SL
	t_F	0.28	0.22 + 0.029*SL	0.22 + 0.030*SL	0.20 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

NR5/NR5D2

5-Input NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	1
1	x	x	x	x	0
x	1	x	x	x	0
x	x	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0

Cell Data

Input Load (SL)										Gate Count	
NR5					*NR5D2*					*NR5*	*NR5D2*
A	B	C	D	E	A	B	C	D	E		
0.6	0.5	0.6	0.5	0.6	0.6	0.5	0.6	0.5	0.6	3.7	3.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NR5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.65	0.58 + 0.032*SL	0.59 + 0.028*SL	0.60 + 0.027*SL
	t_{PHL}	0.41	0.33 + 0.037*SL	0.34 + 0.034*SL	0.35 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
B to Y	t_{PLH}	0.60	0.54 + 0.032*SL	0.55 + 0.028*SL	0.56 + 0.027*SL
	t_{PHL}	0.37	0.30 + 0.037*SL	0.31 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
C to Y	t_{PLH}	0.63	0.57 + 0.032*SL	0.58 + 0.028*SL	0.59 + 0.027*SL
	t_{PHL}	0.39	0.32 + 0.037*SL	0.33 + 0.034*SL	0.34 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
D to Y	t_{PLH}	0.50	0.44 + 0.032*SL	0.45 + 0.028*SL	0.46 + 0.027*SL
	t_{PHL}	0.38	0.31 + 0.037*SL	0.32 + 0.034*SL	0.32 + 0.033*SL
	t_R	0.23	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
E to Y	t_{PLH}	0.50	0.43 + 0.032*SL	0.44 + 0.028*SL	0.45 + 0.027*SL
	t_{PHL}	0.40	0.33 + 0.037*SL	0.34 + 0.034*SL	0.35 + 0.033*SL
	t_R	0.23	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.063*SL	0.07 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NR5D2

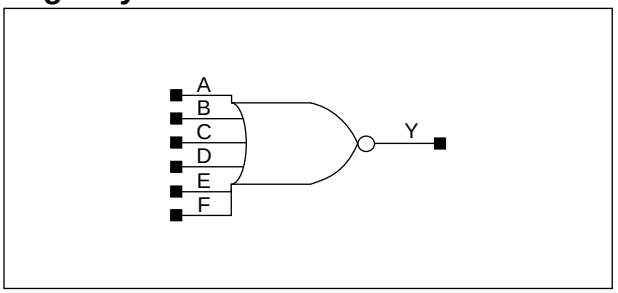
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.67	0.64 + 0.019*SL	0.64 + 0.016*SL	0.67 + 0.013*SL
	t_{PHL}	0.41	0.37 + 0.022*SL	0.38 + 0.018*SL	0.40 + 0.017*SL
	t_R	0.19	0.14 + 0.024*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
B to Y	t_{PLH}	0.63	0.59 + 0.019*SL	0.60 + 0.015*SL	0.62 + 0.013*SL
	t_{PHL}	0.38	0.33 + 0.022*SL	0.34 + 0.018*SL	0.36 + 0.017*SL
	t_R	0.19	0.14 + 0.025*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
C to Y	t_{PLH}	0.66	0.62 + 0.019*SL	0.63 + 0.015*SL	0.66 + 0.013*SL
	t_{PHL}	0.40	0.35 + 0.023*SL	0.37 + 0.018*SL	0.38 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
D to Y	t_{PLH}	0.52	0.48 + 0.019*SL	0.49 + 0.016*SL	0.51 + 0.013*SL
	t_{PHL}	0.39	0.34 + 0.023*SL	0.35 + 0.019*SL	0.37 + 0.017*SL
	t_R	0.18	0.13 + 0.026*SL	0.12 + 0.027*SL	0.11 + 0.029*SL
	t_F	0.17	0.10 + 0.030*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
E to Y	t_{PLH}	0.51	0.48 + 0.019*SL	0.49 + 0.016*SL	0.51 + 0.013*SL
	t_{PHL}	0.41	0.37 + 0.022*SL	0.37 + 0.019*SL	0.39 + 0.017*SL
	t_R	0.18	0.13 + 0.026*SL	0.13 + 0.027*SL	0.11 + 0.029*SL
	t_F	0.17	0.11 + 0.030*SL	0.10 + 0.031*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

NR6/NR6D2

6-Input NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
0	0	0	0	0	0	1
1	x	x	x	x	x	0
x	1	x	x	x	x	0
x	x	1	x	x	x	0
x	x	x	1	x	x	0
x	x	x	x	1	x	0
x	x	x	x	x	1	0

Cell Data

Input Load (SL)												Gate Count	
NR6						*NR6D2*						*NR6*	*NR6D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.6	0.5	0.5	0.7	0.6	0.5	0.6	0.5	0.5	0.6	0.6	0.5	4.3	4.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NR6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.59	0.52 + 0.036*SL	0.54 + 0.030*SL	0.57 + 0.027*SL
	t_{PHL}	0.44	0.37 + 0.039*SL	0.38 + 0.034*SL	0.39 + 0.033*SL
	t_R	0.27	0.15 + 0.057*SL	0.15 + 0.057*SL	0.13 + 0.059*SL
	t_F	0.24	0.12 + 0.060*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
B to Y	t_{PLH}	0.60	0.52 + 0.036*SL	0.54 + 0.030*SL	0.57 + 0.027*SL
	t_{PHL}	0.42	0.34 + 0.039*SL	0.36 + 0.034*SL	0.37 + 0.033*SL
	t_R	0.27	0.15 + 0.057*SL	0.15 + 0.057*SL	0.13 + 0.059*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
C to Y	t_{PLH}	0.60	0.53 + 0.036*SL	0.54 + 0.030*SL	0.57 + 0.027*SL
	t_{PHL}	0.40	0.33 + 0.039*SL	0.34 + 0.034*SL	0.35 + 0.033*SL
	t_R	0.27	0.15 + 0.056*SL	0.15 + 0.057*SL	0.13 + 0.059*SL
	t_F	0.23	0.11 + 0.064*SL	0.11 + 0.063*SL	0.08 + 0.065*SL
D to Y	t_{PLH}	0.59	0.52 + 0.036*SL	0.54 + 0.030*SL	0.57 + 0.027*SL
	t_{PHL}	0.43	0.35 + 0.038*SL	0.36 + 0.034*SL	0.37 + 0.033*SL
	t_R	0.27	0.15 + 0.058*SL	0.15 + 0.057*SL	0.13 + 0.059*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.063*SL	0.08 + 0.065*SL
E to Y	t_{PLH}	0.61	0.53 + 0.036*SL	0.55 + 0.030*SL	0.58 + 0.027*SL
	t_{PHL}	0.42	0.34 + 0.038*SL	0.35 + 0.034*SL	0.36 + 0.033*SL
	t_R	0.27	0.16 + 0.056*SL	0.15 + 0.057*SL	0.13 + 0.059*SL
	t_F	0.23	0.10 + 0.064*SL	0.10 + 0.063*SL	0.08 + 0.065*SL
F to Y	t_{PLH}	0.61	0.54 + 0.036*SL	0.56 + 0.030*SL	0.58 + 0.027*SL
	t_{PHL}	0.39	0.32 + 0.038*SL	0.33 + 0.034*SL	0.34 + 0.033*SL
	t_R	0.27	0.15 + 0.057*SL	0.15 + 0.057*SL	0.13 + 0.059*SL
	t_F	0.23	0.10 + 0.064*SL	0.10 + 0.064*SL	0.08 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NR6D2

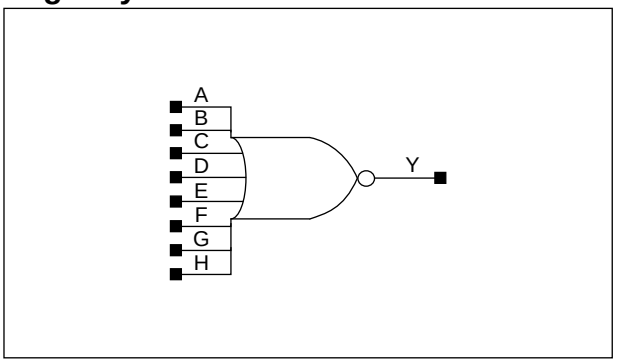
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.62	0.57 + 0.023*SL	0.59 + 0.017*SL	0.62 + 0.014*SL
	t_{PHL}	0.44	0.39 + 0.024*SL	0.41 + 0.019*SL	0.43 + 0.017*SL
	t_R	0.23	0.18 + 0.026*SL	0.18 + 0.027*SL	0.16 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.030*SL	0.11 + 0.032*SL
B to Y	t_{PLH}	0.62	0.58 + 0.023*SL	0.59 + 0.017*SL	0.63 + 0.014*SL
	t_{PHL}	0.42	0.37 + 0.024*SL	0.38 + 0.019*SL	0.41 + 0.017*SL
	t_R	0.23	0.18 + 0.027*SL	0.18 + 0.027*SL	0.16 + 0.028*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
C to Y	t_{PLH}	0.62	0.57 + 0.023*SL	0.59 + 0.017*SL	0.63 + 0.014*SL
	t_{PHL}	0.40	0.35 + 0.023*SL	0.37 + 0.019*SL	0.39 + 0.017*SL
	t_R	0.23	0.18 + 0.026*SL	0.18 + 0.027*SL	0.17 + 0.028*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.10 + 0.032*SL
D to Y	t_{PLH}	0.62	0.57 + 0.023*SL	0.59 + 0.017*SL	0.62 + 0.014*SL
	t_{PHL}	0.42	0.38 + 0.023*SL	0.39 + 0.019*SL	0.41 + 0.017*SL
	t_R	0.23	0.18 + 0.026*SL	0.18 + 0.027*SL	0.16 + 0.028*SL
	t_F	0.18	0.12 + 0.030*SL	0.11 + 0.031*SL	0.10 + 0.032*SL
E to Y	t_{PLH}	0.63	0.59 + 0.023*SL	0.60 + 0.017*SL	0.64 + 0.014*SL
	t_{PHL}	0.41	0.37 + 0.023*SL	0.38 + 0.019*SL	0.40 + 0.017*SL
	t_R	0.23	0.18 + 0.027*SL	0.17 + 0.027*SL	0.16 + 0.028*SL
	t_F	0.17	0.11 + 0.030*SL	0.10 + 0.032*SL	0.10 + 0.032*SL
F to Y	t_{PLH}	0.64	0.59 + 0.023*SL	0.61 + 0.017*SL	0.64 + 0.014*SL
	t_{PHL}	0.39	0.35 + 0.023*SL	0.36 + 0.019*SL	0.38 + 0.017*SL
	t_R	0.23	0.18 + 0.026*SL	0.17 + 0.027*SL	0.16 + 0.028*SL
	t_F	0.17	0.10 + 0.032*SL	0.10 + 0.031*SL	0.10 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

NR8/NR8D2

8-Input NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	0	0	0	0	0	0	1
1	x	x	x	x	x	x	x	0
x	1	x	x	x	x	x	x	0
x	x	1	x	x	x	x	x	0
x	x	x	1	x	x	x	x	0
x	x	x	x	1	x	x	x	0
x	x	x	x	x	1	x	x	0
x	x	x	x	x	x	1	x	0
x	x	x	x	x	x	x	1	0

Cell Data

Input Load (SL)								Gate Count
NR8								*NR8*
A	B	C	D	E	F	G	H	
0.6	0.6	0.6	0.5	0.5	0.6	0.6	0.6	4.3
NR8D2								*NR8D2*
A	B	C	D	E	F	G	H	
0.6	0.6	0.6	0.5	0.5	0.6	0.6	0.6	4.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NR8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.79	0.72 + 0.033*SL	0.73 + 0.028*SL	0.75 + 0.027*SL
	t_{PHL}	0.43	0.36 + 0.038*SL	0.37 + 0.034*SL	0.38 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.08 + 0.066*SL
B to Y	t_{PLH}	0.77	0.70 + 0.033*SL	0.71 + 0.028*SL	0.73 + 0.027*SL
	t_{PHL}	0.43	0.36 + 0.037*SL	0.37 + 0.034*SL	0.37 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.08 + 0.066*SL
C to Y	t_{PLH}	0.72	0.65 + 0.033*SL	0.66 + 0.028*SL	0.68 + 0.027*SL
	t_{PHL}	0.42	0.34 + 0.037*SL	0.35 + 0.034*SL	0.36 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.08 + 0.066*SL
D to Y	t_{PLH}	0.66	0.59 + 0.033*SL	0.60 + 0.028*SL	0.61 + 0.027*SL
	t_{PHL}	0.39	0.32 + 0.037*SL	0.33 + 0.034*SL	0.34 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.22	0.10 + 0.063*SL	0.10 + 0.063*SL	0.08 + 0.066*SL
E to Y	t_{PLH}	0.70	0.63 + 0.033*SL	0.65 + 0.028*SL	0.66 + 0.027*SL
	t_{PHL}	0.38	0.31 + 0.037*SL	0.32 + 0.034*SL	0.32 + 0.033*SL
	t_R	0.24	0.14 + 0.053*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
F to Y	t_{PLH}	0.81	0.75 + 0.032*SL	0.76 + 0.028*SL	0.77 + 0.027*SL
	t_{PHL}	0.42	0.34 + 0.037*SL	0.35 + 0.034*SL	0.36 + 0.033*SL
	t_R	0.24	0.14 + 0.054*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.22	0.09 + 0.063*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
G to Y	t_{PLH}	0.76	0.70 + 0.032*SL	0.71 + 0.028*SL	0.72 + 0.027*SL
	t_{PHL}	0.41	0.33 + 0.037*SL	0.34 + 0.034*SL	0.35 + 0.033*SL
	t_R	0.24	0.14 + 0.054*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
H to Y	t_{PLH}	0.83	0.77 + 0.032*SL	0.78 + 0.028*SL	0.79 + 0.027*SL
	t_{PHL}	0.42	0.35 + 0.037*SL	0.36 + 0.034*SL	0.36 + 0.033*SL
	t_R	0.24	0.14 + 0.054*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

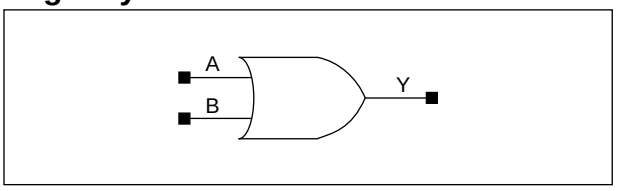
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NR8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.80	0.76 + 0.020*SL	0.78 + 0.016*SL	0.80 + 0.013*SL
	t_{PHL}	0.44	0.39 + 0.023*SL	0.40 + 0.019*SL	0.42 + 0.017*SL
	t_R	0.20	0.14 + 0.025*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.17	0.11 + 0.029*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
B to Y	t_{PLH}	0.78	0.75 + 0.020*SL	0.76 + 0.016*SL	0.78 + 0.013*SL
	t_{PHL}	0.43	0.39 + 0.022*SL	0.40 + 0.019*SL	0.42 + 0.017*SL
	t_R	0.20	0.15 + 0.025*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.030*SL	0.09 + 0.032*SL
C to Y	t_{PLH}	0.74	0.69 + 0.020*SL	0.71 + 0.016*SL	0.73 + 0.013*SL
	t_{PHL}	0.42	0.37 + 0.023*SL	0.38 + 0.019*SL	0.40 + 0.017*SL
	t_R	0.20	0.14 + 0.026*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.17	0.11 + 0.029*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
D to Y	t_{PLH}	0.67	0.63 + 0.020*SL	0.65 + 0.016*SL	0.67 + 0.013*SL
	t_{PHL}	0.39	0.35 + 0.023*SL	0.36 + 0.019*SL	0.38 + 0.017*SL
	t_R	0.20	0.14 + 0.026*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.030*SL	0.09 + 0.032*SL
E to Y	t_{PLH}	0.73	0.69 + 0.020*SL	0.71 + 0.015*SL	0.73 + 0.013*SL
	t_{PHL}	0.39	0.34 + 0.022*SL	0.35 + 0.018*SL	0.37 + 0.017*SL
	t_R	0.20	0.16 + 0.024*SL	0.15 + 0.026*SL	0.13 + 0.028*SL
	t_F	0.16	0.10 + 0.029*SL	0.10 + 0.031*SL	0.08 + 0.032*SL
F to Y	t_{PLH}	0.85	0.81 + 0.019*SL	0.82 + 0.016*SL	0.84 + 0.013*SL
	t_{PHL}	0.42	0.38 + 0.022*SL	0.39 + 0.018*SL	0.41 + 0.017*SL
	t_R	0.20	0.16 + 0.023*SL	0.15 + 0.026*SL	0.13 + 0.028*SL
	t_F	0.16	0.10 + 0.034*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
G to Y	t_{PLH}	0.80	0.76 + 0.019*SL	0.77 + 0.015*SL	0.79 + 0.013*SL
	t_{PHL}	0.41	0.37 + 0.022*SL	0.37 + 0.019*SL	0.39 + 0.017*SL
	t_R	0.21	0.16 + 0.023*SL	0.15 + 0.026*SL	0.13 + 0.028*SL
	t_F	0.16	0.10 + 0.029*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
H to Y	t_{PLH}	0.87	0.83 + 0.020*SL	0.84 + 0.015*SL	0.86 + 0.013*SL
	t_{PHL}	0.43	0.38 + 0.022*SL	0.39 + 0.019*SL	0.41 + 0.017*SL
	t_R	0.20	0.16 + 0.023*SL	0.15 + 0.026*SL	0.13 + 0.028*SL
	t_F	0.16	0.10 + 0.034*SL	0.10 + 0.031*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Cell Data

Input Load (SL)				Gate Count	
OR2		*OR2D2*		*OR2*	*OR2D2*
A	B	A	B		
0.5	0.6	0.5	0.6	1.3	1.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OR2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.16 + 0.029*SL	0.17 + 0.027*SL	0.17 + 0.027*SL
	t_{PHL}	0.42	0.34 + 0.042*SL	0.36 + 0.036*SL	0.38 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.26	0.13 + 0.065*SL	0.14 + 0.063*SL	0.11 + 0.065*SL
B to Y	t_{PLH}	0.24	0.18 + 0.029*SL	0.19 + 0.027*SL	0.19 + 0.027*SL
	t_{PHL}	0.42	0.34 + 0.042*SL	0.36 + 0.036*SL	0.38 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.26	0.13 + 0.063*SL	0.14 + 0.063*SL	0.11 + 0.065*SL

OR2D2

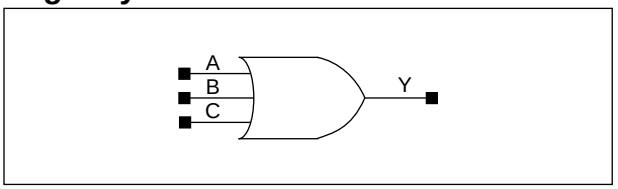
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.19 + 0.017*SL	0.20 + 0.014*SL	0.21 + 0.013*SL
	t_{PHL}	0.47	0.41 + 0.026*SL	0.43 + 0.021*SL	0.47 + 0.017*SL
	t_R	0.15	0.10 + 0.024*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.23	0.17 + 0.030*SL	0.17 + 0.031*SL	0.16 + 0.032*SL
B to Y	t_{PLH}	0.24	0.21 + 0.016*SL	0.22 + 0.014*SL	0.23 + 0.013*SL
	t_{PHL}	0.47	0.41 + 0.026*SL	0.43 + 0.021*SL	0.47 + 0.017*SL
	t_R	0.15	0.10 + 0.027*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.23	0.17 + 0.031*SL	0.17 + 0.031*SL	0.16 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

OR3/OR3D3

3-Input OR with 1X/3X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	0
1	x	x	1
x	1	x	1
x	x	1	1

Cell Data

Input Load (SL)						Gate Count	
OR3			*OR3D3*			*OR3*	*OR3D3*
A	B	C	A	B	C		
0.5	0.6	0.6	0.5	0.6	0.6	1.7	2.3

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OR3

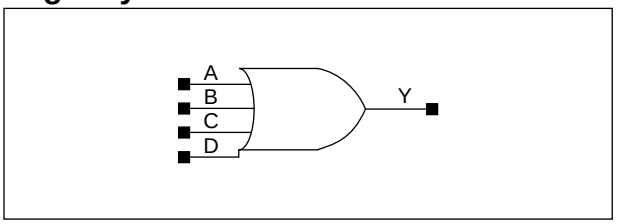
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.23	0.17 + 0.029*SL	0.18 + 0.027*SL	0.18 + 0.027*SL
	t_{PHL}	0.54	0.45 + 0.048*SL	0.47 + 0.039*SL	0.53 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.32	0.19 + 0.065*SL	0.20 + 0.063*SL	0.19 + 0.064*SL
B to Y	t_{PLH}	0.25	0.19 + 0.029*SL	0.20 + 0.027*SL	0.20 + 0.027*SL
	t_{PHL}	0.58	0.48 + 0.047*SL	0.51 + 0.039*SL	0.56 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.32	0.19 + 0.065*SL	0.20 + 0.063*SL	0.19 + 0.064*SL
C to Y	t_{PLH}	0.26	0.20 + 0.030*SL	0.21 + 0.027*SL	0.22 + 0.027*SL
	t_{PHL}	0.59	0.50 + 0.048*SL	0.52 + 0.039*SL	0.57 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.32	0.19 + 0.065*SL	0.20 + 0.063*SL	0.19 + 0.064*SL

OR3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.26	0.24 + 0.013*SL	0.25 + 0.010*SL	0.26 + 0.009*SL
	t_{PHL}	0.76	0.71 + 0.023*SL	0.72 + 0.018*SL	0.77 + 0.013*SL
	t_R	0.15	0.12 + 0.015*SL	0.11 + 0.017*SL	0.10 + 0.019*SL
	t_F	0.39	0.34 + 0.022*SL	0.35 + 0.021*SL	0.35 + 0.020*SL
B to Y	t_{PLH}	0.28	0.26 + 0.012*SL	0.26 + 0.010*SL	0.28 + 0.009*SL
	t_{PHL}	0.80	0.75 + 0.023*SL	0.76 + 0.018*SL	0.81 + 0.013*SL
	t_R	0.16	0.13 + 0.016*SL	0.12 + 0.017*SL	0.11 + 0.019*SL
	t_F	0.39	0.35 + 0.021*SL	0.35 + 0.020*SL	0.35 + 0.020*SL
C to Y	t_{PLH}	0.29	0.27 + 0.013*SL	0.27 + 0.010*SL	0.29 + 0.009*SL
	t_{PHL}	0.81	0.77 + 0.023*SL	0.78 + 0.018*SL	0.83 + 0.013*SL
	t_R	0.16	0.13 + 0.014*SL	0.12 + 0.018*SL	0.11 + 0.019*SL
	t_F	0.39	0.35 + 0.022*SL	0.35 + 0.020*SL	0.35 + 0.020*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	0	0	0
1	x	x	x	1
x	1	x	x	1
x	x	1	x	1
x	x	x	1	1

Cell Data

Input Load (SL)								Gate Count	
OR4				*OR4D2*				*OR4*	*OR4D2*
A	B	C	D	A	B	C	D		
0.4	0.7	0.6	0.5	0.5	0.6	0.6	0.5	2.7	3.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OR4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.19 + 0.029*SL	0.19 + 0.028*SL	0.19 + 0.028*SL
	t_{PHL}	0.43	0.34 + 0.042*SL	0.35 + 0.039*SL	0.37 + 0.037*SL
	t_R	0.24	0.13 + 0.056*SL	0.12 + 0.061*SL	0.10 + 0.063*SL
	t_F	0.31	0.15 + 0.077*SL	0.15 + 0.078*SL	0.13 + 0.080*SL
B to Y	t_{PLH}	0.27	0.21 + 0.029*SL	0.21 + 0.028*SL	0.21 + 0.028*SL
	t_{PHL}	0.43	0.34 + 0.042*SL	0.35 + 0.039*SL	0.37 + 0.037*SL
	t_R	0.25	0.13 + 0.057*SL	0.12 + 0.061*SL	0.11 + 0.063*SL
	t_F	0.31	0.15 + 0.078*SL	0.15 + 0.078*SL	0.13 + 0.080*SL
C to Y	t_{PLH}	0.26	0.20 + 0.030*SL	0.20 + 0.028*SL	0.20 + 0.028*SL
	t_{PHL}	0.44	0.35 + 0.045*SL	0.37 + 0.040*SL	0.39 + 0.037*SL
	t_R	0.23	0.11 + 0.058*SL	0.10 + 0.061*SL	0.09 + 0.063*SL
	t_F	0.32	0.17 + 0.078*SL	0.17 + 0.078*SL	0.14 + 0.080*SL
D to Y	t_{PLH}	0.24	0.18 + 0.030*SL	0.18 + 0.028*SL	0.18 + 0.028*SL
	t_{PHL}	0.45	0.36 + 0.045*SL	0.37 + 0.040*SL	0.39 + 0.037*SL
	t_R	0.22	0.11 + 0.058*SL	0.10 + 0.061*SL	0.08 + 0.063*SL
	t_F	0.32	0.17 + 0.078*SL	0.17 + 0.078*SL	0.14 + 0.080*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

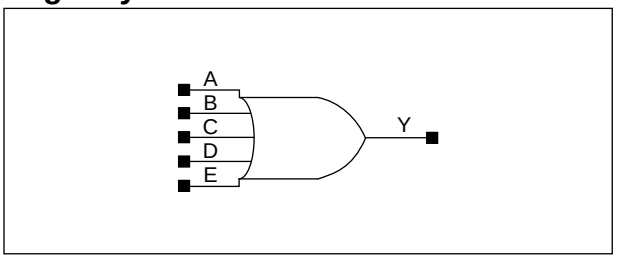
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OR4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.26	0.23 + 0.016*SL	0.23 + 0.014*SL	0.24 + 0.014*SL
	t_{PHL}	0.48	0.44 + 0.024*SL	0.44 + 0.021*SL	0.46 + 0.019*SL
	t_R	0.19	0.14 + 0.025*SL	0.14 + 0.028*SL	0.12 + 0.030*SL
	t_F	0.28	0.21 + 0.034*SL	0.20 + 0.037*SL	0.18 + 0.040*SL
B to Y	t_{PLH}	0.28	0.25 + 0.016*SL	0.25 + 0.014*SL	0.26 + 0.014*SL
	t_{PHL}	0.49	0.44 + 0.024*SL	0.45 + 0.021*SL	0.46 + 0.019*SL
	t_R	0.20	0.15 + 0.026*SL	0.14 + 0.028*SL	0.12 + 0.030*SL
	t_F	0.28	0.21 + 0.033*SL	0.20 + 0.038*SL	0.18 + 0.040*SL
C to Y	t_{PLH}	0.27	0.23 + 0.016*SL	0.24 + 0.015*SL	0.25 + 0.014*SL
	t_{PHL}	0.50	0.44 + 0.026*SL	0.46 + 0.022*SL	0.49 + 0.019*SL
	t_R	0.17	0.12 + 0.026*SL	0.11 + 0.028*SL	0.10 + 0.030*SL
	t_F	0.28	0.21 + 0.036*SL	0.20 + 0.039*SL	0.19 + 0.039*SL
D to Y	t_{PLH}	0.25	0.22 + 0.016*SL	0.22 + 0.014*SL	0.23 + 0.014*SL
	t_{PHL}	0.50	0.44 + 0.026*SL	0.45 + 0.022*SL	0.48 + 0.019*SL
	t_R	0.17	0.13 + 0.022*SL	0.11 + 0.029*SL	0.10 + 0.030*SL
	t_F	0.28	0.21 + 0.036*SL	0.20 + 0.039*SL	0.20 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	C	D	E	Y
0	0	0	0	0	0
1	x	x	x	x	1
x	1	x	x	x	1
x	x	1	x	x	1
x	x	x	1	x	1
x	x	x	x	1	1

Cell Data

Input Load (SL)										Gate Count	
OR5					*OR5D2*					*OR5*	*OR5D2*
A	B	C	D	E	A	B	C	D	E		
0.5	0.6	0.7	0.6	0.5	0.5	0.6	0.7	0.6	0.5	3.0	3.3

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OR5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.26	0.20 + 0.030*SL	0.20 + 0.028*SL	0.20 + 0.028*SL
	t_{PHL}	0.55	0.46 + 0.047*SL	0.47 + 0.042*SL	0.49 + 0.040*SL
	t_R	0.25	0.13 + 0.058*SL	0.12 + 0.061*SL	0.10 + 0.063*SL
	t_F	0.37	0.22 + 0.076*SL	0.21 + 0.081*SL	0.17 + 0.084*SL
B to Y	t_{PLH}	0.28	0.22 + 0.030*SL	0.23 + 0.028*SL	0.23 + 0.028*SL
	t_{PHL}	0.58	0.49 + 0.047*SL	0.50 + 0.042*SL	0.52 + 0.040*SL
	t_R	0.25	0.13 + 0.058*SL	0.13 + 0.060*SL	0.11 + 0.063*SL
	t_F	0.37	0.22 + 0.076*SL	0.21 + 0.081*SL	0.17 + 0.084*SL
C to Y	t_{PLH}	0.29	0.23 + 0.030*SL	0.24 + 0.028*SL	0.24 + 0.028*SL
	t_{PHL}	0.60	0.51 + 0.047*SL	0.52 + 0.042*SL	0.54 + 0.040*SL
	t_R	0.26	0.15 + 0.054*SL	0.13 + 0.061*SL	0.11 + 0.063*SL
	t_F	0.37	0.22 + 0.076*SL	0.21 + 0.081*SL	0.17 + 0.084*SL
D to Y	t_{PLH}	0.25	0.19 + 0.030*SL	0.20 + 0.028*SL	0.20 + 0.028*SL
	t_{PHL}	0.45	0.35 + 0.047*SL	0.37 + 0.042*SL	0.39 + 0.040*SL
	t_R	0.23	0.11 + 0.058*SL	0.10 + 0.061*SL	0.09 + 0.063*SL
	t_F	0.33	0.17 + 0.082*SL	0.17 + 0.083*SL	0.15 + 0.085*SL
E to Y	t_{PLH}	0.23	0.17 + 0.029*SL	0.18 + 0.028*SL	0.18 + 0.028*SL
	t_{PHL}	0.45	0.36 + 0.046*SL	0.37 + 0.042*SL	0.39 + 0.040*SL
	t_R	0.22	0.11 + 0.057*SL	0.10 + 0.061*SL	0.08 + 0.063*SL
	t_F	0.33	0.16 + 0.083*SL	0.17 + 0.083*SL	0.15 + 0.085*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

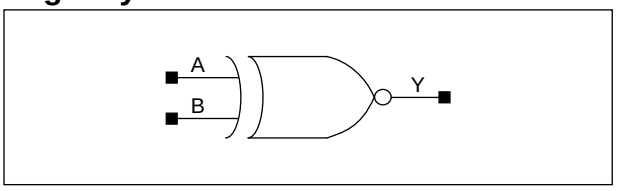
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OR5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.27	0.24 + 0.017*SL	0.25 + 0.014*SL	0.25 + 0.014*SL
	t_{PHL}	0.64	0.59 + 0.027*SL	0.60 + 0.022*SL	0.63 + 0.019*SL
	t_R	0.20	0.15 + 0.026*SL	0.14 + 0.028*SL	0.12 + 0.030*SL
	t_F	0.37	0.31 + 0.030*SL	0.30 + 0.034*SL	0.26 + 0.039*SL
B to Y	t_{PLH}	0.29	0.26 + 0.015*SL	0.26 + 0.014*SL	0.27 + 0.014*SL
	t_{PHL}	0.68	0.63 + 0.027*SL	0.64 + 0.022*SL	0.67 + 0.019*SL
	t_R	0.20	0.15 + 0.026*SL	0.14 + 0.028*SL	0.12 + 0.030*SL
	t_F	0.37	0.31 + 0.031*SL	0.30 + 0.034*SL	0.26 + 0.039*SL
C to Y	t_{PLH}	0.31	0.27 + 0.016*SL	0.28 + 0.014*SL	0.28 + 0.014*SL
	t_{PHL}	0.70	0.64 + 0.027*SL	0.66 + 0.022*SL	0.69 + 0.019*SL
	t_R	0.21	0.16 + 0.026*SL	0.15 + 0.028*SL	0.13 + 0.030*SL
	t_F	0.37	0.31 + 0.030*SL	0.30 + 0.034*SL	0.26 + 0.039*SL
D to Y	t_{PLH}	0.27	0.23 + 0.016*SL	0.24 + 0.015*SL	0.25 + 0.014*SL
	t_{PHL}	0.50	0.45 + 0.026*SL	0.46 + 0.022*SL	0.49 + 0.019*SL
	t_R	0.17	0.12 + 0.026*SL	0.11 + 0.029*SL	0.10 + 0.030*SL
	t_F	0.28	0.21 + 0.036*SL	0.21 + 0.038*SL	0.20 + 0.039*SL
E to Y	t_{PLH}	0.25	0.22 + 0.016*SL	0.22 + 0.014*SL	0.23 + 0.014*SL
	t_{PHL}	0.50	0.45 + 0.026*SL	0.46 + 0.022*SL	0.49 + 0.019*SL
	t_R	0.17	0.13 + 0.023*SL	0.11 + 0.028*SL	0.10 + 0.030*SL
	t_F	0.28	0.21 + 0.036*SL	0.21 + 0.038*SL	0.20 + 0.039*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Cell Data

Input Load (SL)				Gate Count	
XN2		*XN2D2*		*XN2*	*XN2D2*
A	B	A	B		
0.8	1.5	0.8	1.5	2.7	3.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

XN2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.43 + 0.032*SL	0.44 + 0.028*SL	0.45 + 0.027*SL
	t_{PHL}	0.51	0.42 + 0.046*SL	0.44 + 0.037*SL	0.48 + 0.033*SL
	t_R	0.23	0.12 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.30	0.17 + 0.065*SL	0.18 + 0.062*SL	0.15 + 0.064*SL
B to Y	t_{PLH}	0.37	0.31 + 0.032*SL	0.32 + 0.028*SL	0.33 + 0.027*SL
	t_{PHL}	0.40	0.31 + 0.043*SL	0.33 + 0.036*SL	0.36 + 0.033*SL
	t_R	0.23	0.12 + 0.056*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.26	0.13 + 0.066*SL	0.14 + 0.063*SL	0.12 + 0.065*SL

XN2D2

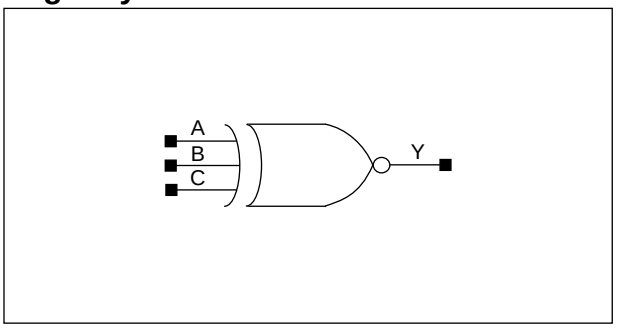
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.50	0.46 + 0.019*SL	0.47 + 0.016*SL	0.49 + 0.013*SL
	t_{PHL}	0.52	0.46 + 0.029*SL	0.48 + 0.022*SL	0.53 + 0.017*SL
	t_R	0.18	0.13 + 0.025*SL	0.13 + 0.027*SL	0.11 + 0.028*SL
	t_F	0.26	0.19 + 0.033*SL	0.19 + 0.032*SL	0.20 + 0.031*SL
B to Y	t_{PLH}	0.37	0.33 + 0.020*SL	0.34 + 0.016*SL	0.37 + 0.013*SL
	t_{PHL}	0.40	0.35 + 0.027*SL	0.37 + 0.022*SL	0.41 + 0.017*SL
	t_R	0.18	0.13 + 0.027*SL	0.13 + 0.027*SL	0.11 + 0.028*SL
	t_F	0.22	0.15 + 0.033*SL	0.15 + 0.032*SL	0.16 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

XN3/XN3D3

3-Input Exclusive-NOR with 1X/3X Drive

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Cell Data

Input Load (SL)						Gate Count	
XN3			*XN3D3*			*XN3*	*XN3D3*
A	B	C	A	B	C		
1.1	0.8	1.5	1.1	0.8	1.5	4.3	5.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

XN3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.40	0.32 + 0.037*SL	0.34 + 0.031*SL	0.38 + 0.027*SL
	t_{PHL}	0.42	0.32 + 0.050*SL	0.34 + 0.041*SL	0.41 + 0.034*SL
	t_R	0.26	0.14 + 0.061*SL	0.15 + 0.058*SL	0.14 + 0.059*SL
	t_F	0.30	0.15 + 0.074*SL	0.17 + 0.067*SL	0.20 + 0.064*SL
B to Y	t_{PLH}	0.69	0.61 + 0.040*SL	0.63 + 0.032*SL	0.68 + 0.027*SL
	t_{PHL}	0.80	0.71 + 0.044*SL	0.73 + 0.036*SL	0.76 + 0.033*SL
	t_R	0.30	0.19 + 0.058*SL	0.19 + 0.056*SL	0.17 + 0.059*SL
	t_F	0.27	0.14 + 0.065*SL	0.15 + 0.063*SL	0.13 + 0.065*SL
C to Y	t_{PLH}	0.58	0.51 + 0.033*SL	0.52 + 0.028*SL	0.53 + 0.027*SL
	t_{PHL}	0.67	0.59 + 0.044*SL	0.61 + 0.036*SL	0.64 + 0.033*SL
	t_R	0.24	0.13 + 0.054*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.065*SL	0.15 + 0.063*SL	0.13 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

XN3D3

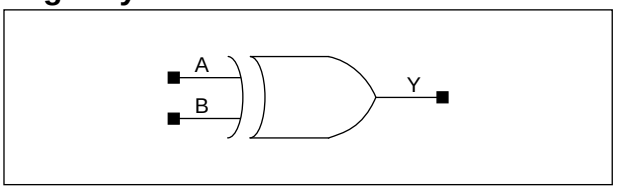
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.45	0.41 + 0.018*SL	0.42 + 0.014*SL	0.47 + 0.010*SL
	t_{PHL}	0.50	0.45 + 0.025*SL	0.46 + 0.020*SL	0.52 + 0.014*SL
	t_R	0.26	0.22 + 0.019*SL	0.23 + 0.018*SL	0.22 + 0.018*SL
	t_F	0.34	0.28 + 0.028*SL	0.29 + 0.024*SL	0.32 + 0.021*SL
B to Y	t_{PLH}	0.75	0.71 + 0.019*SL	0.72 + 0.015*SL	0.77 + 0.010*SL
	t_{PHL}	0.87	0.83 + 0.020*SL	0.84 + 0.016*SL	0.88 + 0.012*SL
	t_R	0.29	0.26 + 0.019*SL	0.26 + 0.017*SL	0.25 + 0.018*SL
	t_F	0.26	0.21 + 0.023*SL	0.21 + 0.021*SL	0.22 + 0.021*SL
C to Y	t_{PLH}	0.63	0.60 + 0.015*SL	0.60 + 0.012*SL	0.63 + 0.009*SL
	t_{PHL}	0.74	0.70 + 0.020*SL	0.71 + 0.016*SL	0.75 + 0.012*SL
	t_R	0.21	0.18 + 0.016*SL	0.17 + 0.017*SL	0.16 + 0.018*SL
	t_F	0.26	0.21 + 0.023*SL	0.21 + 0.021*SL	0.22 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

XO2/XO2D2

2-Input Exclusive-OR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Cell Data

Input Load (SL)				Gate Count	
XO2		*XO2D2*		*XO2*	*XO2D2*
A	B	A	B		
0.7	1.1	0.7	1.1	2.7	3.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

XO2

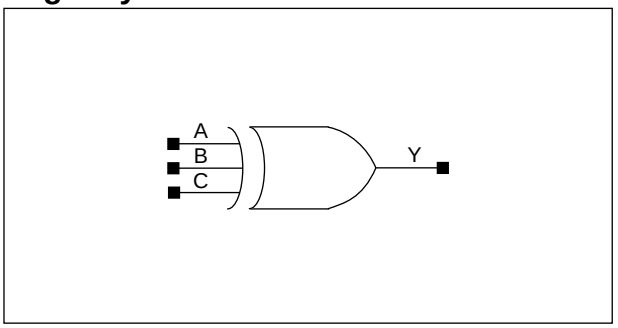
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.42 + 0.032*SL	0.44 + 0.028*SL	0.45 + 0.027*SL
	t_{PHL}	0.51	0.42 + 0.046*SL	0.44 + 0.037*SL	0.48 + 0.033*SL
	t_R	0.23	0.12 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.30	0.17 + 0.065*SL	0.18 + 0.062*SL	0.15 + 0.064*SL
B to Y	t_{PLH}	0.37	0.30 + 0.033*SL	0.31 + 0.028*SL	0.33 + 0.027*SL
	t_{PHL}	0.39	0.30 + 0.044*SL	0.32 + 0.037*SL	0.36 + 0.033*SL
	t_R	0.23	0.12 + 0.058*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.26	0.13 + 0.067*SL	0.13 + 0.064*SL	0.13 + 0.065*SL

XO2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.45 + 0.020*SL	0.47 + 0.016*SL	0.49 + 0.013*SL
	t_{PHL}	0.52	0.46 + 0.029*SL	0.48 + 0.022*SL	0.53 + 0.017*SL
	t_R	0.18	0.13 + 0.026*SL	0.13 + 0.027*SL	0.11 + 0.028*SL
	t_F	0.26	0.19 + 0.033*SL	0.19 + 0.032*SL	0.20 + 0.031*SL
B to Y	t_{PLH}	0.37	0.33 + 0.020*SL	0.34 + 0.016*SL	0.36 + 0.013*SL
	t_{PHL}	0.39	0.34 + 0.028*SL	0.35 + 0.022*SL	0.40 + 0.017*SL
	t_R	0.19	0.14 + 0.025*SL	0.13 + 0.028*SL	0.12 + 0.028*SL
	t_F	0.22	0.15 + 0.034*SL	0.15 + 0.033*SL	0.16 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Cell Data

Input Load (SL)						Gate Count	
XO3			*XO3D3*			*XO3*	*XO3D3*
A	B	C	A	B	C		
1.5	0.7	1.5	1.5	0.7	1.5	4.3	5.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

XO3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.37	0.31 + 0.033*SL	0.32 + 0.028*SL	0.33 + 0.027*SL
	t_{PHL}	0.42	0.31 + 0.054*SL	0.34 + 0.042*SL	0.42 + 0.034*SL
	t_R	0.23	0.12 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.32	0.17 + 0.074*SL	0.19 + 0.067*SL	0.22 + 0.064*SL
B to Y	t_{PLH}	0.69	0.62 + 0.033*SL	0.64 + 0.028*SL	0.65 + 0.027*SL
	t_{PHL}	0.80	0.71 + 0.044*SL	0.73 + 0.036*SL	0.76 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.27	0.14 + 0.065*SL	0.14 + 0.063*SL	0.13 + 0.065*SL
C to Y	t_{PLH}	0.58	0.51 + 0.033*SL	0.52 + 0.028*SL	0.54 + 0.027*SL
	t_{PHL}	0.67	0.58 + 0.044*SL	0.61 + 0.036*SL	0.64 + 0.033*SL
	t_R	0.24	0.13 + 0.054*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.27	0.14 + 0.065*SL	0.14 + 0.063*SL	0.13 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

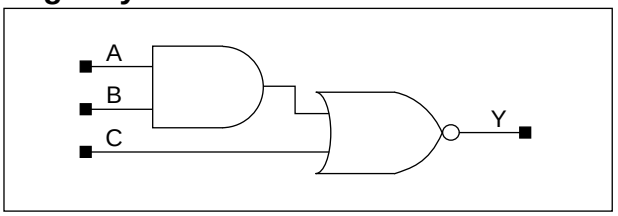
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

XO3D3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.40	0.37 + 0.015*SL	0.38 + 0.012*SL	0.41 + 0.009*SL
	t_{PHL}	0.49	0.44 + 0.025*SL	0.45 + 0.020*SL	0.51 + 0.014*SL
	t_R	0.20	0.16 + 0.018*SL	0.17 + 0.017*SL	0.15 + 0.018*SL
	t_F	0.36	0.30 + 0.027*SL	0.31 + 0.024*SL	0.34 + 0.021*SL
B to Y	t_{PLH}	0.75	0.71 + 0.019*SL	0.72 + 0.015*SL	0.77 + 0.010*SL
	t_{PHL}	0.87	0.82 + 0.020*SL	0.84 + 0.016*SL	0.88 + 0.012*SL
	t_R	0.30	0.26 + 0.018*SL	0.26 + 0.017*SL	0.26 + 0.018*SL
	t_F	0.25	0.21 + 0.023*SL	0.21 + 0.021*SL	0.21 + 0.021*SL
C to Y	t_{PLH}	0.63	0.60 + 0.015*SL	0.61 + 0.012*SL	0.64 + 0.009*SL
	t_{PHL}	0.74	0.70 + 0.020*SL	0.71 + 0.016*SL	0.75 + 0.012*SL
	t_R	0.21	0.17 + 0.016*SL	0.17 + 0.018*SL	0.16 + 0.018*SL
	t_F	0.25	0.21 + 0.023*SL	0.21 + 0.021*SL	0.21 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	C	Y
x	x	1	0
0	x	0	1
x	0	0	1
1	1	x	0

Cell Data

Input Load (SL)						Gate Count	
AO21			*AO21D2*			*AO21*	*AO21D2*
A	B	C	A	B	C		
0.6	0.6	0.9	1.2	1.2	1.9	1.3	2.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.15 + 0.050*SL	0.15 + 0.051*SL	0.15 + 0.051*SL
	t_{PHL}	0.23	0.12 + 0.055*SL	0.12 + 0.053*SL	0.12 + 0.053*SL
	t_R	0.47	0.26 + 0.104*SL	0.24 + 0.113*SL	0.20 + 0.117*SL
	t_F	0.38	0.17 + 0.103*SL	0.15 + 0.111*SL	0.13 + 0.114*SL
B to Y	t_{PLH}	0.24	0.13 + 0.051*SL	0.14 + 0.051*SL	0.13 + 0.051*SL
	t_{PHL}	0.25	0.14 + 0.054*SL	0.15 + 0.053*SL	0.14 + 0.053*SL
	t_R	0.45	0.24 + 0.104*SL	0.21 + 0.114*SL	0.18 + 0.117*SL
	t_F	0.39	0.18 + 0.103*SL	0.16 + 0.110*SL	0.13 + 0.114*SL
C to Y	t_{PLH}	0.29	0.18 + 0.052*SL	0.19 + 0.051*SL	0.19 + 0.051*SL
	t_{PHL}	0.24	0.18 + 0.034*SL	0.18 + 0.033*SL	0.18 + 0.033*SL
	t_R	0.46	0.24 + 0.111*SL	0.22 + 0.115*SL	0.20 + 0.117*SL
	t_F	0.34	0.22 + 0.058*SL	0.21 + 0.061*SL	0.17 + 0.066*SL

AO21D2

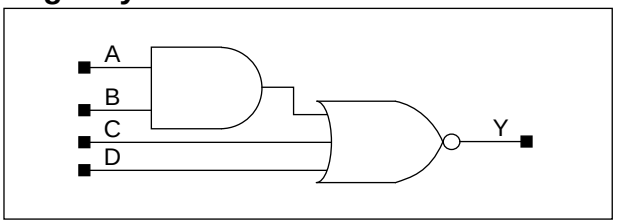
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.15 + 0.026*SL	0.16 + 0.024*SL	0.15 + 0.025*SL
	t_{PHL}	0.18	0.12 + 0.029*SL	0.13 + 0.027*SL	0.13 + 0.026*SL
	t_R	0.37	0.28 + 0.048*SL	0.27 + 0.052*SL	0.23 + 0.057*SL
	t_F	0.28	0.18 + 0.049*SL	0.16 + 0.055*SL	0.14 + 0.057*SL
B to Y	t_{PLH}	0.18	0.12 + 0.028*SL	0.13 + 0.024*SL	0.13 + 0.025*SL
	t_{PHL}	0.19	0.13 + 0.030*SL	0.14 + 0.026*SL	0.14 + 0.026*SL
	t_R	0.34	0.24 + 0.047*SL	0.23 + 0.053*SL	0.19 + 0.057*SL
	t_F	0.29	0.19 + 0.050*SL	0.18 + 0.053*SL	0.14 + 0.057*SL
C to Y	t_{PLH}	0.24	0.18 + 0.026*SL	0.19 + 0.025*SL	0.19 + 0.025*SL
	t_{PHL}	0.21	0.17 + 0.018*SL	0.18 + 0.017*SL	0.18 + 0.016*SL
	t_R	0.35	0.25 + 0.053*SL	0.24 + 0.055*SL	0.22 + 0.057*SL
	t_F	0.28	0.23 + 0.028*SL	0.22 + 0.029*SL	0.20 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

AO211/AO211D2

2-AND into 3-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	1	x	0
x	x	x	1	0
x	0	0	0	1
0	x	0	0	1

Cell Data

Input Load (SL)								Gate Count	
AO211				*AO211D2*				*AO211*	*AO211D2*
A	B	C	D	A	B	C	D		
0.6	0.6	0.7	0.9	1.2	1.2	1.4	1.7	1.7	3.3

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.33	0.18 + 0.074*SL	0.18 + 0.076*SL	0.17 + 0.077*SL
	t_{PHL}	0.24	0.13 + 0.054*SL	0.14 + 0.053*SL	0.14 + 0.053*SL
	t_R	0.75	0.42 + 0.166*SL	0.39 + 0.174*SL	0.38 + 0.176*SL
	t_F	0.40	0.19 + 0.105*SL	0.18 + 0.111*SL	0.16 + 0.114*SL
B to Y	t_{PLH}	0.31	0.16 + 0.073*SL	0.15 + 0.076*SL	0.15 + 0.077*SL
	t_{PHL}	0.26	0.16 + 0.054*SL	0.16 + 0.053*SL	0.16 + 0.053*SL
	t_R	0.71	0.37 + 0.168*SL	0.36 + 0.174*SL	0.34 + 0.176*SL
	t_F	0.41	0.20 + 0.105*SL	0.18 + 0.111*SL	0.15 + 0.114*SL
C to Y	t_{PLH}	0.43	0.27 + 0.078*SL	0.27 + 0.077*SL	0.28 + 0.077*SL
	t_{PHL}	0.25	0.19 + 0.034*SL	0.19 + 0.033*SL	0.19 + 0.033*SL
	t_R	0.76	0.42 + 0.169*SL	0.41 + 0.174*SL	0.39 + 0.175*SL
	t_F	0.35	0.23 + 0.057*SL	0.22 + 0.062*SL	0.18 + 0.066*SL
D to Y	t_{PLH}	0.44	0.28 + 0.078*SL	0.28 + 0.077*SL	0.29 + 0.077*SL
	t_{PHL}	0.25	0.18 + 0.036*SL	0.18 + 0.035*SL	0.20 + 0.033*SL
	t_R	0.76	0.42 + 0.170*SL	0.41 + 0.174*SL	0.39 + 0.176*SL
	t_F	0.41	0.29 + 0.058*SL	0.28 + 0.062*SL	0.24 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO211D2

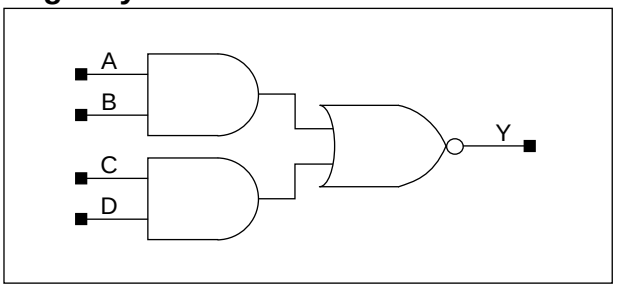
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.19 + 0.034*SL	0.18 + 0.036*SL	0.17 + 0.037*SL
	t_{PHL}	0.19	0.13 + 0.028*SL	0.14 + 0.027*SL	0.14 + 0.026*SL
	t_R	0.58	0.42 + 0.078*SL	0.41 + 0.082*SL	0.38 + 0.086*SL
	t_F	0.29	0.19 + 0.051*SL	0.18 + 0.055*SL	0.16 + 0.057*SL
B to Y	t_{PLH}	0.22	0.15 + 0.034*SL	0.15 + 0.036*SL	0.14 + 0.037*SL
	t_{PHL}	0.20	0.14 + 0.029*SL	0.15 + 0.026*SL	0.15 + 0.026*SL
	t_R	0.52	0.37 + 0.079*SL	0.35 + 0.083*SL	0.33 + 0.086*SL
	t_F	0.30	0.20 + 0.049*SL	0.19 + 0.054*SL	0.16 + 0.057*SL
C to Y	t_{PLH}	0.34	0.27 + 0.038*SL	0.27 + 0.038*SL	0.27 + 0.037*SL
	t_{PHL}	0.22	0.18 + 0.018*SL	0.18 + 0.017*SL	0.19 + 0.017*SL
	t_R	0.59	0.42 + 0.081*SL	0.42 + 0.083*SL	0.40 + 0.085*SL
	t_F	0.29	0.23 + 0.028*SL	0.23 + 0.030*SL	0.20 + 0.032*SL
D to Y	t_{PLH}	0.37	0.29 + 0.039*SL	0.30 + 0.038*SL	0.30 + 0.037*SL
	t_{PHL}	0.24	0.20 + 0.018*SL	0.20 + 0.018*SL	0.21 + 0.017*SL
	t_R	0.58	0.42 + 0.080*SL	0.41 + 0.084*SL	0.40 + 0.085*SL
	t_F	0.35	0.29 + 0.029*SL	0.29 + 0.030*SL	0.27 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

AO22/AO22D2

Two 2-ANDs into 2-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	1	1	0
0	x	0	x	1
0	x	x	0	1
x	0	x	0	1
x	0	0	x	1

Cell Data

Input Load (SL)								Gate Count	
AO22				*AO22D2*				*AO22*	*AO22D2*
A	B	C	D	A	B	C	D		
0.6	0.6	0.9	0.9	1.3	1.2	1.8	0.7	1.7	3.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.15 + 0.050*SL	0.15 + 0.051*SL	0.14 + 0.051*SL
	t_{PHL}	0.26	0.15 + 0.054*SL	0.15 + 0.053*SL	0.15 + 0.053*SL
	t_R	0.47	0.26 + 0.107*SL	0.24 + 0.114*SL	0.21 + 0.117*SL
	t_F	0.42	0.21 + 0.105*SL	0.19 + 0.110*SL	0.16 + 0.114*SL
B to Y	t_{PLH}	0.27	0.17 + 0.049*SL	0.16 + 0.051*SL	0.16 + 0.051*SL
	t_{PHL}	0.23	0.13 + 0.054*SL	0.13 + 0.053*SL	0.13 + 0.053*SL
	t_R	0.50	0.29 + 0.106*SL	0.27 + 0.114*SL	0.23 + 0.117*SL
	t_F	0.41	0.21 + 0.104*SL	0.19 + 0.111*SL	0.17 + 0.114*SL
C to Y	t_{PLH}	0.31	0.20 + 0.053*SL	0.21 + 0.051*SL	0.21 + 0.051*SL
	t_{PHL}	0.38	0.27 + 0.055*SL	0.28 + 0.054*SL	0.28 + 0.053*SL
	t_R	0.47	0.25 + 0.111*SL	0.24 + 0.115*SL	0.21 + 0.117*SL
	t_F	0.57	0.36 + 0.106*SL	0.34 + 0.111*SL	0.32 + 0.114*SL
D to Y	t_{PLH}	0.33	0.22 + 0.052*SL	0.22 + 0.051*SL	0.22 + 0.051*SL
	t_{PHL}	0.36	0.25 + 0.055*SL	0.26 + 0.054*SL	0.26 + 0.053*SL
	t_R	0.49	0.27 + 0.110*SL	0.26 + 0.115*SL	0.24 + 0.117*SL
	t_F	0.57	0.35 + 0.107*SL	0.34 + 0.111*SL	0.32 + 0.114*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO22D2

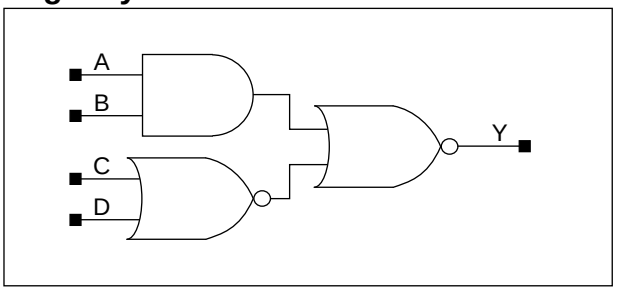
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.14 + 0.026*SL	0.15 + 0.024*SL	0.15 + 0.025*SL
	t_{PHL}	0.20	0.14 + 0.029*SL	0.15 + 0.026*SL	0.15 + 0.026*SL
	t_R	0.36	0.26 + 0.048*SL	0.25 + 0.054*SL	0.22 + 0.057*SL
	t_F	0.32	0.22 + 0.047*SL	0.20 + 0.054*SL	0.18 + 0.057*SL
B to Y	t_{PLH}	0.21	0.16 + 0.025*SL	0.16 + 0.024*SL	0.16 + 0.025*SL
	t_{PHL}	0.18	0.12 + 0.029*SL	0.13 + 0.027*SL	0.13 + 0.026*SL
	t_R	0.39	0.29 + 0.049*SL	0.28 + 0.053*SL	0.24 + 0.057*SL
	t_F	0.31	0.21 + 0.051*SL	0.20 + 0.054*SL	0.18 + 0.057*SL
C to Y	t_{PLH}	0.24	0.19 + 0.026*SL	0.19 + 0.025*SL	0.20 + 0.025*SL
	t_{PHL}	0.32	0.26 + 0.028*SL	0.27 + 0.027*SL	0.27 + 0.026*SL
	t_R	0.35	0.24 + 0.051*SL	0.23 + 0.055*SL	0.21 + 0.057*SL
	t_F	0.45	0.34 + 0.052*SL	0.34 + 0.054*SL	0.32 + 0.056*SL
D to Y	t_{PLH}	0.26	0.21 + 0.026*SL	0.21 + 0.025*SL	0.21 + 0.025*SL
	t_{PHL}	0.30	0.24 + 0.028*SL	0.24 + 0.027*SL	0.25 + 0.027*SL
	t_R	0.37	0.26 + 0.053*SL	0.26 + 0.055*SL	0.24 + 0.057*SL
	t_F	0.45	0.34 + 0.052*SL	0.33 + 0.055*SL	0.32 + 0.056*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

AO22A/AO22D2A

2-AND and 2-NOR into 2-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	1	x	x	0
x	x	0	0	0
Other States				1

Cell Data

Input Load (SL)								Gate Count	
AO22A				*AO22D2A*				*AO22A*	*AO22D2A*
A	B	C	D	A	B	C	D		
1.0	1.0	0.7	0.7	2.1	2.0	0.7	0.7	2.7	4.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO22A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.15 + 0.050*SL	0.15 + 0.051*SL	0.14 + 0.051*SL
	t_{PHL}	0.26	0.15 + 0.054*SL	0.15 + 0.053*SL	0.15 + 0.053*SL
	t_R	0.48	0.26 + 0.107*SL	0.24 + 0.114*SL	0.21 + 0.117*SL
	t_F	0.42	0.21 + 0.105*SL	0.19 + 0.110*SL	0.16 + 0.114*SL
B to Y	t_{PLH}	0.27	0.17 + 0.049*SL	0.16 + 0.051*SL	0.16 + 0.051*SL
	t_{PHL}	0.23	0.13 + 0.055*SL	0.13 + 0.053*SL	0.13 + 0.053*SL
	t_R	0.50	0.29 + 0.106*SL	0.27 + 0.114*SL	0.23 + 0.117*SL
	t_F	0.41	0.20 + 0.107*SL	0.19 + 0.111*SL	0.16 + 0.114*SL
C to Y	t_{PLH}	0.38	0.27 + 0.053*SL	0.28 + 0.052*SL	0.28 + 0.051*SL
	t_{PHL}	0.54	0.42 + 0.056*SL	0.43 + 0.054*SL	0.44 + 0.053*SL
	t_R	0.46	0.23 + 0.113*SL	0.22 + 0.116*SL	0.21 + 0.117*SL
	t_F	0.57	0.35 + 0.110*SL	0.34 + 0.112*SL	0.33 + 0.114*SL
D to Y	t_{PLH}	0.39	0.29 + 0.052*SL	0.29 + 0.052*SL	0.29 + 0.051*SL
	t_{PHL}	0.53	0.42 + 0.057*SL	0.42 + 0.054*SL	0.43 + 0.053*SL
	t_R	0.48	0.26 + 0.113*SL	0.25 + 0.116*SL	0.24 + 0.117*SL
	t_F	0.57	0.34 + 0.111*SL	0.34 + 0.112*SL	0.33 + 0.114*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO22D2A

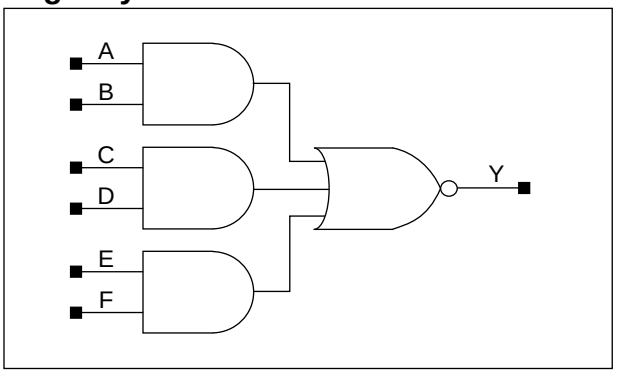
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.14 + 0.026*SL	0.15 + 0.024*SL	0.14 + 0.025*SL
	t_{PHL}	0.20	0.14 + 0.029*SL	0.15 + 0.026*SL	0.15 + 0.026*SL
	t_R	0.36	0.26 + 0.049*SL	0.25 + 0.054*SL	0.22 + 0.057*SL
	t_F	0.32	0.22 + 0.050*SL	0.20 + 0.054*SL	0.18 + 0.057*SL
B to Y	t_{PLH}	0.21	0.16 + 0.025*SL	0.16 + 0.024*SL	0.16 + 0.025*SL
	t_{PHL}	0.18	0.12 + 0.029*SL	0.13 + 0.027*SL	0.13 + 0.026*SL
	t_R	0.39	0.29 + 0.049*SL	0.28 + 0.053*SL	0.24 + 0.057*SL
	t_F	0.31	0.20 + 0.051*SL	0.19 + 0.054*SL	0.17 + 0.057*SL
C to Y	t_{PLH}	0.38	0.33 + 0.026*SL	0.33 + 0.025*SL	0.33 + 0.025*SL
	t_{PHL}	0.49	0.44 + 0.029*SL	0.44 + 0.028*SL	0.45 + 0.027*SL
	t_R	0.36	0.26 + 0.054*SL	0.25 + 0.055*SL	0.24 + 0.057*SL
	t_F	0.47	0.36 + 0.054*SL	0.36 + 0.055*SL	0.34 + 0.056*SL
D to Y	t_{PLH}	0.36	0.31 + 0.026*SL	0.31 + 0.025*SL	0.32 + 0.025*SL
	t_{PHL}	0.54	0.48 + 0.029*SL	0.48 + 0.028*SL	0.49 + 0.027*SL
	t_R	0.34	0.25 + 0.048*SL	0.23 + 0.055*SL	0.21 + 0.057*SL
	t_F	0.46	0.35 + 0.054*SL	0.35 + 0.055*SL	0.33 + 0.056*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

AO222/AO222D2

Three 2-ANDs into 3-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	x	x	x	x	0
x	x	1	1	x	x	0
x	x	x	x	1	1	0
Other States						1

Cell Data

Input Load (SL)												Gate Count	
AO222						*AO222D2*						*AO222*	*AO222D2*
A	B	C	D	E	F	A	B	C	D	E	F		
0.6	0.6	0.6	0.6	0.9	0.9	0.5	0.5	0.5	0.5	0.6	0.6	2.7	4.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.34	0.19 + 0.072*SL	0.18 + 0.076*SL	0.18 + 0.077*SL
	t_{PHL}	0.28	0.17 + 0.053*SL	0.17 + 0.053*SL	0.17 + 0.053*SL
	t_R	0.81	0.46 + 0.172*SL	0.45 + 0.176*SL	0.45 + 0.176*SL
	t_F	0.48	0.27 + 0.106*SL	0.25 + 0.111*SL	0.22 + 0.114*SL
B to Y	t_{PLH}	0.36	0.21 + 0.073*SL	0.20 + 0.076*SL	0.20 + 0.077*SL
	t_{PHL}	0.26	0.15 + 0.054*SL	0.15 + 0.053*SL	0.15 + 0.053*SL
	t_R	0.84	0.50 + 0.171*SL	0.49 + 0.176*SL	0.49 + 0.176*SL
	t_F	0.47	0.26 + 0.108*SL	0.25 + 0.111*SL	0.22 + 0.114*SL
C to Y	t_{PLH}	0.48	0.32 + 0.079*SL	0.33 + 0.078*SL	0.33 + 0.077*SL
	t_{PHL}	0.41	0.30 + 0.055*SL	0.30 + 0.054*SL	0.31 + 0.053*SL
	t_R	0.85	0.51 + 0.170*SL	0.50 + 0.174*SL	0.48 + 0.175*SL
	t_F	0.63	0.41 + 0.108*SL	0.40 + 0.111*SL	0.38 + 0.114*SL
D to Y	t_{PLH}	0.50	0.35 + 0.078*SL	0.35 + 0.077*SL	0.36 + 0.077*SL
	t_{PHL}	0.39	0.28 + 0.055*SL	0.28 + 0.054*SL	0.29 + 0.053*SL
	t_R	0.88	0.54 + 0.170*SL	0.53 + 0.174*SL	0.52 + 0.175*SL
	t_F	0.63	0.41 + 0.109*SL	0.40 + 0.111*SL	0.38 + 0.114*SL
E to Y	t_{PLH}	0.55	0.39 + 0.079*SL	0.40 + 0.078*SL	0.41 + 0.077*SL
	t_{PHL}	0.50	0.39 + 0.059*SL	0.40 + 0.056*SL	0.42 + 0.053*SL
	t_R	0.85	0.51 + 0.170*SL	0.50 + 0.174*SL	0.48 + 0.175*SL
	t_F	0.80	0.59 + 0.108*SL	0.58 + 0.111*SL	0.56 + 0.113*SL
F to Y	t_{PLH}	0.58	0.42 + 0.078*SL	0.42 + 0.077*SL	0.43 + 0.077*SL
	t_{PHL}	0.48	0.36 + 0.059*SL	0.37 + 0.056*SL	0.40 + 0.053*SL
	t_R	0.88	0.54 + 0.170*SL	0.53 + 0.174*SL	0.52 + 0.175*SL
	t_F	0.81	0.59 + 0.110*SL	0.58 + 0.111*SL	0.56 + 0.113*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO222D2

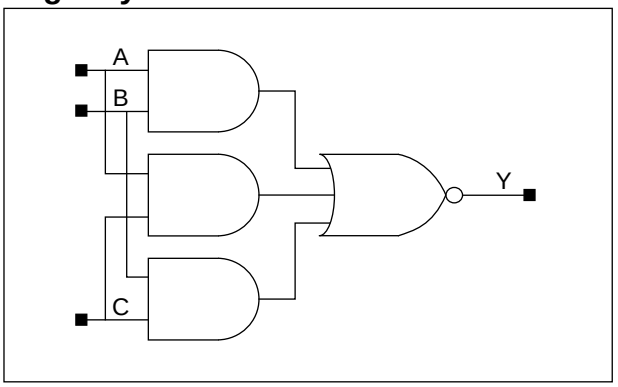
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.63	0.59 + 0.017*SL	0.60 + 0.014*SL	0.61 + 0.013*SL
	t_{PHL}	0.49	0.44 + 0.022*SL	0.45 + 0.018*SL	0.47 + 0.017*SL
	t_R	0.17	0.13 + 0.023*SL	0.12 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
B to Y	t_{PLH}	0.68	0.64 + 0.017*SL	0.65 + 0.014*SL	0.66 + 0.013*SL
	t_{PHL}	0.47	0.42 + 0.022*SL	0.43 + 0.018*SL	0.45 + 0.017*SL
	t_R	0.18	0.13 + 0.022*SL	0.12 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
C to Y	t_{PLH}	0.78	0.74 + 0.017*SL	0.75 + 0.014*SL	0.77 + 0.013*SL
	t_{PHL}	0.58	0.53 + 0.022*SL	0.54 + 0.018*SL	0.56 + 0.017*SL
	t_R	0.17	0.13 + 0.023*SL	0.12 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
D to Y	t_{PLH}	0.83	0.80 + 0.017*SL	0.80 + 0.014*SL	0.82 + 0.013*SL
	t_{PHL}	0.55	0.51 + 0.022*SL	0.52 + 0.018*SL	0.54 + 0.017*SL
	t_R	0.18	0.13 + 0.024*SL	0.12 + 0.025*SL	0.09 + 0.029*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
E to Y	t_{PLH}	0.86	0.83 + 0.017*SL	0.83 + 0.014*SL	0.85 + 0.013*SL
	t_{PHL}	0.63	0.58 + 0.022*SL	0.60 + 0.018*SL	0.61 + 0.017*SL
	t_R	0.17	0.13 + 0.023*SL	0.12 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
F to Y	t_{PLH}	0.91	0.88 + 0.017*SL	0.89 + 0.014*SL	0.90 + 0.013*SL
	t_{PHL}	0.61	0.56 + 0.022*SL	0.57 + 0.018*SL	0.59 + 0.017*SL
	t_R	0.18	0.13 + 0.023*SL	0.12 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.17	0.10 + 0.033*SL	0.11 + 0.030*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

AO222A/AO222D2A

Inverting 2-of-3 Majority with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	Y
1	1	x	0
1	x	1	0
x	1	1	0
0	0	x	1
0	x	0	1
x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
AO222A			*AO222D2A*			*AO222A*	*AO222D2A*
A	B	C	A	B	C		
1.3	1.6	1.7	2.6	3.2	4.2	2.7	5.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO222A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.41	0.27 + 0.069*SL	0.28 + 0.066*SL	0.29 + 0.065*SL
	t_{PHL}	0.41	0.30 + 0.058*SL	0.31 + 0.055*SL	0.32 + 0.053*SL
	t_R	0.75	0.46 + 0.142*SL	0.45 + 0.146*SL	0.45 + 0.147*SL
	t_F	0.60	0.38 + 0.108*SL	0.37 + 0.112*SL	0.36 + 0.113*SL
B to Y	t_{PLH}	0.46	0.32 + 0.069*SL	0.33 + 0.066*SL	0.34 + 0.064*SL
	t_{PHL}	0.46	0.33 + 0.065*SL	0.35 + 0.058*SL	0.39 + 0.054*SL
	t_R	0.76	0.47 + 0.141*SL	0.46 + 0.145*SL	0.45 + 0.147*SL
	t_F	0.75	0.53 + 0.110*SL	0.52 + 0.112*SL	0.52 + 0.113*SL
C to Y	t_{PLH}	0.49	0.35 + 0.067*SL	0.36 + 0.064*SL	0.37 + 0.064*SL
	t_{PHL}	0.44	0.31 + 0.065*SL	0.33 + 0.058*SL	0.37 + 0.054*SL
	t_R	0.69	0.42 + 0.139*SL	0.40 + 0.144*SL	0.38 + 0.146*SL
	t_F	0.77	0.55 + 0.110*SL	0.54 + 0.111*SL	0.53 + 0.113*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO222D2A

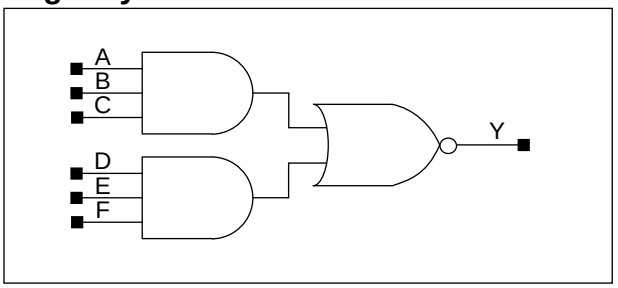
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.33	0.26 + 0.035*SL	0.27 + 0.033*SL	0.28 + 0.032*SL
	t_{PHL}	0.36	0.30 + 0.030*SL	0.30 + 0.028*SL	0.32 + 0.027*SL
	t_R	0.59	0.46 + 0.067*SL	0.45 + 0.070*SL	0.44 + 0.071*SL
	t_F	0.50	0.39 + 0.054*SL	0.39 + 0.055*SL	0.37 + 0.057*SL
B to Y	t_{PLH}	0.38	0.31 + 0.035*SL	0.31 + 0.033*SL	0.32 + 0.031*SL
	t_{PHL}	0.40	0.33 + 0.034*SL	0.34 + 0.030*SL	0.37 + 0.027*SL
	t_R	0.60	0.47 + 0.067*SL	0.46 + 0.070*SL	0.45 + 0.071*SL
	t_F	0.63	0.52 + 0.054*SL	0.52 + 0.056*SL	0.51 + 0.056*SL
C to Y	t_{PLH}	0.41	0.34 + 0.034*SL	0.35 + 0.032*SL	0.35 + 0.031*SL
	t_{PHL}	0.37	0.31 + 0.033*SL	0.31 + 0.030*SL	0.35 + 0.027*SL
	t_R	0.54	0.41 + 0.066*SL	0.40 + 0.069*SL	0.38 + 0.071*SL
	t_F	0.65	0.54 + 0.054*SL	0.54 + 0.055*SL	0.53 + 0.056*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

AO33/AO33D2

Two 3-ANDs into 2-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	Y
1	1	1	x	x	x	0
x	x	x	1	1	1	0
Other States						1

Cell Data

Input Load (SL)												Gate Count	
AO33						*AO33D2*						*AO33*	*AO33D2*
A	B	C	D	E	F	A	B	C	D	E	F		
1.0	0.7	0.6	1.0	1.0	1.0	0.5	0.5	0.5	0.7	0.7	0.7	2.3	3.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO33

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.19 + 0.050*SL	0.19 + 0.051*SL	0.19 + 0.051*SL
	t_{PHL}	0.38	0.23 + 0.075*SL	0.24 + 0.073*SL	0.24 + 0.073*SL
	t_R	0.57	0.35 + 0.110*SL	0.34 + 0.115*SL	0.31 + 0.117*SL
	t_F	0.73	0.42 + 0.155*SL	0.40 + 0.160*SL	0.39 + 0.162*SL
B to Y	t_{PLH}	0.31	0.21 + 0.051*SL	0.21 + 0.051*SL	0.21 + 0.051*SL
	t_{PHL}	0.38	0.23 + 0.075*SL	0.23 + 0.074*SL	0.24 + 0.073*SL
	t_R	0.59	0.37 + 0.110*SL	0.36 + 0.115*SL	0.33 + 0.117*SL
	t_F	0.73	0.41 + 0.158*SL	0.40 + 0.160*SL	0.39 + 0.162*SL
C to Y	t_{PLH}	0.32	0.22 + 0.051*SL	0.22 + 0.051*SL	0.22 + 0.051*SL
	t_{PHL}	0.37	0.21 + 0.076*SL	0.22 + 0.073*SL	0.23 + 0.073*SL
	t_R	0.62	0.41 + 0.108*SL	0.39 + 0.114*SL	0.36 + 0.117*SL
	t_F	0.72	0.41 + 0.158*SL	0.40 + 0.160*SL	0.39 + 0.162*SL
D to Y	t_{PLH}	0.36	0.26 + 0.052*SL	0.26 + 0.052*SL	0.27 + 0.051*SL
	t_{PHL}	0.62	0.47 + 0.075*SL	0.47 + 0.074*SL	0.48 + 0.073*SL
	t_R	0.57	0.34 + 0.112*SL	0.33 + 0.115*SL	0.32 + 0.117*SL
	t_F	0.95	0.63 + 0.159*SL	0.62 + 0.161*SL	0.62 + 0.162*SL
E to Y	t_{PLH}	0.38	0.28 + 0.052*SL	0.28 + 0.052*SL	0.28 + 0.051*SL
	t_{PHL}	0.61	0.46 + 0.075*SL	0.47 + 0.074*SL	0.47 + 0.073*SL
	t_R	0.59	0.37 + 0.112*SL	0.36 + 0.115*SL	0.34 + 0.117*SL
	t_F	0.95	0.63 + 0.158*SL	0.63 + 0.161*SL	0.62 + 0.162*SL
F to Y	t_{PLH}	0.40	0.29 + 0.052*SL	0.29 + 0.052*SL	0.30 + 0.051*SL
	t_{PHL}	0.60	0.45 + 0.075*SL	0.46 + 0.074*SL	0.46 + 0.073*SL
	t_R	0.62	0.39 + 0.112*SL	0.38 + 0.115*SL	0.37 + 0.117*SL
	t_F	0.95	0.63 + 0.159*SL	0.63 + 0.161*SL	0.62 + 0.162*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO33D2

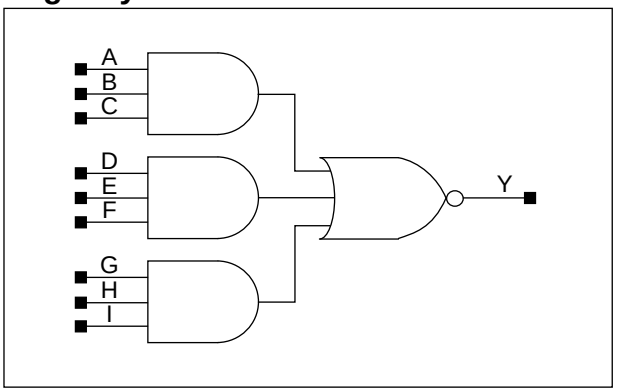
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.55	0.52 + 0.016*SL	0.52 + 0.014*SL	0.53 + 0.013*SL
	t_{PHL}	0.58	0.53 + 0.022*SL	0.54 + 0.018*SL	0.56 + 0.017*SL
	t_R	0.16	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
B to Y	t_{PLH}	0.59	0.55 + 0.017*SL	0.56 + 0.014*SL	0.57 + 0.013*SL
	t_{PHL}	0.58	0.53 + 0.022*SL	0.54 + 0.018*SL	0.56 + 0.017*SL
	t_R	0.16	0.11 + 0.023*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
C to Y	t_{PLH}	0.61	0.58 + 0.017*SL	0.59 + 0.014*SL	0.60 + 0.013*SL
	t_{PHL}	0.56	0.52 + 0.022*SL	0.53 + 0.018*SL	0.55 + 0.017*SL
	t_R	0.16	0.11 + 0.024*SL	0.11 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D to Y	t_{PLH}	0.63	0.60 + 0.016*SL	0.60 + 0.014*SL	0.61 + 0.013*SL
	t_{PHL}	0.72	0.67 + 0.022*SL	0.69 + 0.018*SL	0.70 + 0.017*SL
	t_R	0.16	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.030*SL	0.09 + 0.032*SL
E to Y	t_{PLH}	0.66	0.63 + 0.017*SL	0.64 + 0.014*SL	0.65 + 0.013*SL
	t_{PHL}	0.72	0.67 + 0.022*SL	0.68 + 0.018*SL	0.70 + 0.017*SL
	t_R	0.16	0.11 + 0.025*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.030*SL	0.09 + 0.032*SL
F to Y	t_{PLH}	0.69	0.66 + 0.017*SL	0.67 + 0.014*SL	0.68 + 0.013*SL
	t_{PHL}	0.70	0.66 + 0.022*SL	0.67 + 0.018*SL	0.69 + 0.017*SL
	t_R	0.16	0.12 + 0.023*SL	0.11 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.11 + 0.030*SL	0.11 + 0.031*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

AO333/AO333D2

Three 3-ANDs into 3-NOR with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Y
1	1	1	x	x	x	x	x	x	0
x	x	x	1	1	1	x	x	x	0
x	x	x	x	x	x	1	1	1	0
Other States									1

Cell Data

Input Load (SL)									Gate Count
AO333									*AO333*
A	B	C	D	E	F	G	H	I	
0.6	0.6	0.6	1.0	1.0	1.0	0.8	0.8	0.9	3.3
AO333D2									*AO333D2*
A	B	C	D	E	F	G	H	I	
0.5	0.4	0.5	0.7	0.7	0.7	0.5	0.5	0.6	4.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO333

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.42	0.27 + 0.076*SL	0.27 + 0.077*SL	0.27 + 0.077*SL
	t_{PHL}	0.42	0.27 + 0.075*SL	0.27 + 0.073*SL	0.28 + 0.073*SL
	t_R	0.99	0.64 + 0.173*SL	0.63 + 0.177*SL	0.64 + 0.176*SL
	t_F	0.86	0.54 + 0.156*SL	0.53 + 0.160*SL	0.52 + 0.162*SL
B to Y	t_{PLH}	0.44	0.29 + 0.076*SL	0.29 + 0.077*SL	0.29 + 0.077*SL
	t_{PHL}	0.41	0.26 + 0.076*SL	0.27 + 0.074*SL	0.27 + 0.073*SL
	t_R	1.02	0.68 + 0.173*SL	0.67 + 0.177*SL	0.68 + 0.176*SL
	t_F	0.86	0.54 + 0.158*SL	0.53 + 0.160*SL	0.52 + 0.162*SL
C to Y	t_{PLH}	0.46	0.31 + 0.077*SL	0.31 + 0.077*SL	0.31 + 0.077*SL
	t_{PHL}	0.40	0.25 + 0.076*SL	0.25 + 0.074*SL	0.26 + 0.073*SL
	t_R	1.06	0.72 + 0.172*SL	0.70 + 0.177*SL	0.71 + 0.176*SL
	t_F	0.85	0.54 + 0.158*SL	0.53 + 0.161*SL	0.52 + 0.162*SL
D to Y	t_{PLH}	0.59	0.43 + 0.079*SL	0.43 + 0.078*SL	0.44 + 0.077*SL
	t_{PHL}	0.59	0.44 + 0.077*SL	0.44 + 0.074*SL	0.46 + 0.073*SL
	t_R	1.04	0.69 + 0.171*SL	0.69 + 0.174*SL	0.67 + 0.175*SL
	t_F	1.12	0.81 + 0.156*SL	0.80 + 0.160*SL	0.78 + 0.162*SL
E to Y	t_{PLH}	0.61	0.46 + 0.079*SL	0.46 + 0.077*SL	0.47 + 0.077*SL
	t_{PHL}	0.59	0.43 + 0.077*SL	0.44 + 0.075*SL	0.45 + 0.073*SL
	t_R	1.07	0.73 + 0.172*SL	0.72 + 0.174*SL	0.71 + 0.175*SL
	t_F	1.13	0.81 + 0.156*SL	0.80 + 0.159*SL	0.78 + 0.162*SL
F to Y	t_{PLH}	0.64	0.48 + 0.078*SL	0.48 + 0.078*SL	0.49 + 0.077*SL
	t_{PHL}	0.58	0.42 + 0.077*SL	0.43 + 0.075*SL	0.44 + 0.073*SL
	t_R	1.11	0.77 + 0.172*SL	0.76 + 0.174*SL	0.74 + 0.175*SL
	t_F	1.13	0.82 + 0.155*SL	0.80 + 0.159*SL	0.78 + 0.162*SL
G to Y	t_{PLH}	0.67	0.51 + 0.080*SL	0.52 + 0.078*SL	0.53 + 0.077*SL
	t_{PHL}	0.71	0.55 + 0.082*SL	0.56 + 0.078*SL	0.60 + 0.074*SL
	t_R	1.04	0.70 + 0.171*SL	0.69 + 0.174*SL	0.67 + 0.175*SL
	t_F	1.42	1.11 + 0.156*SL	1.10 + 0.159*SL	1.08 + 0.161*SL
H to Y	t_{PLH}	0.70	0.54 + 0.079*SL	0.55 + 0.078*SL	0.55 + 0.077*SL
	t_{PHL}	0.71	0.54 + 0.082*SL	0.56 + 0.078*SL	0.59 + 0.074*SL
	t_R	1.07	0.73 + 0.171*SL	0.72 + 0.174*SL	0.71 + 0.175*SL
	t_F	1.42	1.11 + 0.156*SL	1.10 + 0.159*SL	1.08 + 0.161*SL
I to Y	t_{PLH}	0.72	0.57 + 0.078*SL	0.57 + 0.078*SL	0.58 + 0.077*SL
	t_{PHL}	0.70	0.53 + 0.082*SL	0.54 + 0.078*SL	0.58 + 0.074*SL
	t_R	1.11	0.77 + 0.171*SL	0.76 + 0.174*SL	0.75 + 0.175*SL
	t_F	1.42	1.11 + 0.157*SL	1.10 + 0.159*SL	1.08 + 0.161*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

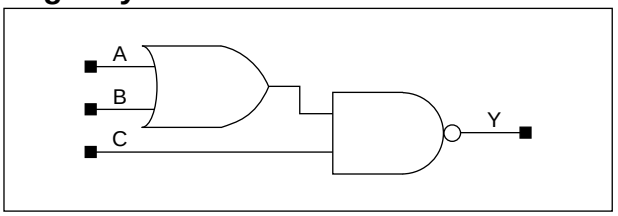
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

AO333D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.77	0.74 + 0.018*SL	0.74 + 0.014*SL	0.76 + 0.013*SL
	t_{PHL}	0.65	0.60 + 0.022*SL	0.61 + 0.018*SL	0.63 + 0.017*SL
	t_R	0.19	0.14 + 0.022*SL	0.14 + 0.025*SL	0.10 + 0.028*SL
	t_F	0.18	0.11 + 0.030*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
B to Y	t_{PLH}	0.81	0.78 + 0.018*SL	0.79 + 0.014*SL	0.80 + 0.013*SL
	t_{PHL}	0.64	0.60 + 0.022*SL	0.61 + 0.018*SL	0.63 + 0.017*SL
	t_R	0.19	0.15 + 0.022*SL	0.14 + 0.025*SL	0.11 + 0.028*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
C to Y	t_{PLH}	0.86	0.82 + 0.018*SL	0.83 + 0.015*SL	0.85 + 0.013*SL
	t_{PHL}	0.63	0.59 + 0.022*SL	0.60 + 0.018*SL	0.62 + 0.017*SL
	t_R	0.20	0.16 + 0.020*SL	0.14 + 0.025*SL	0.11 + 0.028*SL
	t_F	0.18	0.12 + 0.029*SL	0.11 + 0.030*SL	0.10 + 0.032*SL
D to Y	t_{PLH}	0.95	0.91 + 0.018*SL	0.92 + 0.014*SL	0.94 + 0.013*SL
	t_{PHL}	0.77	0.73 + 0.023*SL	0.74 + 0.018*SL	0.76 + 0.017*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.025*SL	0.10 + 0.028*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
E to Y	t_{PLH}	1.00	0.96 + 0.018*SL	0.97 + 0.014*SL	0.99 + 0.013*SL
	t_{PHL}	0.77	0.73 + 0.022*SL	0.74 + 0.018*SL	0.76 + 0.017*SL
	t_R	0.19	0.15 + 0.020*SL	0.14 + 0.025*SL	0.11 + 0.028*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
F to Y	t_{PLH}	1.05	1.01 + 0.018*SL	1.02 + 0.014*SL	1.03 + 0.013*SL
	t_{PHL}	0.76	0.72 + 0.023*SL	0.73 + 0.018*SL	0.74 + 0.017*SL
	t_R	0.20	0.16 + 0.020*SL	0.14 + 0.025*SL	0.11 + 0.028*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
G to Y	t_{PLH}	1.04	1.01 + 0.018*SL	1.02 + 0.014*SL	1.03 + 0.013*SL
	t_{PHL}	0.86	0.82 + 0.022*SL	0.83 + 0.018*SL	0.84 + 0.017*SL
	t_R	0.19	0.15 + 0.022*SL	0.14 + 0.025*SL	0.10 + 0.028*SL
	t_F	0.19	0.13 + 0.030*SL	0.13 + 0.030*SL	0.11 + 0.032*SL
H to Y	t_{PLH}	1.09	1.06 + 0.018*SL	1.07 + 0.014*SL	1.08 + 0.013*SL
	t_{PHL}	0.86	0.81 + 0.022*SL	0.82 + 0.018*SL	0.84 + 0.017*SL
	t_R	0.19	0.14 + 0.023*SL	0.14 + 0.025*SL	0.11 + 0.028*SL
	t_F	0.19	0.13 + 0.031*SL	0.13 + 0.030*SL	0.11 + 0.032*SL
I to Y	t_{PLH}	1.14	1.10 + 0.018*SL	1.11 + 0.014*SL	1.13 + 0.013*SL
	t_{PHL}	0.85	0.80 + 0.022*SL	0.81 + 0.018*SL	0.83 + 0.017*SL
	t_R	0.20	0.15 + 0.023*SL	0.15 + 0.025*SL	0.11 + 0.028*SL
	t_F	0.19	0.13 + 0.029*SL	0.13 + 0.030*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	B	C	Y
1	x	1	0
x	1	1	0
0	0	x	1
x	x	0	1

Cell Data

Input Load (SL)						Gate Count	
OA21			*OA21D2*			*OA21*	*OA21D2*
A	B	C	A	B	C		
0.9	0.6	1.0	1.7	1.2	2.1	1.3	2.3

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OA21

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.14 + 0.052*SL	0.14 + 0.051*SL	0.14 + 0.051*SL
	t_{PHL}	0.29	0.19 + 0.053*SL	0.19 + 0.053*SL	0.19 + 0.053*SL
	t_R	0.43	0.21 + 0.109*SL	0.19 + 0.115*SL	0.17 + 0.117*SL
	t_F	0.47	0.26 + 0.102*SL	0.24 + 0.110*SL	0.20 + 0.114*SL
B to Y	t_{PLH}	0.24	0.14 + 0.051*SL	0.14 + 0.051*SL	0.14 + 0.051*SL
	t_{PHL}	0.25	0.14 + 0.054*SL	0.14 + 0.053*SL	0.14 + 0.053*SL
	t_R	0.44	0.23 + 0.105*SL	0.20 + 0.113*SL	0.17 + 0.117*SL
	t_F	0.39	0.18 + 0.104*SL	0.16 + 0.110*SL	0.13 + 0.114*SL
C to Y	t_{PLH}	0.19	0.13 + 0.030*SL	0.14 + 0.027*SL	0.13 + 0.027*SL
	t_{PHL}	0.29	0.18 + 0.054*SL	0.18 + 0.053*SL	0.18 + 0.053*SL
	t_R	0.29	0.19 + 0.048*SL	0.17 + 0.055*SL	0.13 + 0.060*SL
	t_F	0.45	0.24 + 0.107*SL	0.22 + 0.111*SL	0.20 + 0.114*SL

OA21D2

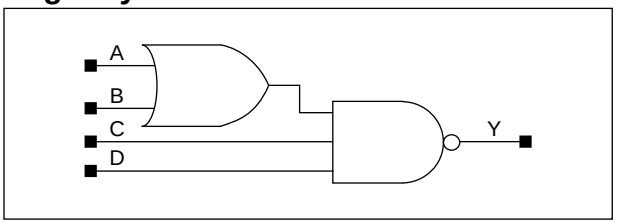
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.14 + 0.028*SL	0.14 + 0.026*SL	0.14 + 0.026*SL
	t_{PHL}	0.24	0.18 + 0.027*SL	0.18 + 0.026*SL	0.18 + 0.026*SL
	t_R	0.32	0.21 + 0.051*SL	0.20 + 0.056*SL	0.18 + 0.058*SL
	t_F	0.36	0.26 + 0.049*SL	0.25 + 0.053*SL	0.22 + 0.057*SL
B to Y	t_{PLH}	0.19	0.13 + 0.029*SL	0.14 + 0.025*SL	0.14 + 0.026*SL
	t_{PHL}	0.19	0.13 + 0.029*SL	0.14 + 0.026*SL	0.14 + 0.026*SL
	t_R	0.33	0.24 + 0.049*SL	0.22 + 0.054*SL	0.18 + 0.058*SL
	t_F	0.29	0.18 + 0.052*SL	0.18 + 0.053*SL	0.14 + 0.057*SL
C to Y	t_{PLH}	0.15	0.12 + 0.017*SL	0.13 + 0.014*SL	0.13 + 0.013*SL
	t_{PHL}	0.23	0.17 + 0.027*SL	0.17 + 0.027*SL	0.18 + 0.026*SL
	t_R	0.23	0.19 + 0.024*SL	0.18 + 0.024*SL	0.15 + 0.028*SL
	t_F	0.34	0.24 + 0.052*SL	0.23 + 0.055*SL	0.21 + 0.057*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

OA211/OA211D2

2-OR into 3-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
1	x	1	1	0
x	1	1	1	0
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1

Cell Data

Input Load (SL)								Gate Count	
OA211				*OA211D2*				*OA211*	*OA211D2*
A	B	C	D	A	B	C	D		
0.9	0.6	1.0	1.0	2.0	2.1	2.1	2.2	1.7	3.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OA211

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.27	0.17 + 0.051*SL	0.17 + 0.051*SL	0.17 + 0.051*SL
	t_{PHL}	0.42	0.27 + 0.073*SL	0.27 + 0.073*SL	0.28 + 0.073*SL
	t_R	0.49	0.27 + 0.111*SL	0.26 + 0.115*SL	0.24 + 0.117*SL
	t_F	0.73	0.42 + 0.154*SL	0.40 + 0.160*SL	0.39 + 0.162*SL
B to Y	t_{PLH}	0.27	0.17 + 0.050*SL	0.17 + 0.051*SL	0.17 + 0.051*SL
	t_{PHL}	0.36	0.21 + 0.073*SL	0.21 + 0.073*SL	0.21 + 0.073*SL
	t_R	0.50	0.29 + 0.107*SL	0.27 + 0.114*SL	0.23 + 0.117*SL
	t_F	0.63	0.32 + 0.156*SL	0.30 + 0.161*SL	0.29 + 0.162*SL
C to Y	t_{PLH}	0.20	0.14 + 0.029*SL	0.15 + 0.027*SL	0.15 + 0.027*SL
	t_{PHL}	0.44	0.29 + 0.075*SL	0.29 + 0.073*SL	0.30 + 0.073*SL
	t_R	0.32	0.21 + 0.051*SL	0.20 + 0.055*SL	0.16 + 0.060*SL
	t_F	0.72	0.41 + 0.158*SL	0.40 + 0.160*SL	0.39 + 0.162*SL
D to Y	t_{PLH}	0.21	0.15 + 0.028*SL	0.16 + 0.027*SL	0.16 + 0.027*SL
	t_{PHL}	0.43	0.28 + 0.075*SL	0.28 + 0.073*SL	0.29 + 0.073*SL
	t_R	0.33	0.23 + 0.050*SL	0.22 + 0.055*SL	0.17 + 0.060*SL
	t_F	0.72	0.40 + 0.159*SL	0.40 + 0.160*SL	0.39 + 0.162*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OA211D2

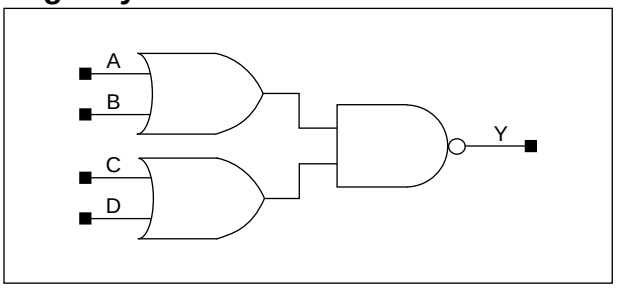
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.16 + 0.027*SL	0.17 + 0.026*SL	0.17 + 0.026*SL
	t_{PHL}	0.34	0.27 + 0.037*SL	0.27 + 0.036*SL	0.27 + 0.036*SL
	t_R	0.38	0.27 + 0.054*SL	0.26 + 0.057*SL	0.25 + 0.058*SL
	t_F	0.57	0.42 + 0.076*SL	0.41 + 0.078*SL	0.39 + 0.081*SL
B to Y	t_{PLH}	0.22	0.16 + 0.027*SL	0.17 + 0.025*SL	0.17 + 0.026*SL
	t_{PHL}	0.28	0.21 + 0.036*SL	0.21 + 0.036*SL	0.21 + 0.036*SL
	t_R	0.39	0.29 + 0.050*SL	0.28 + 0.055*SL	0.25 + 0.058*SL
	t_F	0.47	0.32 + 0.076*SL	0.31 + 0.079*SL	0.29 + 0.081*SL
C to Y	t_{PLH}	0.17	0.13 + 0.016*SL	0.14 + 0.013*SL	0.15 + 0.013*SL
	t_{PHL}	0.36	0.29 + 0.037*SL	0.29 + 0.037*SL	0.29 + 0.036*SL
	t_R	0.26	0.22 + 0.022*SL	0.21 + 0.025*SL	0.18 + 0.028*SL
	t_F	0.56	0.41 + 0.078*SL	0.40 + 0.079*SL	0.39 + 0.081*SL
D to Y	t_{PLH}	0.17	0.14 + 0.015*SL	0.15 + 0.014*SL	0.15 + 0.013*SL
	t_{PHL}	0.35	0.27 + 0.037*SL	0.27 + 0.037*SL	0.28 + 0.036*SL
	t_R	0.28	0.23 + 0.023*SL	0.23 + 0.025*SL	0.19 + 0.028*SL
	t_F	0.56	0.40 + 0.078*SL	0.40 + 0.080*SL	0.39 + 0.081*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

OA22/OA22D2

Two 2-ORs into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	0	0	1
1	x	x	1	0
x	1	x	1	0
1	x	1	x	0
x	1	1	x	0

Cell Data

Input Load (SL)								Gate Count	
OA22				*OA22D2*				*OA22*	*OA22D2*
A	B	C	D	A	B	C	D		
0.9	0.6	0.6	0.9	1.7	1.2	1.3	1.8	1.7	3.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OA22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.26	0.15 + 0.054*SL	0.16 + 0.052*SL	0.16 + 0.051*SL
	t_{PHL}	0.34	0.24 + 0.054*SL	0.24 + 0.053*SL	0.24 + 0.053*SL
	t_R	0.53	0.32 + 0.108*SL	0.30 + 0.115*SL	0.27 + 0.117*SL
	t_F	0.53	0.32 + 0.104*SL	0.30 + 0.111*SL	0.27 + 0.114*SL
B to Y	t_{PLH}	0.26	0.15 + 0.052*SL	0.15 + 0.052*SL	0.16 + 0.051*SL
	t_{PHL}	0.30	0.19 + 0.054*SL	0.19 + 0.053*SL	0.20 + 0.053*SL
	t_R	0.55	0.34 + 0.103*SL	0.31 + 0.113*SL	0.27 + 0.117*SL
	t_F	0.45	0.24 + 0.107*SL	0.23 + 0.111*SL	0.20 + 0.114*SL
C to Y	t_{PLH}	0.29	0.19 + 0.052*SL	0.19 + 0.051*SL	0.19 + 0.051*SL
	t_{PHL}	0.30	0.19 + 0.055*SL	0.20 + 0.053*SL	0.20 + 0.053*SL
	t_R	0.60	0.40 + 0.104*SL	0.37 + 0.113*SL	0.33 + 0.117*SL
	t_F	0.45	0.23 + 0.108*SL	0.22 + 0.112*SL	0.20 + 0.114*SL
D to Y	t_{PLH}	0.30	0.19 + 0.052*SL	0.19 + 0.052*SL	0.20 + 0.051*SL
	t_{PHL}	0.35	0.24 + 0.055*SL	0.24 + 0.053*SL	0.24 + 0.053*SL
	t_R	0.59	0.38 + 0.109*SL	0.36 + 0.114*SL	0.33 + 0.117*SL
	t_F	0.52	0.31 + 0.107*SL	0.29 + 0.111*SL	0.27 + 0.114*SL

*Group1 : SL < 3, *Group2 : 3 ≤SL≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OA22D2

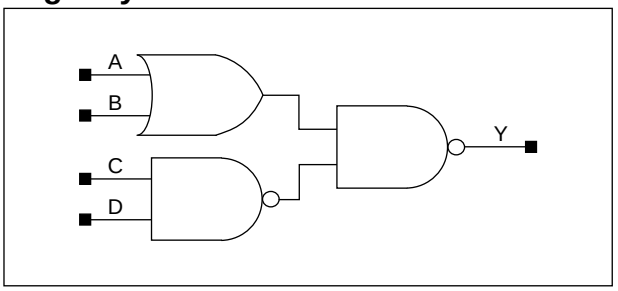
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.15 + 0.028*SL	0.15 + 0.026*SL	0.16 + 0.026*SL
	t_{PHL}	0.29	0.23 + 0.027*SL	0.24 + 0.027*SL	0.24 + 0.026*SL
	t_R	0.43	0.33 + 0.051*SL	0.31 + 0.056*SL	0.29 + 0.058*SL
	t_F	0.43	0.32 + 0.051*SL	0.32 + 0.054*SL	0.29 + 0.057*SL
B to Y	t_{PLH}	0.20	0.15 + 0.029*SL	0.15 + 0.026*SL	0.16 + 0.026*SL
	t_{PHL}	0.25	0.19 + 0.027*SL	0.19 + 0.027*SL	0.20 + 0.026*SL
	t_R	0.45	0.35 + 0.049*SL	0.34 + 0.054*SL	0.29 + 0.058*SL
	t_F	0.35	0.25 + 0.051*SL	0.24 + 0.054*SL	0.22 + 0.057*SL
C to Y	t_{PLH}	0.24	0.19 + 0.026*SL	0.19 + 0.025*SL	0.19 + 0.026*SL
	t_{PHL}	0.24	0.19 + 0.028*SL	0.19 + 0.027*SL	0.20 + 0.026*SL
	t_R	0.39	0.29 + 0.052*SL	0.28 + 0.055*SL	0.25 + 0.058*SL
	t_F	0.34	0.24 + 0.053*SL	0.23 + 0.055*SL	0.22 + 0.057*SL
D to Y	t_{PLH}	0.24	0.19 + 0.027*SL	0.19 + 0.026*SL	0.20 + 0.026*SL
	t_{PHL}	0.29	0.24 + 0.027*SL	0.24 + 0.027*SL	0.24 + 0.026*SL
	t_R	0.48	0.38 + 0.052*SL	0.37 + 0.056*SL	0.35 + 0.058*SL
	t_F	0.42	0.31 + 0.054*SL	0.31 + 0.055*SL	0.29 + 0.057*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

OA22A/OA22D2A

2-OR and 2-NAND into 2-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	Y
0	0	x	x	1
x	x	1	1	1
1	x	0	x	0
1	x	x	0	0
x	1	0	x	0
x	1	x	0	0

Cell Data

Input Load (SL)								Gate Count	
OA22A				*OA22D2A*				*OA22A*	*OA22D2A*
A	B	C	D	A	B	C	D		
0.8	0.8	0.7	0.8	1.6	1.5	0.8	0.8	2.0	3.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OA22A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.14 + 0.053*SL	0.14 + 0.051*SL	0.14 + 0.051*SL
	t_{PHL}	0.29	0.19 + 0.054*SL	0.19 + 0.053*SL	0.19 + 0.053*SL
	t_R	0.43	0.21 + 0.109*SL	0.19 + 0.115*SL	0.17 + 0.117*SL
	t_F	0.47	0.26 + 0.102*SL	0.24 + 0.109*SL	0.20 + 0.114*SL
B to Y	t_{PLH}	0.24	0.14 + 0.052*SL	0.14 + 0.051*SL	0.14 + 0.051*SL
	t_{PHL}	0.25	0.14 + 0.054*SL	0.14 + 0.053*SL	0.14 + 0.053*SL
	t_R	0.44	0.23 + 0.105*SL	0.20 + 0.113*SL	0.17 + 0.117*SL
	t_F	0.39	0.18 + 0.104*SL	0.16 + 0.110*SL	0.13 + 0.114*SL
C to Y	t_{PLH}	0.29	0.23 + 0.030*SL	0.24 + 0.027*SL	0.25 + 0.027*SL
	t_{PHL}	0.47	0.36 + 0.055*SL	0.36 + 0.054*SL	0.37 + 0.053*SL
	t_R	0.27	0.16 + 0.055*SL	0.15 + 0.058*SL	0.13 + 0.060*SL
	t_F	0.44	0.22 + 0.109*SL	0.21 + 0.112*SL	0.20 + 0.114*SL
D to Y	t_{PLH}	0.31	0.25 + 0.030*SL	0.26 + 0.027*SL	0.26 + 0.027*SL
	t_{PHL}	0.45	0.34 + 0.055*SL	0.34 + 0.053*SL	0.35 + 0.053*SL
	t_R	0.26	0.15 + 0.057*SL	0.15 + 0.058*SL	0.13 + 0.060*SL
	t_F	0.44	0.22 + 0.111*SL	0.21 + 0.112*SL	0.20 + 0.114*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OA22D2A

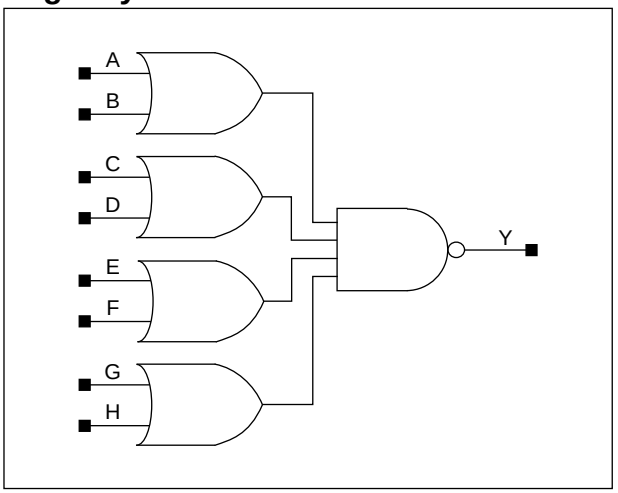
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.13 + 0.029*SL	0.14 + 0.025*SL	0.14 + 0.026*SL
	t_{PHL}	0.19	0.13 + 0.030*SL	0.14 + 0.026*SL	0.14 + 0.026*SL
	t_R	0.33	0.23 + 0.050*SL	0.22 + 0.054*SL	0.18 + 0.058*SL
	t_F	0.29	0.18 + 0.051*SL	0.18 + 0.053*SL	0.15 + 0.057*SL
B to Y	t_{PLH}	0.19	0.14 + 0.028*SL	0.14 + 0.026*SL	0.14 + 0.026*SL
	t_{PHL}	0.24	0.18 + 0.027*SL	0.18 + 0.026*SL	0.18 + 0.026*SL
	t_R	0.32	0.21 + 0.051*SL	0.20 + 0.056*SL	0.18 + 0.058*SL
	t_F	0.36	0.27 + 0.049*SL	0.25 + 0.053*SL	0.22 + 0.057*SL
C to Y	t_{PLH}	0.32	0.29 + 0.017*SL	0.29 + 0.015*SL	0.31 + 0.013*SL
	t_{PHL}	0.47	0.41 + 0.028*SL	0.41 + 0.027*SL	0.42 + 0.026*SL
	t_R	0.23	0.18 + 0.026*SL	0.17 + 0.027*SL	0.16 + 0.029*SL
	t_F	0.34	0.24 + 0.054*SL	0.23 + 0.055*SL	0.22 + 0.057*SL
D to Y	t_{PLH}	0.34	0.31 + 0.017*SL	0.32 + 0.015*SL	0.33 + 0.013*SL
	t_{PHL}	0.45	0.39 + 0.028*SL	0.40 + 0.027*SL	0.40 + 0.026*SL
	t_R	0.23	0.18 + 0.027*SL	0.17 + 0.027*SL	0.16 + 0.029*SL
	t_F	0.34	0.24 + 0.052*SL	0.23 + 0.055*SL	0.21 + 0.057*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

OA2222/OA2222D2

Four 2-ORs into 4-NAND with 1X/2X Drive

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Y
0	0	x	x	x	x	x	x	1
x	x	0	0	x	x	x	x	1
x	x	x	x	0	0	x	x	1
x	x	x	x	x	x	0	0	1
Other States								0

Cell Data

Input Load (SL)								Gate Count
OA2222								*OA2222*
A	B	C	D	E	F	G	H	
0.6	0.5	0.5	0.7	0.6	0.6	0.8	0.8	4.7
OA2222D2								*OA2222D2*
A	B	C	D	E	F	G	H	
0.6	0.5	0.5	0.7	0.6	0.6	0.8	0.8	5.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OA2222

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.55	0.49 + 0.029*SL	0.50 + 0.027*SL	0.50 + 0.027*SL
	t_{PHL}	0.60	0.52 + 0.042*SL	0.54 + 0.036*SL	0.56 + 0.033*SL
	t_R	0.21	0.11 + 0.054*SL	0.10 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.26	0.14 + 0.062*SL	0.13 + 0.063*SL	0.11 + 0.065*SL
B to Y	t_{PLH}	0.55	0.49 + 0.029*SL	0.50 + 0.027*SL	0.50 + 0.027*SL
	t_{PHL}	0.57	0.49 + 0.041*SL	0.50 + 0.036*SL	0.53 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.26	0.13 + 0.064*SL	0.13 + 0.063*SL	0.11 + 0.065*SL
C to Y	t_{PLH}	0.48	0.42 + 0.029*SL	0.43 + 0.027*SL	0.43 + 0.027*SL
	t_{PHL}	0.57	0.48 + 0.041*SL	0.50 + 0.036*SL	0.52 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.26	0.13 + 0.064*SL	0.13 + 0.063*SL	0.11 + 0.065*SL
D to Y	t_{PLH}	0.48	0.42 + 0.029*SL	0.43 + 0.027*SL	0.43 + 0.027*SL
	t_{PHL}	0.60	0.52 + 0.042*SL	0.54 + 0.036*SL	0.56 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.26	0.13 + 0.064*SL	0.13 + 0.063*SL	0.11 + 0.065*SL
E to Y	t_{PLH}	0.58	0.53 + 0.029*SL	0.53 + 0.027*SL	0.53 + 0.027*SL
	t_{PHL}	0.62	0.54 + 0.042*SL	0.55 + 0.036*SL	0.58 + 0.033*SL
	t_R	0.22	0.11 + 0.054*SL	0.10 + 0.057*SL	0.08 + 0.060*SL
	t_F	0.26	0.14 + 0.064*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
F to Y	t_{PLH}	0.58	0.53 + 0.029*SL	0.53 + 0.027*SL	0.53 + 0.027*SL
	t_{PHL}	0.59	0.51 + 0.042*SL	0.52 + 0.036*SL	0.55 + 0.033*SL
	t_R	0.22	0.11 + 0.053*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.26	0.13 + 0.064*SL	0.14 + 0.063*SL	0.11 + 0.065*SL
G to Y	t_{PLH}	0.51	0.45 + 0.029*SL	0.46 + 0.027*SL	0.46 + 0.027*SL
	t_{PHL}	0.59	0.50 + 0.041*SL	0.52 + 0.036*SL	0.55 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.26	0.13 + 0.065*SL	0.14 + 0.062*SL	0.11 + 0.065*SL
H to Y	t_{PLH}	0.51	0.45 + 0.029*SL	0.46 + 0.027*SL	0.46 + 0.027*SL
	t_{PHL}	0.62	0.53 + 0.042*SL	0.55 + 0.036*SL	0.58 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.26	0.13 + 0.065*SL	0.14 + 0.062*SL	0.11 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

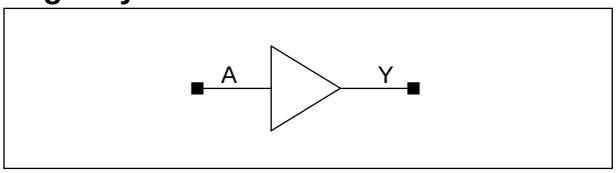
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

OA2222D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.57	0.53 + 0.017*SL	0.54 + 0.014*SL	0.55 + 0.013*SL
	t_{PHL}	0.65	0.60 + 0.026*SL	0.61 + 0.021*SL	0.65 + 0.017*SL
	t_R	0.16	0.11 + 0.025*SL	0.11 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.23	0.17 + 0.031*SL	0.17 + 0.031*SL	0.16 + 0.032*SL
B to Y	t_{PLH}	0.57	0.53 + 0.017*SL	0.54 + 0.014*SL	0.55 + 0.013*SL
	t_{PHL}	0.62	0.57 + 0.026*SL	0.58 + 0.021*SL	0.62 + 0.017*SL
	t_R	0.16	0.11 + 0.024*SL	0.11 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.23	0.17 + 0.031*SL	0.17 + 0.031*SL	0.16 + 0.032*SL
C to Y	t_{PLH}	0.49	0.46 + 0.017*SL	0.47 + 0.014*SL	0.47 + 0.013*SL
	t_{PHL}	0.61	0.56 + 0.026*SL	0.57 + 0.021*SL	0.61 + 0.017*SL
	t_R	0.16	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.23	0.17 + 0.030*SL	0.17 + 0.031*SL	0.16 + 0.032*SL
D to Y	t_{PLH}	0.49	0.46 + 0.017*SL	0.47 + 0.014*SL	0.48 + 0.013*SL
	t_{PHL}	0.65	0.60 + 0.026*SL	0.61 + 0.021*SL	0.65 + 0.017*SL
	t_R	0.16	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.23	0.17 + 0.030*SL	0.17 + 0.031*SL	0.16 + 0.032*SL
E to Y	t_{PLH}	0.60	0.57 + 0.017*SL	0.57 + 0.014*SL	0.58 + 0.013*SL
	t_{PHL}	0.67	0.62 + 0.026*SL	0.63 + 0.021*SL	0.67 + 0.017*SL
	t_R	0.17	0.12 + 0.024*SL	0.12 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.23	0.17 + 0.030*SL	0.17 + 0.031*SL	0.16 + 0.032*SL
F to Y	t_{PLH}	0.60	0.57 + 0.017*SL	0.57 + 0.014*SL	0.58 + 0.013*SL
	t_{PHL}	0.64	0.59 + 0.026*SL	0.60 + 0.021*SL	0.64 + 0.017*SL
	t_R	0.17	0.12 + 0.022*SL	0.11 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.23	0.17 + 0.032*SL	0.17 + 0.031*SL	0.16 + 0.032*SL
G to Y	t_{PLH}	0.52	0.49 + 0.017*SL	0.50 + 0.014*SL	0.51 + 0.013*SL
	t_{PHL}	0.63	0.58 + 0.026*SL	0.60 + 0.021*SL	0.63 + 0.017*SL
	t_R	0.16	0.12 + 0.024*SL	0.11 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.23	0.17 + 0.030*SL	0.17 + 0.031*SL	0.16 + 0.032*SL
H to Y	t_{PLH}	0.52	0.49 + 0.017*SL	0.50 + 0.014*SL	0.51 + 0.013*SL
	t_{PHL}	0.67	0.61 + 0.026*SL	0.63 + 0.021*SL	0.67 + 0.017*SL
	t_R	0.16	0.11 + 0.025*SL	0.11 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.23	0.17 + 0.031*SL	0.17 + 0.031*SL	0.16 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)											
DL1D2	*DL1D4*	*DL2D2*	*DL2D4*	*DL3D2*	*DL3D4*	*DL4D2*	*DL4D4*	*DL5D2*	*DL5D4*	*DL10D2*	*DL10D4*
A	A	A	A	A	A	A	A	A	A	A	A
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
Gate Count											
DL1D2	*DL1D4*	*DL2D2*	*DL2D4*	*DL3D2*	*DL3D4*	*DL4D2*	*DL4D4*	*DL5D2*	*DL5D4*	*DL10D2*	*DL10D4*
3.7	4.3	4.3	5.0	4.7	5.3	5.3	6.0	5.7	6.3	7.3	8.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

DL1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.06	1.02 + 0.016*SL	1.03 + 0.014*SL	1.04 + 0.013*SL
	t_{PHL}	1.07	1.03 + 0.022*SL	1.04 + 0.018*SL	1.06 + 0.017*SL
	t_R	0.14	0.09 + 0.026*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.09 + 0.032*SL

DL1D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	1.11	1.09 + 0.010*SL	1.10 + 0.008*SL	1.11 + 0.007*SL
	t_{PHL}	1.16	1.14 + 0.013*SL	1.14 + 0.011*SL	1.16 + 0.009*SL
	t_R	0.15	0.13 + 0.012*SL	0.12 + 0.013*SL	0.11 + 0.014*SL
	t_F	0.19	0.16 + 0.015*SL	0.16 + 0.015*SL	0.15 + 0.016*SL

DL2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	2.04	2.01 + 0.016*SL	2.02 + 0.014*SL	2.02 + 0.013*SL
	t_{PHL}	2.11	2.07 + 0.022*SL	2.08 + 0.018*SL	2.10 + 0.017*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.18	0.12 + 0.030*SL	0.11 + 0.031*SL	0.10 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

DL2D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	2.11	2.09 + 0.010*SL	2.09 + 0.008*SL	2.11 + 0.007*SL
	t_{PHL}	2.21	2.18 + 0.014*SL	2.19 + 0.011*SL	2.21 + 0.009*SL
	t_R	0.17	0.15 + 0.010*SL	0.14 + 0.012*SL	0.13 + 0.014*SL
	t_F	0.20	0.17 + 0.015*SL	0.18 + 0.014*SL	0.17 + 0.015*SL

DL3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	3.07	3.04 + 0.017*SL	3.05 + 0.014*SL	3.06 + 0.013*SL
	t_{PHL}	3.09	3.04 + 0.022*SL	3.05 + 0.018*SL	3.07 + 0.016*SL
	t_R	0.17	0.12 + 0.024*SL	0.12 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.19	0.13 + 0.029*SL	0.13 + 0.030*SL	0.11 + 0.032*SL

DL3D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	3.15	3.13 + 0.011*SL	3.13 + 0.008*SL	3.15 + 0.007*SL
	t_{PHL}	3.19	3.16 + 0.014*SL	3.17 + 0.011*SL	3.19 + 0.009*SL
	t_R	0.19	0.17 + 0.008*SL	0.16 + 0.012*SL	0.14 + 0.013*SL
	t_F	0.22	0.19 + 0.015*SL	0.19 + 0.014*SL	0.18 + 0.015*SL

DL4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	3.98	3.95 + 0.017*SL	3.96 + 0.014*SL	3.97 + 0.013*SL
	t_{PHL}	4.18	4.13 + 0.023*SL	4.14 + 0.019*SL	4.17 + 0.016*SL
	t_R	0.19	0.15 + 0.020*SL	0.13 + 0.025*SL	0.10 + 0.028*SL
	t_F	0.21	0.15 + 0.027*SL	0.15 + 0.030*SL	0.13 + 0.032*SL

DL4D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	4.06	4.04 + 0.012*SL	4.05 + 0.009*SL	4.07 + 0.007*SL
	t_{PHL}	4.29	4.26 + 0.014*SL	4.27 + 0.011*SL	4.29 + 0.009*SL
	t_R	0.20	0.18 + 0.009*SL	0.18 + 0.011*SL	0.16 + 0.013*SL
	t_F	0.23	0.21 + 0.013*SL	0.20 + 0.014*SL	0.20 + 0.015*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

DL5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	4.98	4.94 + 0.019*SL	4.96 + 0.014*SL	4.97 + 0.013*SL
	t_{PHL}	5.67	5.63 + 0.024*SL	5.64 + 0.019*SL	5.66 + 0.016*SL
	t_R	0.20	0.16 + 0.022*SL	0.15 + 0.024*SL	0.11 + 0.028*SL
	t_F	0.23	0.18 + 0.028*SL	0.17 + 0.029*SL	0.15 + 0.031*SL

DL5D4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	5.07	5.05 + 0.012*SL	5.06 + 0.009*SL	5.07 + 0.007*SL
	t_{PHL}	5.80	5.77 + 0.014*SL	5.78 + 0.011*SL	5.80 + 0.009*SL
	t_R	0.22	0.20 + 0.009*SL	0.19 + 0.011*SL	0.18 + 0.013*SL
	t_F	0.26	0.23 + 0.014*SL	0.23 + 0.014*SL	0.22 + 0.015*SL

DL10D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	9.90	9.86 + 0.022*SL	9.88 + 0.016*SL	9.90 + 0.013*SL
	t_{PHL}	12.95	12.90 + 0.028*SL	12.91 + 0.021*SL	12.95 + 0.017*SL
	t_R	0.26	0.22 + 0.022*SL	0.21 + 0.024*SL	0.17 + 0.028*SL
	t_F	0.34	0.28 + 0.029*SL	0.29 + 0.028*SL	0.26 + 0.031*SL

DL10D4

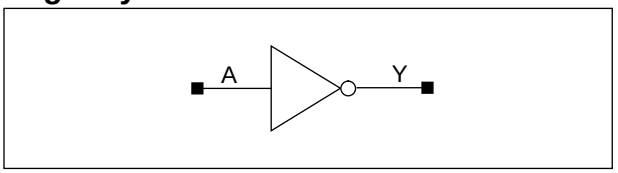
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	10.02	9.99 + 0.014*SL	10.00 + 0.010*SL	10.03 + 0.007*SL
	t_{PHL}	13.13	13.10 + 0.016*SL	13.11 + 0.013*SL	13.14 + 0.009*SL
	t_R	0.29	0.27 + 0.009*SL	0.27 + 0.010*SL	0.25 + 0.012*SL
	t_F	0.39	0.37 + 0.013*SL	0.37 + 0.013*SL	0.36 + 0.014*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

IV/IVD2/IVD3/IVD4/IVD6/IVD8

Inverter with 1X/2X/3X/4X/6X/8X Drive

Logic Symbol



Truth Table

A	Y
0	1
1	0

Cell Data

Input Load (SL)						Gate Count					
IV	*IVD2*	*IVD3*	*IVD4*	*IVD6*	*IVD8*	*IV*	*IVD2*	*IVD3*	*IVD4*	*IVD6*	*IVD8*
A	A	A	A	A	A						
1.0	2.1	3.0	4.0	6.0	8.0	0.7	1.0	1.3	1.7	2.3	3.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

IV

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.16	0.09 + 0.034*SL	0.11 + 0.027*SL	0.11 + 0.027*SL
	t_{PHL}	0.17	0.09 + 0.039*SL	0.11 + 0.033*SL	0.10 + 0.033*SL
	t_R	0.25	0.15 + 0.048*SL	0.13 + 0.054*SL	0.08 + 0.060*SL
	t_F	0.25	0.14 + 0.054*SL	0.12 + 0.061*SL	0.07 + 0.065*SL

IVD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.11	0.07 + 0.021*SL	0.08 + 0.015*SL	0.10 + 0.013*SL
	t_{PHL}	0.11	0.06 + 0.024*SL	0.08 + 0.018*SL	0.10 + 0.016*SL
	t_R	0.18	0.13 + 0.025*SL	0.14 + 0.024*SL	0.10 + 0.028*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.028*SL	0.08 + 0.032*SL

IVD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.10	0.07 + 0.015*SL	0.08 + 0.011*SL	0.10 + 0.009*SL
	t_{PHL}	0.10	0.07 + 0.016*SL	0.08 + 0.013*SL	0.10 + 0.011*SL
	t_R	0.17	0.14 + 0.018*SL	0.14 + 0.016*SL	0.12 + 0.018*SL
	t_F	0.16	0.12 + 0.021*SL	0.13 + 0.018*SL	0.10 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

IVD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.09	0.06 + 0.012*SL	0.07 + 0.009*SL	0.10 + 0.006*SL
	t_{PHL}	0.09	0.06 + 0.014*SL	0.07 + 0.011*SL	0.09 + 0.008*SL
	t_R	0.16	0.13 + 0.014*SL	0.14 + 0.012*SL	0.12 + 0.013*SL
	t_F	0.15	0.12 + 0.015*SL	0.12 + 0.014*SL	0.11 + 0.015*SL

IVD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.08	0.06 + 0.009*SL	0.07 + 0.007*SL	0.09 + 0.004*SL
	t_{PHL}	0.08	0.06 + 0.010*SL	0.07 + 0.008*SL	0.08 + 0.006*SL
	t_R	0.15	0.13 + 0.009*SL	0.13 + 0.008*SL	0.13 + 0.008*SL
	t_F	0.14	0.11 + 0.011*SL	0.12 + 0.010*SL	0.12 + 0.010*SL

IVD8

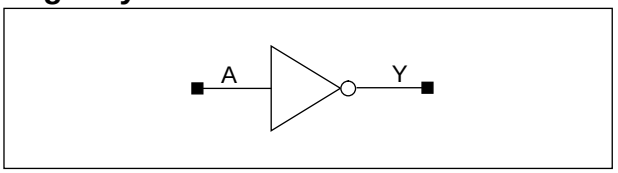
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.07	0.06 + 0.007*SL	0.06 + 0.005*SL	0.08 + 0.004*SL
	t_{PHL}	0.07	0.06 + 0.007*SL	0.06 + 0.006*SL	0.08 + 0.004*SL
	t_R	0.15	0.13 + 0.006*SL	0.13 + 0.007*SL	0.14 + 0.006*SL
	t_F	0.13	0.11 + 0.009*SL	0.12 + 0.007*SL	0.12 + 0.007*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

IVA/IVD2A/IVD3A/IVD4A

Inverter with (2X/4X/6X/8X) P-Transistor, (1X/2X/3X/4X) N-Transistor

Logic Symbol



Truth Table

A	Y
0	1
1	0

Cell Data

Input Load (SL)				Gate Count			
IVA	*IVD2A*	*IVD3A*	*IVD4A*	*IVA*	*IVD2A*	*IVD3A*	*IVD4A*
A	A	A	A				
1.0	2.0	3.0	4.0	0.7	1.0	1.3	1.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

IVA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.16	0.09 + 0.034*SL	0.11 + 0.027*SL	0.11 + 0.027*SL
	t_{PHL}	0.17	0.09 + 0.039*SL	0.11 + 0.033*SL	0.10 + 0.033*SL
	t_R	0.25	0.15 + 0.048*SL	0.13 + 0.054*SL	0.08 + 0.060*SL
	t_F	0.25	0.14 + 0.054*SL	0.12 + 0.061*SL	0.07 + 0.065*SL

IVD2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.11	0.07 + 0.021*SL	0.08 + 0.015*SL	0.10 + 0.013*SL
	t_{PHL}	0.11	0.06 + 0.024*SL	0.08 + 0.018*SL	0.10 + 0.016*SL
	t_R	0.18	0.13 + 0.025*SL	0.14 + 0.024*SL	0.10 + 0.028*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.028*SL	0.08 + 0.032*SL

IVD3A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.10	0.07 + 0.015*SL	0.08 + 0.011*SL	0.10 + 0.009*SL
	t_{PHL}	0.10	0.07 + 0.016*SL	0.08 + 0.013*SL	0.10 + 0.011*SL
	t_R	0.17	0.14 + 0.018*SL	0.14 + 0.016*SL	0.12 + 0.018*SL
	t_F	0.16	0.12 + 0.021*SL	0.13 + 0.018*SL	0.10 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

IVD4A

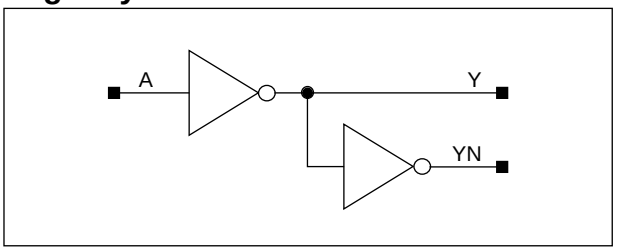
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.09	0.06 + 0.012*SL	0.07 + 0.009*SL	0.10 + 0.006*SL
	t_{PHL}	0.09	0.06 + 0.014*SL	0.07 + 0.011*SL	0.09 + 0.008*SL
	t_R	0.16	0.13 + 0.014*SL	0.14 + 0.012*SL	0.12 + 0.013*SL
	t_F	0.15	0.12 + 0.015*SL	0.12 + 0.014*SL	0.11 + 0.015*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

IVCD(11/13)/IVCD(22/26)/IVCD44

1X IV into (1X/3X) IV/2X IV into (2X/6X) IV/4X IV into 4X IV

Logic Symbol



Truth Table

A	Y	YN
1	0	1
0	1	0

Cell Data

Input Load (SL)					Gate Count				
IVCD11	*IVCD13*	*IVCD22*	*IVCD26*	*IVCD44*	*IVCD11*	*IVCD13*	*IVCD22*	*IVCD26*	*IVCD44*
A	A	A	A	A					
1.0	1.0	2.0	2.0	4.0	1.0	1.7	1.7	3.0	3.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

IVCD11

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.12 + 0.030*SL	0.14 + 0.026*SL	0.13 + 0.027*SL
	t_{PHL}	0.20	0.12 + 0.036*SL	0.13 + 0.033*SL	0.13 + 0.033*SL
	t_R	0.30	0.21 + 0.046*SL	0.18 + 0.055*SL	0.14 + 0.060*SL
	t_F	0.30	0.20 + 0.053*SL	0.17 + 0.061*SL	0.13 + 0.065*SL
Y to YN	t_{PLH}	0.16	0.09 + 0.034*SL	0.11 + 0.027*SL	0.11 + 0.027*SL
	t_{PHL}	0.17	0.09 + 0.039*SL	0.11 + 0.033*SL	0.10 + 0.033*SL
	t_R	0.25	0.15 + 0.048*SL	0.13 + 0.055*SL	0.08 + 0.060*SL
	t_F	0.25	0.14 + 0.054*SL	0.12 + 0.061*SL	0.07 + 0.065*SL

IVCD13

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.24	0.18 + 0.027*SL	0.19 + 0.026*SL	0.18 + 0.027*SL
	t_{PHL}	0.25	0.19 + 0.032*SL	0.18 + 0.033*SL	0.18 + 0.033*SL
	t_R	0.42	0.31 + 0.055*SL	0.31 + 0.057*SL	0.28 + 0.060*SL
	t_F	0.45	0.32 + 0.061*SL	0.32 + 0.063*SL	0.29 + 0.066*SL
Y to YN	t_{PLH}	0.10	0.07 + 0.015*SL	0.08 + 0.011*SL	0.10 + 0.009*SL
	t_{PHL}	0.10	0.07 + 0.017*SL	0.08 + 0.013*SL	0.10 + 0.011*SL
	t_R	0.17	0.14 + 0.018*SL	0.14 + 0.016*SL	0.12 + 0.018*SL
	t_F	0.16	0.12 + 0.021*SL	0.13 + 0.018*SL	0.10 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

IVCD22

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.14	0.11 + 0.017*SL	0.12 + 0.014*SL	0.13 + 0.013*SL
	t_{PHL}	0.15	0.11 + 0.020*SL	0.12 + 0.017*SL	0.12 + 0.016*SL
	t_R	0.24	0.20 + 0.018*SL	0.18 + 0.024*SL	0.15 + 0.028*SL
	t_F	0.24	0.19 + 0.024*SL	0.18 + 0.028*SL	0.14 + 0.032*SL
Y to YN	t_{PLH}	0.11	0.07 + 0.020*SL	0.08 + 0.015*SL	0.10 + 0.013*SL
	t_{PHL}	0.11	0.06 + 0.024*SL	0.08 + 0.018*SL	0.10 + 0.016*SL
	t_R	0.18	0.13 + 0.025*SL	0.14 + 0.024*SL	0.10 + 0.028*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.028*SL	0.08 + 0.032*SL

IVCD26

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.20	0.17 + 0.014*SL	0.17 + 0.013*SL	0.17 + 0.013*SL
	t_{PHL}	0.21	0.17 + 0.017*SL	0.18 + 0.016*SL	0.17 + 0.016*SL
	t_R	0.35	0.29 + 0.028*SL	0.29 + 0.027*SL	0.28 + 0.029*SL
	t_F	0.38	0.33 + 0.023*SL	0.31 + 0.031*SL	0.29 + 0.032*SL
Y to YN	t_{PLH}	0.08	0.06 + 0.009*SL	0.07 + 0.007*SL	0.09 + 0.004*SL
	t_{PHL}	0.08	0.06 + 0.010*SL	0.07 + 0.008*SL	0.08 + 0.006*SL
	t_R	0.15	0.13 + 0.009*SL	0.13 + 0.008*SL	0.13 + 0.008*SL
	t_F	0.14	0.11 + 0.011*SL	0.12 + 0.010*SL	0.12 + 0.010*SL

IVCD44

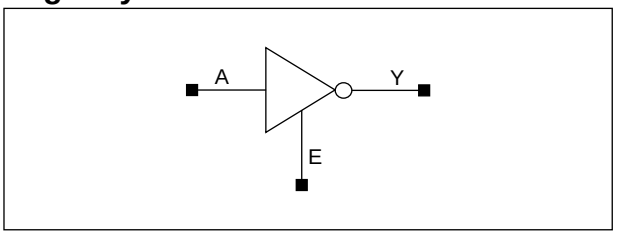
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.12	0.11 + 0.009*SL	0.11 + 0.008*SL	0.12 + 0.006*SL
	t_{PHL}	0.13	0.10 + 0.011*SL	0.11 + 0.009*SL	0.12 + 0.008*SL
	t_R	0.22	0.20 + 0.010*SL	0.20 + 0.010*SL	0.17 + 0.013*SL
	t_F	0.22	0.19 + 0.012*SL	0.19 + 0.012*SL	0.16 + 0.015*SL
Y to YN	t_{PLH}	0.09	0.06 + 0.012*SL	0.07 + 0.009*SL	0.10 + 0.006*SL
	t_{PHL}	0.09	0.06 + 0.014*SL	0.07 + 0.011*SL	0.09 + 0.008*SL
	t_R	0.16	0.13 + 0.014*SL	0.14 + 0.012*SL	0.12 + 0.013*SL
	t_F	0.15	0.12 + 0.015*SL	0.11 + 0.017*SL	0.13 + 0.015*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

IVT/IVTD2/IVTD4/IVTD8

Inverting Tri-State Buffer with Enable High, 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

A	E	Y
x	0	Hi-Z
0	1	1
1	1	0

Cell Data

Input Load (SL)								Output Load (SL)				Gate Count			
IVT		*IVTD2*		*IVTD4*		*IVTD8*		*IVT*	IVTD2	*IVTD4*	IVTD8	*IVT*	*IVTD2*	*IVTD4*	*IVTD8*
A	E	A	E	A	E	A	E	Y	Y	Y	Y				
0.7	1.1	0.7	1.4	0.7	2.3	0.7	3.8	1.0	1.8	3.3	10.1	2.3	3.0	4.3	7.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

IVT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.41	0.37 + 0.020*SL	0.39 + 0.016*SL	0.41 + 0.014*SL
	t_{PHL}	0.42	0.34 + 0.039*SL	0.34 + 0.038*SL	0.35 + 0.037*SL
	t_R	0.18	0.13 + 0.027*SL	0.12 + 0.028*SL	0.11 + 0.030*SL
	t_F	0.28	0.13 + 0.076*SL	0.12 + 0.079*SL	0.10 + 0.081*SL
E to Y	t_{PLH}	0.26	0.22 + 0.020*SL	0.23 + 0.016*SL	0.25 + 0.014*SL
	t_{PHL}	0.17	0.08 + 0.047*SL	0.10 + 0.038*SL	0.11 + 0.038*SL
	t_R	0.19	0.14 + 0.026*SL	0.13 + 0.028*SL	0.12 + 0.030*SL
	t_F	0.30	0.16 + 0.072*SL	0.14 + 0.076*SL	0.10 + 0.081*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.39	0.39 + -0.001*SL	0.39 + 0.000*SL	0.39 + 0.000*SL

IVTD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.48	0.46 + 0.013*SL	0.46 + 0.010*SL	0.49 + 0.007*SL
	t_{PHL}	0.47	0.44 + 0.020*SL	0.44 + 0.019*SL	0.44 + 0.019*SL
	t_R	0.21	0.18 + 0.015*SL	0.19 + 0.013*SL	0.18 + 0.014*SL
	t_F	0.23	0.16 + 0.035*SL	0.16 + 0.037*SL	0.13 + 0.040*SL
E to Y	t_{PLH}	0.33	0.31 + 0.013*SL	0.31 + 0.010*SL	0.34 + 0.007*SL
	t_{PHL}	0.12	0.06 + 0.029*SL	0.08 + 0.021*SL	0.10 + 0.019*SL
	t_R	0.22	0.19 + 0.014*SL	0.19 + 0.013*SL	0.18 + 0.014*SL
	t_F	0.22	0.15 + 0.038*SL	0.15 + 0.037*SL	0.12 + 0.040*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.56	0.56 + 0.001*SL	0.56 + 0.000*SL	0.57 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

IVTD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.61	0.60 + 0.009*SL	0.60 + 0.008*SL	0.63 + 0.005*SL
	t_{PHL}	0.68	0.65 + 0.013*SL	0.66 + 0.011*SL	0.67 + 0.010*SL
	t_R	0.29	0.28 + 0.005*SL	0.27 + 0.007*SL	0.27 + 0.007*SL
	t_F	0.30	0.27 + 0.013*SL	0.26 + 0.017*SL	0.24 + 0.019*SL
E to Y	t_{PLH}	0.47	0.45 + 0.010*SL	0.45 + 0.008*SL	0.48 + 0.005*SL
	t_{PHL}	0.07	0.04 + 0.014*SL	0.05 + 0.012*SL	0.07 + 0.010*SL
	t_R	0.29	0.27 + 0.007*SL	0.27 + 0.007*SL	0.27 + 0.007*SL
	t_F	0.18	0.14 + 0.020*SL	0.14 + 0.019*SL	0.14 + 0.020*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.81	0.81 + 0.001*SL	0.81 + 0.000*SL	0.81 + 0.000*SL

IVTD8

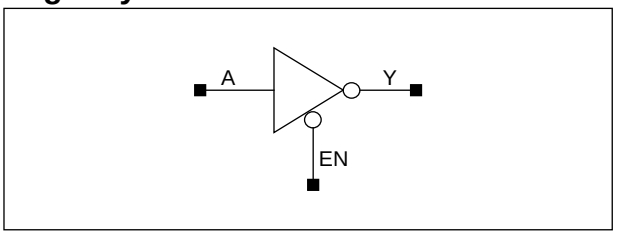
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.92	0.91 + 0.006*SL	0.91 + 0.005*SL	0.92 + 0.004*SL
	t_{PHL}	1.09	1.07 + 0.008*SL	1.07 + 0.007*SL	1.09 + 0.005*SL
	t_R	0.50	0.50 + 0.002*SL	0.50 + 0.003*SL	0.49 + 0.004*SL
	t_F	0.52	0.52 + 0.004*SL	0.51 + 0.005*SL	0.48 + 0.008*SL
E to Y	t_{PLH}	0.78	0.77 + 0.006*SL	0.77 + 0.005*SL	0.78 + 0.004*SL
	t_{PHL}	0.05	0.04 + 0.007*SL	0.04 + 0.007*SL	0.05 + 0.005*SL
	t_R	0.51	0.50 + 0.002*SL	0.50 + 0.003*SL	0.49 + 0.004*SL
	t_F	0.16	0.14 + 0.010*SL	0.14 + 0.010*SL	0.14 + 0.010*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	1.41	1.41 + 0.001*SL	1.41 + 0.000*SL	1.42 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

IVTN/IVTND2/IVTND4/IVTND8

Inverting Tri-State Buffer with Enable Low, 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

A	EN	Y
x	1	Hi-Z
0	0	1
1	0	0

Cell Data

Input Load (SL)							
IVTN		*IVTND2*		*IVTND4*		*IVTND8*	
A	EN	A	EN	A	EN	A	EN
0.7	0.7	0.7	0.7	0.8	0.7	0.8	0.7

Output Load (SL)				Gate Count			
IVTN	IVTND2	*IVTND4*	IVTND8	*IVTN*	*IVTND2*	*IVTND4*	*IVTND8*
Y	Y	Y	Y				
1.4	2.5	3.3	10.2	2.7	3.3	4.7	7.3

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

IVTN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.40	0.36 + 0.021*SL	0.37 + 0.016*SL	0.39 + 0.014*SL
	t_{PHL}	0.44	0.36 + 0.041*SL	0.37 + 0.038*SL	0.38 + 0.038*SL
	t_R	0.17	0.12 + 0.028*SL	0.11 + 0.029*SL	0.10 + 0.030*SL
	t_F	0.29	0.14 + 0.078*SL	0.13 + 0.079*SL	0.12 + 0.081*SL
EN to Y	t_{PLH}	0.43	0.39 + 0.021*SL	0.40 + 0.016*SL	0.42 + 0.014*SL
	t_{PHL}	0.32	0.24 + 0.043*SL	0.25 + 0.039*SL	0.26 + 0.038*SL
	t_R	0.17	0.12 + 0.027*SL	0.12 + 0.028*SL	0.10 + 0.030*SL
	t_F	0.27	0.12 + 0.079*SL	0.11 + 0.080*SL	0.11 + 0.081*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.40	0.40 + 0.000*SL	0.40 + 0.000*SL	0.40 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

IVTND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.46	0.43 + 0.015*SL	0.44 + 0.011*SL	0.47 + 0.007*SL
	t_{PHL}	0.50	0.46 + 0.022*SL	0.46 + 0.020*SL	0.48 + 0.019*SL
	t_R	0.19	0.16 + 0.014*SL	0.16 + 0.014*SL	0.16 + 0.014*SL
	t_F	0.24	0.17 + 0.036*SL	0.16 + 0.039*SL	0.15 + 0.040*SL
EN to Y	t_{PLH}	0.51	0.49 + 0.015*SL	0.50 + 0.011*SL	0.53 + 0.007*SL
	t_{PHL}	0.29	0.24 + 0.024*SL	0.25 + 0.021*SL	0.27 + 0.019*SL
	t_R	0.19	0.16 + 0.014*SL	0.17 + 0.014*SL	0.16 + 0.014*SL
	t_F	0.19	0.11 + 0.040*SL	0.12 + 0.040*SL	0.11 + 0.040*SL
	t_{PLZ}	0.21	0.21 + 0.000*SL	0.21 + 0.000*SL	0.21 + 0.000*SL
	t_{PHZ}	0.57	0.57 + 0.001*SL	0.57 + 0.000*SL	0.57 + 0.000*SL

IVTND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.60	0.58 + 0.009*SL	0.59 + 0.008*SL	0.62 + 0.005*SL
	t_{PHL}	0.69	0.66 + 0.013*SL	0.67 + 0.011*SL	0.68 + 0.010*SL
	t_R	0.29	0.27 + 0.008*SL	0.27 + 0.007*SL	0.27 + 0.007*SL
	t_F	0.31	0.28 + 0.013*SL	0.27 + 0.016*SL	0.24 + 0.019*SL
EN to Y	t_{PLH}	0.71	0.69 + 0.009*SL	0.70 + 0.008*SL	0.72 + 0.005*SL
	t_{PHL}	0.30	0.27 + 0.013*SL	0.27 + 0.012*SL	0.29 + 0.010*SL
	t_R	0.29	0.28 + 0.007*SL	0.28 + 0.007*SL	0.28 + 0.007*SL
	t_F	0.17	0.12 + 0.021*SL	0.12 + 0.021*SL	0.13 + 0.020*SL
	t_{PLZ}	0.26	0.26 + 0.000*SL	0.26 + 0.000*SL	0.26 + 0.000*SL
	t_{PHZ}	0.91	0.91 + 0.000*SL	0.91 + 0.000*SL	0.91 + 0.000*SL

IVTND8

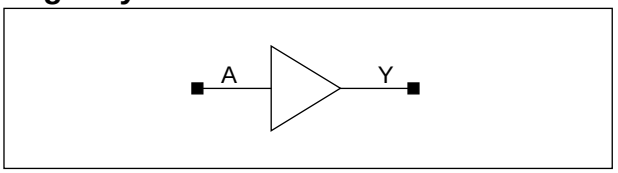
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.91	0.90 + 0.006*SL	0.90 + 0.005*SL	0.92 + 0.004*SL
	t_{PHL}	1.10	1.09 + 0.008*SL	1.09 + 0.007*SL	1.10 + 0.005*SL
	t_R	0.51	0.50 + 0.002*SL	0.50 + 0.003*SL	0.50 + 0.004*SL
	t_F	0.54	0.53 + 0.004*SL	0.53 + 0.005*SL	0.50 + 0.008*SL
EN to Y	t_{PLH}	1.13	1.12 + 0.006*SL	1.12 + 0.005*SL	1.14 + 0.004*SL
	t_{PHL}	0.34	0.33 + 0.008*SL	0.33 + 0.007*SL	0.34 + 0.006*SL
	t_R	0.51	0.51 + 0.002*SL	0.51 + 0.003*SL	0.50 + 0.004*SL
	t_F	0.18	0.15 + 0.012*SL	0.16 + 0.010*SL	0.16 + 0.010*SL
	t_{PLZ}	0.38	0.38 + 0.000*SL	0.38 + 0.000*SL	0.38 + 0.000*SL
	t_{PHZ}	1.61	1.61 + 0.000*SL	1.61 + 0.000*SL	1.61 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

NID/NID2/NID3/NID4/NID6/NID8

Non-Inverting Buffer with 1X/2X/3X/4X/6X/8X Drive

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)						Gate Count					
NID	*NID2*	*NID3*	*NID4*	*NID6*	*NID8*	*NID*	*NID2*	*NID3*	*NID4*	*NID6*	*NID8*
A	A	A	A	A	A						
0.8	0.8	0.8	1.5	1.5	1.5	1.0	1.3	1.7	2.3	3.0	3.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NID

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.21	0.15 + 0.029*SL	0.16 + 0.027*SL	0.16 + 0.027*SL
	t_{PHL}	0.31	0.24 + 0.037*SL	0.25 + 0.033*SL	0.25 + 0.033*SL
	t_R	0.21	0.10 + 0.052*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.063*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

NID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.19 + 0.016*SL	0.19 + 0.014*SL	0.20 + 0.013*SL
	t_{PHL}	0.32	0.28 + 0.022*SL	0.29 + 0.018*SL	0.30 + 0.017*SL
	t_R	0.15	0.10 + 0.025*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.08 + 0.032*SL

NID3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.23 + 0.010*SL	0.23 + 0.010*SL	0.24 + 0.009*SL
	t_{PHL}	0.36	0.33 + 0.016*SL	0.34 + 0.013*SL	0.36 + 0.011*SL
	t_R	0.16	0.11 + 0.021*SL	0.13 + 0.015*SL	0.10 + 0.019*SL
	t_F	0.17	0.13 + 0.021*SL	0.13 + 0.020*SL	0.12 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NID4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.19	0.17 + 0.008*SL	0.17 + 0.008*SL	0.18 + 0.006*SL
	t_{PHL}	0.28	0.25 + 0.012*SL	0.26 + 0.010*SL	0.27 + 0.008*SL
	t_R	0.12	0.09 + 0.012*SL	0.09 + 0.013*SL	0.08 + 0.014*SL
	t_F	0.12	0.09 + 0.016*SL	0.09 + 0.016*SL	0.09 + 0.016*SL

NID6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.22	0.21 + 0.007*SL	0.21 + 0.005*SL	0.22 + 0.004*SL
	t_{PHL}	0.32	0.30 + 0.008*SL	0.31 + 0.007*SL	0.32 + 0.006*SL
	t_R	0.12	0.11 + 0.008*SL	0.11 + 0.008*SL	0.10 + 0.009*SL
	t_F	0.13	0.11 + 0.010*SL	0.11 + 0.010*SL	0.11 + 0.010*SL

NID8

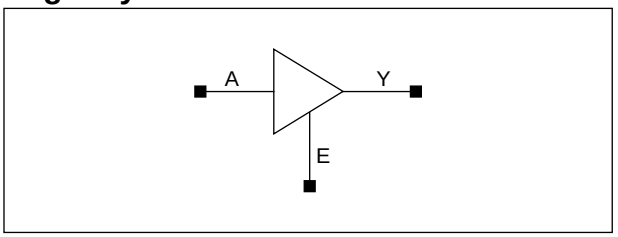
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.25	0.24 + 0.005*SL	0.24 + 0.005*SL	0.26 + 0.003*SL
	t_{PHL}	0.36	0.35 + 0.007*SL	0.35 + 0.006*SL	0.37 + 0.005*SL
	t_R	0.15	0.13 + 0.006*SL	0.14 + 0.004*SL	0.12 + 0.007*SL
	t_F	0.16	0.14 + 0.007*SL	0.14 + 0.007*SL	0.14 + 0.008*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

NIT/NITD2/NITD4/NITD8

Non-Inverting Tri-State Buffer with Enable High, 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

A	E	Y
x	0	Hi-Z
0	1	0
1	1	1

Cell Data

Input Load (SL)								Output Load (SL)				Gate Count			
NIT		*NITD2*		*NITD4*		*NITD8*		*NIT*	*NITD2*	*NITD4*	*NITD8*	*NIT*	*NITD2*	*NITD4*	*NITD8*
A	E	A	E	A	E	A	E	Y	Y	Y	Y				
0.7	0.8	0.7	1.2	0.5	2.1	0.5	3.7	1.4	3.7	4.3	8.6	1.7	2.3	3.7	6.3

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NIT

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.29	0.25 + 0.019*SL	0.26 + 0.016*SL	0.28 + 0.014*SL
	t_{PHL}	0.38	0.30 + 0.039*SL	0.31 + 0.038*SL	0.31 + 0.037*SL
	t_R	0.19	0.14 + 0.025*SL	0.13 + 0.028*SL	0.11 + 0.030*SL
	t_F	0.28	0.13 + 0.076*SL	0.12 + 0.079*SL	0.10 + 0.081*SL
E to Y	t_{PLH}	0.26	0.22 + 0.020*SL	0.23 + 0.016*SL	0.25 + 0.014*SL
	t_{PHL}	0.17	0.08 + 0.047*SL	0.11 + 0.038*SL	0.11 + 0.038*SL
	t_R	0.19	0.14 + 0.025*SL	0.13 + 0.028*SL	0.12 + 0.030*SL
	t_F	0.30	0.16 + 0.071*SL	0.14 + 0.077*SL	0.10 + 0.081*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.39	0.39 + 0.000*SL	0.39 + 0.000*SL	0.39 + 0.000*SL

NITD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.35	0.33 + 0.013*SL	0.34 + 0.010*SL	0.36 + 0.007*SL
	t_{PHL}	0.44	0.40 + 0.020*SL	0.40 + 0.019*SL	0.41 + 0.019*SL
	t_R	0.21	0.18 + 0.014*SL	0.19 + 0.013*SL	0.18 + 0.014*SL
	t_F	0.23	0.17 + 0.033*SL	0.16 + 0.037*SL	0.13 + 0.040*SL
E to Y	t_{PLH}	0.33	0.31 + 0.013*SL	0.32 + 0.010*SL	0.34 + 0.007*SL
	t_{PHL}	0.12	0.06 + 0.029*SL	0.08 + 0.021*SL	0.10 + 0.019*SL
	t_R	0.22	0.19 + 0.012*SL	0.19 + 0.013*SL	0.18 + 0.014*SL
	t_F	0.22	0.15 + 0.037*SL	0.15 + 0.037*SL	0.12 + 0.040*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.57	0.57 + 0.000*SL	0.57 + 0.000*SL	0.57 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NITD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.47 + 0.009*SL	0.48 + 0.008*SL	0.50 + 0.005*SL
	t_{PHL}	0.63	0.60 + 0.012*SL	0.61 + 0.011*SL	0.62 + 0.010*SL
	t_R	0.30	0.29 + 0.006*SL	0.28 + 0.007*SL	0.29 + 0.007*SL
	t_F	0.30	0.28 + 0.013*SL	0.27 + 0.015*SL	0.23 + 0.019*SL
E to Y	t_{PLH}	0.48	0.46 + 0.009*SL	0.46 + 0.007*SL	0.49 + 0.005*SL
	t_{PHL}	0.08	0.05 + 0.015*SL	0.05 + 0.012*SL	0.08 + 0.010*SL
	t_R	0.30	0.28 + 0.007*SL	0.29 + 0.007*SL	0.29 + 0.007*SL
	t_F	0.18	0.14 + 0.020*SL	0.15 + 0.019*SL	0.14 + 0.020*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.86	0.86 + 0.001*SL	0.86 + 0.000*SL	0.86 + 0.000*SL

NITD8

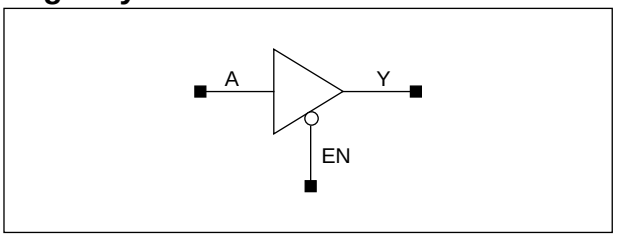
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.80	0.79 + 0.005*SL	0.79 + 0.005*SL	0.80 + 0.004*SL
	t_{PHL}	1.02	1.01 + 0.007*SL	1.01 + 0.007*SL	1.02 + 0.005*SL
	t_R	0.52	0.52 + 0.002*SL	0.52 + 0.003*SL	0.51 + 0.003*SL
	t_F	0.53	0.52 + 0.004*SL	0.52 + 0.004*SL	0.49 + 0.007*SL
E to Y	t_{PLH}	0.79	0.78 + 0.006*SL	0.79 + 0.005*SL	0.80 + 0.004*SL
	t_{PHL}	0.06	0.04 + 0.008*SL	0.05 + 0.007*SL	0.06 + 0.005*SL
	t_R	0.52	0.52 + 0.002*SL	0.52 + 0.003*SL	0.51 + 0.003*SL
	t_F	0.17	0.14 + 0.011*SL	0.15 + 0.010*SL	0.15 + 0.010*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	1.51	1.51 + 0.001*SL	1.51 + 0.000*SL	1.51 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

NITN/NITND2/NITND4/NITND8

Non-Inverting Tri-State Buffer with Enable Low, 1X/2X/4X/8X Drive

Logic Symbol



Truth Table

A	EN	Y
x	1	Hi-Z
0	0	0
1	0	1

Cell Data

Input Load (SL)							
NITN		*NITND2*		*NITND4*		*NITND8*	
A	EN	A	EN	A	EN	A	EN
0.4	0.7	0.4	0.7	0.8	0.8	0.8	0.8

Output Load (SL)				Gate Count			
NITN	*NITND2*	*NITND4*	*NITND8*	*NITN*	*NITND2*	*NITND4*	*NITND8*
Y	Y	Y	Y				
1.3	2.1	6.1	8.0	2.3	2.7	4.0	6.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NITN

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.28	0.24 + 0.021*SL	0.25 + 0.016*SL	0.27 + 0.014*SL
	t_{PHL}	0.40	0.31 + 0.041*SL	0.32 + 0.038*SL	0.33 + 0.038*SL
	t_R	0.18	0.12 + 0.027*SL	0.12 + 0.028*SL	0.10 + 0.030*SL
	t_F	0.29	0.13 + 0.079*SL	0.13 + 0.079*SL	0.11 + 0.081*SL
EN to Y	t_{PLH}	0.42	0.38 + 0.021*SL	0.39 + 0.016*SL	0.42 + 0.014*SL
	t_{PHL}	0.32	0.24 + 0.043*SL	0.25 + 0.039*SL	0.26 + 0.038*SL
	t_R	0.17	0.11 + 0.029*SL	0.12 + 0.028*SL	0.10 + 0.030*SL
	t_F	0.27	0.12 + 0.078*SL	0.11 + 0.080*SL	0.10 + 0.081*SL
	t_{PLZ}	-129.81	-129.81 + 0.000*SL	-129.81 + 0.000*SL	-129.81 + 0.000*SL
	t_{PHZ}	0.43	0.43 + 0.000*SL	0.43 + 0.000*SL	0.43 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

NITND2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.34	0.32 + 0.014*SL	0.33 + 0.011*SL	0.36 + 0.007*SL
	t_{PHL}	0.44	0.40 + 0.022*SL	0.41 + 0.020*SL	0.41 + 0.019*SL
	t_R	0.20	0.17 + 0.013*SL	0.17 + 0.014*SL	0.17 + 0.014*SL
	t_F	0.23	0.16 + 0.036*SL	0.15 + 0.038*SL	0.14 + 0.040*SL
EN to Y	t_{PLH}	0.51	0.48 + 0.014*SL	0.49 + 0.010*SL	0.52 + 0.007*SL
	t_{PHL}	0.30	0.25 + 0.024*SL	0.26 + 0.021*SL	0.28 + 0.019*SL
	t_R	0.20	0.18 + 0.014*SL	0.18 + 0.013*SL	0.17 + 0.014*SL
	t_F	0.20	0.12 + 0.040*SL	0.12 + 0.039*SL	0.11 + 0.040*SL
	t_{PLZ}	0.27	0.27 + 0.000*SL	0.27 + 0.000*SL	0.27 + 0.000*SL
	t_{PHZ}	0.61	0.61 + 0.001*SL	0.61 + 0.000*SL	0.61 + 0.000*SL

NITND4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.49	0.47 + 0.009*SL	0.48 + 0.008*SL	0.50 + 0.005*SL
	t_{PHL}	0.63	0.60 + 0.013*SL	0.61 + 0.011*SL	0.62 + 0.009*SL
	t_R	0.30	0.28 + 0.006*SL	0.28 + 0.007*SL	0.29 + 0.007*SL
	t_F	0.30	0.28 + 0.012*SL	0.27 + 0.016*SL	0.24 + 0.019*SL
EN to Y	t_{PLH}	0.70	0.68 + 0.009*SL	0.68 + 0.008*SL	0.71 + 0.005*SL
	t_{PHL}	0.30	0.27 + 0.014*SL	0.28 + 0.012*SL	0.30 + 0.010*SL
	t_R	0.30	0.29 + 0.007*SL	0.29 + 0.007*SL	0.29 + 0.007*SL
	t_F	0.17	0.13 + 0.021*SL	0.13 + 0.021*SL	0.13 + 0.020*SL
	t_{PLZ}	0.11	0.11 + 0.000*SL	0.11 + 0.000*SL	0.11 + 0.000*SL
	t_{PHZ}	0.96	0.96 + 0.000*SL	0.96 + 0.000*SL	0.97 + 0.000*SL

NITND8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.80	0.79 + 0.005*SL	0.79 + 0.005*SL	0.80 + 0.004*SL
	t_{PHL}	1.03	1.01 + 0.007*SL	1.01 + 0.007*SL	1.03 + 0.005*SL
	t_R	0.52	0.52 + 0.002*SL	0.52 + 0.003*SL	0.51 + 0.003*SL
	t_F	0.53	0.53 + 0.004*SL	0.53 + 0.005*SL	0.50 + 0.007*SL
EN to Y	t_{PLH}	1.10	1.09 + 0.005*SL	1.09 + 0.005*SL	1.10 + 0.004*SL
	t_{PHL}	0.35	0.33 + 0.008*SL	0.33 + 0.007*SL	0.35 + 0.006*SL
	t_R	0.53	0.52 + 0.002*SL	0.52 + 0.003*SL	0.51 + 0.003*SL
	t_F	0.18	0.15 + 0.012*SL	0.16 + 0.011*SL	0.16 + 0.010*SL
	t_{PLZ}	0.15	0.15 + 0.000*SL	0.15 + 0.000*SL	0.15 + 0.000*SL
	t_{PHZ}	1.70	1.69 + 0.001*SL	1.69 + 0.000*SL	1.70 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Cell Names & Function Descriptions

Cell Name	Function Description
FD1	D Flip-Flop
FD1D2	D Flip-Flop with 2X Drive
FD1CS	D Flip-Flop with Scan Clock
FD1CSD2	D Flip-Flop with Scan Clock, 2X Drive
FD1S	D Flip-Flop with Scan
FD1SD2	D Flip-Flop with Scan, 2X Drive
FD1Q	D Flip-Flop with Q Output Only
FD1QD2	D Flip-Flop with Q Output Only, 2X Drive
FD1X2	2-Bit D Flip-Flop
FD1X4	4-Bit D Flip-Flop
YFD1	Fast D Flip-Flop
YFD1D2	Fast D Flip-Flop with 2X Drive
FD2	D Flip-Flop with Reset
FD2D2	D Flip-Flop with Reset, 2X Drive
FD2CS	D Flip-Flop with Reset, Scan Clock
FD2CSD2	D Flip-Flop with Reset, Scan Clock, 2X Drive
FD2S	D Flip-Flop with Reset, Scan
FD2SD2	D Flip-Flop with Reset, Scan, 2X Drive
FD2Q	D Flip-Flop with Reset, Q Output Only
FD2QD2	D Flip-Flop with Reset, Q Output Only, 2X Drive
FD2X2	2-Bit D Flip-Flop with Reset
FD2X4	4-Bit D Flip-Flop with Reset
YFD2	Fast D Flip-Flop with Reset
YFD2D2	Fast D Flip-Flop with Reset, 2X Drive
FD2T	D Flip-Flop with Reset, Tri-State Output
FD2TD2	D Flip-Flop with Reset, Tri-State Output, 2X Drive
FD2TCS	D Flip-Flop with Reset, Scan Clock, Tri-State Output
FD2TCSD2	D Flip-Flop with Reset, Scan Clock, Tri-State Output, 2X Drive
FD2TS	D Flip-Flop with Reset, Scan, Tri-State Output
FD2TSD2	D Flip-Flop with Reset, Scan, Tri-State Output, 2X Drive
FD3	D Flip-Flop with Set
FD3D2	D Flip-Flop with Set, 2X Drive
FD3CS	D Flip-Flop with Set, Scan Clock
FD3CSD2	D Flip-Flop with Set, Scan Clock, 2X Drive

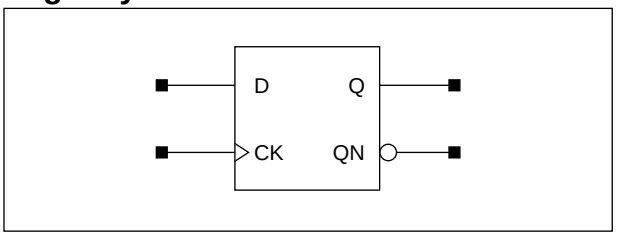
Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
FD3S	D Flip-Flop with Set, Scan
FD3SD2	D Flip-Flop with Set, Scan, 2X Drive
FD3Q	D Flip-Flop with Set, Q Output Only
FD3QD2	D Flip-Flop with Set, Q Output Only, 2X Drive
FD3X2	2-Bit D Flip-Flop with Set
FD3X4	4-Bit D Flip-Flop with Set
YFD3	Fast D Flip-Flop with Set
YFD3D2	Fast D Flip-Flop with Set, 2X Drive
FD4	D Flip-Flop with Reset, Set
FD4D2	D Flip-Flop with Reset, Set, 2X Drive
FD4CS	D Flip-Flop with Reset, Set, Scan Clock
FD4CSD2	D Flip-Flop with Reset, Set, Scan Clock, 2X Drive
FD4S	D Flip-Flop with Reset, Set, Scan
FD4SD2	D Flip-Flop with Reset, Set, Scan, 2X Drive
FD4Q	D Flip-Flop with Reset, Set, Q Output Only
FD4QD2	D Flip-Flop with Reset, Set, Q Output Only, 2X Drive
FD4X2	2-Bit D Flip-Flop with Reset, Set
FD4X4	4-Bit D Flip-Flop with Reset, Set
YFD4	Fast D Flip-Flop with Reset, Set
YFD4D2	Fast D Flip-Flop with Reset, Set, 2X Drive
FD5	D Flip-Flop with Negative Edge Trigger
FD5D2	D Flip-Flop with Negative Edge Trigger, 2X Drive
FD5S	D Flip-Flop with Negative Edge Trigger, Scan
FD5SD2	D Flip-Flop with Negative Edge Trigger, Scan, 2X Drive
FD5X4	4-Bit Flip-Flop with Negative Edge Trigger
FD6	D Flip-Flop with Negative Edge Trigger, Reset
FD6D2	D Flip-Flop with Negative Edge Trigger, Reset, 2X Drive
FD6S	D Flip-Flop with Negative Edge Trigger, Reset, Scan
FD6SD2	D Flip-Flop with Negative Edge Trigger, Reset, Scan, 2X Drive
FD7	D Flip-Flop with Negative Edge Trigger, Set
FD7D2	D Flip-Flop with Negative Edge Trigger, Set, 2X Drive
FD7S	D Flip-Flop with Negative Edge Trigger, Set, Scan
FD7SD2	D Flip-Flop with Negative Edge Trigger, Set, Scan, 2X Drive
FD8	D Flip-Flop with Negative Edge Trigger, Reset, Set

Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
FD8D2	D Flip-Flop with Negative Edge Trigger, Reset, Set, 2X Drive
FD8S	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan
FD8SD2	D Flip-Flop with Negative Edge Trigger, Reset, Set, Scan, 2X Drive
FDS2	D Flip-Flop with Synchronous Clear
FDS2D2	D Flip-Flop with Synchronous Clear, 2X Drive
FDS2CS	D Flip-Flop with Synchronous Clear, Scan Clock
FDS2CSD2	D Flip-Flop with Synchronous Clear, Scan Clock, 2X Drive
FDS2S	D Flip-Flop with Synchronous Clear, Scan
FDS2SD2	D Flip-Flop with Synchronous Clear, Scan, 2X Drive
FDS3	D Flip-Flop with Synchronous Set
FDS3D2	D Flip-Flop with Synchronous Set, 2X Drive
FG1	D Flip-Flop with CK Enable
FG1X4	4-Bit D Flip-Flop with CK Enable
FG2	D Flip-Flop with CK Enable, Reset
FG2X4	4-Bit D Flip-Flop with CK Enable, Reset
FJ1	JK Flip-Flop
FJ1D2	JK Flip-Flop with 2X Drive
FJ1S	JK Flip-Flop with Scan
FJ1SD2	JK Flip-Flop with Scan, 2X Drive
FJ2	JK Flip-Flop with Reset
FJ2D2	JK Flip-Flop with Reset, 2X Drive
FJ2S	JK Flip-Flop with Reset, Scan
FJ2SD2	JK Flip-Flop with Reset, Scan, 2X Drive
FJ4	JK Flip-Flop with Reset, Set
FJ4D2	JK Flip-Flop with Reset, Set, 2X Drive
FJ4S	JK Flip-Flop with Reset, Set, Scan
FJ4SD2	JK Flip-Flop with Reset, Set, Scan, 2X Drive
FT2	Toggle Flip-Flop with Reset
FT2D2	Toggle Flip-Flop with Reset, 2X Drive
FT3	Toggle Flip-Flop with Set
FT3D2	Toggle Flip-Flop with Set, 2X Drive

Logic Symbol



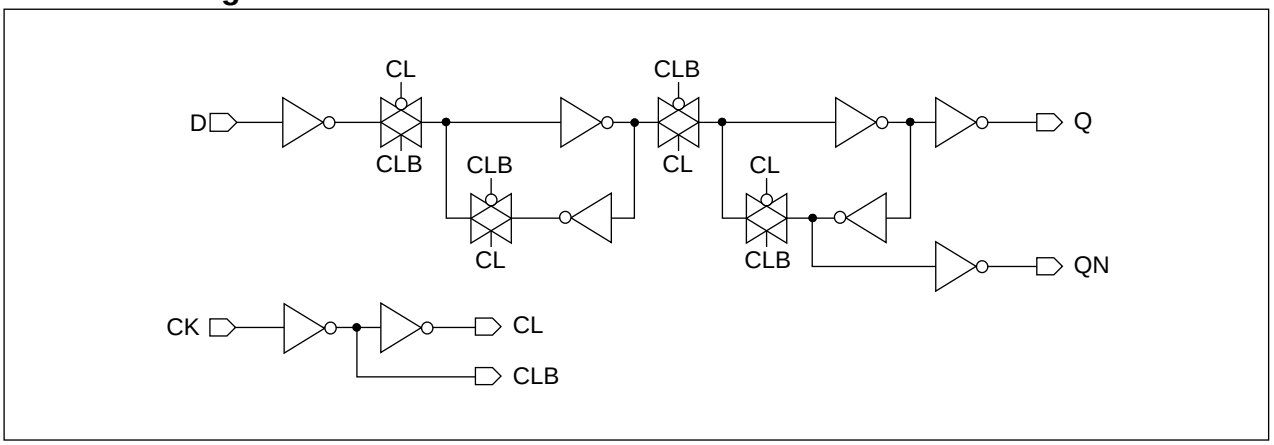
Truth Table

D	CK	Q (n+1)	QN (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
FD1		*FD1D2*		*FD1*	*FD1D2*
D	CK	D	CK		
0.6	0.6	0.6	0.6	5.3	6.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD1	FD1D2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Input Setup Time (D to CK)	t_{SU}	0.49	0.49
Input Hold Time (D to CK)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40, SL: Standard Load)

FD1

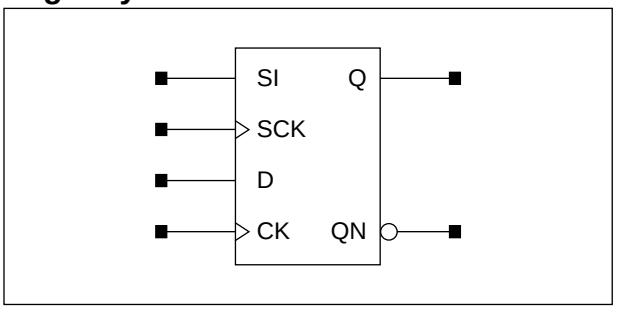
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.57 + 0.030*SL	0.57 + 0.028*SL	0.58 + 0.027*SL
	t_{PHL}	0.70	0.62 + 0.040*SL	0.64 + 0.034*SL	0.65 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to QN	t_{PLH}	0.76	0.70 + 0.027*SL	0.71 + 0.027*SL	0.71 + 0.027*SL
	t_{PHL}	0.79	0.72 + 0.035*SL	0.73 + 0.033*SL	0.73 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

FD1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.59 + 0.018*SL	0.60 + 0.015*SL	0.61 + 0.013*SL
	t_{PHL}	0.70	0.66 + 0.023*SL	0.67 + 0.019*SL	0.69 + 0.017*SL
	t_R	0.17	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
CK to QN	t_{PLH}	0.83	0.80 + 0.014*SL	0.80 + 0.013*SL	0.80 + 0.013*SL
	t_{PHL}	0.86	0.82 + 0.019*SL	0.83 + 0.017*SL	0.83 + 0.016*SL
	t_R	0.15	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Logic Symbol



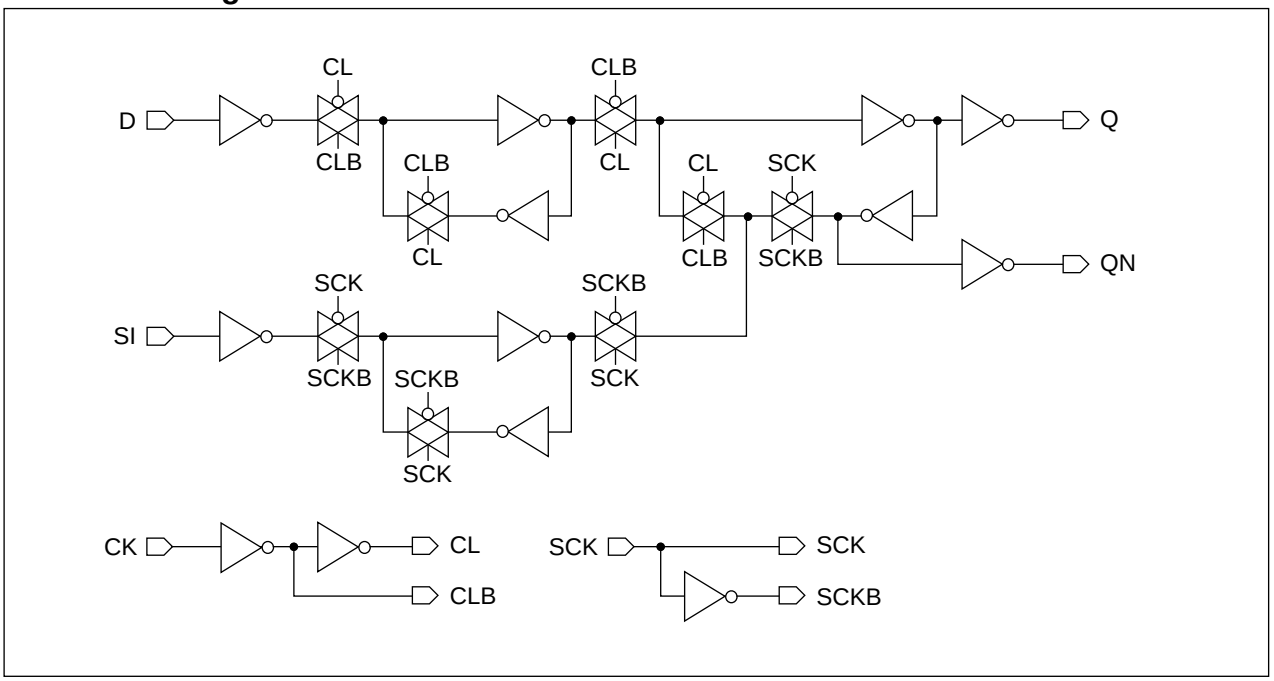
Truth Table

SI	SCK	D	CK	Q (n+1)	QN (n+1)
x	0	0	↑	0	1
x	0	1	↑	1	0
0	↑	x	0	0	1
1	↑	x	0	1	0

Cell Data

Input Load (SL)								Gate Count	
FD1CS				*FD1CSD2*				*FD1CS*	*FD1CSD2*
SI	SCK	D	CK	SI	SCK	D	CK		
0.5	1.2	0.5	0.5	0.5	1.2	0.5	0.5	8.7	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD1CS	FD1CSD2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (SCK)	t_{PWL}	0.79	0.79
Pulse Width High (SCK)	t_{PWH}	0.79	0.79
Input Setup Time (D to CK)	t_{SU}	0.49	0.49
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.71	0.71
Input Hold Time (SI to SCK)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD1CS

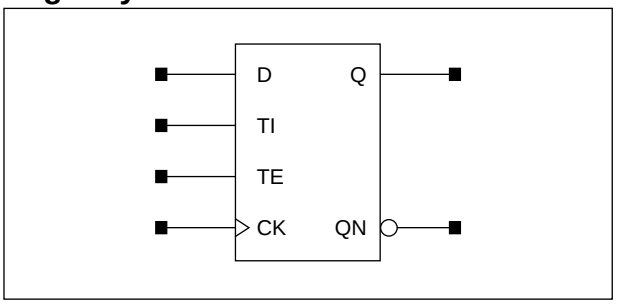
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.57 + 0.030*SL	0.58 + 0.028*SL	0.59 + 0.027*SL
	t_{PHL}	0.70	0.62 + 0.039*SL	0.63 + 0.035*SL	0.65 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.10 + 0.065*SL
SCK to Q	t_{PLH}	0.66	0.60 + 0.033*SL	0.61 + 0.028*SL	0.62 + 0.027*SL
	t_{PHL}	0.60	0.52 + 0.040*SL	0.53 + 0.035*SL	0.55 + 0.033*SL
	t_R	0.25	0.14 + 0.054*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
CK to QN	t_{PLH}	0.81	0.75 + 0.032*SL	0.76 + 0.028*SL	0.77 + 0.027*SL
	t_{PHL}	0.88	0.80 + 0.039*SL	0.81 + 0.035*SL	0.83 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.25	0.12 + 0.064*SL	0.12 + 0.064*SL	0.11 + 0.065*SL
SCK to QN	t_{PLH}	0.65	0.59 + 0.028*SL	0.60 + 0.027*SL	0.60 + 0.027*SL
	t_{PHL}	0.83	0.76 + 0.035*SL	0.76 + 0.033*SL	0.77 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.063*SL	0.09 + 0.064*SL	0.08 + 0.066*SL

FD1CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.60 + 0.018*SL	0.61 + 0.015*SL	0.63 + 0.013*SL
	t_{PHL}	0.70	0.65 + 0.023*SL	0.66 + 0.019*SL	0.69 + 0.017*SL
	t_R	0.17	0.12 + 0.026*SL	0.11 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SCK to Q	t_{PLH}	0.68	0.64 + 0.019*SL	0.65 + 0.015*SL	0.67 + 0.013*SL
	t_{PHL}	0.60	0.56 + 0.024*SL	0.57 + 0.019*SL	0.60 + 0.017*SL
	t_R	0.20	0.15 + 0.024*SL	0.15 + 0.025*SL	0.12 + 0.028*SL
	t_F	0.19	0.12 + 0.032*SL	0.13 + 0.031*SL	0.11 + 0.032*SL
CK to QN	t_{PLH}	0.88	0.85 + 0.016*SL	0.85 + 0.014*SL	0.86 + 0.013*SL
	t_{PHL}	0.94	0.90 + 0.022*SL	0.91 + 0.019*SL	0.92 + 0.017*SL
	t_R	0.19	0.14 + 0.024*SL	0.13 + 0.026*SL	0.11 + 0.028*SL
	t_F	0.20	0.13 + 0.033*SL	0.13 + 0.031*SL	0.13 + 0.032*SL
SCK to QN	t_{PLH}	0.72	0.69 + 0.014*SL	0.70 + 0.013*SL	0.70 + 0.013*SL
	t_{PHL}	0.92	0.88 + 0.017*SL	0.88 + 0.017*SL	0.89 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.030*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



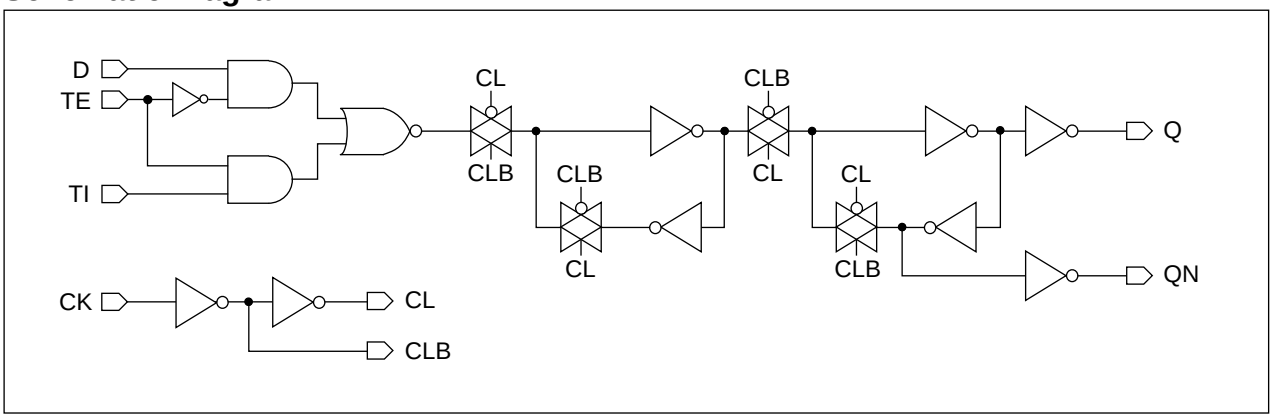
Truth Table

D	TI	TE	CK	Q (n+1)	QN (n+1)
0	x	0	↑	0	1
1	x	0	↑	1	0
x	0	1	↑	0	1
x	1	1	↑	1	0

Cell Data

Input Load (SL)								Gate Count	
FD1S				*FD1SD2*				*FD1S*	*FD1SD2*
D	TI	TE	CK	D	TI	TE	CK		
0.6	0.6	1.1	0.6	0.6	0.6	1.1	0.6	7.0	7.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD1S	FD1SD2
Pulse Width Low (CK)	t_{PWL}	0.95	0.85
Pulse Width High (CK)	t_{PWH}	0.77	0.77
Input Setup Time (D to CK)	t_{SU}	0.71	0.71
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.71	0.71
Input Hold Time (TI to CK)	t_{HD}	0.44	0.33
Input Setup Time (TE to CK)	t_{SU}	0.74	0.74
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD1S

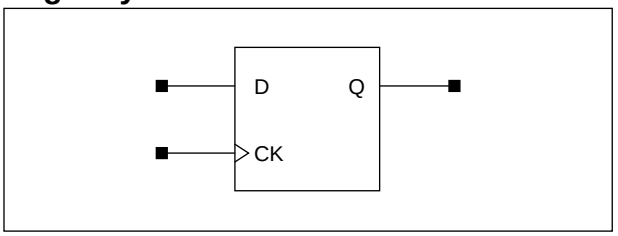
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.58 + 0.030*SL	0.58 + 0.028*SL	0.59 + 0.027*SL
	t_{PHL}	0.72	0.64 + 0.040*SL	0.66 + 0.034*SL	0.67 + 0.033*SL
	t_R	0.22	0.12 + 0.054*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to QN	t_{PLH}	0.78	0.72 + 0.028*SL	0.72 + 0.027*SL	0.72 + 0.027*SL
	t_{PHL}	0.80	0.73 + 0.035*SL	0.73 + 0.033*SL	0.74 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

FD1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.60 + 0.018*SL	0.61 + 0.015*SL	0.63 + 0.013*SL
	t_{PHL}	0.72	0.67 + 0.023*SL	0.68 + 0.020*SL	0.71 + 0.017*SL
	t_R	0.17	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
CK to QN	t_{PLH}	0.84	0.81 + 0.014*SL	0.82 + 0.013*SL	0.82 + 0.013*SL
	t_{PHL}	0.87	0.83 + 0.019*SL	0.83 + 0.017*SL	0.84 + 0.016*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Logic Symbol



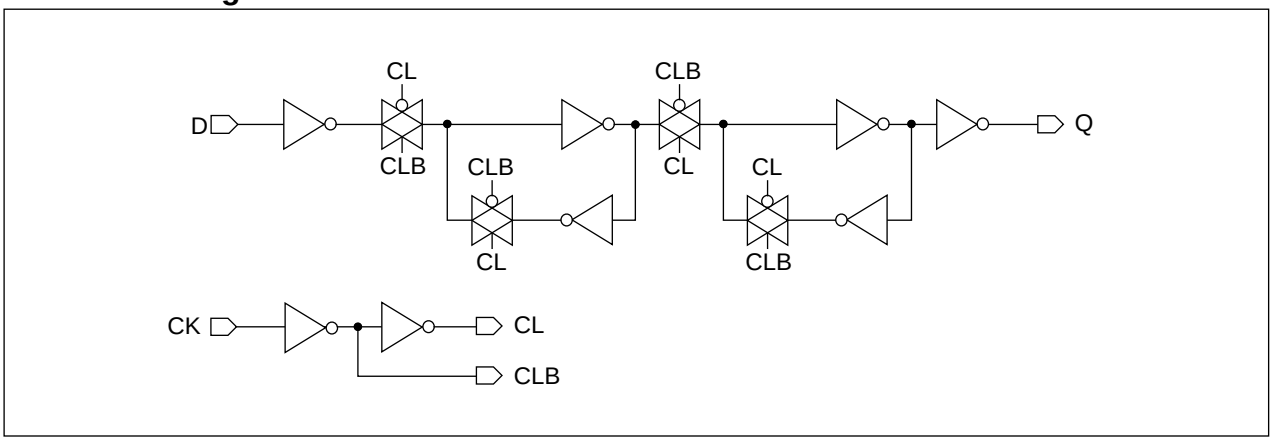
Truth Table

D	CK	Q (n+1)
0	↑	0
1	↑	1
x	↓	Q (n)

Cell Data

Input Load (SL)				Gate Count	
FD1Q		*FD1QD2*		*FD1Q*	*FD1QD2*
D	CK	D	CK		
0.6	0.6	0.6	0.6	5.0	5.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD1Q	FD1QD2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Input Setup Time (D to CK)	t_{SU}	0.49	0.49
Input Hold Time (D to CK)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD1Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.62	0.56 + 0.030*SL	0.57 + 0.027*SL	0.58 + 0.027*SL
	t_{PHL}	0.69	0.61 + 0.038*SL	0.63 + 0.034*SL	0.64 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.23	0.11 + 0.061*SL	0.11 + 0.063*SL	0.08 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

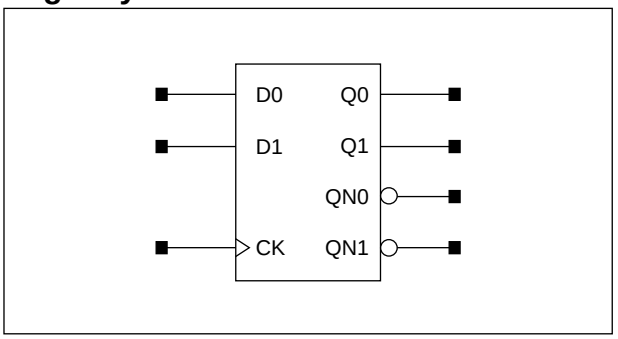
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD1QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.59 + 0.017*SL	0.60 + 0.015*SL	0.61 + 0.013*SL
	t_{PHL}	0.69	0.64 + 0.024*SL	0.66 + 0.019*SL	0.68 + 0.017*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.031*SL	0.12 + 0.031*SL	0.10 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

Dn	CK	Qn (n+1)	QNn (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Qn (n)	QNn (n)

Cell Data

Input Load (SL)		Gate Count
Dn	CK	
0.6	0.6	9.7

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (CK)	t_{PWL}	0.93
Pulse Width High (CK)	t_{PWH}	0.79
Input Setup Time (D0 to CK)	t_{SU}	0.41
Input Hold Time (D0 to CK)	t_{HD}	0.33
Input Setup Time (D1 to CK)	t_{SU}	0.41
Input Hold Time (D1 to CK)	t_{HD}	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

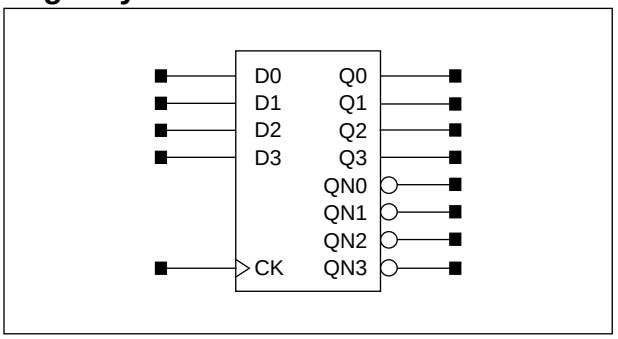
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.70	0.64 + 0.030*SL	0.65 + 0.028*SL	0.66 + 0.027*SL
	t_{PHL}	0.87	0.79 + 0.040*SL	0.81 + 0.034*SL	0.82 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q1	t_{PLH}	0.70	0.64 + 0.030*SL	0.65 + 0.028*SL	0.66 + 0.027*SL
	t_{PHL}	0.87	0.79 + 0.040*SL	0.81 + 0.034*SL	0.82 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to QN0	t_{PLH}	0.93	0.88 + 0.028*SL	0.88 + 0.027*SL	0.88 + 0.027*SL
	t_{PHL}	0.87	0.80 + 0.035*SL	0.80 + 0.033*SL	0.81 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
CK to QN1	t_{PLH}	0.93	0.87 + 0.028*SL	0.88 + 0.027*SL	0.88 + 0.027*SL
	t_{PHL}	0.87	0.80 + 0.035*SL	0.80 + 0.033*SL	0.81 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

FD1X4

4-Bit D Flip-Flop

Logic Symbol



Truth Table

Dn	CK	Qn (n+1)	QNn (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Qn (n)	QNn (n)

Cell Data

Input Load (SL)		Gate Count
Dn	CK	
0.6	0.6	18.3

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (CK)	t_{PWL}	1.42
Pulse Width High (CK)	t_{PWH}	0.90
Input Setup Time (D0 to CK)	t_{SU}	0.33
Input Hold Time (D0 to CK)	t_{HD}	0.52
Input Setup Time (D1 to CK)	t_{SU}	0.33
Input Hold Time (D1 to CK)	t_{HD}	0.52
Input Setup Time (D2 to CK)	t_{SU}	0.36
Input Hold Time (D2 to CK)	t_{HD}	0.52
Input Setup Time (D3 to CK)	t_{SU}	0.52
Input Hold Time (D3 to CK)	t_{HD}	0.52

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

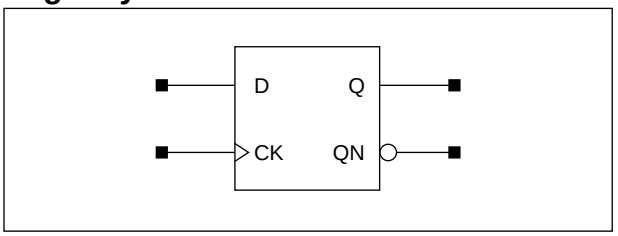
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.83	0.77 + 0.030*SL	0.78 + 0.028*SL	0.79 + 0.027*SL
	t_{PHL}	1.18	1.10 + 0.040*SL	1.12 + 0.034*SL	1.13 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q1	t_{PLH}	0.84	0.78 + 0.030*SL	0.78 + 0.028*SL	0.79 + 0.027*SL
	t_{PHL}	1.18	1.10 + 0.040*SL	1.12 + 0.034*SL	1.13 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q2	t_{PLH}	0.83	0.77 + 0.030*SL	0.78 + 0.028*SL	0.79 + 0.027*SL
	t_{PHL}	1.18	1.10 + 0.040*SL	1.12 + 0.034*SL	1.13 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q3	t_{PLH}	0.83	0.77 + 0.030*SL	0.78 + 0.028*SL	0.79 + 0.027*SL
	t_{PHL}	1.18	1.10 + 0.040*SL	1.12 + 0.034*SL	1.13 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to QN0	t_{PLH}	1.24	1.18 + 0.028*SL	1.19 + 0.027*SL	1.19 + 0.027*SL
	t_{PHL}	1.00	0.93 + 0.035*SL	0.93 + 0.033*SL	0.94 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
CK to QN1	t_{PLH}	1.24	1.18 + 0.028*SL	1.19 + 0.027*SL	1.19 + 0.027*SL
	t_{PHL}	1.00	0.93 + 0.035*SL	0.93 + 0.033*SL	0.94 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
CK to QN2	t_{PLH}	1.24	1.18 + 0.028*SL	1.19 + 0.027*SL	1.18 + 0.027*SL
	t_{PHL}	1.00	0.93 + 0.035*SL	0.93 + 0.033*SL	0.94 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
CK to QN3	t_{PLH}	1.24	1.18 + 0.028*SL	1.18 + 0.027*SL	1.18 + 0.027*SL
	t_{PHL}	1.00	0.93 + 0.036*SL	0.93 + 0.033*SL	0.94 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

YFD1/YFD1D2

Fast D Flip-Flop with 1X/2X Drive

Logic Symbol



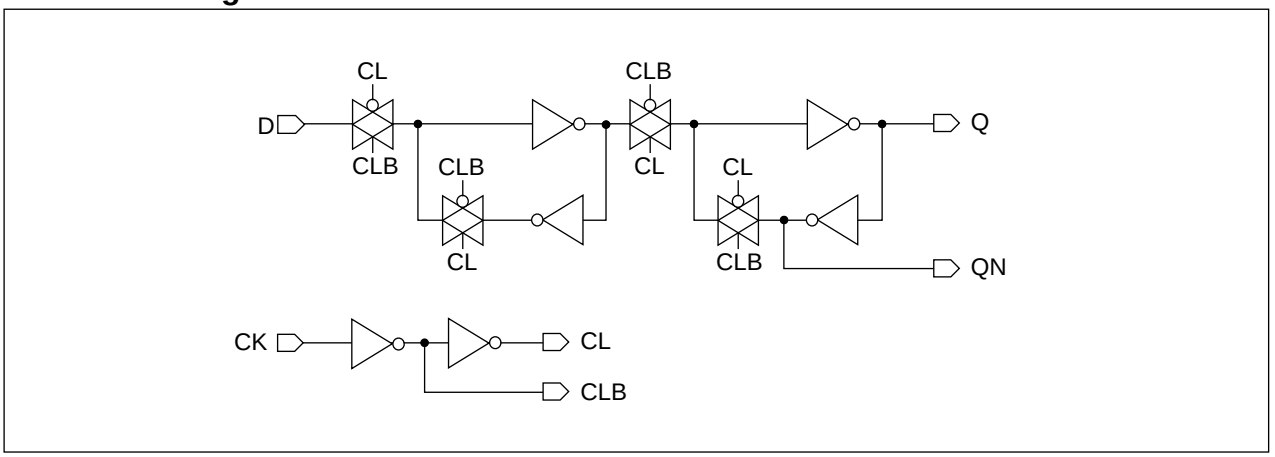
Truth Table

D	CK	Q (n+1)	QN (n+1)
0	↑	0	1
1	↑	1	0
x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
YFD1		*YFD1D2*		*YFD1*	*YFD1D2*
D	CK	D	CK		
1.9	0.6	1.9	0.6	5.0	5.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		YFD1	YFD1D2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Input Setup Time (D to CK)	t_{SU}	0.38	0.38
Input Hold Time (D to CK)	t_{HD}	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40, SL: Standard Load)

YFD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.54	0.48 + 0.030*SL	0.48 + 0.028*SL	0.49 + 0.027*SL
	t_{PHL}	0.63	0.54 + 0.045*SL	0.56 + 0.038*SL	0.60 + 0.033*SL
	t_R	0.29	0.18 + 0.053*SL	0.17 + 0.057*SL	0.15 + 0.060*SL
	t_F	0.38	0.25 + 0.062*SL	0.25 + 0.062*SL	0.24 + 0.064*SL
CK to QN	t_{PLH}	0.78	0.61 + 0.088*SL	0.63 + 0.081*SL	0.67 + 0.077*SL
	t_{PHL}	0.70	0.55 + 0.076*SL	0.56 + 0.073*SL	0.56 + 0.073*SL
	t_R	0.25	0.11 + 0.070*SL	0.11 + 0.071*SL	0.10 + 0.071*SL
	t_F	0.24	0.09 + 0.074*SL	0.09 + 0.075*SL	0.08 + 0.075*SL

YFD1D2

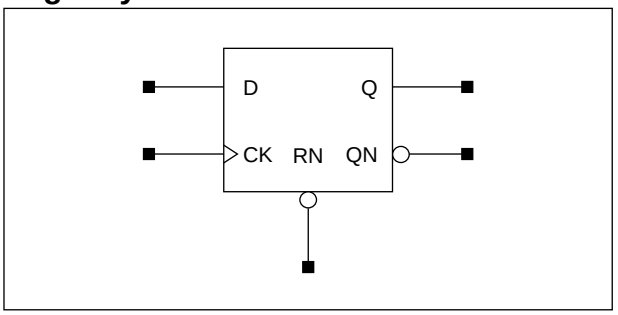
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.55	0.52 + 0.017*SL	0.53 + 0.015*SL	0.54 + 0.013*SL
	t_{PHL}	0.68	0.62 + 0.027*SL	0.63 + 0.023*SL	0.68 + 0.018*SL
	t_R	0.24	0.20 + 0.024*SL	0.19 + 0.027*SL	0.17 + 0.028*SL
	t_F	0.38	0.31 + 0.031*SL	0.31 + 0.031*SL	0.31 + 0.031*SL
CK to QN	t_{PLH}	0.79	0.69 + 0.050*SL	0.70 + 0.044*SL	0.75 + 0.039*SL
	t_{PHL}	0.66	0.58 + 0.040*SL	0.59 + 0.038*SL	0.60 + 0.036*SL
	t_R	0.18	0.11 + 0.034*SL	0.12 + 0.034*SL	0.11 + 0.035*SL
	t_F	0.15	0.08 + 0.037*SL	0.08 + 0.037*SL	0.07 + 0.037*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

FD2/FD2D2

D Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



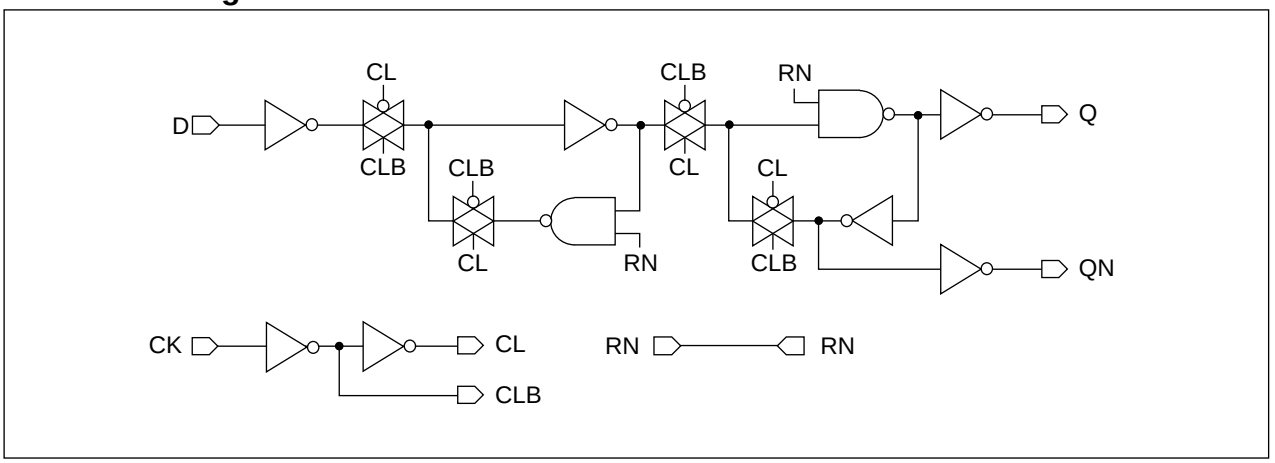
Truth Table

D	CK	RN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FD2			*FD2D2*			*FD2*	*FD2D2*
D	CK	RN	D	CK	RN		
0.6	0.6	1.1	0.6	0.6	1.1	6.3	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD2	FD2D2
Pulse Width Low (CK)	t_{PWL}	0.82	0.82
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Input Setup Time (D to CK)	t_{SU}	0.52	0.52
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.66	0.66

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.69	0.62 + 0.035*SL	0.63 + 0.029*SL	0.66 + 0.027*SL
	t_{PHL}	0.73	0.65 + 0.040*SL	0.67 + 0.035*SL	0.69 + 0.033*SL
	t_R	0.25	0.14 + 0.056*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q	t_{PHL}	0.37	0.29 + 0.040*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to QN	t_{PLH}	0.79	0.73 + 0.028*SL	0.74 + 0.027*SL	0.74 + 0.027*SL
	t_{PHL}	0.86	0.79 + 0.035*SL	0.80 + 0.033*SL	0.80 + 0.033*SL
	t_R	0.20	0.09 + 0.055*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
RN to QN	t_{PLH}	0.43	0.37 + 0.028*SL	0.37 + 0.027*SL	0.37 + 0.027*SL
	t_R	0.20	0.10 + 0.053*SL	0.08 + 0.059*SL	0.07 + 0.060*SL

FD2D2

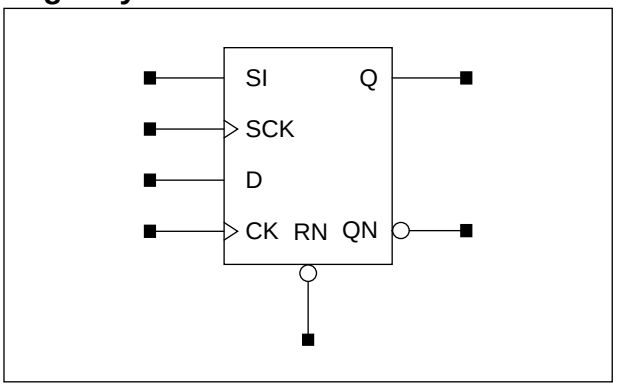
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.70	0.65 + 0.022*SL	0.67 + 0.017*SL	0.70 + 0.013*SL
	t_{PHL}	0.73	0.68 + 0.024*SL	0.70 + 0.019*SL	0.72 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.19	0.12 + 0.032*SL	0.13 + 0.031*SL	0.11 + 0.032*SL
RN to Q	t_{PHL}	0.36	0.32 + 0.024*SL	0.33 + 0.019*SL	0.36 + 0.017*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
CK to QN	t_{PLH}	0.86	0.83 + 0.014*SL	0.83 + 0.013*SL	0.83 + 0.013*SL
	t_{PHL}	0.96	0.92 + 0.017*SL	0.92 + 0.017*SL	0.93 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.18	0.11 + 0.034*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
RN to QN	t_{PLH}	0.49	0.46 + 0.014*SL	0.46 + 0.013*SL	0.47 + 0.013*SL
	t_R	0.15	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

FD2CS/FD2CSD2

D Flip-Flop with Reset, Scan Clock, 1X/2X Drive

Logic Symbol



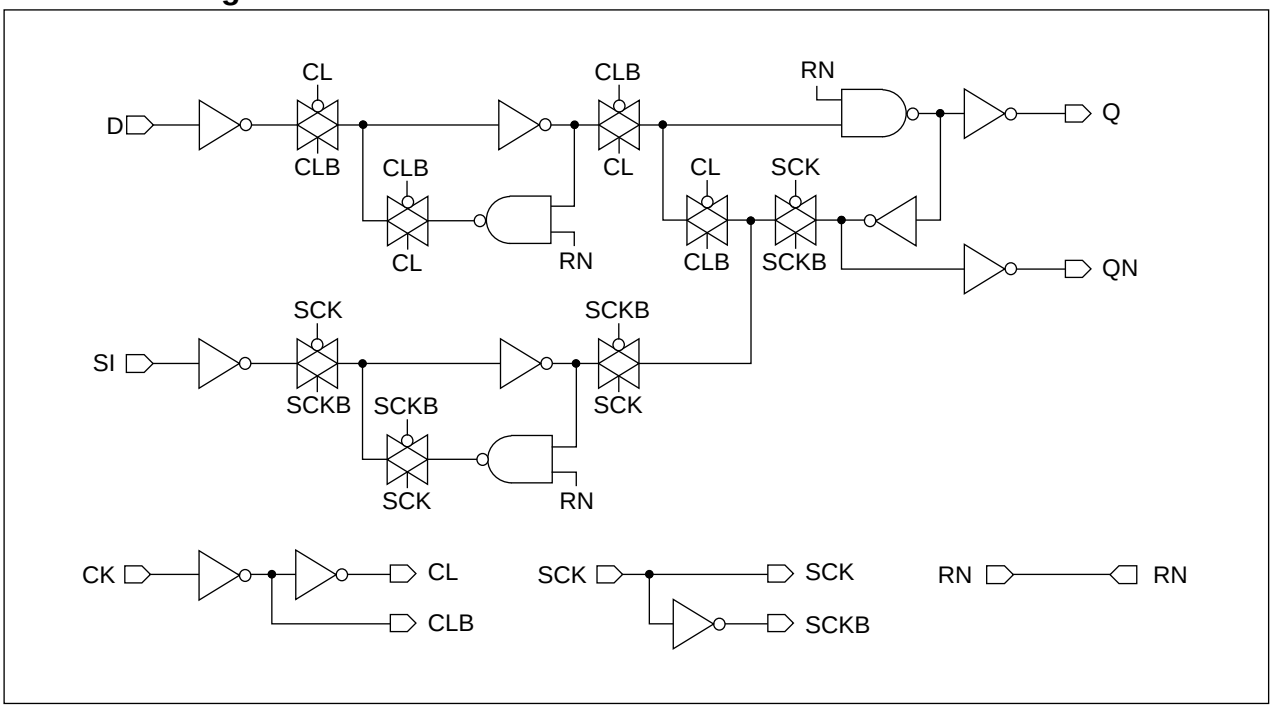
Truth Table

SI	SCK	D	CK	RN	Q (n+1)	QN (n+1)
x	0	0	⎍	1	0	1
x	0	1	⎍	1	1	0
0	⎍	x	0	1	0	1
1	⎍	x	0	1	1	0
x	x	x	x	0	0	1

Cell Data

Input Load (SL)										Gate Count	
FD2CS					*FD2CSD2*					*FD2CS*	*FD2CSD2*
SI	SCK	D	CK	RN	SI	SCK	D	CK	RN		
0.5	1.2	0.5	0.5	1.4	0.5	1.2	0.5	0.5	1.4	10.3	10.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD2CS	FD2CSD2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (SCK)	t_{PWL}	0.79	0.79
Pulse Width High (SCK)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Input Setup Time (D to CK)	t_{SU}	0.52	0.52
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.74	0.74
Input Hold Time (SI to SCK)	t_{HD}	0.33	0.33
Recovery Time (RN to CK)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.66	0.66
Recovery Time (RN to SCK)	t_{RC}	0.33	0.33
Input Hold Time (RN to SCK)	t_{HD}	0.49	0.49

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD2CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.72	0.66 + 0.034*SL	0.67 + 0.029*SL	0.69 + 0.027*SL
	t_{PHL}	0.71	0.63 + 0.039*SL	0.65 + 0.035*SL	0.67 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.058*SL	0.12 + 0.059*SL
	t_F	0.24	0.11 + 0.065*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
SCK to Q	t_{PLH}	0.78	0.71 + 0.036*SL	0.72 + 0.030*SL	0.75 + 0.027*SL
	t_{PHL}	0.61	0.53 + 0.040*SL	0.54 + 0.035*SL	0.56 + 0.033*SL
	t_R	0.28	0.17 + 0.056*SL	0.17 + 0.056*SL	0.14 + 0.059*SL
	t_F	0.25	0.13 + 0.061*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
RN to Q	t_{PHL}	0.39	0.31 + 0.040*SL	0.32 + 0.035*SL	0.34 + 0.033*SL
	t_F	0.25	0.12 + 0.064*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
CK to QN	t_{PLH}	0.83	0.76 + 0.032*SL	0.78 + 0.028*SL	0.79 + 0.027*SL
	t_{PHL}	0.98	0.91 + 0.038*SL	0.92 + 0.035*SL	0.93 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.25	0.13 + 0.064*SL	0.13 + 0.064*SL	0.11 + 0.065*SL
SCK to QN	t_{PLH}	0.66	0.60 + 0.027*SL	0.60 + 0.027*SL	0.60 + 0.027*SL
	t_{PHL}	0.95	0.88 + 0.034*SL	0.89 + 0.033*SL	0.89 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.23	0.10 + 0.062*SL	0.10 + 0.064*SL	0.08 + 0.066*SL
RN to QN	t_{PLH}	0.51	0.44 + 0.032*SL	0.45 + 0.028*SL	0.46 + 0.027*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

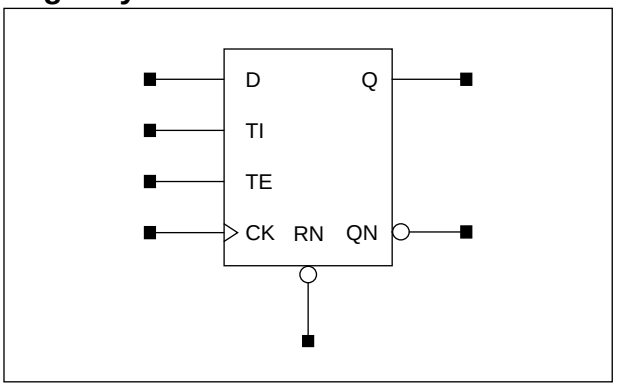
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD2CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.75	0.71 + 0.022*SL	0.72 + 0.017*SL	0.75 + 0.014*SL
	t_{PHL}	0.72	0.67 + 0.023*SL	0.68 + 0.020*SL	0.71 + 0.017*SL
	t_R	0.21	0.16 + 0.028*SL	0.16 + 0.026*SL	0.14 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SCK to Q	t_{PLH}	0.82	0.77 + 0.022*SL	0.79 + 0.017*SL	0.82 + 0.014*SL
	t_{PHL}	0.62	0.57 + 0.024*SL	0.58 + 0.020*SL	0.61 + 0.017*SL
	t_R	0.24	0.19 + 0.026*SL	0.19 + 0.026*SL	0.17 + 0.028*SL
	t_F	0.19	0.13 + 0.031*SL	0.13 + 0.031*SL	0.12 + 0.032*SL
RN to Q	t_{PHL}	0.38	0.34 + 0.024*SL	0.35 + 0.020*SL	0.38 + 0.017*SL
	t_F	0.19	0.12 + 0.033*SL	0.13 + 0.031*SL	0.12 + 0.032*SL
CK to QN	t_{PLH}	0.90	0.86 + 0.016*SL	0.87 + 0.014*SL	0.88 + 0.013*SL
	t_{PHL}	1.09	1.05 + 0.021*SL	1.06 + 0.017*SL	1.06 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.026*SL	0.11 + 0.028*SL
	t_F	0.21	0.15 + 0.030*SL	0.15 + 0.031*SL	0.13 + 0.032*SL
SCK to QN	t_{PLH}	0.73	0.71 + 0.014*SL	0.71 + 0.013*SL	0.71 + 0.013*SL
	t_{PHL}	1.08	1.05 + 0.016*SL	1.05 + 0.016*SL	1.04 + 0.016*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.18	0.11 + 0.033*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
RN to QN	t_{PLH}	0.57	0.53 + 0.016*SL	0.54 + 0.014*SL	0.55 + 0.013*SL
	t_R	0.19	0.14 + 0.025*SL	0.13 + 0.026*SL	0.11 + 0.028*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Logic Symbol



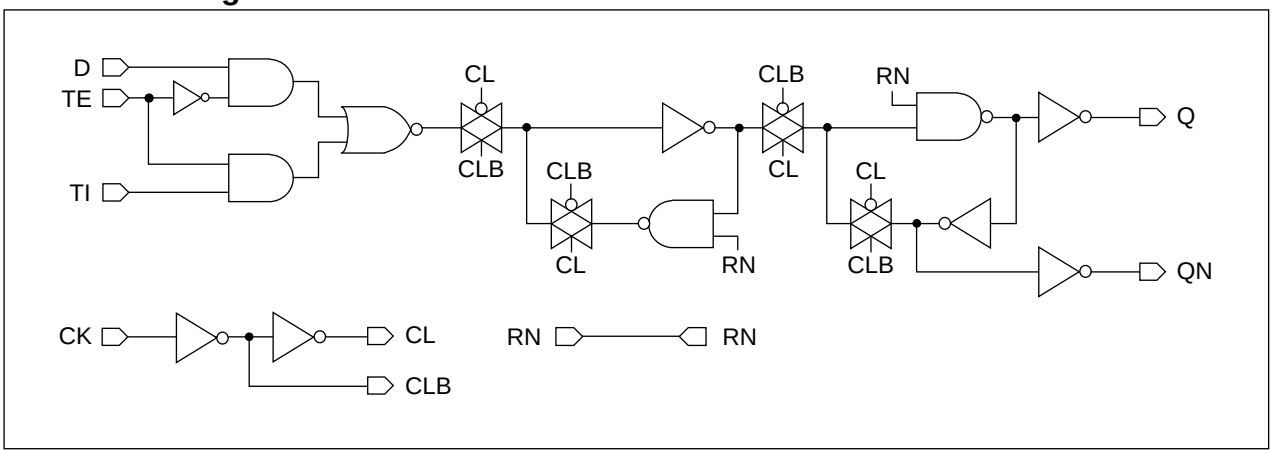
Truth Table

D	TI	TE	CK	RN	Q (n+1)	QN (n+1)
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	0	1

Cell Data

Input Load (SL)										Gate Count	
FD2S					*FD2CSD2*					*FD2S*	*FD2SD2*
D	TI	TE	CK	RN	SI	SCK	D	CK	RN		
0.6	0.6	1.1	0.6	1.3	0.5	1.2	0.5	0.5	1.4	8.0	8.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD2S	FD2SD2
Pulse Width Low (CK)	t_{PWL}	0.85	0.85
Pulse Width High (CK)	t_{PWH}	0.77	0.77
Pulse Width Low (RN)	t_{PWL}	0.77	0.77
Input Setup Time (D to CK)	t_{SU}	0.71	0.71
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.71	0.71
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.76	0.76
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.71

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD2S

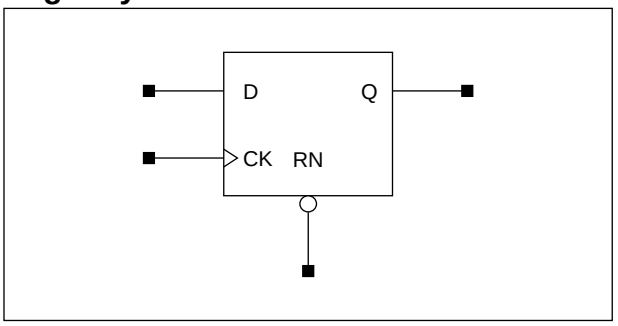
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.70	0.63 + 0.035*SL	0.64 + 0.030*SL	0.67 + 0.027*SL
	t_{PHL}	0.75	0.67 + 0.040*SL	0.69 + 0.035*SL	0.70 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q	t_{PHL}	0.37	0.29 + 0.040*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to QN	t_{PLH}	0.81	0.75 + 0.028*SL	0.76 + 0.027*SL	0.76 + 0.027*SL
	t_{PHL}	0.87	0.80 + 0.035*SL	0.81 + 0.033*SL	0.81 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.07 + 0.066*SL
RN to QN	t_{PLH}	0.43	0.37 + 0.028*SL	0.37 + 0.027*SL	0.37 + 0.027*SL
	t_R	0.20	0.10 + 0.054*SL	0.08 + 0.059*SL	0.07 + 0.060*SL

FD2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.71	0.66 + 0.022*SL	0.68 + 0.017*SL	0.71 + 0.013*SL
	t_{PHL}	0.75	0.70 + 0.024*SL	0.72 + 0.020*SL	0.74 + 0.017*SL
	t_R	0.20	0.15 + 0.025*SL	0.14 + 0.028*SL	0.14 + 0.028*SL
	t_F	0.19	0.12 + 0.031*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
RN to Q	t_{PHL}	0.36	0.32 + 0.023*SL	0.33 + 0.019*SL	0.36 + 0.017*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
CK to QN	t_{PLH}	0.88	0.85 + 0.013*SL	0.85 + 0.013*SL	0.85 + 0.013*SL
	t_{PHL}	0.97	0.93 + 0.017*SL	0.93 + 0.017*SL	0.94 + 0.016*SL
	t_R	0.15	0.11 + 0.025*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.10 + 0.032*SL
RN to QN	t_{PLH}	0.49	0.46 + 0.014*SL	0.46 + 0.013*SL	0.47 + 0.013*SL
	t_R	0.15	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



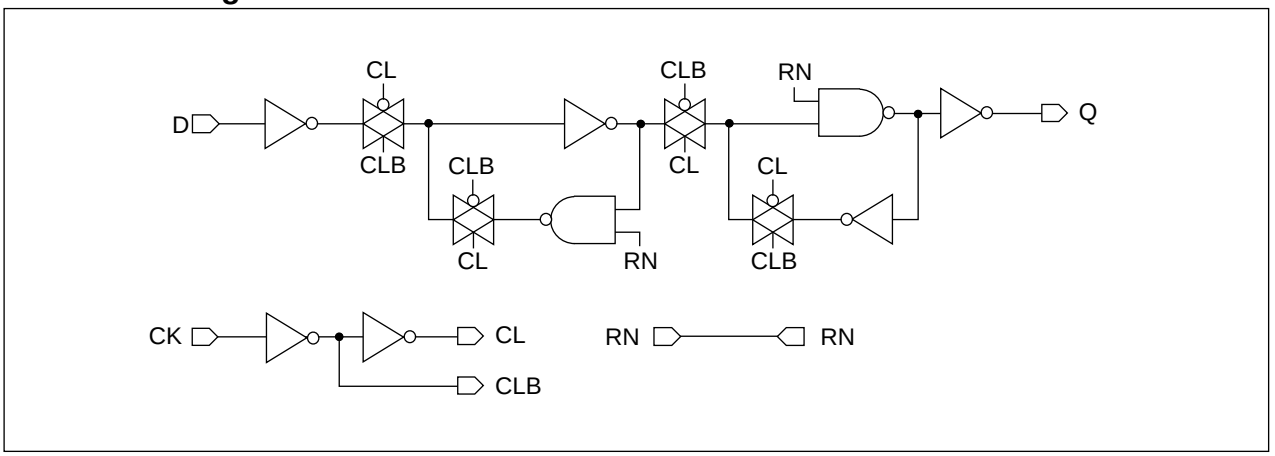
Truth Table

D	CK	RN	Q (n+1)
0	↑	1	0
1	↑	1	1
x	x	0	0
x	↓	x	Q (n)

Cell Data

Input Load (SL)						Gate Count	
FD2Q			*FD2QD2*			*FD2Q*	*FD2QD2*
D	CK	RN	D	CK	RN		
0.6	0.6	1.1	0.6	0.6	1.1	6.0	6.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD2Q	FD2QD2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Input Setup Time (D to CK)	t_{SU}	0.52	0.52
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.66	0.66

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD2Q

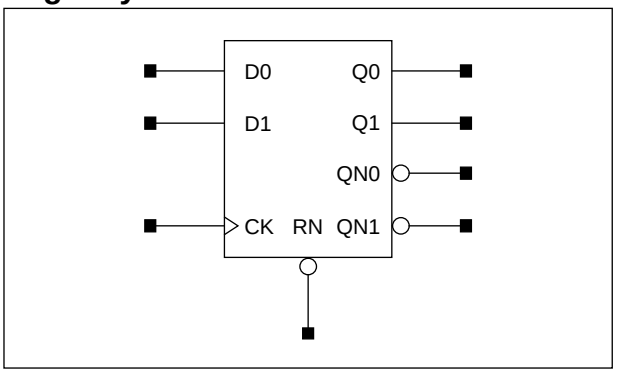
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.68	0.62 + 0.034*SL	0.63 + 0.029*SL	0.65 + 0.027*SL
	t_{PHL}	0.72	0.64 + 0.039*SL	0.66 + 0.034*SL	0.67 + 0.033*SL
	t_R	0.25	0.13 + 0.057*SL	0.13 + 0.057*SL	0.11 + 0.060*SL
	t_F	0.24	0.12 + 0.060*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to Q	t_{PHL}	0.36	0.28 + 0.038*SL	0.29 + 0.034*SL	0.31 + 0.033*SL
	t_F	0.23	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

FD2QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.69	0.65 + 0.021*SL	0.66 + 0.017*SL	0.69 + 0.013*SL
	t_{PHL}	0.72	0.67 + 0.024*SL	0.69 + 0.019*SL	0.71 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.030*SL	0.11 + 0.032*SL
RN to Q	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.019*SL	0.35 + 0.017*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.10 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

Dn	CK	RN	Qn (n+1)	QNn (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
Dn	CK	RN	
0.6	0.6	2.3	11.7

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (CK)	t_{PWL}	0.96
Pulse Width High (CK)	t_{PWH}	0.79
Pulse Width Low (RN)	t_{PWL}	0.79
Input Setup Time (D0 to CK)	t_{SU}	0.38
Input Hold Time (D0 to CK)	t_{HD}	0.36
Input Setup Time (D1 to CK)	t_{SU}	0.38
Input Hold Time (D1 to CK)	t_{HD}	0.36
Recovery Time (RN)	t_{RC}	0.33
Input Hold Time (RN to CK)	t_{HD}	0.76

FD2X2

2-Bit D Flip-Flop with Reset

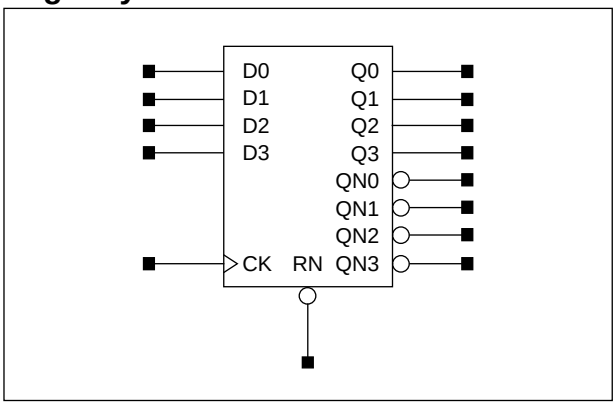
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.77	0.70 + 0.035*SL	0.72 + 0.030*SL	0.74 + 0.027*SL
	t_{PHL}	0.92	0.84 + 0.040*SL	0.86 + 0.034*SL	0.88 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q0	t_{PHL}	0.37	0.29 + 0.040*SL	0.31 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q1	t_{PLH}	0.77	0.70 + 0.035*SL	0.72 + 0.029*SL	0.74 + 0.027*SL
	t_{PHL}	0.92	0.84 + 0.040*SL	0.86 + 0.035*SL	0.87 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.063*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q1	t_{PHL}	0.37	0.29 + 0.040*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to QN0	t_{PLH}	0.98	0.93 + 0.028*SL	0.93 + 0.027*SL	0.93 + 0.027*SL
	t_{PHL}	0.95	0.88 + 0.035*SL	0.88 + 0.033*SL	0.89 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.08 + 0.066*SL
RN to QN0	t_{PLH}	0.43	0.38 + 0.028*SL	0.38 + 0.027*SL	0.38 + 0.027*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
CK to QN1	t_{PLH}	0.98	0.92 + 0.028*SL	0.93 + 0.027*SL	0.93 + 0.027*SL
	t_{PHL}	0.94	0.87 + 0.035*SL	0.88 + 0.033*SL	0.88 + 0.033*SL
	t_R	0.20	0.09 + 0.055*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
RN to QN1	t_{PLH}	0.43	0.37 + 0.028*SL	0.37 + 0.027*SL	0.37 + 0.027*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

Dn	CK	RN	Qn (n+1)	QNn (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
Dn	CK	RN	
0.6	0.6	4.8	22.3

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (CK)	t_{PWL}	0.96
Pulse Width High (CK)	t_{PWH}	0.79
Pulse Width Low (RN)	t_{PWL}	0.79
Input Setup Time (D0 to CK)	t_{SU}	0.38
Input Hold Time (D0 to CK)	t_{HD}	0.36
Input Setup Time (D1 to CK)	t_{SU}	0.38
Input Hold Time (D1 to CK)	t_{HD}	0.36
Input Setup Time (D2 to CK)	t_{SU}	0.33
Input Hold Time (D2 to CK)	t_{HD}	0.96
Input Setup Time (D3 to CK)	t_{SU}	0.79
Input Hold Time (D3 to CK)	t_{HD}	0.79
Recovery Time (RN)	t_{RC}	0.38
Input Hold Time (RN to CK)	t_{HD}	0.93

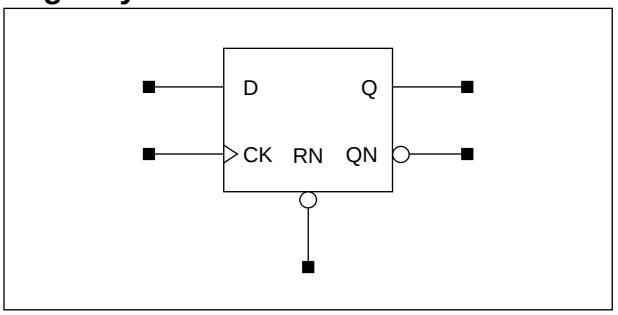
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.92	0.85 + 0.035*SL	0.86 + 0.030*SL	0.89 + 0.027*SL
	t_{PHL}	1.26	1.18 + 0.040*SL	1.19 + 0.034*SL	1.21 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q0	t_{PHL}	0.37	0.29 + 0.040*SL	0.31 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q1	t_{PLH}	0.92	0.85 + 0.035*SL	0.86 + 0.030*SL	0.89 + 0.027*SL
	t_{PHL}	1.26	1.18 + 0.040*SL	1.19 + 0.035*SL	1.21 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q1	t_{PHL}	0.37	0.29 + 0.040*SL	0.31 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q2	t_{PLH}	0.92	0.85 + 0.035*SL	0.86 + 0.030*SL	0.89 + 0.027*SL
	t_{PHL}	1.26	1.18 + 0.040*SL	1.19 + 0.034*SL	1.21 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q2	t_{PHL}	0.37	0.29 + 0.040*SL	0.31 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q3	t_{PLH}	0.91	0.84 + 0.035*SL	0.86 + 0.030*SL	0.88 + 0.027*SL
	t_{PHL}	1.25	1.18 + 0.040*SL	1.19 + 0.034*SL	1.21 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q3	t_{PHL}	0.37	0.29 + 0.040*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to QN0	t_{PLH}	1.31	1.26 + 0.028*SL	1.26 + 0.027*SL	1.26 + 0.027*SL
	t_{PHL}	1.09	1.02 + 0.035*SL	1.02 + 0.033*SL	1.02 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.08 + 0.066*SL
RN to QN0	t_{PLH}	0.43	0.38 + 0.028*SL	0.38 + 0.027*SL	0.38 + 0.027*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
CK to QN1	t_{PLH}	1.31	1.26 + 0.028*SL	1.26 + 0.027*SL	1.26 + 0.027*SL
	t_{PHL}	1.09	1.02 + 0.035*SL	1.02 + 0.033*SL	1.02 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.23	0.10 + 0.061*SL	0.10 + 0.063*SL	0.08 + 0.066*SL
RN to QN1	t_{PLH}	0.43	0.38 + 0.028*SL	0.38 + 0.027*SL	0.38 + 0.027*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
CK to QN2	t_{PLH}	1.31	1.26 + 0.028*SL	1.26 + 0.027*SL	1.26 + 0.027*SL
	t_{PHL}	1.09	1.02 + 0.035*SL	1.02 + 0.033*SL	1.02 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.08 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



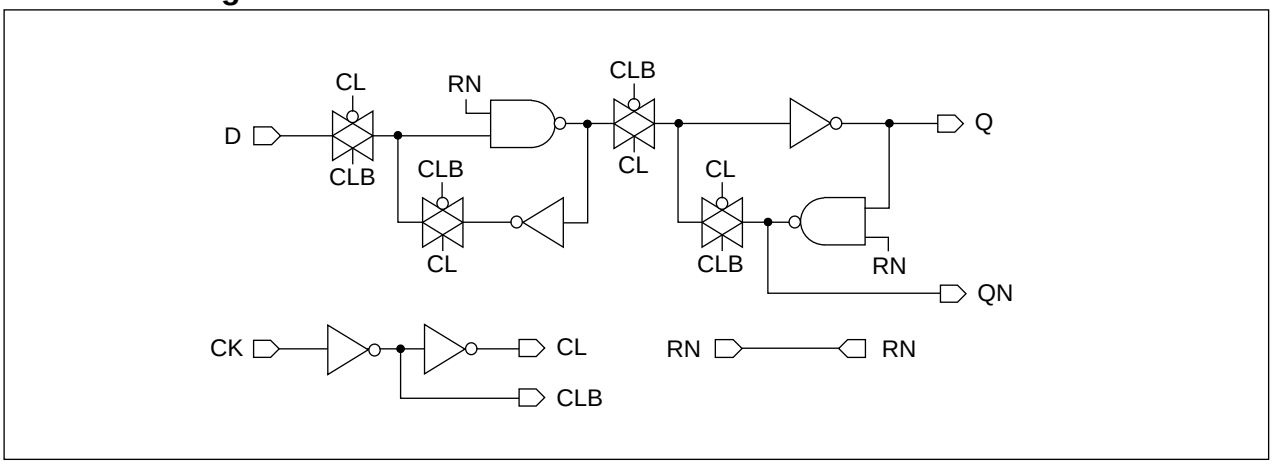
Truth Table

D	CK	RN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
YFD2			*YFD2D2*			*YFD2*	*YFD2D2*
D	CK	RN	D	CK	RN		
1.8	0.6	1.3	1.8	0.6	2.3	5.3	6.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		YFD2	YFD2D2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.87	0.93
Input Setup Time (D to CK)	t_{SU}	0.41	0.41
Input Hold Time (D to CK)	t_{HD}	0.44	0.44
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

YFD2

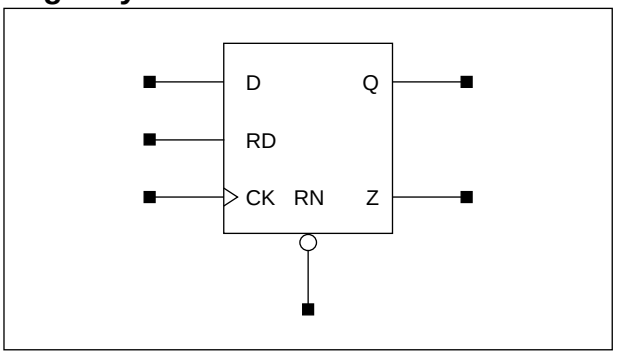
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.59	0.52 + 0.034*SL	0.53 + 0.030*SL	0.56 + 0.027*SL
	t_{PHL}	0.63	0.54 + 0.045*SL	0.56 + 0.038*SL	0.61 + 0.033*SL
	t_R	0.32	0.21 + 0.057*SL	0.21 + 0.057*SL	0.19 + 0.059*SL
	t_F	0.38	0.25 + 0.065*SL	0.25 + 0.063*SL	0.24 + 0.064*SL
RN to Q	t_{PHL}	0.67	0.58 + 0.045*SL	0.60 + 0.037*SL	0.64 + 0.033*SL
	t_F	0.40	0.28 + 0.059*SL	0.28 + 0.060*SL	0.23 + 0.064*SL
CK to QN	t_{PLH}	0.83	0.65 + 0.089*SL	0.67 + 0.082*SL	0.71 + 0.078*SL
	t_{PHL}	0.77	0.61 + 0.076*SL	0.63 + 0.072*SL	0.65 + 0.069*SL
	t_R	0.31	0.17 + 0.071*SL	0.16 + 0.073*SL	0.15 + 0.074*SL
	t_F	0.31	0.14 + 0.085*SL	0.14 + 0.085*SL	0.14 + 0.085*SL
RN to QN	t_{PLH}	0.18	0.12 + 0.033*SL	0.13 + 0.028*SL	0.13 + 0.028*SL
	t_R	0.28	0.18 + 0.052*SL	0.17 + 0.057*SL	0.24 + 0.050*SL

YFD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.61	0.58 + 0.019*SL	0.58 + 0.017*SL	0.61 + 0.014*SL
	t_{PHL}	0.69	0.63 + 0.027*SL	0.64 + 0.023*SL	0.69 + 0.018*SL
	t_R	0.29	0.24 + 0.024*SL	0.23 + 0.028*SL	0.22 + 0.028*SL
	t_F	0.38	0.32 + 0.029*SL	0.32 + 0.032*SL	0.32 + 0.032*SL
RN to Q	t_{PHL}	0.72	0.66 + 0.026*SL	0.68 + 0.022*SL	0.72 + 0.017*SL
	t_F	0.38	0.32 + 0.029*SL	0.32 + 0.029*SL	0.30 + 0.031*SL
CK to QN	t_{PLH}	0.82	0.72 + 0.049*SL	0.74 + 0.045*SL	0.79 + 0.040*SL
	t_{PHL}	0.75	0.66 + 0.042*SL	0.67 + 0.039*SL	0.70 + 0.036*SL
	t_R	0.22	0.15 + 0.035*SL	0.15 + 0.035*SL	0.14 + 0.036*SL
	t_F	0.21	0.13 + 0.042*SL	0.13 + 0.043*SL	0.12 + 0.043*SL
RN to QN	t_{PLH}	0.15	0.11 + 0.017*SL	0.12 + 0.014*SL	0.13 + 0.014*SL
	t_R	0.23	0.18 + 0.023*SL	0.17 + 0.026*SL	0.17 + 0.026*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

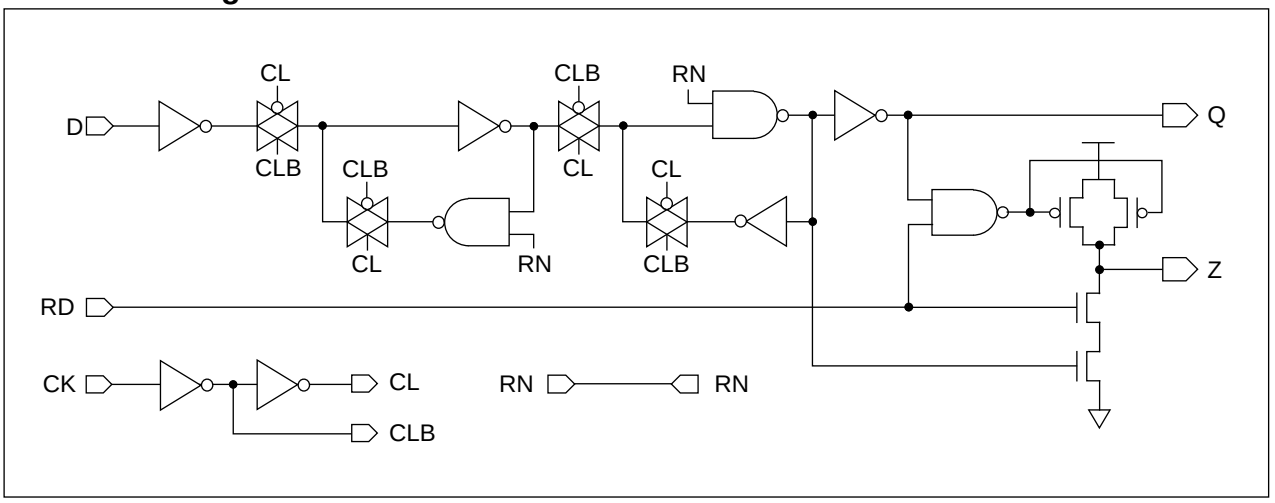
D	RD*	CK	RN	Q (n+1)	Z (n+1)
0	1	↑	1	0	0
1	1	↑	1	1	1
x	1	x	0	0	0
x	0	x	1	x	Hi-Z
x	1	↓	1	Q (n)	Z (n)

* RD is a tri-state enable pin.

Cell Data

Input Load (SL)								Output Load (SL)		Gate Count	
FD2T				*FD2TD2*				*FD2T*	*FD2TD2*	*FD2T*	*FD2TD2*
D	RD	CK	RN	D	RD	CK	RN	Z	Z		
0.6	1.1	0.6	1.1	0.6	1.3	0.6	1.1	1.4	2.3	7.3	8.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD2T	FD2TD2
Pulse Width Low (CK)	t_{PWL}	0.82	0.82
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Input Setup Time (D to CK)	t_{SU}	0.52	0.52
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.66	0.66

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD2T

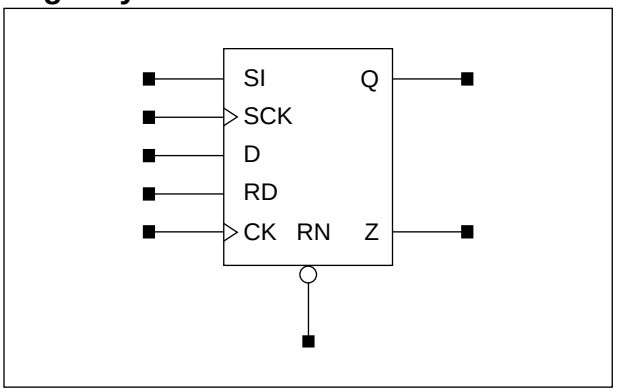
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.75	0.67 + 0.036*SL	0.69 + 0.029*SL	0.72 + 0.027*SL
	t_{PHL}	0.78	0.70 + 0.038*SL	0.72 + 0.034*SL	0.73 + 0.033*SL
	t_R	0.30	0.19 + 0.056*SL	0.19 + 0.056*SL	0.16 + 0.059*SL
	t_F	0.29	0.17 + 0.062*SL	0.17 + 0.062*SL	0.14 + 0.065*SL
RN to Q	t_{PHL}	0.41	0.34 + 0.038*SL	0.35 + 0.034*SL	0.36 + 0.033*SL
	t_F	0.28	0.16 + 0.062*SL	0.16 + 0.063*SL	0.13 + 0.065*SL
CK to Z	t_{PLH}	0.97	0.85 + 0.059*SL	0.88 + 0.048*SL	0.95 + 0.041*SL
	t_{PHL}	1.07	0.92 + 0.077*SL	0.94 + 0.070*SL	0.97 + 0.066*SL
	t_R	0.16	0.10 + 0.031*SL	0.10 + 0.030*SL	0.09 + 0.031*SL
	t_F	0.49	0.25 + 0.119*SL	0.28 + 0.109*SL	0.32 + 0.105*SL
RN to Z	t_{PHL}	0.70	0.55 + 0.077*SL	0.57 + 0.070*SL	0.61 + 0.066*SL
	t_F	0.49	0.25 + 0.119*SL	0.28 + 0.109*SL	0.32 + 0.105*SL
RD to Z	t_{PLH}	0.25	0.21 + 0.021*SL	0.22 + 0.016*SL	0.25 + 0.014*SL
	t_{PHL}	0.14	0.05 + 0.043*SL	0.07 + 0.038*SL	0.08 + 0.037*SL
	t_R	0.16	0.10 + 0.030*SL	0.10 + 0.029*SL	0.09 + 0.030*SL
	t_F	0.30	0.16 + 0.072*SL	0.15 + 0.077*SL	0.11 + 0.081*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.33	0.33 + 0.000*SL	0.32 + 0.000*SL	0.33 + 0.000*SL

FD2TD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.77	0.72 + 0.022*SL	0.74 + 0.017*SL	0.77 + 0.014*SL
	t_{PHL}	0.79	0.74 + 0.024*SL	0.75 + 0.020*SL	0.78 + 0.017*SL
	t_R	0.25	0.19 + 0.027*SL	0.19 + 0.027*SL	0.18 + 0.028*SL
	t_F	0.23	0.16 + 0.031*SL	0.17 + 0.030*SL	0.15 + 0.032*SL
RN to Q	t_{PHL}	0.42	0.37 + 0.024*SL	0.38 + 0.020*SL	0.41 + 0.017*SL
	t_F	0.22	0.16 + 0.032*SL	0.16 + 0.030*SL	0.14 + 0.032*SL
CK to Z	t_{PLH}	1.02	0.94 + 0.038*SL	0.97 + 0.030*SL	1.04 + 0.022*SL
	t_{PHL}	1.10	1.01 + 0.045*SL	1.03 + 0.039*SL	1.08 + 0.034*SL
	t_R	0.16	0.13 + 0.019*SL	0.13 + 0.016*SL	0.14 + 0.015*SL
	t_F	0.41	0.27 + 0.070*SL	0.31 + 0.059*SL	0.36 + 0.054*SL
RN to Z	t_{PHL}	0.73	0.64 + 0.045*SL	0.66 + 0.039*SL	0.70 + 0.034*SL
	t_F	0.42	0.28 + 0.069*SL	0.31 + 0.058*SL	0.35 + 0.054*SL
RD to Z	t_{PLH}	0.28	0.25 + 0.015*SL	0.26 + 0.011*SL	0.30 + 0.007*SL
	t_{PHL}	0.10	0.05 + 0.026*SL	0.07 + 0.021*SL	0.08 + 0.019*SL
	t_R	0.17	0.13 + 0.018*SL	0.14 + 0.015*SL	0.15 + 0.014*SL
	t_F	0.24	0.16 + 0.037*SL	0.17 + 0.037*SL	0.14 + 0.040*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.45	0.45 + 0.000*SL	0.45 + 0.000*SL	0.45 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

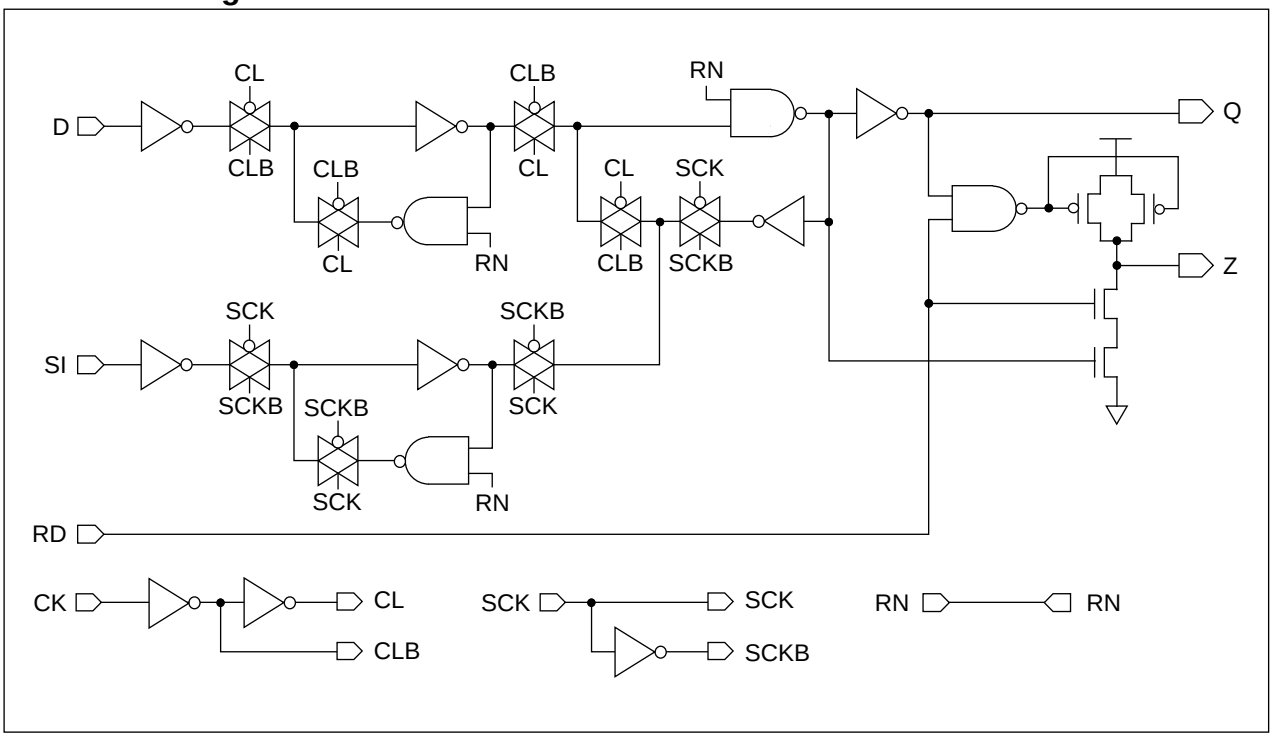
SI	SCK	D	RD	CK	RN	Q (n+1)	Z (n+1)
x	0	0	1	⎍	1	0	0
x	0	1	1	⎍	1	1	1
0	⎍	x	1	0	1	0	0
1	⎍	x	1	0	1	1	1
x	x	x	1	x	0	0	0
x	x	x	0	x	1	x	Hi-Z

* RD is a tri-state enable pin.

Cell Data

Input Load (SL)												Output Load (SL)		Gate Count	
FD2TCS						*FD2TCSD2*						*FD2TCS*	*FD2TCS D2*	*FD2TCS*	*FD2TCS D2*
SI	SCK	D	RD	CK	RN	SI	SCK	D	RD	CK	RN	Z	Z		
0.6	1.8	0.6	1.0	0.6	1.7	0.6	1.8	0.6	1.3	0.6	1.8	1.4	2.5	11.3	12.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD2TCS	FD2TCSD2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (SCK)	t_{PWL}	0.79	0.79
Pulse Width High (SCK)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Input Setup Time (D to CK)	t_{SU}	0.52	0.52
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.74	0.74
Input Hold Time (SI to SCK)	t_{HD}	0.33	0.33
Recovery Time (RN to CK)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.66	0.66
Recovery Time (RN to SCK)	t_{RC}	0.33	0.33
Input Hold Time (RN to SCK)	t_{HD}	0.49	0.66

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD2TCS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.75	0.68 + 0.035*SL	0.70 + 0.030*SL	0.72 + 0.027*SL
	t_{PHL}	0.77	0.69 + 0.039*SL	0.71 + 0.034*SL	0.72 + 0.033*SL
	t_R	0.30	0.18 + 0.057*SL	0.18 + 0.057*SL	0.16 + 0.059*SL
	t_F	0.29	0.16 + 0.062*SL	0.16 + 0.063*SL	0.14 + 0.065*SL
SCK to Q	t_{PLH}	0.79	0.71 + 0.037*SL	0.73 + 0.030*SL	0.76 + 0.027*SL
	t_{PHL}	0.67	0.60 + 0.039*SL	0.61 + 0.034*SL	0.62 + 0.033*SL
	t_R	0.32	0.21 + 0.054*SL	0.21 + 0.056*SL	0.18 + 0.059*SL
	t_F	0.30	0.17 + 0.060*SL	0.17 + 0.062*SL	0.14 + 0.065*SL
RN to Q	t_{PHL}	0.41	0.33 + 0.039*SL	0.34 + 0.035*SL	0.36 + 0.033*SL
	t_F	0.28	0.16 + 0.063*SL	0.16 + 0.063*SL	0.13 + 0.065*SL
CK to Z	t_{PLH}	0.97	0.86 + 0.059*SL	0.89 + 0.048*SL	0.95 + 0.041*SL
	t_{PHL}	1.07	0.91 + 0.077*SL	0.93 + 0.071*SL	0.97 + 0.066*SL
	t_R	0.16	0.10 + 0.032*SL	0.10 + 0.030*SL	0.09 + 0.031*SL
	t_F	0.49	0.26 + 0.118*SL	0.28 + 0.109*SL	0.32 + 0.105*SL
SCK to Z	t_{PLH}	1.01	0.89 + 0.060*SL	0.92 + 0.048*SL	0.99 + 0.041*SL
	t_{PHL}	0.97	0.81 + 0.077*SL	0.83 + 0.071*SL	0.87 + 0.066*SL
	t_R	0.16	0.10 + 0.030*SL	0.10 + 0.030*SL	0.09 + 0.031*SL
	t_F	0.49	0.25 + 0.120*SL	0.28 + 0.110*SL	0.32 + 0.105*SL
RN to Z	t_{PHL}	0.70	0.55 + 0.077*SL	0.57 + 0.070*SL	0.61 + 0.066*SL
	t_F	0.50	0.27 + 0.116*SL	0.29 + 0.108*SL	0.32 + 0.105*SL
RD to Z	t_{PLH}	0.24	0.20 + 0.022*SL	0.21 + 0.016*SL	0.24 + 0.014*SL
	t_{PHL}	0.14	0.05 + 0.043*SL	0.07 + 0.038*SL	0.07 + 0.037*SL
	t_R	0.17	0.11 + 0.029*SL	0.11 + 0.028*SL	0.10 + 0.030*SL
	t_F	0.30	0.16 + 0.073*SL	0.15 + 0.077*SL	0.11 + 0.081*SL
	t_{PLZ}	0.17	0.17 + 0.000*SL	0.17 + 0.000*SL	0.17 + 0.000*SL
	t_{PHZ}	0.33	0.33 + 0.000*SL	0.33 + 0.000*SL	0.33 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD2TCSD2

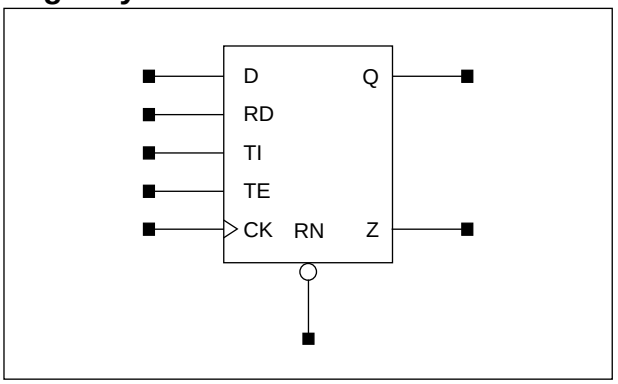
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.81	0.76 + 0.023*SL	0.78 + 0.017*SL	0.82 + 0.014*SL
	t_{PHL}	0.76	0.71 + 0.023*SL	0.72 + 0.020*SL	0.75 + 0.017*SL
	t_R	0.24	0.19 + 0.026*SL	0.19 + 0.027*SL	0.18 + 0.028*SL
	t_F	0.21	0.15 + 0.030*SL	0.15 + 0.031*SL	0.14 + 0.032*SL
SCK to Q	t_{PLH}	0.89	0.85 + 0.024*SL	0.86 + 0.018*SL	0.91 + 0.014*SL
	t_{PHL}	0.66	0.62 + 0.024*SL	0.63 + 0.019*SL	0.66 + 0.017*SL
	t_R	0.28	0.22 + 0.027*SL	0.23 + 0.026*SL	0.21 + 0.028*SL
	t_F	0.22	0.16 + 0.030*SL	0.16 + 0.031*SL	0.15 + 0.032*SL
RN to Q	t_{PHL}	0.43	0.38 + 0.024*SL	0.39 + 0.019*SL	0.42 + 0.017*SL
	t_F	0.22	0.16 + 0.032*SL	0.16 + 0.030*SL	0.14 + 0.032*SL
CK to Z	t_{PLH}	1.06	0.98 + 0.039*SL	1.00 + 0.030*SL	1.08 + 0.022*SL
	t_{PHL}	1.08	0.99 + 0.045*SL	1.00 + 0.039*SL	1.05 + 0.035*SL
	t_R	0.15	0.12 + 0.017*SL	0.12 + 0.016*SL	0.13 + 0.015*SL
	t_F	0.36	0.23 + 0.068*SL	0.25 + 0.061*SL	0.32 + 0.054*SL
SCK to Z	t_{PLH}	1.14	1.06 + 0.040*SL	1.09 + 0.030*SL	1.17 + 0.022*SL
	t_{PHL}	0.99	0.90 + 0.045*SL	0.91 + 0.039*SL	0.96 + 0.034*SL
	t_R	0.16	0.12 + 0.019*SL	0.13 + 0.015*SL	0.13 + 0.015*SL
	t_F	0.36	0.22 + 0.068*SL	0.24 + 0.061*SL	0.31 + 0.054*SL
RN to Z	t_{PHL}	0.74	0.66 + 0.044*SL	0.67 + 0.039*SL	0.71 + 0.034*SL
	t_F	0.36	0.22 + 0.067*SL	0.24 + 0.061*SL	0.30 + 0.054*SL
RD to Z	t_{PLH}	0.28	0.25 + 0.017*SL	0.27 + 0.011*SL	0.30 + 0.007*SL
	t_{PHL}	0.09	0.04 + 0.025*SL	0.05 + 0.021*SL	0.07 + 0.019*SL
	t_R	0.15	0.11 + 0.018*SL	0.12 + 0.016*SL	0.13 + 0.014*SL
	t_F	0.22	0.15 + 0.037*SL	0.15 + 0.037*SL	0.12 + 0.040*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.45	0.45 + 0.000*SL	0.45 + 0.000*SL	0.45 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

FD2TS/FD2TSD2

D Flip-Flop with Reset, Scan, Tri-State Output, 1X/2X Drive

Logic Symbol



Truth Table

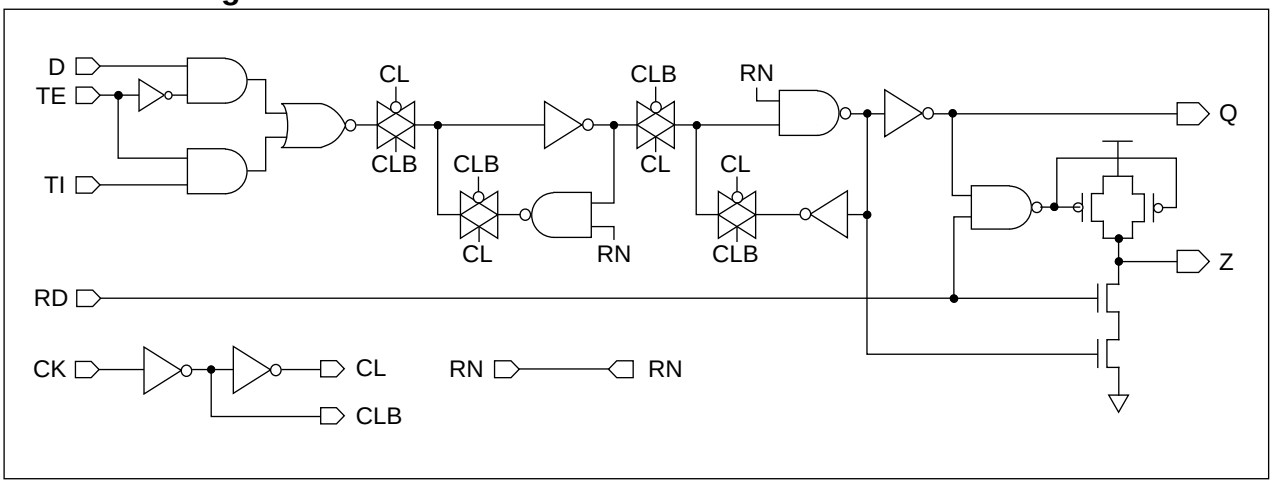
D	RD	TI	TE	CK	RN	Q (n+1)	Z (n+1)
0	1	x	0	↑	1	0	0
1	1	x	0	↑	1	1	1
x	1	0	1	↑	1	0	0
x	1	1	1	↑	1	1	1
x	1	x	x	x	0	0	0
x	0	x	x	x	1	x	Hi-Z
x	1	x	x	↓	1	Q (n)	Z (n)

* RD is a tri-state enable pin.

Cell Data

Input Load (SL)												Output Load (SL)		Gate Count	
FD2TS						*FD2TSD2*						*FD2TS*	*FD2TSD2*	*FD2TS*	*FD2TSD2*
D	RD	TI	TE	CK	RN	D	RD	TI	TE	CK	RN	Z	Z		
0.6	1.1	0.6	1.1	0.6	1.3	0.6	1.3	0.6	1.1	0.6	1.3	1.4	2.3	9.0	10.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD2TS	FD2TSD2
Pulse Width Low (CK)	t_{PWL}	0.85	0.85
Pulse Width High (CK)	t_{PWH}	0.77	0.77
Pulse Width Low (RN)	t_{PWL}	0.77	0.77
Input Setup Time (D to CK)	t_{SU}	0.71	0.71
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.71	0.71
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.33	0.33
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.71

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD2TS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.76	0.68 + 0.036*SL	0.70 + 0.029*SL	0.73 + 0.027*SL
	t_{PHL}	0.80	0.72 + 0.039*SL	0.73 + 0.034*SL	0.75 + 0.033*SL
	t_R	0.30	0.19 + 0.056*SL	0.19 + 0.057*SL	0.16 + 0.059*SL
	t_F	0.29	0.17 + 0.061*SL	0.16 + 0.062*SL	0.14 + 0.065*SL
RN to Q	t_{PHL}	0.41	0.34 + 0.038*SL	0.35 + 0.034*SL	0.36 + 0.033*SL
	t_F	0.28	0.16 + 0.062*SL	0.16 + 0.063*SL	0.13 + 0.065*SL
CK to Z	t_{PLH}	0.98	0.86 + 0.059*SL	0.89 + 0.048*SL	0.96 + 0.041*SL
	t_{PHL}	1.09	0.94 + 0.077*SL	0.95 + 0.071*SL	0.99 + 0.066*SL
	t_R	0.16	0.10 + 0.032*SL	0.10 + 0.030*SL	0.09 + 0.031*SL
	t_F	0.49	0.25 + 0.119*SL	0.28 + 0.110*SL	0.32 + 0.105*SL
RN to Z	t_{PHL}	0.70	0.55 + 0.077*SL	0.57 + 0.070*SL	0.61 + 0.066*SL
	t_F	0.49	0.26 + 0.118*SL	0.28 + 0.109*SL	0.32 + 0.105*SL
RD to Z	t_{PLH}	0.25	0.21 + 0.020*SL	0.22 + 0.016*SL	0.25 + 0.014*SL
	t_{PHL}	0.14	0.05 + 0.044*SL	0.07 + 0.038*SL	0.07 + 0.037*SL
	t_R	0.16	0.09 + 0.032*SL	0.10 + 0.029*SL	0.09 + 0.030*SL
	t_F	0.31	0.16 + 0.071*SL	0.15 + 0.077*SL	0.11 + 0.081*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.33	0.33 + 0.000*SL	0.33 + 0.000*SL	0.32 + 0.000*SL

FD2TSD2

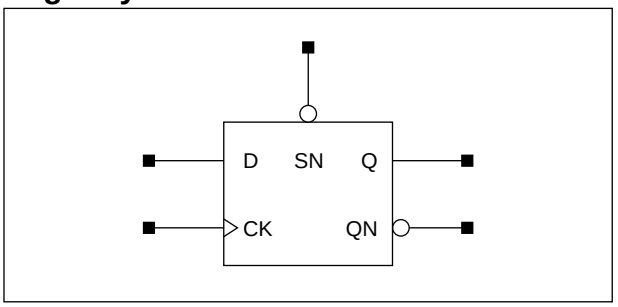
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.78	0.73 + 0.022*SL	0.75 + 0.017*SL	0.78 + 0.014*SL
	t_{PHL}	0.81	0.76 + 0.024*SL	0.77 + 0.020*SL	0.80 + 0.017*SL
	t_R	0.25	0.19 + 0.027*SL	0.19 + 0.027*SL	0.18 + 0.028*SL
	t_F	0.23	0.16 + 0.031*SL	0.17 + 0.030*SL	0.15 + 0.032*SL
RN to Q	t_{PHL}	0.42	0.37 + 0.024*SL	0.39 + 0.019*SL	0.41 + 0.017*SL
	t_F	0.22	0.15 + 0.032*SL	0.16 + 0.030*SL	0.14 + 0.032*SL
CK to Z	t_{PLH}	1.03	0.95 + 0.038*SL	0.98 + 0.030*SL	1.05 + 0.022*SL
	t_{PHL}	1.12	1.03 + 0.045*SL	1.05 + 0.039*SL	1.09 + 0.035*SL
	t_R	0.16	0.13 + 0.017*SL	0.13 + 0.016*SL	0.14 + 0.015*SL
	t_F	0.41	0.27 + 0.071*SL	0.31 + 0.059*SL	0.35 + 0.054*SL
RN to Z	t_{PHL}	0.73	0.64 + 0.045*SL	0.66 + 0.039*SL	0.70 + 0.034*SL
	t_F	0.42	0.27 + 0.071*SL	0.31 + 0.058*SL	0.35 + 0.054*SL
RD to Z	t_{PLH}	0.28	0.25 + 0.015*SL	0.26 + 0.011*SL	0.30 + 0.007*SL
	t_{PHL}	0.10	0.05 + 0.026*SL	0.06 + 0.021*SL	0.08 + 0.019*SL
	t_R	0.17	0.13 + 0.017*SL	0.14 + 0.015*SL	0.15 + 0.014*SL
	t_F	0.24	0.17 + 0.036*SL	0.17 + 0.037*SL	0.14 + 0.040*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.45	0.45 + 0.000*SL	0.45 + 0.000*SL	0.45 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

FD3/FD3D2

D Flip-Flop with Set, 1X/2X Drive

Logic Symbol



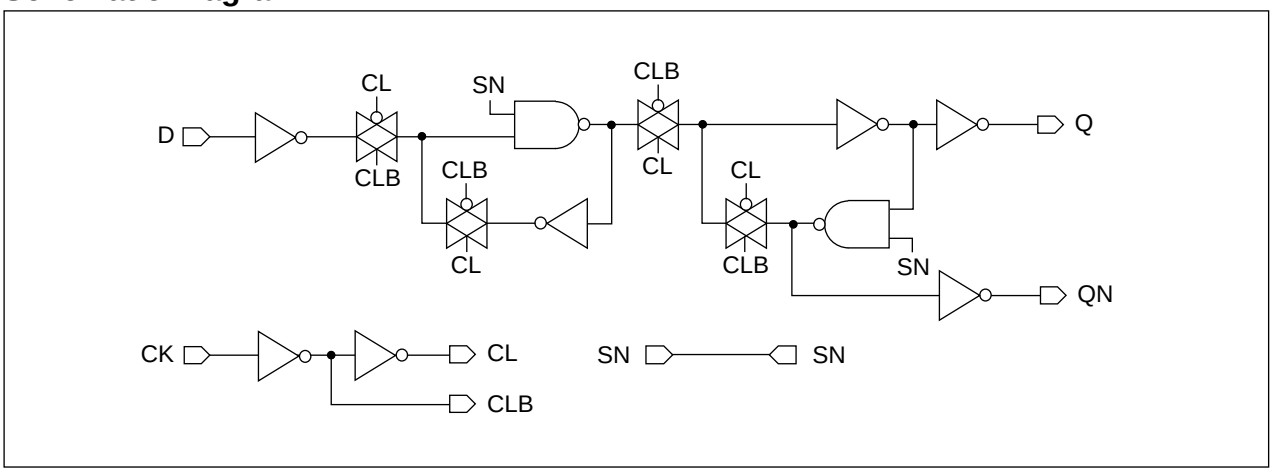
Truth Table

D	CK	SN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FD3			*FD3D2*			*FD3*	*FD3D2*
D	CK	SN	D	CK	SN		
0.6	0.6	1.1	0.6	0.6	1.1	6.7	7.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD3	FD3D2
Pulse Width Low (CK)	t_{PWL}	0.82	0.82
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (SN)	t_{PWL}	0.85	0.85
Input Setup Time (D to CK)	t_{SU}	0.55	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.57 + 0.030*SL	0.58 + 0.028*SL	0.59 + 0.027*SL
	t_{PHL}	0.75	0.67 + 0.039*SL	0.69 + 0.035*SL	0.70 + 0.033*SL
	t_R	0.22	0.12 + 0.054*SL	0.10 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
SN to Q	t_{PLH}	0.67	0.61 + 0.030*SL	0.62 + 0.027*SL	0.63 + 0.027*SL
	t_R	0.23	0.12 + 0.053*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
CK to QN	t_{PLH}	0.88	0.82 + 0.032*SL	0.83 + 0.028*SL	0.84 + 0.027*SL
	t_{PHL}	0.84	0.77 + 0.037*SL	0.77 + 0.034*SL	0.78 + 0.033*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.061*SL	0.10 + 0.063*SL	0.08 + 0.065*SL
SN to QN	t_{PHL}	0.35	0.27 + 0.038*SL	0.28 + 0.034*SL	0.30 + 0.033*SL
	t_F	0.23	0.10 + 0.062*SL	0.10 + 0.064*SL	0.08 + 0.065*SL

FD3D2

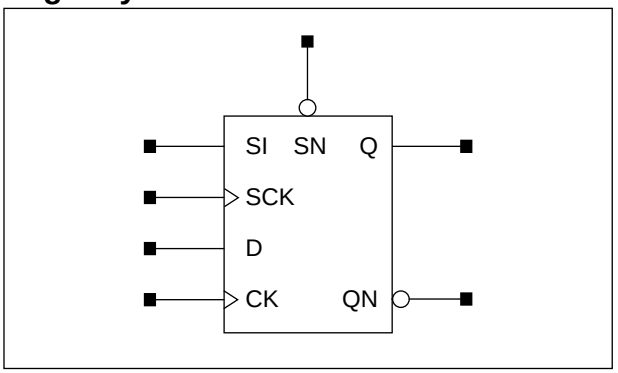
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.59 + 0.018*SL	0.60 + 0.015*SL	0.62 + 0.013*SL
	t_{PHL}	0.75	0.71 + 0.023*SL	0.72 + 0.019*SL	0.74 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.033*SL	0.13 + 0.030*SL	0.11 + 0.032*SL
SN to Q	t_{PLH}	0.68	0.64 + 0.018*SL	0.65 + 0.015*SL	0.67 + 0.013*SL
	t_R	0.17	0.12 + 0.025*SL	0.12 + 0.026*SL	0.10 + 0.029*SL
CK to QN	t_{PLH}	0.96	0.92 + 0.018*SL	0.93 + 0.015*SL	0.95 + 0.013*SL
	t_{PHL}	0.90	0.86 + 0.020*SL	0.87 + 0.018*SL	0.88 + 0.016*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SN to QN	t_{PHL}	0.35	0.31 + 0.023*SL	0.32 + 0.019*SL	0.34 + 0.017*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.10 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

FD3CS/FD3CSD2

D Flip-Flop with Set, Scan Clock, 1X/2X Drive

Logic Symbol



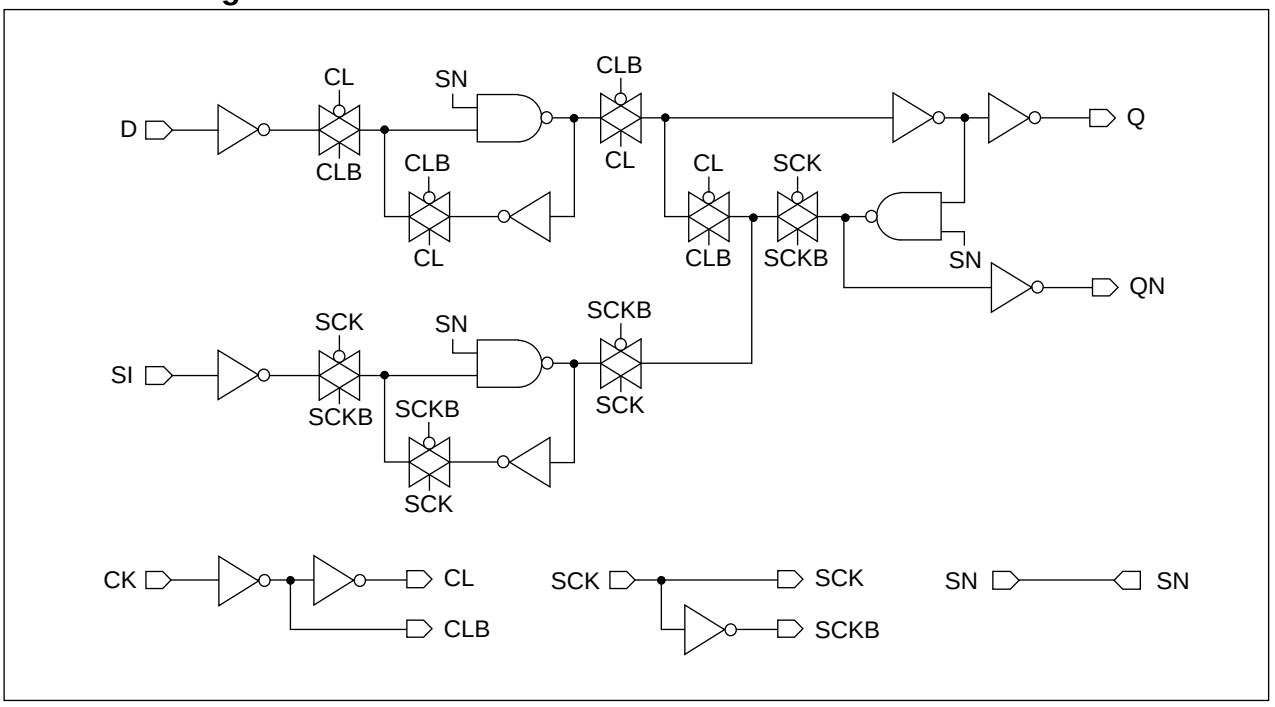
Truth Table

SI	SCK	D	CK	SN	Q (n+1)	QN (n+1)
x	0	0	↑	1	0	1
x	0	1	↑	1	1	0
0	↑	x	0	1	0	1
1	↑	x	0	1	1	0
x	x	x	x	0	1	0

Cell Data

Input Load (SL)										Gate Count	
FD3CS					*FD3CSD2*					*FD3CS*	*FD3CS D2*
SI	SCK	D	CK	SN	SI	SCK	D	CK	SN		
0.5	1.2	0.5	0.5	1.4	0.5	1.2	0.5	0.5	1.4	10.7	11.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD3CS	FD3CSD2
Pulse Width Low (CK)	t_{PWL}	0.82	0.82
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (SCK)	t_{PWL}	0.79	0.79
Pulse Width High (SCK)	t_{PWH}	0.79	0.79
Pulse Width Low (SN)	t_{PWL}	0.82	0.85
Input Setup Time (D to CK)	t_{SU}	0.55	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.76	0.76
Input Hold Time (SI to SCK)	t_{HD}	0.44	0.33
Recovery Time (SN to CK)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.44	0.44
Recovery Time (SN to SCK)	t_{RC}	0.44	0.44
Input Hold Time (SN to SCK)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD3CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.57 + 0.030*SL	0.58 + 0.027*SL	0.58 + 0.027*SL
	t_{PHL}	0.74	0.66 + 0.039*SL	0.68 + 0.035*SL	0.69 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.064*SL	0.10 + 0.065*SL
SCK to Q	t_{PLH}	0.65	0.59 + 0.032*SL	0.60 + 0.028*SL	0.61 + 0.027*SL
	t_{PHL}	0.67	0.59 + 0.040*SL	0.61 + 0.035*SL	0.62 + 0.033*SL
	t_R	0.25	0.14 + 0.054*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.25	0.12 + 0.063*SL	0.13 + 0.063*SL	0.10 + 0.065*SL
SN to Q	t_{PLH}	0.67	0.61 + 0.031*SL	0.62 + 0.027*SL	0.63 + 0.027*SL
	t_R	0.23	0.12 + 0.054*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
CK to QN	t_{PLH}	0.97	0.89 + 0.037*SL	0.91 + 0.031*SL	0.94 + 0.027*SL
	t_{PHL}	0.92	0.84 + 0.040*SL	0.85 + 0.036*SL	0.88 + 0.033*SL
	t_R	0.29	0.18 + 0.056*SL	0.18 + 0.056*SL	0.15 + 0.059*SL
	t_F	0.26	0.14 + 0.064*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
SCK to QN	t_{PLH}	0.80	0.74 + 0.032*SL	0.75 + 0.028*SL	0.76 + 0.027*SL
	t_{PHL}	0.87	0.80 + 0.036*SL	0.80 + 0.033*SL	0.81 + 0.033*SL
	t_R	0.24	0.12 + 0.057*SL	0.12 + 0.058*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
SN to QN	t_{PHL}	0.42	0.34 + 0.042*SL	0.36 + 0.036*SL	0.38 + 0.033*SL
	t_F	0.26	0.13 + 0.065*SL	0.13 + 0.063*SL	0.12 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

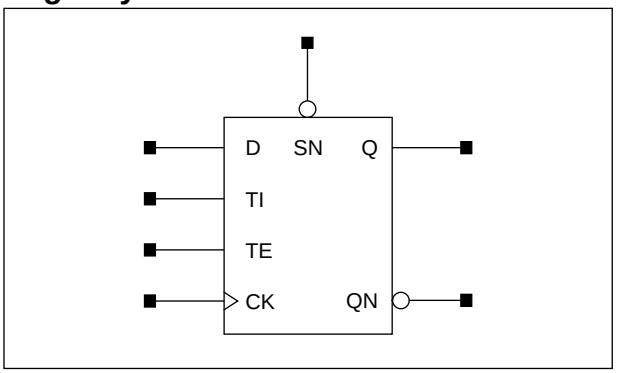
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD3CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.60 + 0.018*SL	0.61 + 0.015*SL	0.62 + 0.013*SL
	t_{PHL}	0.75	0.70 + 0.023*SL	0.71 + 0.019*SL	0.74 + 0.017*SL
	t_R	0.17	0.12 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SCK to Q	t_{PLH}	0.67	0.64 + 0.020*SL	0.65 + 0.015*SL	0.67 + 0.013*SL
	t_{PHL}	0.69	0.64 + 0.024*SL	0.65 + 0.019*SL	0.68 + 0.017*SL
	t_R	0.20	0.15 + 0.024*SL	0.15 + 0.025*SL	0.12 + 0.028*SL
	t_F	0.19	0.13 + 0.030*SL	0.13 + 0.031*SL	0.12 + 0.032*SL
SN to Q	t_{PLH}	0.68	0.64 + 0.018*SL	0.66 + 0.015*SL	0.67 + 0.013*SL
	t_R	0.17	0.12 + 0.025*SL	0.12 + 0.026*SL	0.10 + 0.029*SL
CK to QN	t_{PLH}	1.03	0.99 + 0.022*SL	1.00 + 0.017*SL	1.04 + 0.014*SL
	t_{PHL}	0.98	0.93 + 0.024*SL	0.95 + 0.019*SL	0.97 + 0.017*SL
	t_R	0.25	0.19 + 0.027*SL	0.19 + 0.027*SL	0.18 + 0.028*SL
	t_F	0.21	0.15 + 0.031*SL	0.15 + 0.031*SL	0.14 + 0.032*SL
SCK to QN	t_{PLH}	0.88	0.85 + 0.017*SL	0.85 + 0.015*SL	0.87 + 0.013*SL
	t_{PHL}	0.96	0.92 + 0.019*SL	0.92 + 0.017*SL	0.93 + 0.016*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.030*SL	0.11 + 0.032*SL
SN to QN	t_{PHL}	0.42	0.37 + 0.025*SL	0.38 + 0.020*SL	0.42 + 0.017*SL
	t_F	0.20	0.14 + 0.031*SL	0.14 + 0.031*SL	0.13 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Logic Symbol



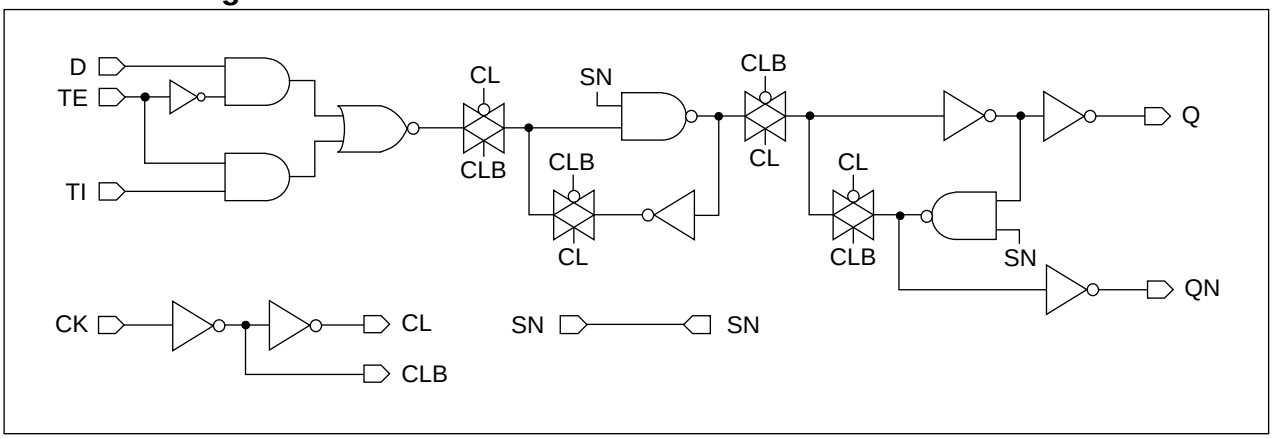
Truth Table

D	TI	TE	CK	SN	Q (n+1)	QN (n+1)
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	1	0
x	x	x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
FD3S					*FD3SD2*					*FD3S*	*FD3SD2*
D	TI	TE	CK	SN	D	TI	TE	CK	SN		
0.6	0.6	1.1	0.6	1.3	0.6	0.6	1.1	0.6	1.3	8.3	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD3S	FD3SD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87
Pulse Width High (CK)	t_{PWH}	0.77	0.77
Pulse Width Low (SN)	t_{PWL}	0.85	0.85
Input Setup Time (D to CK)	t_{SU}	0.74	0.74
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.74	0.74
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.79	0.79
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD3S

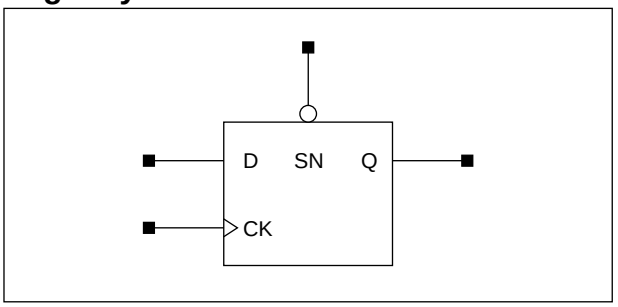
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.58 + 0.030*SL	0.59 + 0.028*SL	0.60 + 0.027*SL
	t_{PHL}	0.77	0.69 + 0.039*SL	0.71 + 0.035*SL	0.72 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
SN to Q	t_{PLH}	0.67	0.61 + 0.030*SL	0.62 + 0.027*SL	0.63 + 0.027*SL
	t_R	0.23	0.12 + 0.054*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
CK to QN	t_{PLH}	0.90	0.84 + 0.032*SL	0.85 + 0.028*SL	0.86 + 0.027*SL
	t_{PHL}	0.85	0.78 + 0.036*SL	0.78 + 0.034*SL	0.79 + 0.033*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.11 + 0.063*SL	0.08 + 0.065*SL
SN to QN	t_{PHL}	0.35	0.27 + 0.038*SL	0.28 + 0.034*SL	0.30 + 0.033*SL
	t_F	0.23	0.10 + 0.062*SL	0.10 + 0.064*SL	0.08 + 0.065*SL

FD3SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.61 + 0.018*SL	0.62 + 0.015*SL	0.63 + 0.013*SL
	t_{PHL}	0.77	0.73 + 0.023*SL	0.74 + 0.019*SL	0.76 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SN to Q	t_{PLH}	0.68	0.64 + 0.018*SL	0.65 + 0.015*SL	0.67 + 0.013*SL
	t_R	0.17	0.12 + 0.026*SL	0.12 + 0.026*SL	0.09 + 0.029*SL
CK to QN	t_{PLH}	0.98	0.94 + 0.018*SL	0.95 + 0.015*SL	0.97 + 0.013*SL
	t_{PHL}	0.91	0.87 + 0.020*SL	0.88 + 0.018*SL	0.89 + 0.016*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SN to QN	t_{PHL}	0.35	0.31 + 0.023*SL	0.32 + 0.019*SL	0.34 + 0.017*SL
	t_F	0.17	0.10 + 0.033*SL	0.11 + 0.031*SL	0.10 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



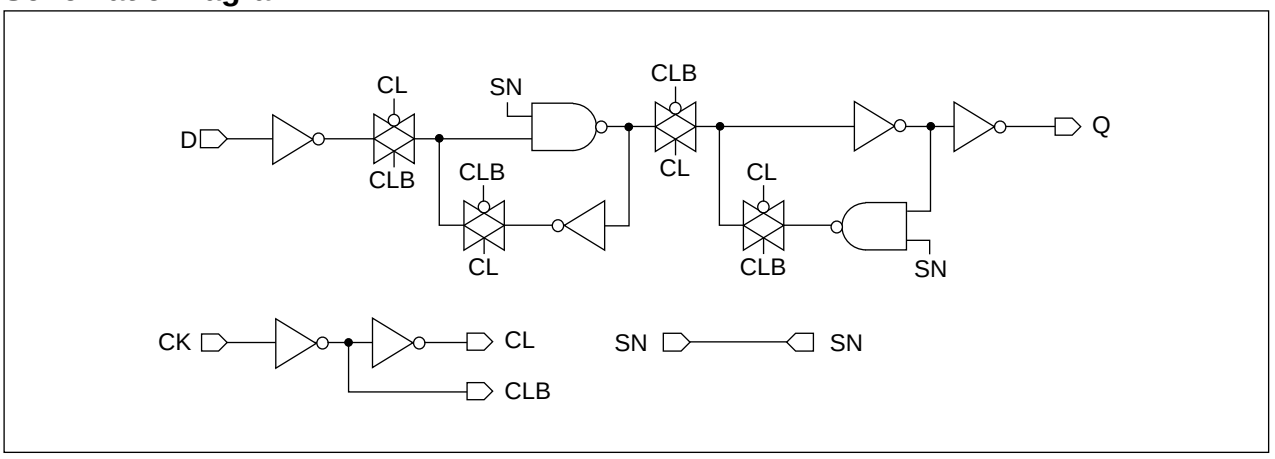
Truth Table

D	CK	SN	Q (n+1)
0	↑	1	0
1	↑	1	1
x	x	0	1
x	↓	x	Q (n)

Cell Data

Input Load (SL)						Gate Count	
FD3Q			*FD3QD2*			*FD3Q*	*FD3QD2*
D	CK	SN	D	CK	SN		
0.6	0.6	0.9	0.6	0.6	0.9	6.3	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD3Q	FD3QD2
Pulse Width Low (CK)	t_{PWL}	0.82	0.82
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (SN)	t_{PWL}	0.85	0.85
Input Setup Time (D to CK)	t_{SU}	0.55	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD3Q

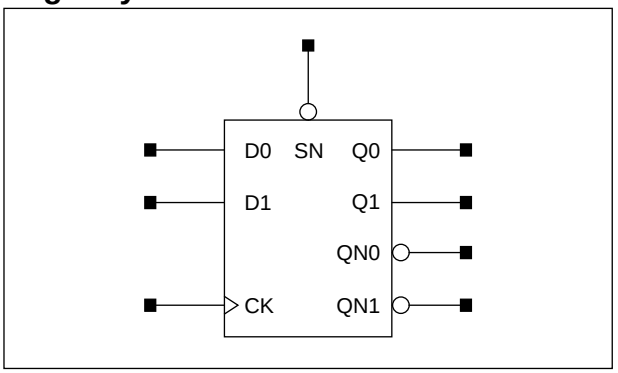
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.57 + 0.030*SL	0.57 + 0.027*SL	0.58 + 0.027*SL
	t_{PHL}	0.74	0.66 + 0.039*SL	0.67 + 0.034*SL	0.68 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
SN to Q	t_{PLH}	0.66	0.60 + 0.030*SL	0.61 + 0.027*SL	0.62 + 0.027*SL
	t_R	0.22	0.12 + 0.053*SL	0.11 + 0.057*SL	0.08 + 0.060*SL

FD3QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.59 + 0.018*SL	0.60 + 0.015*SL	0.62 + 0.013*SL
	t_{PHL}	0.74	0.69 + 0.023*SL	0.70 + 0.019*SL	0.73 + 0.017*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SN to Q	t_{PLH}	0.67	0.63 + 0.017*SL	0.64 + 0.014*SL	0.66 + 0.013*SL
	t_R	0.17	0.12 + 0.025*SL	0.12 + 0.026*SL	0.09 + 0.029*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

Dn	CK	SN	Qn (n+1)	QNn (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
Dn	CK	SN	
0.6	0.6	2.3	12.3

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (CK)	t_{PWL}	0.98
Pulse Width High (CK)	t_{PWH}	0.79
Pulse Width Low (SN)	t_{PWL}	0.85
Input Setup Time (D0 to CK)	t_{SU}	0.46
Input Hold Time (D0 to CK)	t_{HD}	0.33
Input Setup Time (D1 to CK)	t_{SU}	0.45
Input Hold Time (D1 to CK)	t_{HD}	0.33
Recovery Time (SN)	t_{RC}	0.33
Input Hold Time (SN to CK)	t_{HD}	0.60

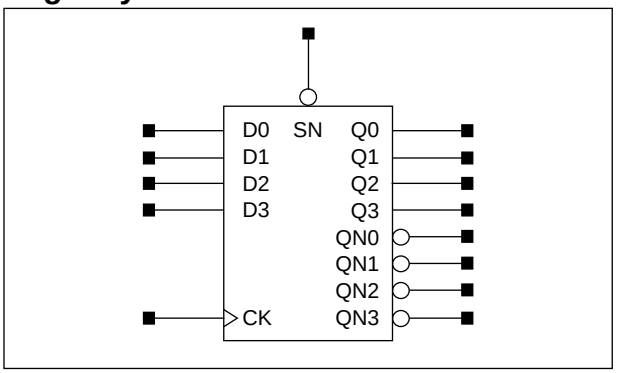
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.72	0.66 + 0.030*SL	0.67 + 0.028*SL	0.67 + 0.027*SL
	t_{PHL}	0.95	0.87 + 0.039*SL	0.88 + 0.035*SL	0.90 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.063*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
SN to Q0	t_{PLH}	0.68	0.62 + 0.030*SL	0.62 + 0.027*SL	0.63 + 0.027*SL
	t_R	0.23	0.12 + 0.053*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
CK to Q1	t_{PLH}	0.71	0.65 + 0.030*SL	0.66 + 0.028*SL	0.67 + 0.027*SL
	t_{PHL}	0.95	0.87 + 0.039*SL	0.88 + 0.035*SL	0.90 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
SN to Q1	t_{PLH}	0.67	0.61 + 0.031*SL	0.62 + 0.027*SL	0.62 + 0.027*SL
	t_R	0.23	0.13 + 0.051*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
CK to QN0	t_{PLH}	1.09	1.02 + 0.032*SL	1.03 + 0.028*SL	1.05 + 0.027*SL
	t_{PHL}	0.93	0.86 + 0.036*SL	0.86 + 0.034*SL	0.87 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.11 + 0.063*SL	0.08 + 0.065*SL
SN to QN0	t_{PHL}	0.35	0.28 + 0.038*SL	0.29 + 0.034*SL	0.30 + 0.033*SL
	t_F	0.23	0.10 + 0.063*SL	0.10 + 0.064*SL	0.08 + 0.065*SL
CK to QN1	t_{PLH}	1.08	1.02 + 0.032*SL	1.03 + 0.028*SL	1.04 + 0.027*SL
	t_{PHL}	0.92	0.85 + 0.037*SL	0.86 + 0.033*SL	0.86 + 0.033*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.063*SL	0.11 + 0.063*SL	0.08 + 0.065*SL
SN to QN1	t_{PHL}	0.35	0.27 + 0.039*SL	0.29 + 0.034*SL	0.30 + 0.033*SL
	t_F	0.23	0.10 + 0.064*SL	0.10 + 0.064*SL	0.08 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

Dn	CK	SN	Qn (n+1)	QNn (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
Dn	CK	SN	
0.6	0.6	4.8	23.7

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (CK)	t_{PWL}	1.50
Pulse Width High (CK)	t_{PWH}	0.96
Pulse Width Low (SN)	t_{PWL}	0.85
Input Setup Time (D0 to CK)	t_{SU}	0.36
Input Hold Time (D0 to CK)	t_{HD}	0.55
Input Setup Time (D1 to CK)	t_{SU}	0.36
Input Hold Time (D1 to CK)	t_{HD}	0.55
Input Setup Time (D2 to CK)	t_{SU}	0.36
Input Hold Time (D2 to CK)	t_{HD}	0.55
Input Setup Time (D3 to CK)	t_{SU}	0.36
Input Hold Time (D3 to CK)	t_{HD}	0.55
Recovery Time (SN)	t_{RC}	0.33
Input Hold Time (SN to CK)	t_{HD}	0.87

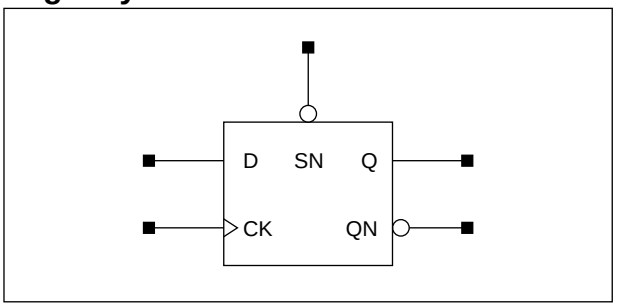
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.86	0.80 + 0.030*SL	0.81 + 0.028*SL	0.81 + 0.027*SL
	t_{PHL}	1.30	1.22 + 0.039*SL	1.23 + 0.035*SL	1.25 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
SN to Q0	t_{PLH}	0.67	0.61 + 0.031*SL	0.62 + 0.027*SL	0.62 + 0.027*SL
	t_R	0.23	0.13 + 0.052*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
CK to Q1	t_{PLH}	0.86	0.80 + 0.030*SL	0.81 + 0.028*SL	0.81 + 0.027*SL
	t_{PHL}	1.30	1.22 + 0.039*SL	1.23 + 0.035*SL	1.25 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
SN to Q1	t_{PLH}	0.67	0.61 + 0.031*SL	0.62 + 0.027*SL	0.62 + 0.027*SL
	t_R	0.23	0.13 + 0.052*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
CK to Q2	t_{PLH}	0.86	0.80 + 0.030*SL	0.81 + 0.028*SL	0.81 + 0.027*SL
	t_{PHL}	1.30	1.22 + 0.039*SL	1.23 + 0.035*SL	1.25 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
SN to Q2	t_{PLH}	0.67	0.61 + 0.031*SL	0.62 + 0.027*SL	0.62 + 0.027*SL
	t_R	0.23	0.13 + 0.052*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
CK to Q3	t_{PLH}	0.86	0.80 + 0.030*SL	0.80 + 0.028*SL	0.81 + 0.027*SL
	t_{PHL}	1.29	1.22 + 0.039*SL	1.23 + 0.035*SL	1.24 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
SN to Q3	t_{PLH}	0.67	0.61 + 0.031*SL	0.62 + 0.027*SL	0.62 + 0.027*SL
	t_R	0.23	0.13 + 0.052*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
CK to QN0	t_{PLH}	1.43	1.37 + 0.032*SL	1.38 + 0.028*SL	1.39 + 0.027*SL
	t_{PHL}	1.07	0.99 + 0.037*SL	1.00 + 0.034*SL	1.01 + 0.033*SL
	t_R	0.24	0.12 + 0.057*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.11 + 0.063*SL	0.08 + 0.065*SL
SN to QN0	t_{PHL}	0.35	0.28 + 0.038*SL	0.29 + 0.034*SL	0.30 + 0.033*SL
	t_F	0.23	0.10 + 0.063*SL	0.10 + 0.064*SL	0.08 + 0.065*SL
CK to QN1	t_{PLH}	1.43	1.37 + 0.032*SL	1.38 + 0.028*SL	1.39 + 0.027*SL
	t_{PHL}	1.07	0.99 + 0.037*SL	1.00 + 0.034*SL	1.01 + 0.033*SL
	t_R	0.24	0.12 + 0.057*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.11 + 0.063*SL	0.08 + 0.065*SL
SN to QN1	t_{PHL}	0.35	0.28 + 0.038*SL	0.29 + 0.034*SL	0.30 + 0.033*SL
	t_F	0.23	0.10 + 0.063*SL	0.10 + 0.064*SL	0.08 + 0.065*SL
CK to QN2	t_{PLH}	1.43	1.37 + 0.032*SL	1.38 + 0.028*SL	1.39 + 0.027*SL
	t_{PHL}	1.07	0.99 + 0.037*SL	1.00 + 0.034*SL	1.01 + 0.033*SL
	t_R	0.24	0.12 + 0.057*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.11 + 0.063*SL	0.08 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Logic Symbol



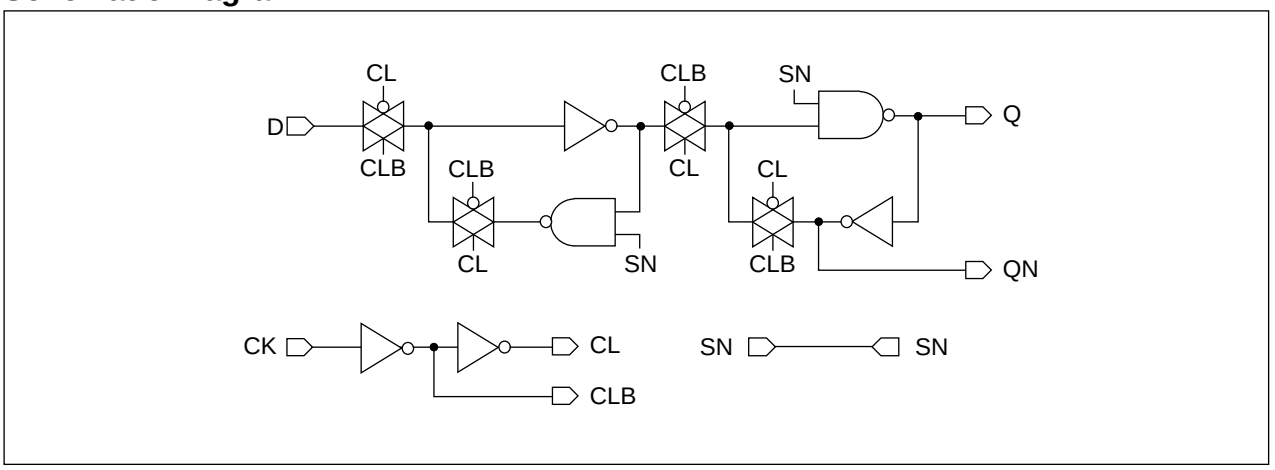
Truth Table

D	CK	SN	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0
x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
YFD3			*YFD3D2*			*YFD3*	*YFD3D2*
D	CK	SN	D	CK	SN		
1.9	0.6	1.3	1.9	0.6	2.5	5.0	6.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		YFD3	YFD3D2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (SN)	t_{PWL}	0.79	0.79
Input Setup Time (D to CK)	t_{SU}	0.38	0.38
Input Hold Time (D to CK)	t_{HD}	0.44	0.44
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.66	0.60

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

YFD3

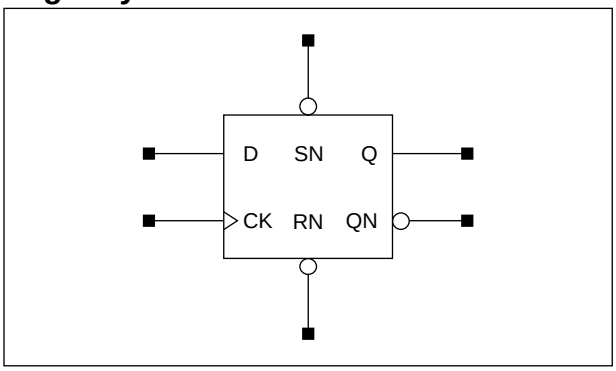
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.58	0.52 + 0.030*SL	0.52 + 0.029*SL	0.53 + 0.028*SL
	t_{PHL}	0.63	0.54 + 0.041*SL	0.55 + 0.039*SL	0.56 + 0.037*SL
	t_R	0.33	0.22 + 0.055*SL	0.21 + 0.060*SL	0.18 + 0.062*SL
	t_F	0.43	0.29 + 0.070*SL	0.27 + 0.076*SL	0.23 + 0.080*SL
SN to Q	t_{PLH}	0.20	0.14 + 0.030*SL	0.15 + 0.028*SL	0.26 + 0.016*SL
	t_R	0.32	0.22 + 0.051*SL	0.26 + 0.037*SL	0.33 + 0.029*SL
CK to QN	t_{PLH}	0.79	0.62 + 0.088*SL	0.62 + 0.085*SL	0.63 + 0.084*SL
	t_{PHL}	0.75	0.59 + 0.077*SL	0.60 + 0.075*SL	0.60 + 0.074*SL
	t_R	0.27	0.12 + 0.074*SL	0.12 + 0.075*SL	0.11 + 0.076*SL
	t_F	0.24	0.09 + 0.076*SL	0.09 + 0.076*SL	0.09 + 0.076*SL
SN to QN	t_{PHL}	0.36	0.21 + 0.076*SL	0.23 + 0.070*SL	0.36 + 0.056*SL
	t_F	0.24	0.09 + 0.073*SL	0.10 + 0.069*SL	0.11 + 0.069*SL

YFD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.59	0.56 + 0.017*SL	0.56 + 0.015*SL	0.58 + 0.014*SL
	t_{PHL}	0.73	0.67 + 0.028*SL	0.68 + 0.024*SL	0.73 + 0.020*SL
	t_R	0.28	0.23 + 0.026*SL	0.22 + 0.027*SL	0.20 + 0.030*SL
	t_F	0.45	0.38 + 0.037*SL	0.37 + 0.038*SL	0.36 + 0.039*SL
SN to Q	t_{PLH}	0.17	0.14 + 0.015*SL	0.15 + 0.014*SL	0.17 + 0.011*SL
	t_R	0.28	0.24 + 0.020*SL	0.23 + 0.026*SL	0.33 + 0.015*SL
CK to QN	t_{PLH}	0.84	0.74 + 0.051*SL	0.75 + 0.047*SL	0.80 + 0.042*SL
	t_{PHL}	0.70	0.62 + 0.040*SL	0.63 + 0.038*SL	0.64 + 0.037*SL
	t_R	0.20	0.13 + 0.035*SL	0.13 + 0.036*SL	0.12 + 0.037*SL
	t_F	0.16	0.08 + 0.037*SL	0.08 + 0.037*SL	0.08 + 0.038*SL
SN to QN	t_{PHL}	0.28	0.21 + 0.038*SL	0.21 + 0.037*SL	0.27 + 0.030*SL
	t_F	0.16	0.09 + 0.036*SL	0.08 + 0.037*SL	0.12 + 0.034*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



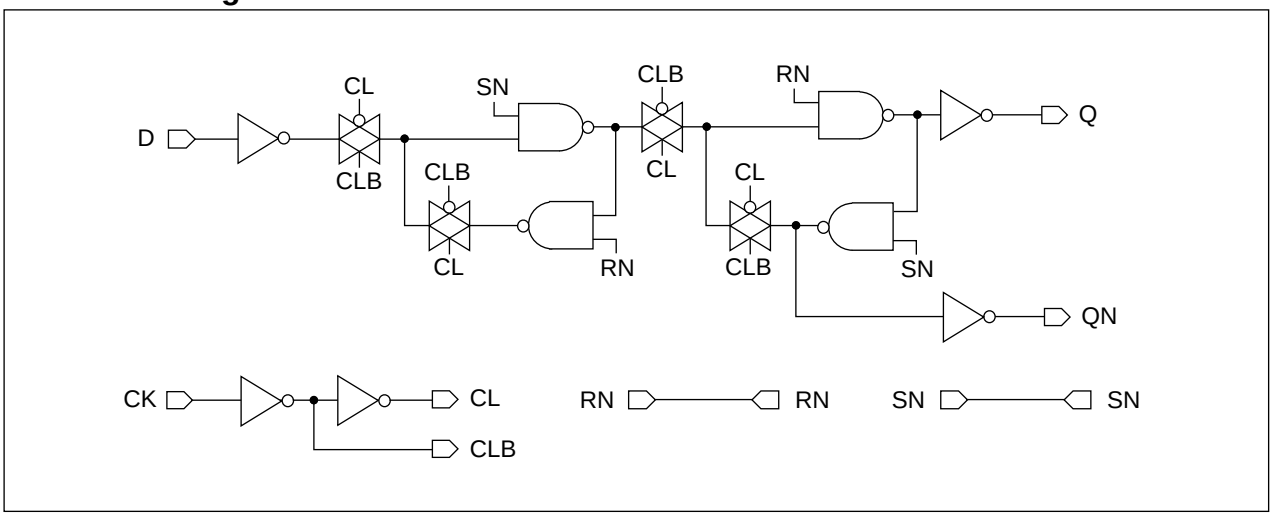
Truth Table

D	CK	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
FD4				*FD4D2*				*FD4*	*FD4D2*
D	CK	RN	SN	D	CK	RN	SN		
0.6	0.6	1.1	1.1	0.6	0.6	1.1	1.1	7.7	8.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD4	FD4D2
Pulse Width Low (CK)	t_{PWL}	0.85	0.85
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Pulse Width Low (SN)	t_{PWL}	0.85	0.87
Input Setup Time (D to CK)	t_{SU}	0.55	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.71
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD4

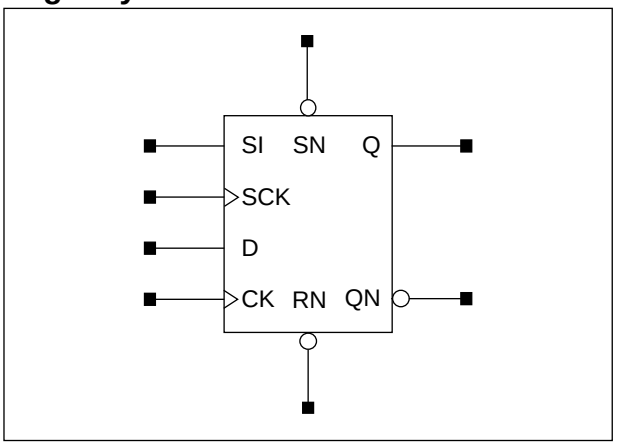
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.70	0.63 + 0.034*SL	0.64 + 0.029*SL	0.66 + 0.027*SL
	t_{PHL}	0.78	0.70 + 0.040*SL	0.72 + 0.035*SL	0.73 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.13 + 0.058*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q	t_{PLH}	0.33	0.26 + 0.034*SL	0.28 + 0.028*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.064*SL	0.11 + 0.064*SL	0.09 + 0.065*SL
SN to Q	t_{PLH}	0.73	0.66 + 0.034*SL	0.67 + 0.029*SL	0.69 + 0.027*SL
	t_R	0.25	0.15 + 0.054*SL	0.14 + 0.057*SL	0.11 + 0.060*SL
CK to QN	t_{PLH}	0.92	0.86 + 0.033*SL	0.87 + 0.028*SL	0.88 + 0.027*SL
	t_{PHL}	0.92	0.85 + 0.036*SL	0.86 + 0.034*SL	0.87 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to QN	t_{PLH}	0.51	0.45 + 0.033*SL	0.46 + 0.028*SL	0.47 + 0.027*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
SN to QN	t_{PLH}	0.33	0.26 + 0.033*SL	0.27 + 0.028*SL	0.29 + 0.027*SL
	t_{PHL}	0.36	0.28 + 0.038*SL	0.29 + 0.034*SL	0.30 + 0.033*SL
	t_R	0.24	0.12 + 0.057*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.10 + 0.062*SL	0.10 + 0.064*SL	0.08 + 0.065*SL

FD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.70	0.66 + 0.021*SL	0.67 + 0.017*SL	0.70 + 0.013*SL
	t_{PHL}	0.78	0.74 + 0.024*SL	0.75 + 0.019*SL	0.78 + 0.017*SL
	t_R	0.20	0.15 + 0.025*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.19	0.13 + 0.030*SL	0.13 + 0.031*SL	0.12 + 0.032*SL
RN to Q	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.34 + 0.013*SL
	t_{PHL}	0.36	0.32 + 0.023*SL	0.33 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.14 + 0.025*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.11 + 0.032*SL
SN to Q	t_{PLH}	0.74	0.69 + 0.021*SL	0.71 + 0.017*SL	0.74 + 0.013*SL
	t_R	0.21	0.15 + 0.027*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
CK to QN	t_{PLH}	0.99	0.96 + 0.018*SL	0.97 + 0.016*SL	0.99 + 0.013*SL
	t_{PHL}	1.02	0.98 + 0.019*SL	0.98 + 0.017*SL	0.99 + 0.016*SL
	t_R	0.20	0.14 + 0.026*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.19	0.13 + 0.031*SL	0.13 + 0.030*SL	0.12 + 0.032*SL
RN to QN	t_{PLH}	0.58	0.54 + 0.018*SL	0.55 + 0.015*SL	0.57 + 0.013*SL
	t_R	0.19	0.15 + 0.025*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
SN to QN	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.34 + 0.013*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.13 + 0.027*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.10 + 0.032*SL

*Group1 : SL < 3. *Group2 : 3 ≦ SL ≦ 10. *Group3 : 10 < SL

Logic Symbol



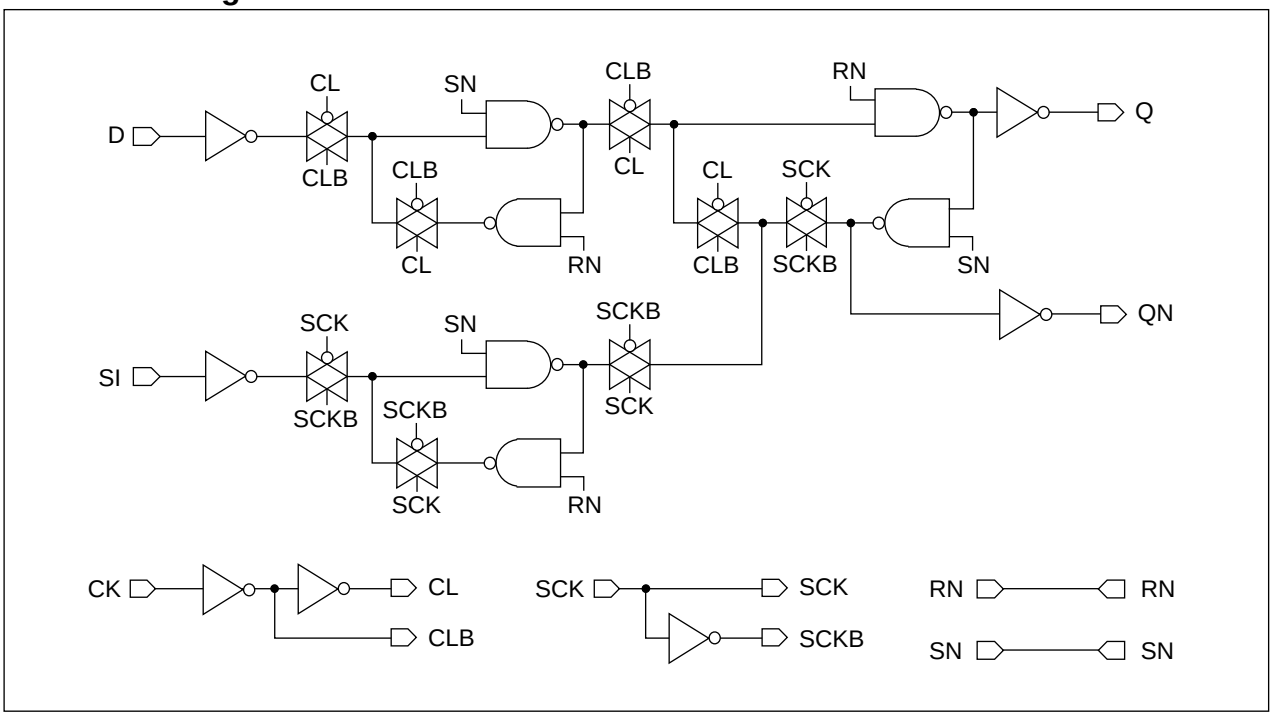
Truth Table

SI	SCK	D	CK	RN	SN	Q (n+1)	QN (n+1)
x	0	0	⎍	1	1	0	1
x	0	1	⎍	1	1	1	0
0	⎍	x	0	1	1	0	1
1	⎍	x	0	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0

Cell Data

Input Load (SL)						Gate Count
FD4CS						*FD4CS*
SI	SCK	D	CK	RN	SN	
0.5	1.2	0.5	0.5	1.4	1.4	12.3
FD4CSD2						*FD4CSD2*
SI	SCK	D	CK	RN	SN	
0.5	1.2	0.5	0.5	1.4	1.4	12.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD4CS	FD4CSD2
Pulse Width Low (CK)	t_{PWL}	0.85	0.85
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (SCK)	t_{PWL}	0.79	0.79
Pulse Width High (SCK)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.87	0.87
Pulse Width Low (SN)	t_{PWL}	0.79	0.79
Input Setup Time (D to CK)	t_{SU}	0.35	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.79	0.79
Input Hold Time (SI to SCK)	t_{HD}	0.33	0.33
Recovery Time (RN to CK)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.71
Recovery Time (RN to SCK)	t_{RC}	0.33	0.33
Input Hold Time (RN to SCK)	t_{HD}	0.55	0.55
Recovery Time (SN to CK)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.44	0.44
Recovery Time (SN to SCK)	t_{RC}	0.46	0.46
Input Hold Time (SN to SCK)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD4CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.72	0.65 + 0.034*SL	0.67 + 0.029*SL	0.69 + 0.027*SL
	t_{PHL}	0.76	0.68 + 0.040*SL	0.69 + 0.035*SL	0.71 + 0.033*SL
	t_R	0.25	0.14 + 0.056*SL	0.14 + 0.058*SL	0.12 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
SCK to Q	t_{PLH}	0.77	0.70 + 0.035*SL	0.72 + 0.030*SL	0.75 + 0.027*SL
	t_{PHL}	0.68	0.60 + 0.040*SL	0.61 + 0.035*SL	0.63 + 0.033*SL
	t_R	0.28	0.17 + 0.055*SL	0.17 + 0.056*SL	0.14 + 0.059*SL
	t_F	0.25	0.13 + 0.065*SL	0.13 + 0.062*SL	0.10 + 0.065*SL
SN to Q	t_{PLH}	0.77	0.70 + 0.034*SL	0.71 + 0.029*SL	0.73 + 0.027*SL
	t_R	0.26	0.15 + 0.055*SL	0.14 + 0.056*SL	0.11 + 0.060*SL
RN to Q	t_{PLH}	0.32	0.25 + 0.034*SL	0.26 + 0.029*SL	0.28 + 0.027*SL
	t_{PHL}	0.39	0.31 + 0.039*SL	0.32 + 0.035*SL	0.34 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.13 + 0.057*SL	0.11 + 0.060*SL
	t_F	0.24	0.12 + 0.064*SL	0.12 + 0.064*SL	0.10 + 0.065*SL
CK to QN	t_{PLH}	0.98	0.91 + 0.038*SL	0.93 + 0.031*SL	0.96 + 0.027*SL
	t_{PHL}	1.03	0.95 + 0.040*SL	0.96 + 0.035*SL	0.98 + 0.033*SL
	t_R	0.29	0.18 + 0.057*SL	0.18 + 0.056*SL	0.15 + 0.059*SL
	t_F	0.27	0.15 + 0.060*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
SCK to QN	t_{PLH}	0.81	0.74 + 0.032*SL	0.75 + 0.028*SL	0.77 + 0.027*SL
	t_{PHL}	1.00	0.93 + 0.035*SL	0.93 + 0.033*SL	0.94 + 0.033*SL
	t_R	0.24	0.12 + 0.057*SL	0.12 + 0.058*SL	0.10 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
SN to QN	t_{PLH}	0.41	0.33 + 0.038*SL	0.35 + 0.031*SL	0.39 + 0.027*SL
	t_{PHL}	0.42	0.34 + 0.041*SL	0.36 + 0.036*SL	0.39 + 0.033*SL
	t_R	0.29	0.17 + 0.057*SL	0.17 + 0.056*SL	0.15 + 0.059*SL
	t_F	0.26	0.13 + 0.063*SL	0.13 + 0.064*SL	0.12 + 0.065*SL
RN to QN	t_{PLH}	0.61	0.54 + 0.037*SL	0.56 + 0.030*SL	0.59 + 0.027*SL
	t_R	0.29	0.17 + 0.057*SL	0.18 + 0.056*SL	0.15 + 0.059*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

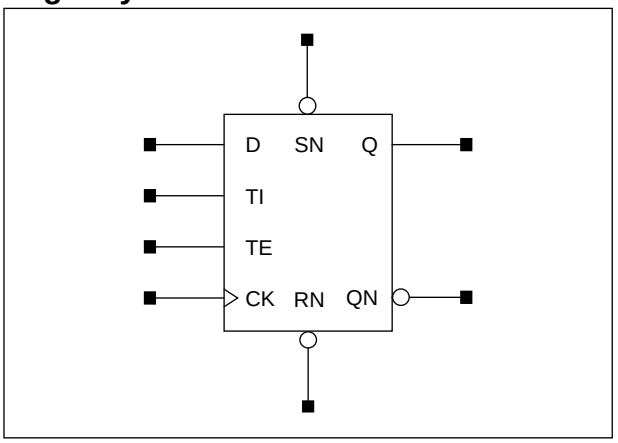
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD4CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.74	0.70 + 0.022*SL	0.71 + 0.016*SL	0.74 + 0.014*SL
	t_{PHL}	0.76	0.72 + 0.024*SL	0.73 + 0.020*SL	0.76 + 0.017*SL
	t_R	0.21	0.16 + 0.025*SL	0.16 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.19	0.12 + 0.033*SL	0.13 + 0.030*SL	0.11 + 0.032*SL
SCK to Q	t_{PLH}	0.81	0.76 + 0.023*SL	0.78 + 0.017*SL	0.81 + 0.014*SL
	t_{PHL}	0.69	0.64 + 0.024*SL	0.65 + 0.020*SL	0.68 + 0.017*SL
	t_R	0.24	0.19 + 0.025*SL	0.19 + 0.026*SL	0.17 + 0.028*SL
	t_F	0.20	0.14 + 0.030*SL	0.14 + 0.031*SL	0.12 + 0.032*SL
SN to Q	t_{PLH}	0.79	0.75 + 0.021*SL	0.76 + 0.016*SL	0.79 + 0.013*SL
	t_R	0.21	0.16 + 0.024*SL	0.16 + 0.027*SL	0.14 + 0.028*SL
RN to Q	t_{PLH}	0.33	0.29 + 0.020*SL	0.30 + 0.016*SL	0.33 + 0.013*SL
	t_{PHL}	0.38	0.34 + 0.024*SL	0.35 + 0.019*SL	0.38 + 0.017*SL
	t_R	0.20	0.14 + 0.027*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
CK to QN	t_{PLH}	1.05	1.01 + 0.022*SL	1.02 + 0.017*SL	1.05 + 0.014*SL
	t_{PHL}	1.12	1.08 + 0.022*SL	1.09 + 0.018*SL	1.11 + 0.017*SL
	t_R	0.25	0.19 + 0.027*SL	0.19 + 0.027*SL	0.18 + 0.028*SL
	t_F	0.22	0.16 + 0.034*SL	0.16 + 0.031*SL	0.15 + 0.032*SL
SCK to QN	t_{PLH}	0.89	0.85 + 0.017*SL	0.86 + 0.015*SL	0.88 + 0.013*SL
	t_{PHL}	1.12	1.08 + 0.018*SL	1.09 + 0.016*SL	1.09 + 0.016*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.19	0.13 + 0.033*SL	0.14 + 0.030*SL	0.11 + 0.032*SL
SN to QN	t_{PLH}	0.41	0.36 + 0.024*SL	0.38 + 0.018*SL	0.42 + 0.014*SL
	t_{PHL}	0.42	0.37 + 0.025*SL	0.38 + 0.020*SL	0.42 + 0.017*SL
	t_R	0.24	0.18 + 0.027*SL	0.18 + 0.027*SL	0.18 + 0.028*SL
	t_F	0.20	0.14 + 0.032*SL	0.14 + 0.031*SL	0.13 + 0.032*SL
RN to QN	t_{PLH}	0.67	0.63 + 0.022*SL	0.64 + 0.017*SL	0.67 + 0.014*SL
	t_R	0.24	0.19 + 0.027*SL	0.19 + 0.027*SL	0.18 + 0.028*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



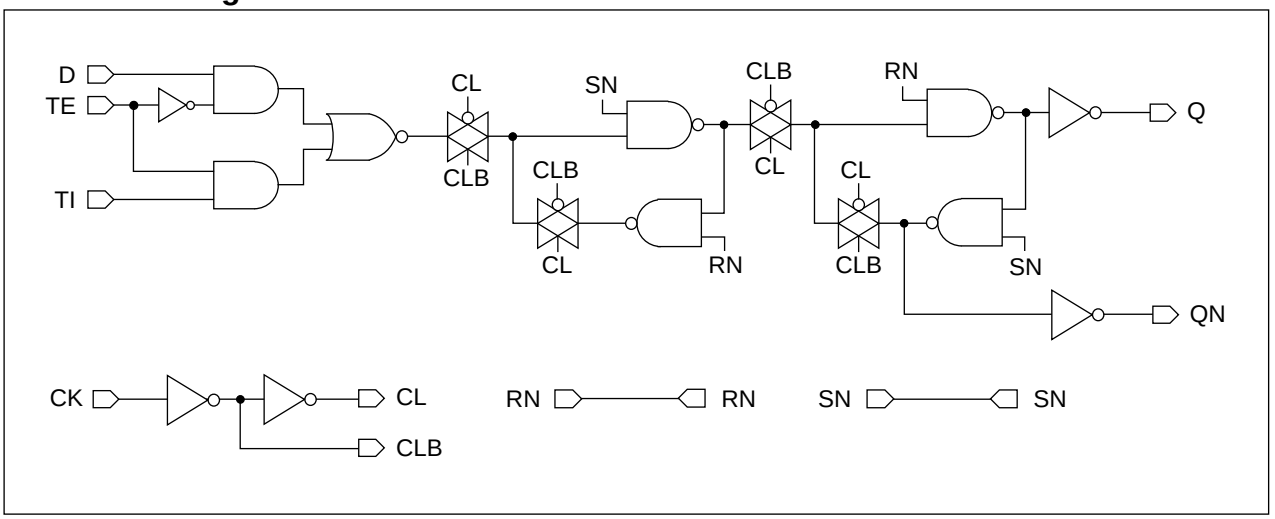
Truth Table

D	TI	TE	CK	RN	SN	Q (n+1)	QN (n+1)
0	x	0	↑	1	1	0	1
1	x	0	↑	1	1	1	0
x	0	1	↑	1	1	0	1
x	1	1	↑	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	x	x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count
FD4S						*FD4S*
D	TI	TE	CK	RN	SN	
0.6	0.6	1.1	0.6	1.6	1.6	9.3
FD4SD2						*FD4SD2*
D	TI	TE	CK	RN	SN	
0.6	0.6	1.1	0.6	1.6	1.6	10.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD4S	FD4SD2
Pulse Width Low (CK)	t_{PWL}	0.87	0.87
Pulse Width High (CK)	t_{PWH}	0.77	0.77
Pulse Width Low (RN)	t_{PWL}	0.77	0.77
Pulse Width Low (SN)	t_{PWL}	0.85	0.87
Input Setup Time (D to CK)	t_{SU}	0.74	0.76
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.76	0.76
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.82	0.82
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.71
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD4S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.71	0.64 + 0.035*SL	0.65 + 0.029*SL	0.67 + 0.027*SL
	t_{PHL}	0.80	0.72 + 0.039*SL	0.74 + 0.035*SL	0.75 + 0.033*SL
	t_R	0.25	0.14 + 0.056*SL	0.13 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.061*SL	0.12 + 0.062*SL	0.09 + 0.065*SL
RN to Q	t_{PLH}	0.33	0.26 + 0.034*SL	0.28 + 0.028*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.063*SL	0.11 + 0.064*SL	0.09 + 0.065*SL
SN to Q	t_{PLH}	0.72	0.66 + 0.034*SL	0.67 + 0.029*SL	0.69 + 0.027*SL
	t_R	0.26	0.14 + 0.056*SL	0.14 + 0.056*SL	0.11 + 0.060*SL
CK to QN	t_{PLH}	0.94	0.88 + 0.033*SL	0.89 + 0.028*SL	0.91 + 0.027*SL
	t_{PHL}	0.93	0.86 + 0.036*SL	0.87 + 0.034*SL	0.88 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to QN	t_{PLH}	0.51	0.45 + 0.033*SL	0.46 + 0.028*SL	0.47 + 0.027*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
SN to QN	t_{PLH}	0.33	0.26 + 0.033*SL	0.27 + 0.028*SL	0.29 + 0.027*SL
	t_{PHL}	0.36	0.28 + 0.038*SL	0.29 + 0.034*SL	0.30 + 0.033*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.10 + 0.063*SL	0.10 + 0.064*SL	0.08 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD4SD2

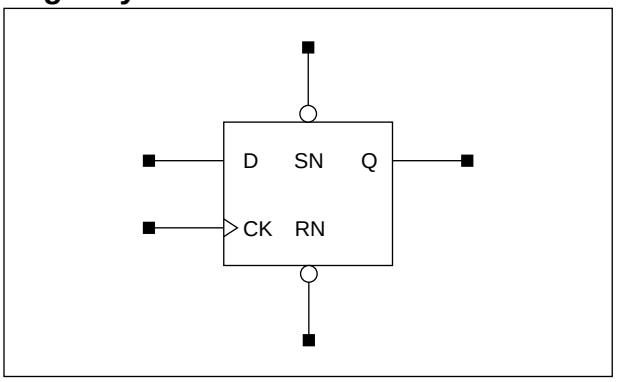
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.71	0.67 + 0.021*SL	0.68 + 0.017*SL	0.71 + 0.013*SL
	t_{PHL}	0.80	0.76 + 0.024*SL	0.77 + 0.020*SL	0.80 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.19	0.13 + 0.030*SL	0.13 + 0.031*SL	0.12 + 0.032*SL
RN to Q	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.34 + 0.013*SL
	t_{PHL}	0.36	0.32 + 0.023*SL	0.33 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.11 + 0.032*SL
SN to Q	t_{PLH}	0.74	0.69 + 0.021*SL	0.71 + 0.016*SL	0.74 + 0.013*SL
	t_R	0.21	0.16 + 0.025*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
CK to QN	t_{PLH}	1.02	0.98 + 0.018*SL	0.99 + 0.015*SL	1.01 + 0.013*SL
	t_{PHL}	1.03	0.99 + 0.019*SL	0.99 + 0.017*SL	1.00 + 0.016*SL
	t_R	0.20	0.14 + 0.026*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.19	0.13 + 0.032*SL	0.13 + 0.030*SL	0.12 + 0.032*SL
RN to QN	t_{PLH}	0.58	0.54 + 0.018*SL	0.55 + 0.015*SL	0.57 + 0.013*SL
	t_R	0.20	0.15 + 0.023*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
SN to QN	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.34 + 0.013*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.13 + 0.027*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.10 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

FD4Q/FD4QD2

D Flip-Flop with Reset, Set, Q Output Only, 1X/2X Drive

Logic Symbol



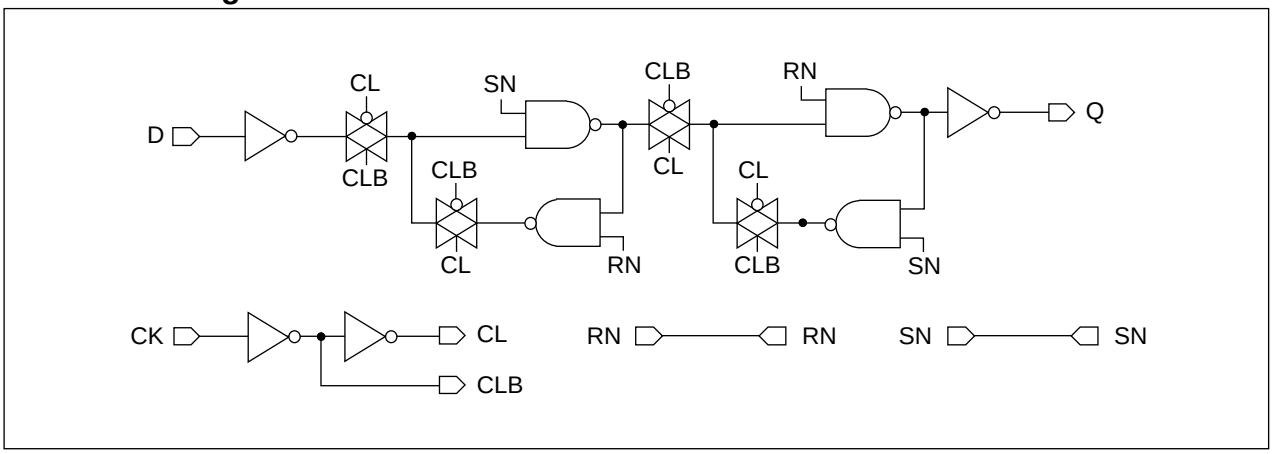
Truth Table

D	CK	RN	SN	Q (n+1)
0	↑	1	1	0
1	↑	1	1	1
x	x	1	0	1
x	x	0	1	0
x	x	0	0	0
x	↓	1	1	Q (n)

Cell Data

Input Load (SL)								Gate Count	
FD4Q				*FD4QD2*				*FD4Q*	*FD4QD2*
D	CK	RN	SN	D	CK	RN	SN		
0.6	0.6	1.1	1.0	0.6	0.6	1.1	1.0	7.3	7.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD4Q	FD4QD2
Pulse Width Low (CK)	t_{PWL}	0.85	0.85
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Pulse Width Low (SN)	t_{PWL}	0.85	0.87
Input Setup Time (D to CK)	t_{SU}	0.55	0.55
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.71
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD4Q

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.68	0.62 + 0.034*SL	0.63 + 0.029*SL	0.65 + 0.027*SL
	t_{PHL}	0.77	0.69 + 0.039*SL	0.71 + 0.034*SL	0.72 + 0.033*SL
	t_R	0.25	0.13 + 0.056*SL	0.13 + 0.057*SL	0.11 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to Q	t_{PLH}	0.32	0.25 + 0.034*SL	0.27 + 0.028*SL	0.28 + 0.027*SL
	t_{PHL}	0.36	0.28 + 0.039*SL	0.29 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.063*SL	0.10 + 0.064*SL	0.09 + 0.065*SL
SN to Q	t_{PLH}	0.71	0.65 + 0.034*SL	0.66 + 0.029*SL	0.68 + 0.027*SL
	t_R	0.25	0.14 + 0.054*SL	0.14 + 0.057*SL	0.11 + 0.060*SL

FD4QD2

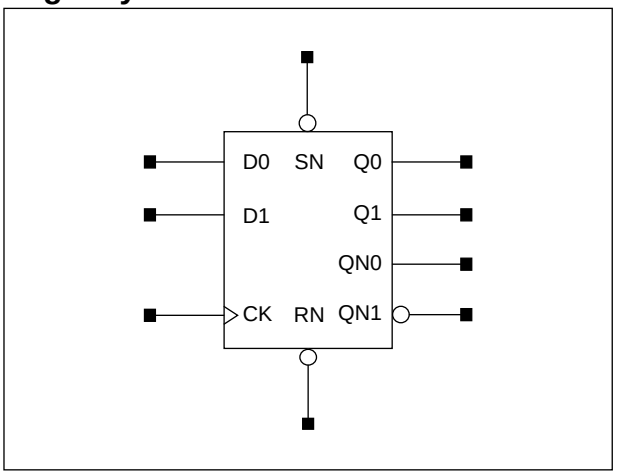
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.69	0.65 + 0.020*SL	0.67 + 0.016*SL	0.69 + 0.013*SL
	t_{PHL}	0.77	0.72 + 0.024*SL	0.74 + 0.019*SL	0.76 + 0.017*SL
	t_R	0.20	0.15 + 0.027*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.19	0.13 + 0.031*SL	0.13 + 0.030*SL	0.11 + 0.032*SL
RN to Q	t_{PLH}	0.33	0.29 + 0.020*SL	0.30 + 0.016*SL	0.33 + 0.013*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.13 + 0.026*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.10 + 0.032*SL
SN to Q	t_{PLH}	0.73	0.68 + 0.021*SL	0.70 + 0.016*SL	0.73 + 0.013*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

FD4X2

2-Bit D Flip-Flop with Reset, Set

Logic Symbol



Truth Table

Dn	CK	RN	SN	Qn (n+1)	QNn (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↓	1	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)				Gate Count
Dn	CK	RN	SN	
0.6	0.6	2.4	2.5	14.3

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (CK)	t_{PWL}	0.96
Pulse Width High (CK)	t_{PWH}	0.79
Pulse Width Low (RN)	t_{PWL}	0.79
Pulse Width Low (SN)	t_{PWL}	0.85
Input Setup Time (D0 to CK)	t_{SU}	0.46
Input Hold Time (D0 to CK)	t_{HD}	0.33
Input Setup Time (D1 to CK)	t_{SU}	0.46
Input Hold Time (D1 to CK)	t_{HD}	0.33
Recovery Time (RN)	t_{RC}	0.33
Input Hold Time (RN to CK)	t_{HD}	0.76
Recovery Time (SN)	t_{RC}	0.33
Input Hold Time (SN to CK)	t_{HD}	0.60

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

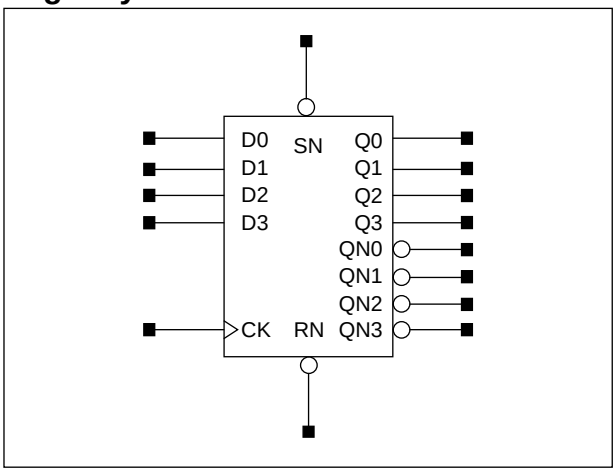
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.77	0.70 + 0.035*SL	0.71 + 0.029*SL	0.74 + 0.027*SL
	t_{PHL}	0.95	0.87 + 0.040*SL	0.89 + 0.035*SL	0.90 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.13 + 0.058*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
RN to Q0	t_{PLH}	0.34	0.27 + 0.033*SL	0.28 + 0.029*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.31 + 0.035*SL	0.32 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.064*SL	0.09 + 0.065*SL
SN to Q0	t_{PLH}	0.73	0.66 + 0.034*SL	0.67 + 0.029*SL	0.69 + 0.027*SL
	t_R	0.26	0.15 + 0.055*SL	0.14 + 0.056*SL	0.11 + 0.060*SL
CK to Q1	t_{PLH}	0.76	0.70 + 0.034*SL	0.71 + 0.029*SL	0.73 + 0.027*SL
	t_{PHL}	0.95	0.87 + 0.039*SL	0.88 + 0.035*SL	0.90 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.13 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.13 + 0.060*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q1	t_{PLH}	0.33	0.26 + 0.034*SL	0.28 + 0.028*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
SN to Q1	t_{PLH}	0.72	0.66 + 0.034*SL	0.67 + 0.029*SL	0.69 + 0.027*SL
	t_R	0.25	0.14 + 0.055*SL	0.14 + 0.056*SL	0.11 + 0.060*SL
CK to QN0	t_{PLH}	1.10	1.03 + 0.033*SL	1.04 + 0.028*SL	1.06 + 0.027*SL
	t_{PHL}	1.00	0.93 + 0.036*SL	0.93 + 0.034*SL	0.94 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to QN0	t_{PLH}	0.52	0.45 + 0.033*SL	0.47 + 0.028*SL	0.48 + 0.027*SL
	t_R	0.24	0.13 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
SN to QN0	t_{PLH}	0.33	0.26 + 0.034*SL	0.28 + 0.028*SL	0.29 + 0.027*SL
	t_{PHL}	0.36	0.29 + 0.039*SL	0.30 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.24	0.12 + 0.057*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.064*SL	0.09 + 0.065*SL
CK to QN1	t_{PLH}	1.09	1.02 + 0.033*SL	1.04 + 0.028*SL	1.05 + 0.027*SL
	t_{PHL}	0.99	0.92 + 0.036*SL	0.93 + 0.034*SL	0.93 + 0.033*SL
	t_R	0.24	0.13 + 0.057*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to QN1	t_{PLH}	0.51	0.45 + 0.033*SL	0.46 + 0.028*SL	0.47 + 0.027*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
SN to QN1	t_{PLH}	0.33	0.26 + 0.034*SL	0.27 + 0.028*SL	0.29 + 0.027*SL
	t_{PHL}	0.36	0.28 + 0.038*SL	0.29 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.10 + 0.063*SL	0.10 + 0.064*SL	0.08 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

FD4X4

4-Bit D Flip-Flop with Reset, Set

Logic Symbol



Truth Table

Dn	CK	RN	SN	Qn (n+1)	QNn (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↓	1	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)				Gate Count
Dn	CK	RN	SN	
0.6	0.6	7.0	7.3	27.7

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (CK)	t_{PWL}	1.45
Pulse Width High (CK)	t_{PWH}	0.93
Pulse Width Low (RN)	t_{PWL}	0.79
Pulse Width Low (SN)	t_{PWL}	0.85
Input Setup Time (D0 to CK)	t_{SU}	0.38
Input Hold Time (D0 to CK)	t_{HD}	0.52
Input Setup Time (D1 to CK)	t_{SU}	0.38
Input Hold Time (D1 to CK)	t_{HD}	0.52
Input Setup Time (D2 to CK)	t_{SU}	0.38
Input Hold Time (D2 to CK)	t_{HD}	0.52
Input Setup Time (D3 to CK)	t_{SU}	0.38
Input Hold Time (D3 to CK)	t_{HD}	0.52
Recovery Time (RN)	t_{RC}	0.33
Input Hold Time (RN to CK)	t_{HD}	0.93
Recovery Time (SN)	t_{RC}	0.33
Input Hold Time (SN to CK)	t_{HD}	0.87

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	0.90	0.84 + 0.035*SL	0.85 + 0.029*SL	0.87 + 0.027*SL
	t_{PHL}	1.28	1.20 + 0.040*SL	1.22 + 0.035*SL	1.23 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
RN to Q0	t_{PLH}	0.34	0.27 + 0.033*SL	0.28 + 0.028*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.31 + 0.035*SL	0.32 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
SN to Q0	t_{PLH}	0.72	0.66 + 0.035*SL	0.67 + 0.029*SL	0.69 + 0.027*SL
	t_R	0.25	0.14 + 0.056*SL	0.14 + 0.056*SL	0.11 + 0.059*SL
CK to Q1	t_{PLH}	0.90	0.84 + 0.035*SL	0.85 + 0.029*SL	0.87 + 0.027*SL
	t_{PHL}	1.28	1.20 + 0.039*SL	1.22 + 0.035*SL	1.23 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.13 + 0.061*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
RN to Q1	t_{PLH}	0.34	0.27 + 0.033*SL	0.28 + 0.028*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.31 + 0.035*SL	0.32 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.064*SL	0.09 + 0.065*SL
SN to Q1	t_{PLH}	0.72	0.66 + 0.034*SL	0.67 + 0.029*SL	0.69 + 0.027*SL
	t_R	0.25	0.14 + 0.056*SL	0.14 + 0.056*SL	0.11 + 0.059*SL
CK to Q2	t_{PLH}	0.90	0.84 + 0.035*SL	0.85 + 0.029*SL	0.87 + 0.027*SL
	t_{PHL}	1.28	1.20 + 0.040*SL	1.22 + 0.035*SL	1.23 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
RN to Q2	t_{PLH}	0.34	0.27 + 0.033*SL	0.28 + 0.028*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.31 + 0.035*SL	0.32 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
SN to Q2	t_{PLH}	0.72	0.66 + 0.035*SL	0.67 + 0.029*SL	0.69 + 0.027*SL
	t_R	0.25	0.14 + 0.056*SL	0.14 + 0.056*SL	0.11 + 0.059*SL
CK to Q3	t_{PLH}	0.90	0.83 + 0.035*SL	0.85 + 0.029*SL	0.87 + 0.027*SL
	t_{PHL}	1.28	1.20 + 0.039*SL	1.21 + 0.035*SL	1.23 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.13 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.061*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
RN to Q3	t_{PLH}	0.33	0.26 + 0.034*SL	0.28 + 0.028*SL	0.29 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.063*SL	0.11 + 0.064*SL	0.09 + 0.065*SL
SN to Q3	t_{PLH}	0.72	0.65 + 0.034*SL	0.67 + 0.029*SL	0.69 + 0.027*SL
	t_R	0.25	0.14 + 0.056*SL	0.14 + 0.056*SL	0.11 + 0.060*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

(Continued)

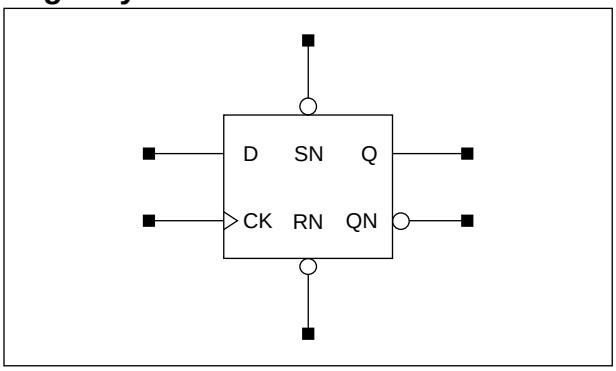
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN0	t_{PLH}	1.42	1.36 + 0.033*SL	1.37 + 0.029*SL	1.39 + 0.027*SL
	t_{PHL}	1.13	1.06 + 0.037*SL	1.07 + 0.033*SL	1.08 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to QN0	t_{PLH}	0.52	0.45 + 0.033*SL	0.47 + 0.028*SL	0.48 + 0.027*SL
	t_R	0.24	0.13 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
SN to QN0	t_{PLH}	0.33	0.27 + 0.033*SL	0.28 + 0.028*SL	0.29 + 0.027*SL
	t_{PHL}	0.36	0.29 + 0.038*SL	0.30 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.24	0.12 + 0.057*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.10 + 0.063*SL	0.10 + 0.064*SL	0.09 + 0.065*SL
CK to QN1	t_{PLH}	1.42	1.36 + 0.033*SL	1.37 + 0.028*SL	1.39 + 0.027*SL
	t_{PHL}	1.13	1.06 + 0.037*SL	1.07 + 0.033*SL	1.08 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to QN1	t_{PLH}	0.52	0.45 + 0.033*SL	0.47 + 0.028*SL	0.48 + 0.027*SL
	t_R	0.24	0.13 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
SN to QN1	t_{PLH}	0.33	0.27 + 0.033*SL	0.28 + 0.028*SL	0.29 + 0.027*SL
	t_{PHL}	0.36	0.29 + 0.038*SL	0.30 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.24	0.12 + 0.057*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.064*SL	0.09 + 0.065*SL
CK to QN2	t_{PLH}	1.42	1.36 + 0.033*SL	1.37 + 0.028*SL	1.39 + 0.027*SL
	t_{PHL}	1.13	1.06 + 0.037*SL	1.07 + 0.033*SL	1.08 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to QN2	t_{PLH}	0.52	0.45 + 0.033*SL	0.47 + 0.028*SL	0.48 + 0.027*SL
	t_R	0.24	0.13 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
SN to QN2	t_{PLH}	0.33	0.27 + 0.033*SL	0.28 + 0.028*SL	0.29 + 0.027*SL
	t_{PHL}	0.36	0.29 + 0.038*SL	0.30 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.24	0.12 + 0.057*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.10 + 0.063*SL	0.10 + 0.064*SL	0.09 + 0.065*SL
CK to QN3	t_{PLH}	1.42	1.35 + 0.033*SL	1.36 + 0.028*SL	1.38 + 0.027*SL
	t_{PHL}	1.13	1.06 + 0.036*SL	1.06 + 0.033*SL	1.07 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to QN3	t_{PLH}	0.51	0.45 + 0.033*SL	0.46 + 0.028*SL	0.47 + 0.027*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
SN to QN3	t_{PLH}	0.33	0.26 + 0.033*SL	0.27 + 0.028*SL	0.29 + 0.027*SL
	t_{PHL}	0.36	0.28 + 0.038*SL	0.29 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.10 + 0.062*SL	0.10 + 0.064*SL	0.08 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Logic Symbol



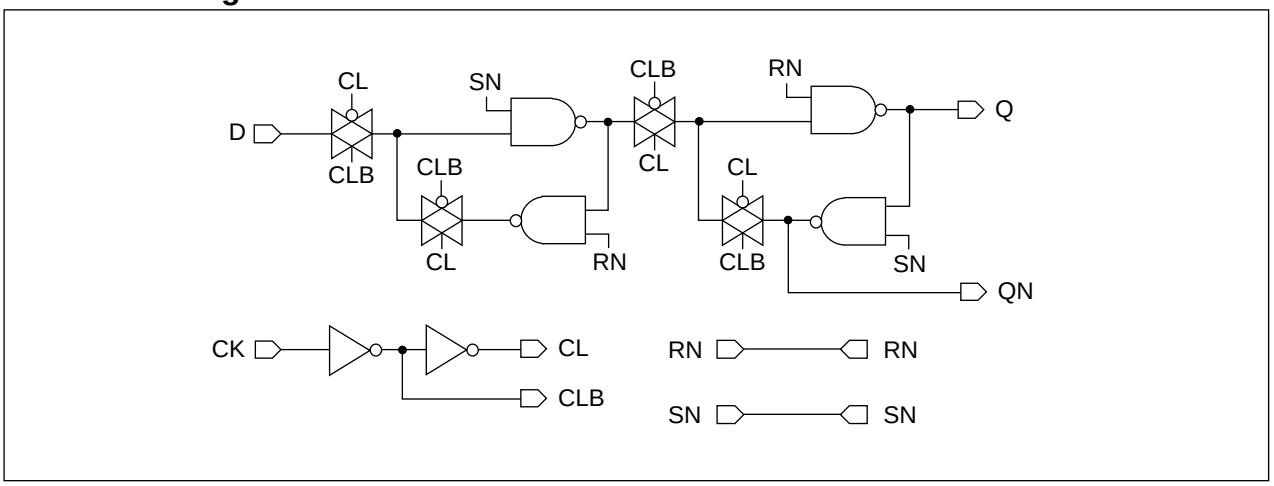
Truth Table

D	CK	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	1
x	↓	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
YFD4				*YFD4D2*				*YFD4*	*YFD4D2*
D	CK	RN	SN	D	CK	RN	SN		
1.8	0.6	1.7	1.9	1.8	0.6	2.8	3.1	6.3	7.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		YFD4	YFD4D2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.87	0.98
Pulse Width Low (SN)	t_{PWL}	0.79	0.79
Input Setup Time (D to CK)	t_{SU}	0.44	0.44
Input Hold Time (D to CK)	t_{HD}	0.44	0.44
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.44	0.44
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.71	0.66

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

YFD4

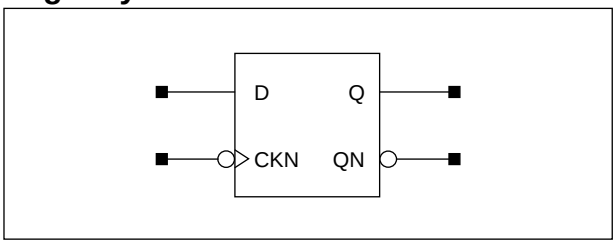
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.57 + 0.034*SL	0.58 + 0.030*SL	0.60 + 0.028*SL
	t_{PHL}	0.63	0.55 + 0.042*SL	0.55 + 0.039*SL	0.57 + 0.037*SL
	t_R	0.37	0.25 + 0.058*SL	0.25 + 0.060*SL	0.23 + 0.062*SL
	t_F	0.43	0.28 + 0.072*SL	0.27 + 0.077*SL	0.24 + 0.080*SL
RN to Q	t_{PHL}	0.65	0.57 + 0.044*SL	0.58 + 0.039*SL	0.60 + 0.037*SL
	t_F	0.44	0.30 + 0.070*SL	0.29 + 0.075*SL	0.24 + 0.080*SL
SN to Q	t_{PLH}	0.20	0.14 + 0.030*SL	0.15 + 0.028*SL	0.25 + 0.017*SL
	t_{PHL}	0.22	0.15 + 0.038*SL	0.15 + 0.037*SL	0.15 + 0.037*SL
	t_R	0.32	0.21 + 0.053*SL	0.24 + 0.042*SL	0.37 + 0.029*SL
	t_F	0.38	0.23 + 0.073*SL	0.22 + 0.077*SL	0.18 + 0.081*SL
CK to QN	t_{PLH}	0.84	0.66 + 0.089*SL	0.67 + 0.087*SL	0.68 + 0.086*SL
	t_{PHL}	0.82	0.67 + 0.076*SL	0.68 + 0.073*SL	0.70 + 0.071*SL
	t_R	0.33	0.18 + 0.077*SL	0.17 + 0.077*SL	0.17 + 0.078*SL
	t_F	0.32	0.15 + 0.086*SL	0.15 + 0.085*SL	0.15 + 0.086*SL
RN to QN	t_{PLH}	0.19	0.12 + 0.032*SL	0.13 + 0.028*SL	0.13 + 0.028*SL
	t_{PHL}	0.20	0.12 + 0.040*SL	0.13 + 0.037*SL	0.13 + 0.037*SL
	t_R	0.29	0.18 + 0.051*SL	0.17 + 0.057*SL	0.22 + 0.051*SL
	t_F	0.34	0.19 + 0.071*SL	0.18 + 0.077*SL	0.14 + 0.081*SL
SN to QN	t_{PHL}	0.38	0.24 + 0.073*SL	0.25 + 0.069*SL	0.37 + 0.057*SL
	t_F	0.31	0.15 + 0.082*SL	0.14 + 0.084*SL	0.16 + 0.082*SL

YFD4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.66	0.63 + 0.019*SL	0.63 + 0.017*SL	0.66 + 0.014*SL
	t_{PHL}	0.74	0.68 + 0.028*SL	0.69 + 0.025*SL	0.74 + 0.020*SL
	t_R	0.33	0.27 + 0.027*SL	0.27 + 0.028*SL	0.26 + 0.029*SL
	t_F	0.46	0.39 + 0.035*SL	0.38 + 0.038*SL	0.37 + 0.039*SL
RN to Q	t_{PHL}	0.77	0.71 + 0.028*SL	0.72 + 0.024*SL	0.76 + 0.019*SL
	t_F	0.46	0.39 + 0.035*SL	0.38 + 0.036*SL	0.36 + 0.038*SL
SN to Q	t_{PLH}	0.18	0.15 + 0.015*SL	0.15 + 0.014*SL	0.17 + 0.012*SL
	t_{PHL}	0.16	0.12 + 0.022*SL	0.12 + 0.020*SL	0.13 + 0.019*SL
	t_R	0.29	0.24 + 0.021*SL	0.23 + 0.027*SL	0.33 + 0.016*SL
	t_F	0.30	0.22 + 0.038*SL	0.21 + 0.040*SL	0.21 + 0.040*SL
CK to QN	t_{PLH}	0.89	0.79 + 0.051*SL	0.80 + 0.048*SL	0.84 + 0.043*SL
	t_{PHL}	0.79	0.71 + 0.041*SL	0.72 + 0.038*SL	0.74 + 0.035*SL
	t_R	0.25	0.17 + 0.037*SL	0.18 + 0.037*SL	0.16 + 0.038*SL
	t_F	0.21	0.13 + 0.043*SL	0.13 + 0.042*SL	0.13 + 0.043*SL
RN to QN	t_{PLH}	0.14	0.10 + 0.018*SL	0.11 + 0.015*SL	0.12 + 0.013*SL
	t_{PHL}	0.15	0.11 + 0.023*SL	0.12 + 0.019*SL	0.12 + 0.019*SL
	t_R	0.22	0.17 + 0.024*SL	0.16 + 0.026*SL	0.15 + 0.027*SL
	t_F	0.24	0.18 + 0.031*SL	0.17 + 0.037*SL	0.14 + 0.040*SL
SN to QN	t_{PHL}	0.30	0.23 + 0.037*SL	0.23 + 0.035*SL	0.27 + 0.031*SL
	t_F	0.21	0.13 + 0.040*SL	0.12 + 0.042*SL	0.14 + 0.041*SL

*Group1 : SL < 3. *Group2 : 3 ≦ SL ≦ 10. *Group3 : 10 < SL

Logic Symbol



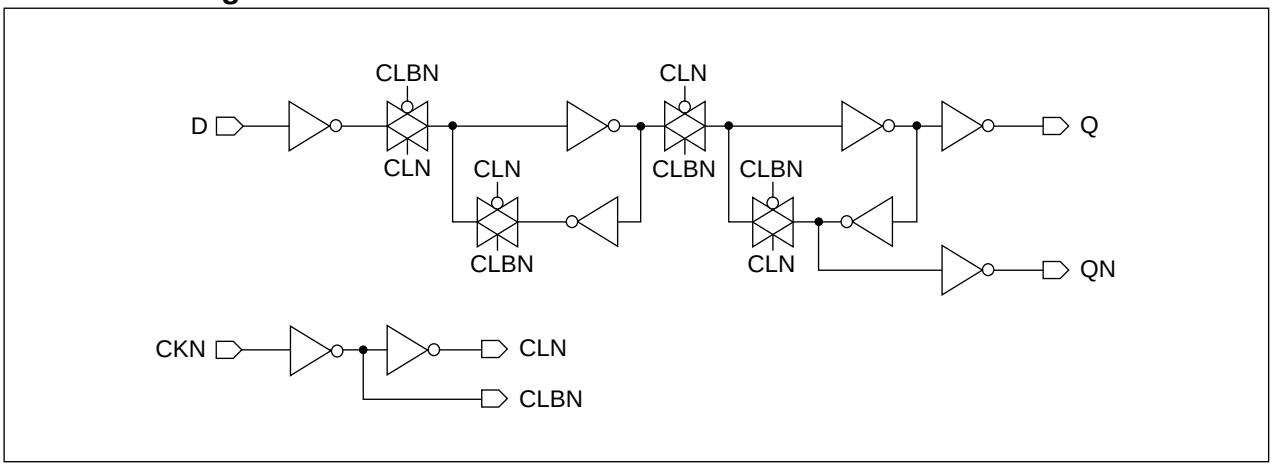
Truth Table

D	CKN	Q (n+1)	QN (n+1)
0	↓	0	1
1	↓	1	0
x	↑	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
FD5		*FD5D2*		*FD5*	*FD5D2*
D	CKN	D	CKN		
0.6	0.6	0.6	0.6	5.3	6.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD5	FD5D2
Pulse Width Low (CKN)	t_{PWL}	0.85	0.85
Pulse Width High (CKN)	t_{PWH}	0.79	0.79
Input Setup Time (D to CKN)	t_{SU}	0.41	0.41
Input Hold Time (D to CKN)	t_{HD}	0.55	0.55

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD5

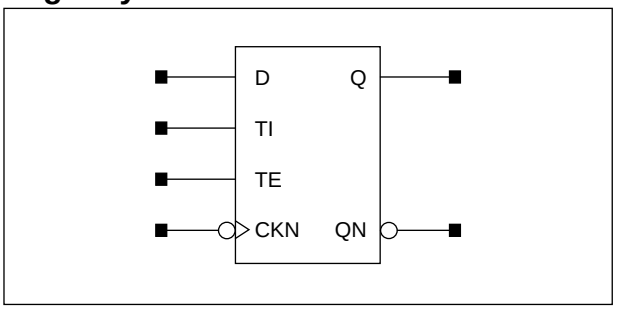
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.81	0.75 + 0.031*SL	0.75 + 0.028*SL	0.76 + 0.027*SL
	t_{PHL}	0.73	0.65 + 0.040*SL	0.67 + 0.034*SL	0.68 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CKN to QN	t_{PLH}	0.79	0.73 + 0.027*SL	0.74 + 0.027*SL	0.74 + 0.027*SL
	t_{PHL}	0.97	0.90 + 0.035*SL	0.91 + 0.033*SL	0.91 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

FD5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.81	0.77 + 0.018*SL	0.78 + 0.015*SL	0.80 + 0.013*SL
	t_{PHL}	0.73	0.68 + 0.024*SL	0.69 + 0.019*SL	0.72 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.11 + 0.032*SL
CKN to QN	t_{PLH}	0.85	0.83 + 0.014*SL	0.83 + 0.013*SL	0.83 + 0.013*SL
	t_{PHL}	1.04	1.00 + 0.019*SL	1.01 + 0.017*SL	1.02 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Logic Symbol



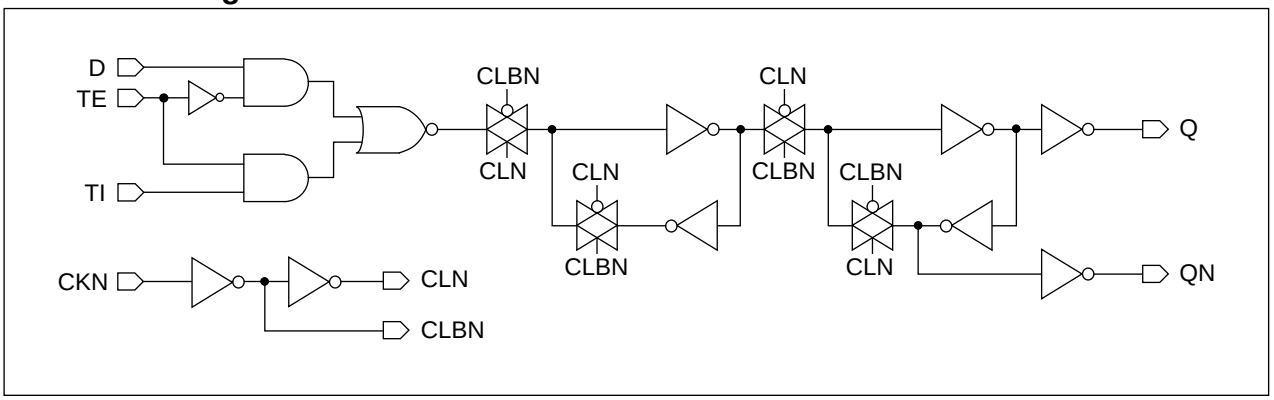
Truth Table

D	TI	TE	CKN	Q (n+1)	QN (n+1)
0	x	0	↓	0	1
1	x	0	↓	1	0
x	0	1	↓	0	1
x	1	1	↓	1	0
x	x	x	↑	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
FD5S				*FD5SD2*				*FD5S*	*FD5SD2*
D	TI	TE	CKN	D	TI	TE	CKN		
0.6	0.6	1.1	0.6	0.6	0.6	1.1	0.6	7.0	7.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD5S	FD5SD2
Pulse Width Low (CKN)	t_{PWL}	0.85	0.85
Pulse Width High (CKN)	t_{PWH}	0.77	0.77
Input Setup Time (D to CKN)	t_{SU}	0.57	0.57
Input Hold Time (D to CKN)	t_{HD}	0.46	0.46
Input Setup Time (TI to CKN)	t_{SU}	0.57	0.57
Input Hold Time (TI to CKN)	t_{HD}	0.38	0.38
Input Setup Time (TE to CKN)	t_{SU}	0.60	0.60
Input Hold Time (TE to CKN)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD5S

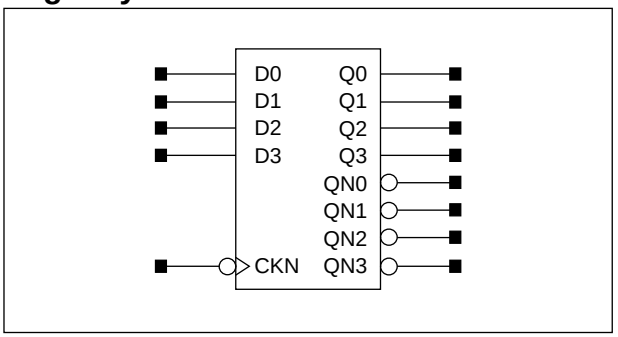
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.82	0.76 + 0.031*SL	0.77 + 0.028*SL	0.78 + 0.027*SL
	t_{PHL}	0.75	0.67 + 0.039*SL	0.68 + 0.035*SL	0.70 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CKN to QN	t_{PLH}	0.80	0.75 + 0.028*SL	0.75 + 0.027*SL	0.75 + 0.027*SL
	t_{PHL}	0.99	0.92 + 0.035*SL	0.92 + 0.033*SL	0.93 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

FD5SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.83	0.79 + 0.018*SL	0.80 + 0.015*SL	0.81 + 0.013*SL
	t_{PHL}	0.74	0.70 + 0.023*SL	0.71 + 0.019*SL	0.73 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
CKN to QN	t_{PLH}	0.87	0.84 + 0.014*SL	0.84 + 0.013*SL	0.84 + 0.013*SL
	t_{PHL}	1.06	1.02 + 0.019*SL	1.03 + 0.017*SL	1.03 + 0.016*SL
	t_R	0.15	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

Dn	CKN	Qn (n+1)	QNn (n+1)
0	↓	0	1
1	↓	1	0
x	↑	Qn (n)	QNn (n)

Cell Data

Input Load (SL)		Gate Count
Dn	CKN	
0.6	0.6	18.3

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (CKN)	t_{PWL}	1.31
Pulse Width High (CKN)	t_{PWH}	1.12
Input Setup Time (D0 to CKN)	t_{SU}	0.33
Input Hold Time (D0 to CKN)	t_{HD}	0.96
Input Setup Time (D1 to CKN)	t_{SU}	0.33
Input Hold Time (D1 to CKN)	t_{HD}	0.96
Input Setup Time (D2 to CKN)	t_{SU}	0.33
Input Hold Time (D2 to CKN)	t_{HD}	0.96
Input Setup Time (D3 to CKN)	t_{SU}	0.36
Input Hold Time (D3 to CKN)	t_{HD}	0.96

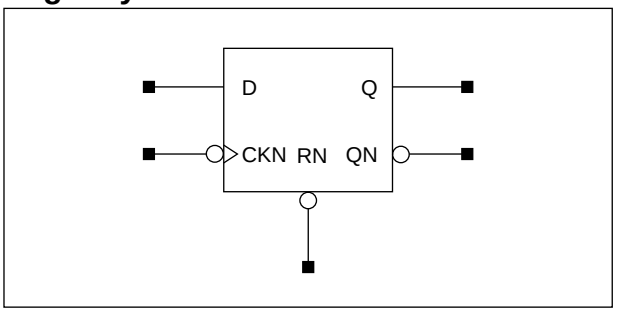
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q0	t_{PLH}	1.37	1.30 + 0.031*SL	1.31 + 0.028*SL	1.32 + 0.027*SL
	t_{PHL}	1.06	0.98 + 0.040*SL	1.00 + 0.034*SL	1.01 + 0.033*SL
	t_R	0.23	0.12 + 0.054*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
CKN to Q1	t_{PLH}	1.37	1.30 + 0.031*SL	1.31 + 0.028*SL	1.32 + 0.027*SL
	t_{PHL}	1.06	0.98 + 0.040*SL	1.00 + 0.034*SL	1.01 + 0.033*SL
	t_R	0.23	0.12 + 0.054*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
CKN to Q2	t_{PLH}	1.37	1.30 + 0.031*SL	1.31 + 0.028*SL	1.32 + 0.027*SL
	t_{PHL}	1.06	0.98 + 0.040*SL	1.00 + 0.034*SL	1.01 + 0.033*SL
	t_R	0.23	0.12 + 0.054*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
CKN to Q3	t_{PLH}	1.37	1.30 + 0.031*SL	1.31 + 0.028*SL	1.32 + 0.027*SL
	t_{PHL}	1.06	0.98 + 0.039*SL	1.00 + 0.034*SL	1.01 + 0.033*SL
	t_R	0.23	0.12 + 0.054*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.063*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
CKN to QN0	t_{PLH}	1.09	1.04 + 0.028*SL	1.04 + 0.027*SL	1.04 + 0.027*SL
	t_{PHL}	1.53	1.46 + 0.035*SL	1.47 + 0.033*SL	1.47 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
CKN to QN1	t_{PLH}	1.10	1.04 + 0.028*SL	1.04 + 0.027*SL	1.04 + 0.027*SL
	t_{PHL}	1.53	1.46 + 0.035*SL	1.47 + 0.033*SL	1.47 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
CKN to QN2	t_{PLH}	1.10	1.04 + 0.028*SL	1.04 + 0.027*SL	1.04 + 0.027*SL
	t_{PHL}	1.53	1.46 + 0.035*SL	1.47 + 0.033*SL	1.47 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
CKN to QN3	t_{PLH}	1.09	1.04 + 0.028*SL	1.04 + 0.027*SL	1.04 + 0.027*SL
	t_{PHL}	1.53	1.46 + 0.035*SL	1.47 + 0.033*SL	1.47 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.063*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



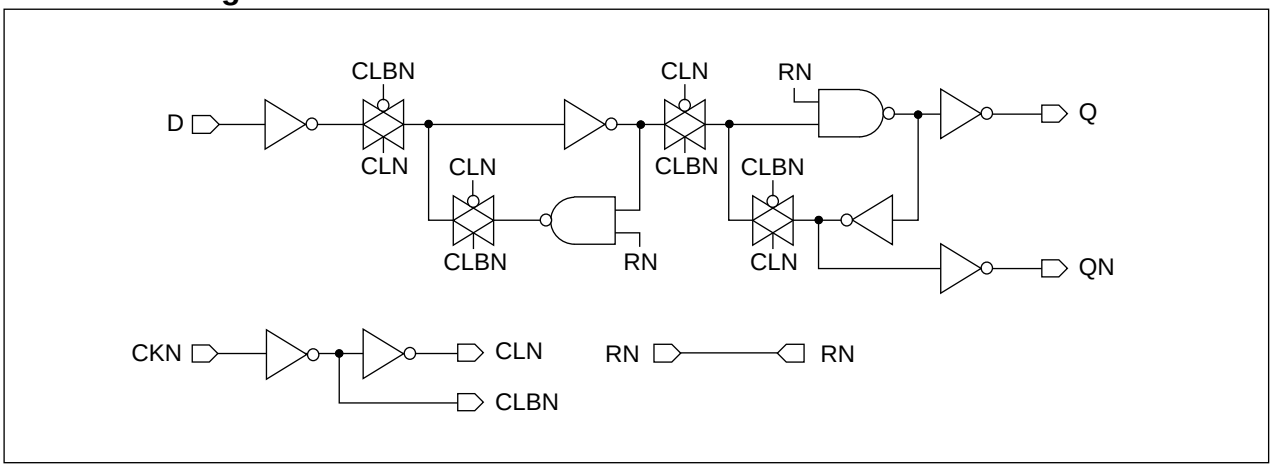
Truth Table

D	CKN	RN	Q (n+1)	QN (n+1)
0	↓	1	0	1
1	↓	1	1	0
x	x	0	0	1
x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FD6			*FD6D2*			*FD6*	*FD6D2*
D	CKN	RN	D	CKN	RN		
0.6	0.6	1.3	0.6	0.6	1.3	6.3	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD6	FD6D2
Pulse Width Low (CKN)	t_{PWL}	0.85	0.87
Pulse Width High (CKN)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Input Setup Time (D to CKN)	t_{SU}	0.41	0.41
Input Hold Time (D to CKN)	t_{HD}	0.55	0.55
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CKN)	t_{HD}	0.82	0.82

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD6

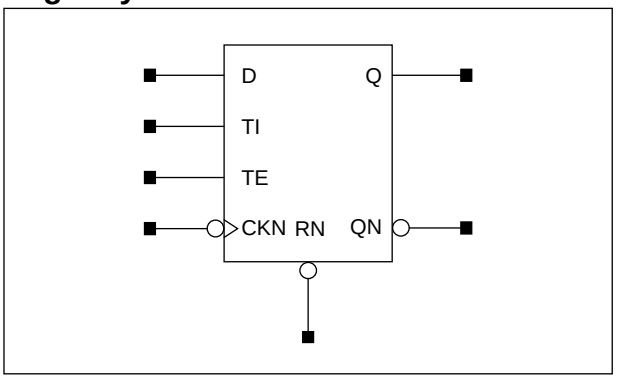
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.88	0.81 + 0.035*SL	0.82 + 0.030*SL	0.85 + 0.027*SL
	t_{PHL}	0.77	0.69 + 0.040*SL	0.70 + 0.034*SL	0.72 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q	t_{PHL}	0.37	0.29 + 0.040*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CKN to QN	t_{PLH}	0.82	0.77 + 0.028*SL	0.77 + 0.027*SL	0.77 + 0.027*SL
	t_{PHL}	1.05	0.98 + 0.035*SL	0.99 + 0.033*SL	0.99 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.07 + 0.066*SL
RN to QN	t_{PLH}	0.43	0.37 + 0.028*SL	0.37 + 0.027*SL	0.37 + 0.027*SL
	t_R	0.20	0.09 + 0.055*SL	0.08 + 0.059*SL	0.07 + 0.060*SL

FD6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.89	0.84 + 0.021*SL	0.86 + 0.017*SL	0.89 + 0.013*SL
	t_{PHL}	0.76	0.72 + 0.024*SL	0.73 + 0.020*SL	0.76 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.19	0.12 + 0.033*SL	0.13 + 0.030*SL	0.11 + 0.032*SL
RN to Q	t_{PHL}	0.36	0.32 + 0.023*SL	0.33 + 0.019*SL	0.36 + 0.017*SL
	t_F	0.18	0.12 + 0.031*SL	0.11 + 0.031*SL	0.11 + 0.032*SL
CKN to QN	t_{PLH}	0.89	0.86 + 0.014*SL	0.86 + 0.013*SL	0.87 + 0.013*SL
	t_{PHL}	1.15	1.11 + 0.017*SL	1.12 + 0.016*SL	1.12 + 0.016*SL
	t_R	0.15	0.11 + 0.025*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
RN to QN	t_{PLH}	0.49	0.46 + 0.014*SL	0.46 + 0.013*SL	0.47 + 0.013*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.026*SL	0.08 + 0.029*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



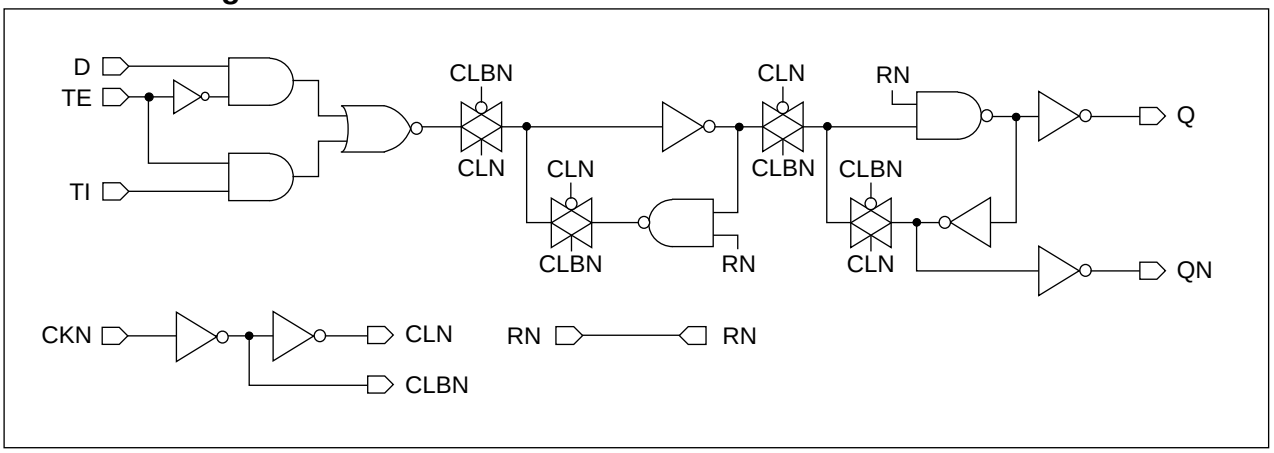
Truth Table

D	TI	TE	CKN	RN	Q (n+1)	QN (n+1)
0	x	0	↓	1	0	1
1	x	0	↓	1	1	0
x	0	1	↓	1	0	1
x	1	1	↓	1	1	0
x	x	x	x	0	0	1
x	x	x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
FD6S					*FD6SD2*					*FD6S*	*FD6S D2*
D	TI	TE	CKN	RN	D	TI	TE	CKN	RN		
0.6	0.6	1.1	0.6	1.3	0.6	0.6	1.1	0.6	1.3	8.0	8.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD6S	FD6SD2
Pulse Width Low (CKN)	t_{PWL}	0.87	0.87
Pulse Width High (CKN)	t_{PWH}	0.77	0.77
Pulse Width Low (RN)	t_{PWL}	0.77	0.77
Input Setup Time (D to CKN)	t_{SU}	0.60	0.60
Input Hold Time (D to CKN)	t_{HD}	0.45	0.46
Input Setup Time (TI to CKN)	t_{SU}	0.60	0.60
Input Hold Time (TI to CKN)	t_{HD}	0.38	0.38
Input Setup Time (TE to CKN)	t_{SU}	0.60	0.60
Input Hold Time (TE to CKN)	t_{HD}	0.33	0.38
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CKN)	t_{HD}	0.87	0.82

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD6S

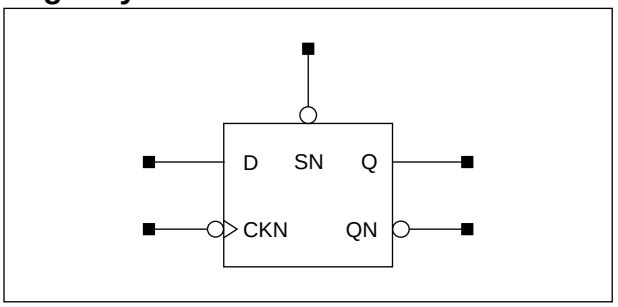
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.89	0.82 + 0.035*SL	0.83 + 0.030*SL	0.86 + 0.027*SL
	t_{PHL}	0.78	0.70 + 0.040*SL	0.71 + 0.034*SL	0.73 + 0.033*SL
	t_R	0.25	0.14 + 0.058*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.063*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q	t_{PHL}	0.37	0.29 + 0.040*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CKN to QN	t_{PLH}	0.84	0.78 + 0.028*SL	0.78 + 0.027*SL	0.78 + 0.027*SL
	t_{PHL}	1.06	0.99 + 0.035*SL	1.00 + 0.033*SL	1.00 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.10 + 0.063*SL	0.08 + 0.066*SL
RN to QN	t_{PLH}	0.43	0.37 + 0.028*SL	0.37 + 0.027*SL	0.37 + 0.027*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.059*SL	0.07 + 0.060*SL

FD6SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.90	0.85 + 0.021*SL	0.87 + 0.017*SL	0.90 + 0.013*SL
	t_{PHL}	0.78	0.73 + 0.024*SL	0.74 + 0.020*SL	0.77 + 0.017*SL
	t_R	0.20	0.15 + 0.025*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.19	0.12 + 0.032*SL	0.13 + 0.031*SL	0.11 + 0.032*SL
RN to Q	t_{PHL}	0.36	0.32 + 0.024*SL	0.33 + 0.019*SL	0.36 + 0.017*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
CKN to QN	t_{PLH}	0.90	0.88 + 0.014*SL	0.88 + 0.013*SL	0.88 + 0.013*SL
	t_{PHL}	1.16	1.12 + 0.017*SL	1.13 + 0.016*SL	1.13 + 0.016*SL
	t_R	0.15	0.11 + 0.025*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.18	0.12 + 0.029*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
RN to QN	t_{PLH}	0.49	0.46 + 0.014*SL	0.46 + 0.013*SL	0.47 + 0.013*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.026*SL	0.08 + 0.029*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



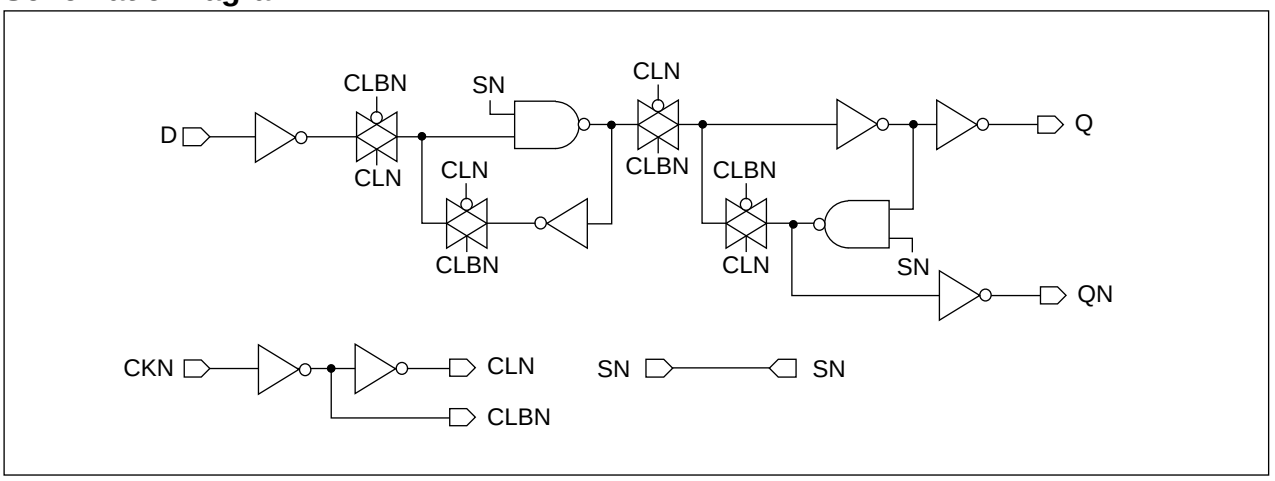
Truth Table

D	CKN	SN	Q (n+1)	QN (n+1)
0	↓	1	0	1
1	↓	1	1	0
x	x	0	1	0
x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FD7			*FD7D2*			*FD7*	*FD7D2*
D	CKN	SN	D	CKN	SN		
0.6	0.6	1.1	0.6	0.6	1.1	6.7	7.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD7	FD7D2
Pulse Width Low (CKN)	t_{PWL}	0.85	0.87
Pulse Width High (CKN)	t_{PWH}	0.79	0.79
Pulse Width Low (SN)	t_{PWL}	0.85	0.85
Input Setup Time (D to CKN)	t_{SU}	0.46	0.46
Input Hold Time (D to CKN)	t_{HD}	0.55	0.55
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CKN)	t_{HD}	0.55	0.55

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD7

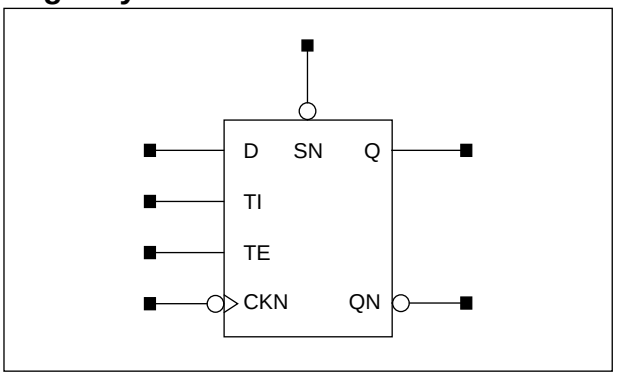
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.82	0.75 + 0.031*SL	0.76 + 0.028*SL	0.77 + 0.027*SL
	t_{PHL}	0.78	0.70 + 0.039*SL	0.72 + 0.034*SL	0.73 + 0.033*SL
	t_R	0.23	0.12 + 0.054*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
SN to Q	t_{PLH}	0.67	0.61 + 0.030*SL	0.62 + 0.027*SL	0.63 + 0.027*SL
	t_R	0.23	0.12 + 0.053*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
CKN to QN	t_{PLH}	0.91	0.85 + 0.033*SL	0.86 + 0.028*SL	0.87 + 0.027*SL
	t_{PHL}	1.03	0.95 + 0.037*SL	0.96 + 0.034*SL	0.97 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.11 + 0.063*SL	0.08 + 0.065*SL
SN to QN	t_{PHL}	0.35	0.27 + 0.039*SL	0.29 + 0.034*SL	0.30 + 0.033*SL
	t_F	0.23	0.10 + 0.062*SL	0.10 + 0.064*SL	0.08 + 0.065*SL

FD7D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.82	0.79 + 0.018*SL	0.79 + 0.015*SL	0.81 + 0.013*SL
	t_{PHL}	0.78	0.73 + 0.024*SL	0.75 + 0.019*SL	0.77 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.12 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.030*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SN to Q	t_{PLH}	0.68	0.64 + 0.018*SL	0.65 + 0.014*SL	0.67 + 0.013*SL
	t_R	0.17	0.12 + 0.025*SL	0.12 + 0.026*SL	0.09 + 0.029*SL
CKN to QN	t_{PLH}	0.99	0.95 + 0.018*SL	0.96 + 0.015*SL	0.98 + 0.013*SL
	t_{PHL}	1.09	1.05 + 0.020*SL	1.06 + 0.018*SL	1.07 + 0.016*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.030*SL	0.11 + 0.032*SL
SN to QN	t_{PHL}	0.35	0.31 + 0.023*SL	0.32 + 0.019*SL	0.34 + 0.017*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.10 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



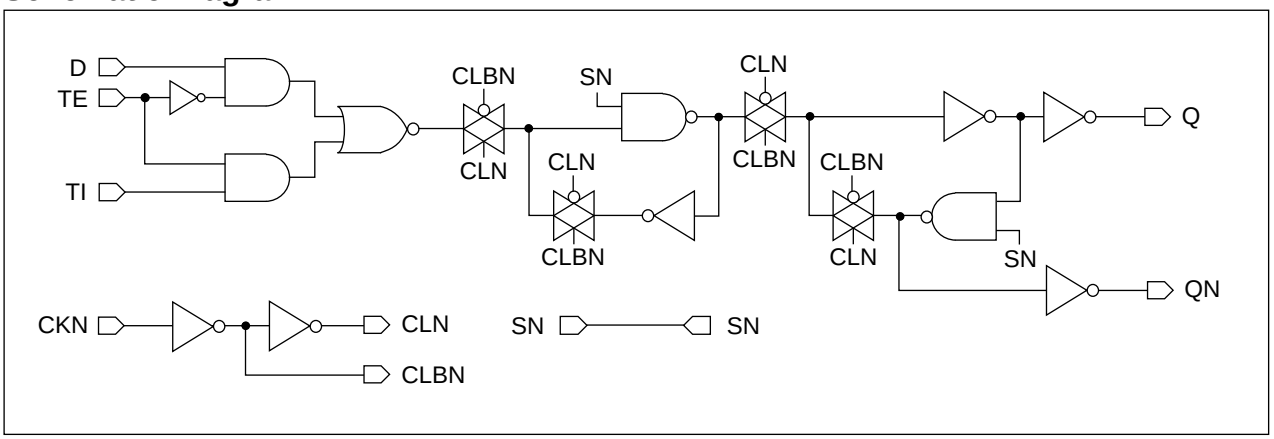
Truth Table

D	TI	TE	CKN	SN	Q (n+1)	QN (n+1)
0	x	0	↓	1	0	1
1	x	0	↓	1	1	0
x	0	1	↓	1	0	1
x	1	1	↓	1	1	0
x	x	x	x	0	1	0
x	x	x	↑	1	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
FD7S					*FD7SD2*					*FD7S*	*FD7SD2*
D	TI	TE	CKN	SN	D	TI	TE	CKN	SN		
0.6	0.6	1.1	0.6	1.3	0.6	0.6	1.1	0.6	1.3	8.3	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD7S	FD7SD2
Pulse Width Low (CKN)	t_{PWL}	0.85	0.87
Pulse Width High (CKN)	t_{PWH}	0.77	0.77
Pulse Width Low (SN)	t_{PWL}	0.85	0.85
Input Setup Time (D to CKN)	t_{SU}	0.63	0.63
Input Hold Time (D to CKN)	t_{HD}	0.46	0.46
Input Setup Time (TI to CKN)	t_{SU}	0.66	0.66
Input Hold Time (TI to CKN)	t_{HD}	0.38	0.38
Input Setup Time (TE to CKN)	t_{SU}	0.66	0.66
Input Hold Time (TE to CKN)	t_{HD}	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CKN)	t_{HD}	0.55	0.55

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD7S

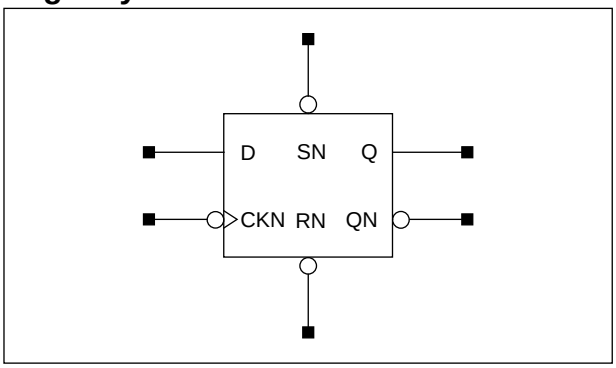
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.83	0.77 + 0.030*SL	0.78 + 0.028*SL	0.78 + 0.027*SL
	t_{PHL}	0.79	0.72 + 0.039*SL	0.73 + 0.034*SL	0.74 + 0.033*SL
	t_R	0.23	0.12 + 0.053*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
SN to Q	t_{PLH}	0.67	0.61 + 0.030*SL	0.62 + 0.027*SL	0.63 + 0.027*SL
	t_R	0.23	0.12 + 0.053*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
CKN to QN	t_{PLH}	0.93	0.86 + 0.033*SL	0.87 + 0.028*SL	0.89 + 0.027*SL
	t_{PHL}	1.04	0.97 + 0.036*SL	0.97 + 0.034*SL	0.98 + 0.033*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.063*SL	0.08 + 0.065*SL
SN to QN	t_{PHL}	0.35	0.27 + 0.038*SL	0.28 + 0.034*SL	0.30 + 0.033*SL
	t_F	0.23	0.10 + 0.062*SL	0.10 + 0.064*SL	0.08 + 0.065*SL

FD7SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.83	0.80 + 0.018*SL	0.81 + 0.015*SL	0.82 + 0.013*SL
	t_{PHL}	0.80	0.75 + 0.023*SL	0.76 + 0.019*SL	0.78 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.12 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SN to Q	t_{PLH}	0.68	0.64 + 0.018*SL	0.65 + 0.014*SL	0.67 + 0.013*SL
	t_R	0.17	0.12 + 0.025*SL	0.12 + 0.026*SL	0.10 + 0.029*SL
CKN to QN	t_{PLH}	1.00	0.96 + 0.018*SL	0.97 + 0.015*SL	0.99 + 0.013*SL
	t_{PHL}	1.11	1.06 + 0.020*SL	1.07 + 0.018*SL	1.08 + 0.016*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SN to QN	t_{PHL}	0.35	0.31 + 0.023*SL	0.32 + 0.019*SL	0.34 + 0.017*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.10 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



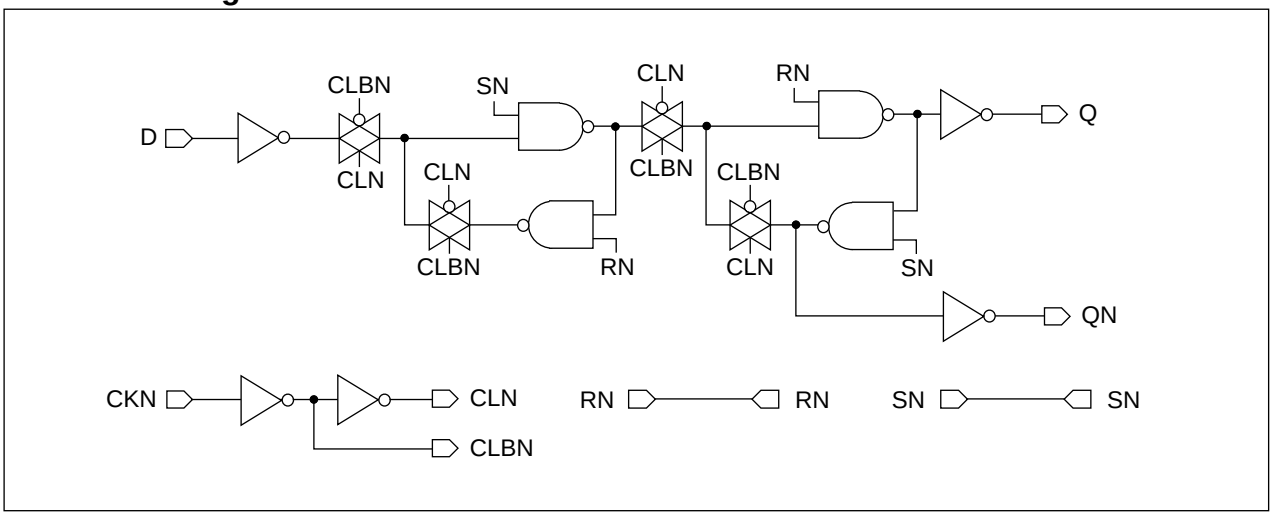
Truth Table

D	CKN	RN	SN	Q (n+1)	QN (n+1)
0	↓	1	1	0	1
1	↓	1	1	1	0
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	0	0
x	↑	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)								Gate Count	
FD8				*FD8D2*				*FD8*	*FD8D2*
D	CKN	RN	SN	D	CKN	RN	SN		
0.6	0.6	1.4	1.1	0.6	0.6	1.4	1.1	7.7	8.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD8	FD8D2
Pulse Width Low (CKN)	t_{PWL}	0.85	0.85
Pulse Width High (CKN)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Pulse Width Low (SN)	t_{PWL}	0.85	0.87
Input Setup Time (D to CKN)	t_{SU}	0.49	0.49
Input Hold Time (D to CKN)	t_{HD}	0.52	0.52
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CKN)	t_{HD}	0.87	0.87
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CKN)	t_{HD}	0.55	0.55

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD8

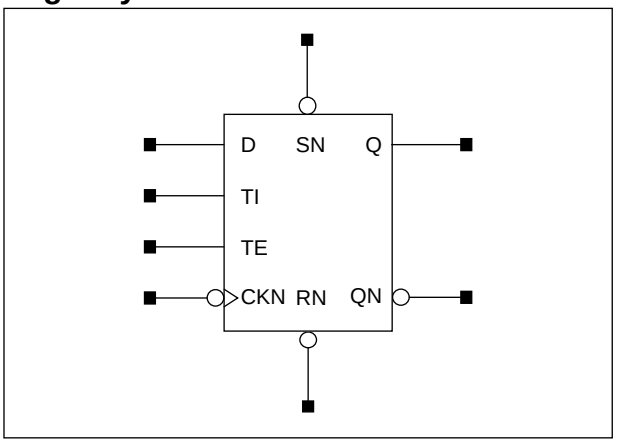
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.84	0.77 + 0.034*SL	0.79 + 0.029*SL	0.81 + 0.027*SL
	t_{PHL}	0.79	0.71 + 0.040*SL	0.73 + 0.035*SL	0.75 + 0.033*SL
	t_R	0.25	0.14 + 0.058*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q	t_{PLH}	0.33	0.26 + 0.034*SL	0.28 + 0.028*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_R	0.24	0.13 + 0.057*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.063*SL	0.11 + 0.064*SL	0.09 + 0.065*SL
SN to Q	t_{PLH}	0.73	0.66 + 0.034*SL	0.67 + 0.029*SL	0.69 + 0.027*SL
	t_R	0.25	0.14 + 0.056*SL	0.14 + 0.056*SL	0.11 + 0.060*SL
CKN to QN	t_{PLH}	0.94	0.87 + 0.033*SL	0.88 + 0.028*SL	0.90 + 0.027*SL
	t_{PHL}	1.07	1.00 + 0.037*SL	1.01 + 0.033*SL	1.01 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.062*SL	0.09 + 0.065*SL
RN to QN	t_{PLH}	0.51	0.45 + 0.033*SL	0.46 + 0.028*SL	0.47 + 0.027*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
SN to QN	t_{PLH}	0.33	0.26 + 0.033*SL	0.27 + 0.028*SL	0.29 + 0.027*SL
	t_{PHL}	0.36	0.28 + 0.039*SL	0.29 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.10 + 0.063*SL	0.10 + 0.063*SL	0.08 + 0.065*SL

FD8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.85	0.81 + 0.022*SL	0.82 + 0.016*SL	0.85 + 0.013*SL
	t_{PHL}	0.80	0.75 + 0.024*SL	0.76 + 0.020*SL	0.79 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.19	0.13 + 0.030*SL	0.13 + 0.031*SL	0.12 + 0.032*SL
RN to Q	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.34 + 0.013*SL
	t_{PHL}	0.36	0.32 + 0.023*SL	0.33 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.11 + 0.032*SL
SN to Q	t_{PLH}	0.74	0.69 + 0.021*SL	0.71 + 0.016*SL	0.74 + 0.013*SL
	t_R	0.21	0.16 + 0.025*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
CKN to QN	t_{PLH}	1.01	0.97 + 0.018*SL	0.98 + 0.015*SL	1.00 + 0.013*SL
	t_{PHL}	1.16	1.13 + 0.019*SL	1.13 + 0.017*SL	1.14 + 0.016*SL
	t_R	0.20	0.14 + 0.026*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.19	0.13 + 0.031*SL	0.13 + 0.030*SL	0.12 + 0.032*SL
RN to QN	t_{PLH}	0.58	0.54 + 0.018*SL	0.55 + 0.015*SL	0.57 + 0.013*SL
	t_R	0.19	0.15 + 0.025*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
SN to QN	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.34 + 0.013*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.33 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.13 + 0.027*SL	0.13 + 0.028*SL	0.12 + 0.028*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.10 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



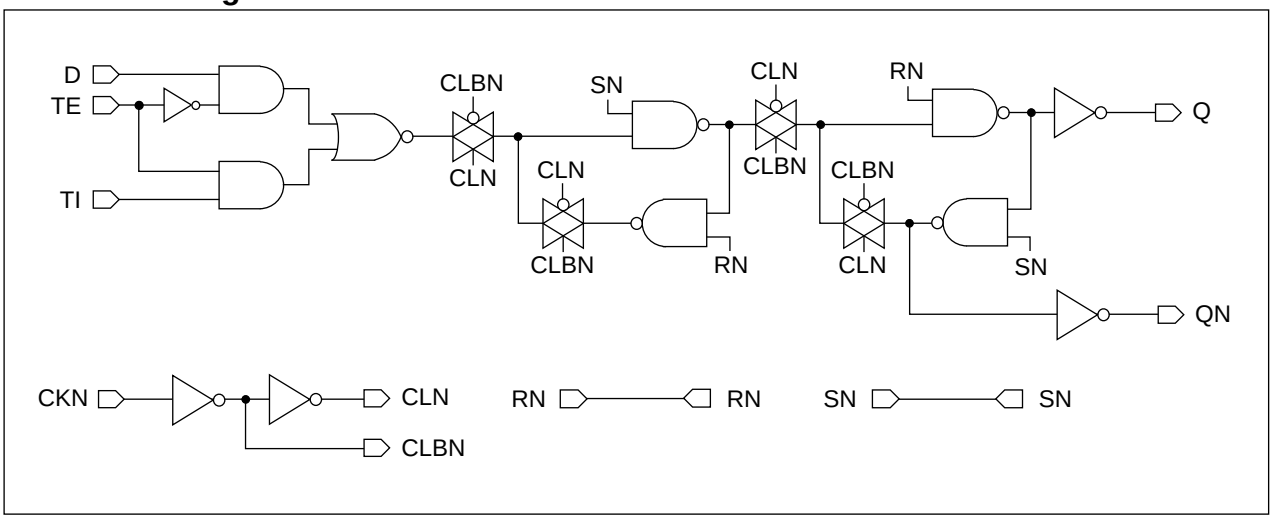
Truth Table

D	TI	TE	CKN	RN	SN	Q (n+1)	QN (n+1)
0	x	0	↓	1	1	0	1
1	x	0	↓	1	1	1	0
x	0	1	↓	1	1	0	1
x	1	1	↓	1	1	1	0
x	x	x	x	1	0	1	0
x	x	x	x	0	1	0	1
x	x	x	x	0	0	0	0
x	x	x	↑	1	1	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count
FD8S						*FD8S*
D	TI	TE	CKN	RN	SN	
0.6	0.6	1.1	0.6	1.6	1.6	9.3
FD8SD2						*FD8SD2*
D	TI	TE	CKN	RN	SN	
0.6	0.6	1.1	0.6	1.6	1.6	10.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FD8S	FD8SD2
Pulse Width Low (CKN)	t_{PWL}	0.85	0.87
Pulse Width High (CKN)	t_{PWH}	0.77	0.77
Pulse Width Low (RN)	t_{PWL}	0.77	0.77
Pulse Width Low (SN)	t_{PWL}	0.85	0.87
Input Setup Time (D to CKN)	t_{SU}	0.68	0.68
Input Hold Time (D to CKN)	t_{HD}	0.44	0.44
Input Setup Time (TI to CKN)	t_{SU}	0.68	0.68
Input Hold Time (TI to CKN)	t_{HD}	0.38	0.38
Input Setup Time (TE to CKN)	t_{SU}	0.68	0.68
Input Hold Time (TE to CKN)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CKN)	t_{HD}	0.87	0.87
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CKN)	t_{HD}	0.55	0.55

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD8S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.86	0.79 + 0.035*SL	0.80 + 0.029*SL	0.83 + 0.027*SL
	t_{PHL}	0.80	0.72 + 0.040*SL	0.74 + 0.034*SL	0.75 + 0.033*SL
	t_R	0.25	0.14 + 0.056*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q	t_{PLH}	0.33	0.26 + 0.034*SL	0.28 + 0.028*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.063*SL	0.11 + 0.064*SL	0.09 + 0.065*SL
SN to Q	t_{PLH}	0.73	0.66 + 0.034*SL	0.67 + 0.029*SL	0.69 + 0.027*SL
	t_R	0.25	0.14 + 0.056*SL	0.14 + 0.056*SL	0.11 + 0.060*SL
CKN to QN	t_{PLH}	0.94	0.88 + 0.033*SL	0.89 + 0.028*SL	0.91 + 0.027*SL
	t_{PHL}	1.09	1.01 + 0.036*SL	1.02 + 0.034*SL	1.03 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to QN	t_{PLH}	0.51	0.44 + 0.033*SL	0.46 + 0.028*SL	0.47 + 0.027*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
SN to QN	t_{PLH}	0.33	0.26 + 0.033*SL	0.27 + 0.028*SL	0.29 + 0.027*SL
	t_{PHL}	0.36	0.28 + 0.039*SL	0.29 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.24	0.12 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.10 + 0.062*SL	0.10 + 0.064*SL	0.08 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FD8SD2

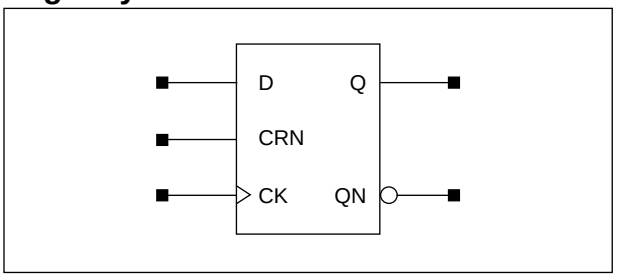
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CKN to Q	t_{PLH}	0.87	0.82 + 0.022*SL	0.84 + 0.017*SL	0.87 + 0.013*SL
	t_{PHL}	0.81	0.76 + 0.024*SL	0.77 + 0.019*SL	0.80 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.19	0.13 + 0.030*SL	0.13 + 0.031*SL	0.12 + 0.032*SL
RN to Q	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.34 + 0.013*SL
	t_{PHL}	0.36	0.32 + 0.023*SL	0.33 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.18	0.11 + 0.031*SL	0.11 + 0.031*SL	0.11 + 0.032*SL
SN to Q	t_{PLH}	0.74	0.69 + 0.021*SL	0.71 + 0.016*SL	0.74 + 0.013*SL
	t_R	0.21	0.15 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
CKN to QN	t_{PLH}	1.02	0.98 + 0.018*SL	0.99 + 0.015*SL	1.01 + 0.013*SL
	t_{PHL}	1.18	1.14 + 0.019*SL	1.15 + 0.017*SL	1.15 + 0.016*SL
	t_R	0.20	0.14 + 0.027*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.19	0.13 + 0.031*SL	0.13 + 0.030*SL	0.12 + 0.032*SL
RN to QN	t_{PLH}	0.58	0.54 + 0.018*SL	0.55 + 0.015*SL	0.57 + 0.013*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
SN to QN	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.34 + 0.013*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.33 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.13 + 0.028*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.031*SL	0.10 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

FDS2/FDS2D2

D Flip-Flop with Synchronous Clear, 1X/2X Drive

Logic Symbol



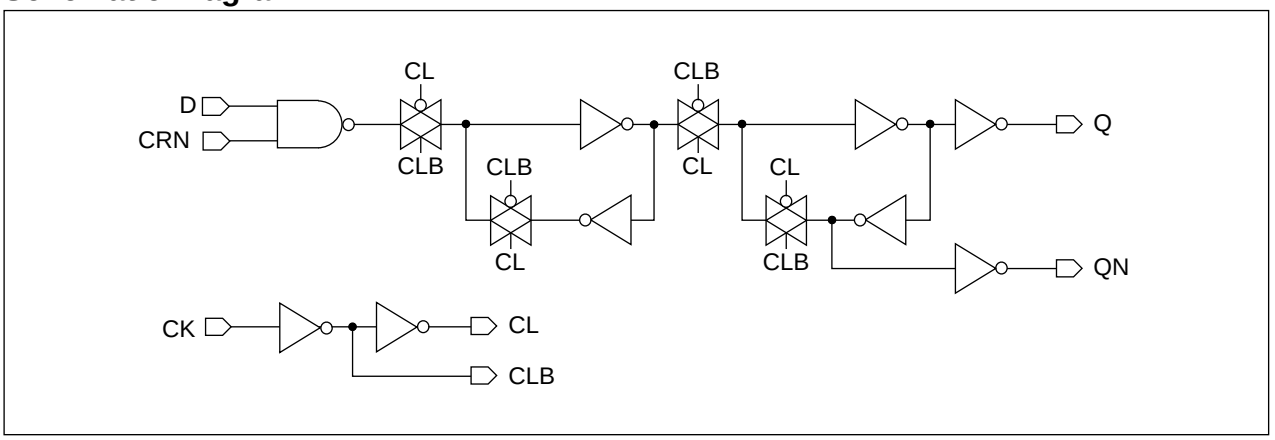
Truth Table

D	CRN	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	0	1
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FDS2			*FDS2D2*			*FDS2*	*FDS2D2*
D	CRN	CK	D	CRN	CK		
0.7	0.6	0.6	0.7	0.6	0.6	6.0	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FDS2	FDS2D2
Pulse Width Low (CK)	t_{PWL}	0.82	0.82
Pulse Width High (CK)	t_{PWH}	0.77	0.77
Input Setup Time (D to CK)	t_{SU}	0.57	0.57
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (CRN to CK)	t_{SU}	0.57	0.57
Input Hold Time (CRN to CK)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FDS2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.57 + 0.030*SL	0.58 + 0.028*SL	0.59 + 0.027*SL
	t_{PHL}	0.71	0.63 + 0.039*SL	0.65 + 0.035*SL	0.66 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to QN	t_{PLH}	0.77	0.71 + 0.027*SL	0.71 + 0.027*SL	0.71 + 0.027*SL
	t_{PHL}	0.79	0.72 + 0.035*SL	0.73 + 0.033*SL	0.73 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

FDS2D2

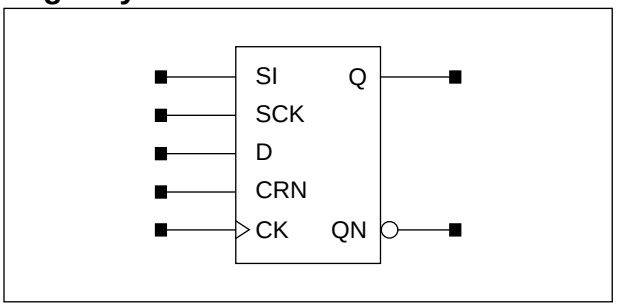
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.63	0.59 + 0.018*SL	0.60 + 0.015*SL	0.62 + 0.013*SL
	t_{PHL}	0.71	0.66 + 0.024*SL	0.67 + 0.019*SL	0.70 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
CK to QN	t_{PLH}	0.83	0.81 + 0.014*SL	0.81 + 0.013*SL	0.81 + 0.013*SL
	t_{PHL}	0.86	0.82 + 0.019*SL	0.83 + 0.017*SL	0.84 + 0.016*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

FDS2CS/FDS2CSD2

D Flip-Flop with Synchronous Clear, Scan Clock, 1X/2X Drive

Logic Symbol



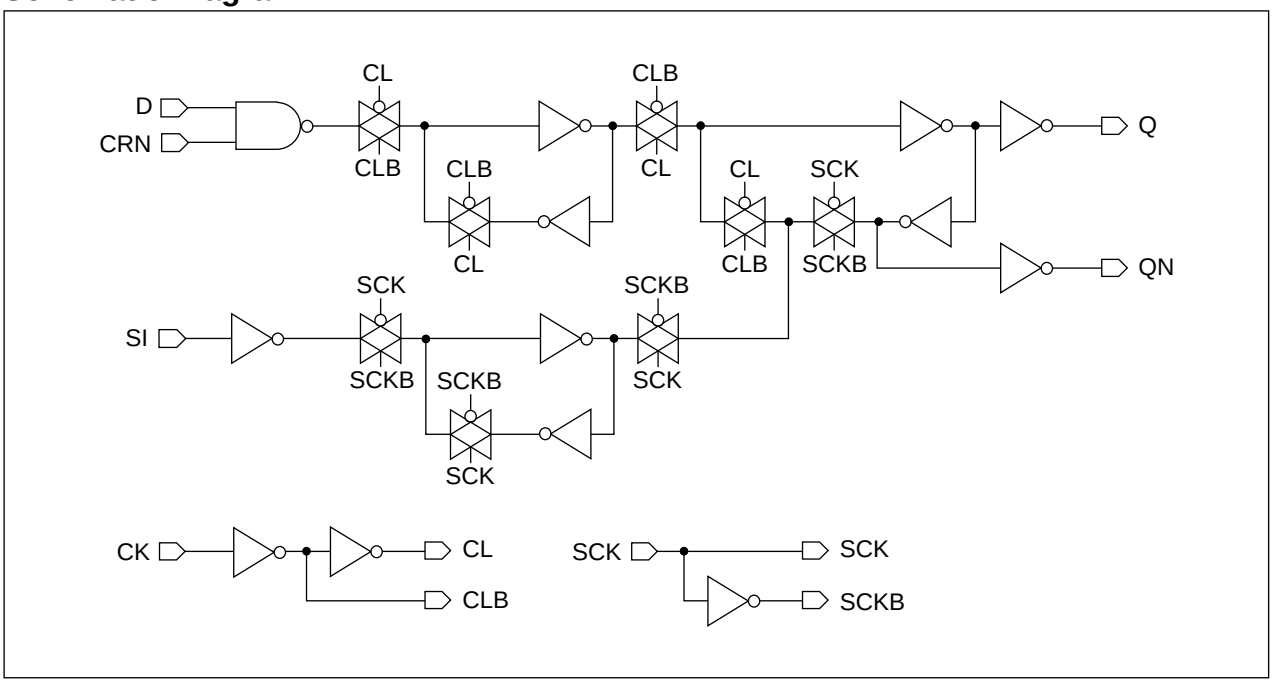
Truth Table

SI	SCK	D	CRN	CK	Q (n+1)	QN (n+1)
x	0	0	1	↑	0	1
x	0	1	1	↑	1	0
0	↑	x	1	0	0	1
1	↑	x	1	0	1	0
x	x	x	0	↑	0	1

Cell Data

Input Load (SL)										Gate Count	
FDS2CS					*FDS2CSD2*					*FDS2CS*	*FDS2CS D2*
SI	SCK	D	CRN	CK	SI	SCK	D	CRN	CK		
0.5	1.2	0.5	0.5	0.5	0.5	1.2	0.5	0.5	0.5	9.3	9.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FDS2CS	FDS2CSD2
Pulse Width Low (CK)	t_{PWL}	0.82	0.82
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (SCK)	t_{PWL}	0.79	0.79
Pulse Width High (SCK)	t_{PWH}	0.79	0.79
Input Setup Time (D to CK)	t_{SU}	0.57	0.57
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (SI to SCK)	t_{SU}	0.71	0.71
Input Hold Time (SI to SCK)	t_{HD}	0.33	0.33
Input Setup Time (CRN to CK)	t_{SU}	0.33	0.33
Input Hold Time (CRN to CK)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FDS2CS

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.58 + 0.030*SL	0.58 + 0.028*SL	0.59 + 0.027*SL
	t_{PHL}	0.70	0.63 + 0.039*SL	0.64 + 0.035*SL	0.66 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.10 + 0.065*SL
SCK to Q	t_{PLH}	0.66	0.60 + 0.032*SL	0.61 + 0.028*SL	0.62 + 0.027*SL
	t_{PHL}	0.60	0.52 + 0.040*SL	0.53 + 0.035*SL	0.55 + 0.033*SL
	t_R	0.25	0.14 + 0.054*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
CK to QN	t_{PLH}	0.82	0.76 + 0.032*SL	0.77 + 0.028*SL	0.78 + 0.027*SL
	t_{PHL}	0.88	0.80 + 0.039*SL	0.81 + 0.035*SL	0.83 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.25	0.12 + 0.064*SL	0.12 + 0.064*SL	0.11 + 0.065*SL
SCK to QN	t_{PLH}	0.65	0.59 + 0.028*SL	0.60 + 0.027*SL	0.60 + 0.027*SL
	t_{PHL}	0.83	0.76 + 0.035*SL	0.76 + 0.033*SL	0.77 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.064*SL	0.10 + 0.064*SL	0.08 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

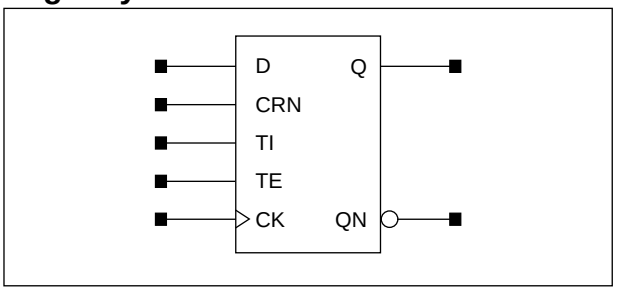
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FDS2CSD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.64	0.61 + 0.018*SL	0.62 + 0.015*SL	0.63 + 0.013*SL
	t_{PHL}	0.70	0.66 + 0.024*SL	0.67 + 0.019*SL	0.69 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SCK to Q	t_{PLH}	0.68	0.64 + 0.019*SL	0.65 + 0.015*SL	0.67 + 0.013*SL
	t_{PHL}	0.60	0.56 + 0.024*SL	0.57 + 0.019*SL	0.60 + 0.017*SL
	t_R	0.20	0.15 + 0.025*SL	0.15 + 0.025*SL	0.12 + 0.028*SL
	t_F	0.19	0.12 + 0.031*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
CK to QN	t_{PLH}	0.88	0.85 + 0.016*SL	0.86 + 0.014*SL	0.87 + 0.013*SL
	t_{PHL}	0.94	0.90 + 0.022*SL	0.91 + 0.018*SL	0.93 + 0.017*SL
	t_R	0.19	0.13 + 0.026*SL	0.13 + 0.026*SL	0.11 + 0.028*SL
	t_F	0.20	0.13 + 0.032*SL	0.13 + 0.031*SL	0.13 + 0.032*SL
SCK to QN	t_{PLH}	0.72	0.69 + 0.014*SL	0.70 + 0.013*SL	0.70 + 0.013*SL
	t_{PHL}	0.92	0.88 + 0.017*SL	0.88 + 0.017*SL	0.89 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.030*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



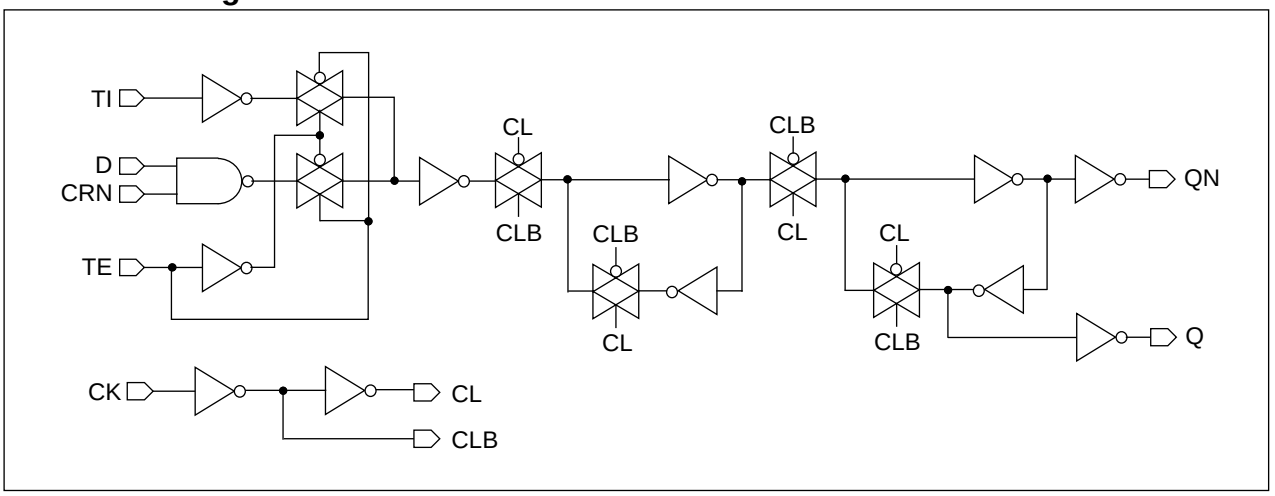
Truth Table

D	CRN	TI	TE	CK	Q (n+1)	QN (n+1)
0	1	x	0	↑	0	1
1	1	x	0	↑	1	0
x	0	x	0	↑	0	1
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0
x	x	x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)										Gate Count	
FDS2S					*FDS2SD2*					*FDS2S*	*FDS2SD2*
D	CRN	TI	TE	CK	D	CRN	TI	TE	CK		
0.6	0.6	0.6	1.3	0.6	0.6	0.6	0.6	1.3	0.6	8.0	8.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FDS2S	FDS2SD2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.77	0.77
Input Setup Time (D to CK)	t_{SU}	0.74	0.74
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (CRN to CK)	t_{SU}	0.74	0.74
Input Hold Time (CRN to CK)	t_{HD}	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.71	0.71
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.63	0.63
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FDS2S

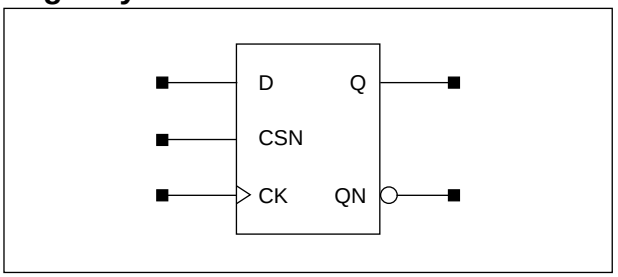
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.76	0.71 + 0.028*SL	0.71 + 0.027*SL	0.71 + 0.027*SL
	t_{PHL}	0.79	0.72 + 0.036*SL	0.73 + 0.033*SL	0.73 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
CK to QN	t_{PLH}	0.63	0.57 + 0.030*SL	0.58 + 0.028*SL	0.58 + 0.027*SL
	t_{PHL}	0.71	0.63 + 0.040*SL	0.64 + 0.035*SL	0.66 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

FDS2SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.83	0.80 + 0.014*SL	0.80 + 0.013*SL	0.80 + 0.013*SL
	t_{PHL}	0.86	0.82 + 0.019*SL	0.83 + 0.017*SL	0.83 + 0.016*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
CK to QN	t_{PLH}	0.63	0.59 + 0.018*SL	0.60 + 0.015*SL	0.62 + 0.013*SL
	t_{PHL}	0.70	0.66 + 0.023*SL	0.67 + 0.019*SL	0.69 + 0.017*SL
	t_R	0.17	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Logic Symbol



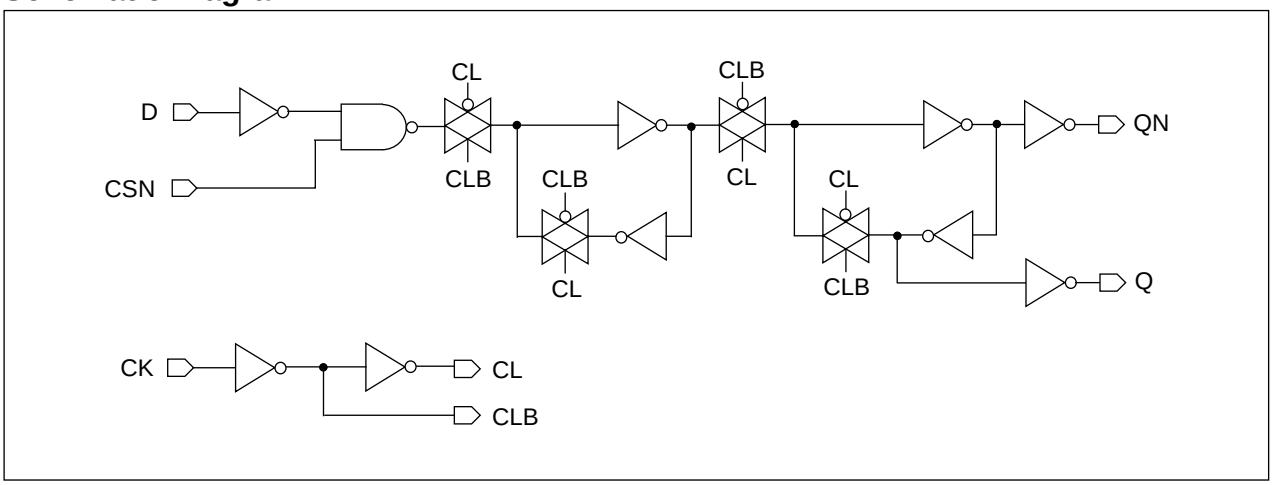
Truth Table

D	CSN	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	↑	1	0
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FDS3			*FDS3D2*			*FDS3*	*FDS3D2*
D	CSN	CK	D	CSN	CK		
0.6	0.4	0.6	0.6	0.4	0.6	6.3	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FDS2	FDS2D2
Pulse Width Low (CK)	t_{PWL}	0.82	0.82
Pulse Width High (CK)	t_{PWH}	0.77	0.77
Input Setup Time (D to CK)	t_{SU}	0.57	0.57
Input Hold Time (D to CK)	t_{HD}	0.33	0.33
Input Setup Time (CSN to CK)	t_{SU}	0.57	0.57
Input Hold Time (CSN to CK)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FDS3

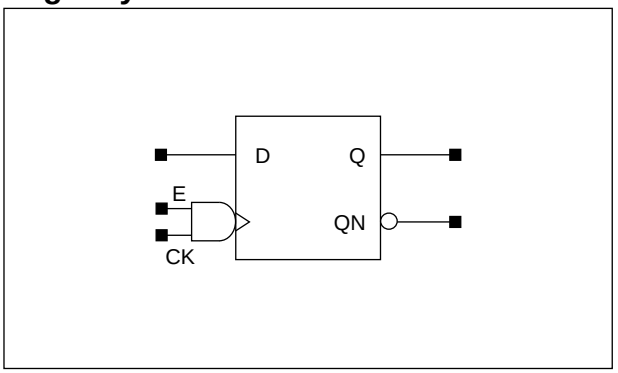
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.77	0.71 + 0.028*SL	0.72 + 0.027*SL	0.72 + 0.027*SL
	t_{PHL}	0.80	0.73 + 0.035*SL	0.73 + 0.033*SL	0.73 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
CK to QN	t_{PLH}	0.63	0.57 + 0.030*SL	0.58 + 0.028*SL	0.59 + 0.027*SL
	t_{PHL}	0.71	0.64 + 0.039*SL	0.65 + 0.035*SL	0.66 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

FDS3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.84	0.81 + 0.014*SL	0.81 + 0.013*SL	0.81 + 0.013*SL
	t_{PHL}	0.86	0.83 + 0.019*SL	0.83 + 0.017*SL	0.84 + 0.016*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
CK to QN	t_{PLH}	0.63	0.60 + 0.018*SL	0.61 + 0.015*SL	0.62 + 0.013*SL
	t_{PHL}	0.71	0.66 + 0.024*SL	0.68 + 0.019*SL	0.70 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Logic Symbol



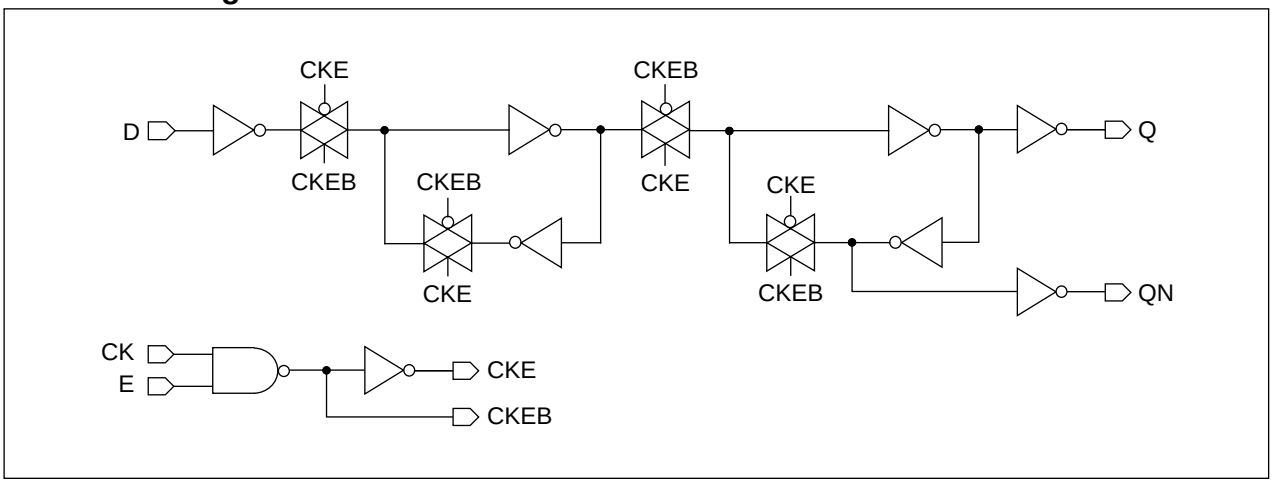
Truth Table

D	E	CK	Q (n+1)	QN (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	x	Q (n)	QN (n)
x	x	↓	Q (n)	QN (n)

Cell Data

Input Load (SL)			Gate Count
D	E	CK	
0.6	0.6	0.6	5.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (CK)	t_{PWL}	0.82
Pulse Width High (CK)	t_{PWH}	0.79
Pulse Width Low (E)	t_{PWL}	0.79
Pulse Width High (E)	t_{PWH}	0.79
Input Setup Time (D to CK)	t_{SU}	0.44
Input Hold Time (D to CK)	t_{HD}	0.33
Input Setup Time (D to E)	t_{SU}	0.41
Input Hold Time (D to E)	t_{HD}	0.33

FG1

D Flip-Flop with CK Enable

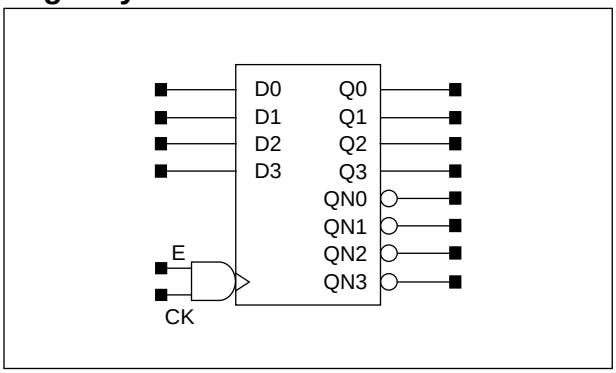
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.70	0.64 + 0.031*SL	0.65 + 0.028*SL	0.66 + 0.027*SL
	t_{PHL}	0.77	0.69 + 0.039*SL	0.71 + 0.034*SL	0.72 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
E to Q	t_{PLH}	0.72	0.66 + 0.030*SL	0.67 + 0.028*SL	0.68 + 0.027*SL
	t_{PHL}	0.80	0.72 + 0.040*SL	0.73 + 0.034*SL	0.75 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to QN	t_{PLH}	0.83	0.77 + 0.028*SL	0.78 + 0.027*SL	0.78 + 0.027*SL
	t_{PHL}	0.86	0.79 + 0.036*SL	0.80 + 0.033*SL	0.80 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
E to QN	t_{PLH}	0.85	0.79 + 0.028*SL	0.80 + 0.027*SL	0.80 + 0.027*SL
	t_{PHL}	0.89	0.82 + 0.035*SL	0.82 + 0.033*SL	0.82 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

Dn	E	CK	Qn (n+1)	QNn (n+1)
0	1	↑	0	1
1	1	↑	1	0
x	0	x	Qn (n)	QNn (n)
x	x	↓	Qn (n)	QNn (n)

Cell Data

Input Load (SL)			Gate Count
Dn	E	CK	
0.6	0.6	0.6	18.7

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (CK)	t_{PWL}	1.59
Pulse Width High (CK)	t_{PWH}	1.09
Pulse Width Low (E)	t_{PWL}	1.48
Pulse Width High (E)	t_{PWH}	1.12
Input Setup Time (D0 to CK)	t_{SU}	0.33
Input Hold Time (D0 to CK)	t_{HD}	0.71
Input Setup Time (D0 to E)	t_{SU}	0.33
Input Hold Time (D0 to E)	t_{HD}	0.74
Input Setup Time (D1 to CK)	t_{SU}	0.33
Input Hold Time (D1 to CK)	t_{HD}	0.71
Input Setup Time (D1 to E)	t_{SU}	0.33
Input Hold Time (D1 to E)	t_{HD}	0.74
Input Setup Time (D2 to CK)	t_{SU}	0.33
Input Hold Time (D2 to CK)	t_{HD}	0.71
Input Setup Time (D2 to E)	t_{SU}	0.33
Input Hold Time (D2 to E)	t_{HD}	0.74
Input Setup Time (D3 to CK)	t_{SU}	0.33
Input Hold Time (D3 to CK)	t_{HD}	0.74
Input Setup Time (D3 to E)	t_{SU}	0.36
Input Hold Time (D3 to E)	t_{HD}	0.74

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	1.02	0.96 + 0.030*SL	0.96 + 0.028*SL	0.97 + 0.027*SL
	t_{PHL}	1.38	1.30 + 0.040*SL	1.31 + 0.034*SL	1.33 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
E to Q0	t_{PLH}	1.04	0.98 + 0.030*SL	0.98 + 0.028*SL	0.99 + 0.027*SL
	t_{PHL}	1.40	1.32 + 0.040*SL	1.33 + 0.034*SL	1.35 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q1	t_{PLH}	1.02	0.96 + 0.030*SL	0.96 + 0.028*SL	0.97 + 0.027*SL
	t_{PHL}	1.38	1.30 + 0.040*SL	1.31 + 0.034*SL	1.33 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
E to Q1	t_{PLH}	1.04	0.98 + 0.030*SL	0.99 + 0.028*SL	0.99 + 0.027*SL
	t_{PHL}	1.40	1.32 + 0.040*SL	1.33 + 0.034*SL	1.35 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q2	t_{PLH}	1.02	0.96 + 0.030*SL	0.96 + 0.028*SL	0.97 + 0.027*SL
	t_{PHL}	1.38	1.30 + 0.040*SL	1.31 + 0.034*SL	1.33 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
E to Q2	t_{PLH}	1.04	0.98 + 0.030*SL	0.98 + 0.028*SL	0.99 + 0.027*SL
	t_{PHL}	1.40	1.32 + 0.040*SL	1.33 + 0.034*SL	1.35 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q3	t_{PLH}	1.02	0.96 + 0.030*SL	0.96 + 0.028*SL	0.97 + 0.027*SL
	t_{PHL}	1.38	1.30 + 0.039*SL	1.31 + 0.034*SL	1.33 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
E to Q3	t_{PLH}	1.04	0.98 + 0.030*SL	0.98 + 0.028*SL	0.99 + 0.027*SL
	t_{PHL}	1.40	1.32 + 0.040*SL	1.33 + 0.034*SL	1.35 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to QN0	t_{PLH}	1.43	1.38 + 0.028*SL	1.38 + 0.027*SL	1.38 + 0.027*SL
	t_{PHL}	1.18	1.11 + 0.035*SL	1.12 + 0.033*SL	1.12 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
E to QN0	t_{PLH}	1.45	1.40 + 0.028*SL	1.40 + 0.027*SL	1.40 + 0.027*SL
	t_{PHL}	1.20	1.13 + 0.035*SL	1.14 + 0.033*SL	1.14 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

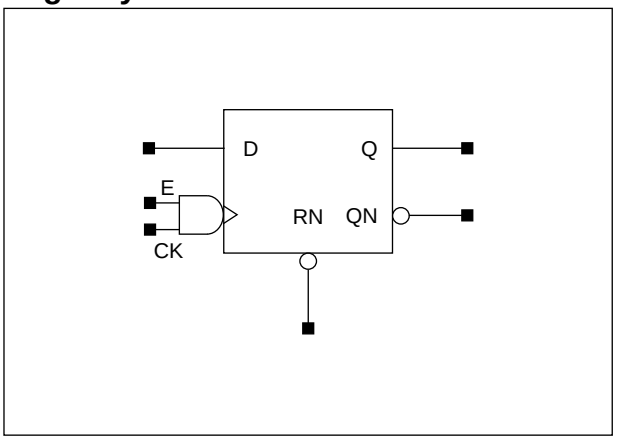
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN1	t_{PLH}	1.43	1.38 + 0.028*SL	1.38 + 0.027*SL	1.38 + 0.027*SL
	t_{PHL}	1.18	1.11 + 0.035*SL	1.12 + 0.033*SL	1.12 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
E to QN1	t_{PLH}	1.45	1.40 + 0.028*SL	1.40 + 0.027*SL	1.40 + 0.027*SL
	t_{PHL}	1.20	1.13 + 0.035*SL	1.14 + 0.033*SL	1.14 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
CK to QN2	t_{PLH}	1.43	1.38 + 0.028*SL	1.38 + 0.027*SL	1.38 + 0.027*SL
	t_{PHL}	1.18	1.11 + 0.035*SL	1.12 + 0.033*SL	1.12 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
E to QN2	t_{PLH}	1.45	1.40 + 0.028*SL	1.40 + 0.027*SL	1.40 + 0.027*SL
	t_{PHL}	1.20	1.13 + 0.035*SL	1.14 + 0.033*SL	1.14 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.064*SL	0.10 + 0.063*SL	0.07 + 0.066*SL
CK to QN3	t_{PLH}	1.43	1.37 + 0.028*SL	1.38 + 0.027*SL	1.38 + 0.027*SL
	t_{PHL}	1.18	1.11 + 0.035*SL	1.11 + 0.033*SL	1.12 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
E to QN3	t_{PLH}	1.45	1.40 + 0.028*SL	1.40 + 0.027*SL	1.40 + 0.027*SL
	t_{PHL}	1.20	1.13 + 0.035*SL	1.14 + 0.033*SL	1.14 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

FG2

D Flip-Flop with CK Enable, Reset

Logic Symbol



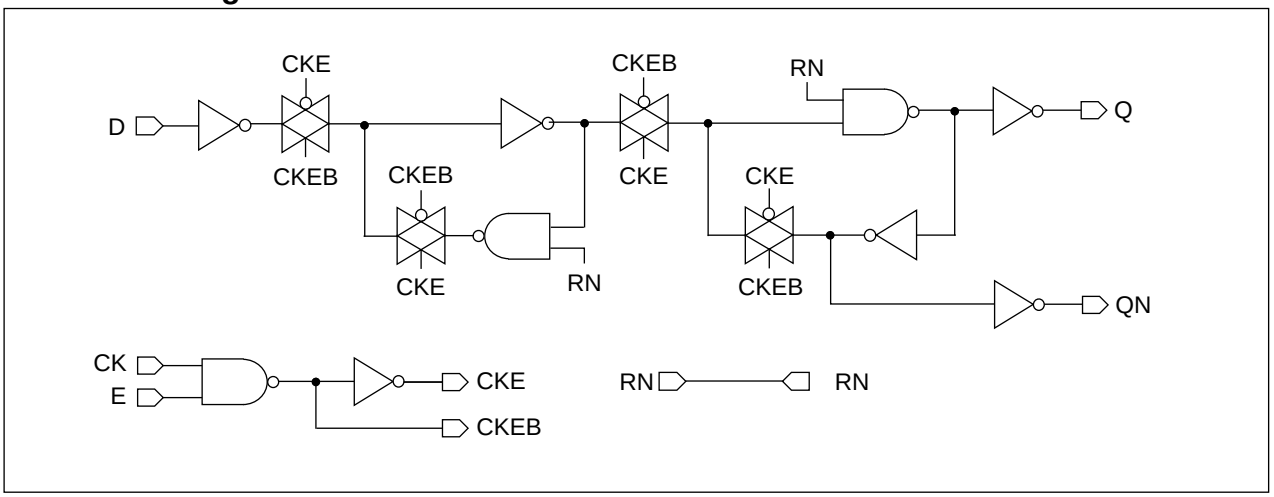
Truth Table

D	E	CK	RN	Q (n+1)	QN (n+1)
0	1	↑	1	0	1
1	1	↑	1	1	0
x	0	x	1	Q (n)	QN (n)
x	x	x	0	0	1
x	x	↓	1	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count
D	E	CK	RN	
0.6	0.6	0.6	1.1	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (CK)	t_{PWL}	0.82
Pulse Width High (CK)	t_{PWH}	0.79
Pulse Width Low (E)	t_{PWL}	0.79
Pulse Width High (E)	t_{PWH}	0.79
Pulse Width Low (RN)	t_{PWL}	0.79
Input Setup Time (D to CK)	t_{SU}	0.44
Input Hold Time (D to CK)	t_{HD}	0.33
Input Setup Time (D to E)	t_{SU}	0.44
Input Hold Time (D to E)	t_{HD}	0.33
Recovery Time (RN)	t_{RC}	0.33
Input Hold Time (RN to CK)	t_{HD}	0.76
Recovery Time (RN to E)	t_{RC}	0.33
Input Hold Time (RN to E)	t_{HD}	0.76

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

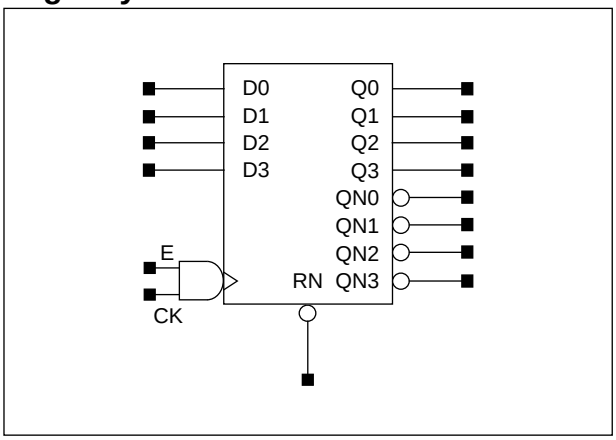
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.76	0.69 + 0.035*SL	0.71 + 0.030*SL	0.73 + 0.027*SL
	t_{PHL}	0.81	0.73 + 0.040*SL	0.74 + 0.034*SL	0.76 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.063*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
E to Q	t_{PLH}	0.78	0.72 + 0.035*SL	0.73 + 0.029*SL	0.75 + 0.027*SL
	t_{PHL}	0.83	0.75 + 0.040*SL	0.76 + 0.035*SL	0.78 + 0.033*SL
	t_R	0.25	0.14 + 0.058*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.063*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q	t_{PHL}	0.37	0.29 + 0.040*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to QN	t_{PLH}	0.86	0.81 + 0.029*SL	0.81 + 0.027*SL	0.81 + 0.027*SL
	t_{PHL}	0.94	0.87 + 0.035*SL	0.87 + 0.033*SL	0.87 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.07 + 0.066*SL
E to QN	t_{PLH}	0.89	0.83 + 0.028*SL	0.83 + 0.027*SL	0.83 + 0.027*SL
	t_{PHL}	0.96	0.89 + 0.035*SL	0.89 + 0.033*SL	0.90 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.07 + 0.066*SL
RN to QN	t_{PLH}	0.43	0.37 + 0.028*SL	0.37 + 0.027*SL	0.37 + 0.027*SL
	t_R	0.20	0.09 + 0.055*SL	0.08 + 0.059*SL	0.07 + 0.060*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

FG2X4

4-Bit D Flip-Flop with CK Enable, Reset

Logic Symbol



Truth Table

Dn	E	CK	RN	Qn (n+1)	QNn (n+1)
0	1	↑	1	0	1
1	1	↑	1	1	0
x	0	x	1	Qn (n)	QNn (n)
x	x	x	0	0	1
x	x	↓	1	Qn (n)	QNn (n)

Cell Data

Input Load (SL)				Gate Count
Dn	E	CK	RN	
0.6	0.6	0.6	0.6	22.7

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (CK)	t_{PWL}	1.67
Pulse Width High (CK)	t_{PWH}	1.15
Pulse Width Low (E)	t_{PWL}	1.61
Pulse Width High (E)	t_{PWH}	1.18
Pulse Width Low (RN)	t_{PWL}	0.79
Input Setup Time (D0 to CK)	t_{SU}	0.41
Input Hold Time (D0 to CK)	t_{HD}	0.75
Input Setup Time (D0 to E)	t_{SU}	0.33
Input Hold Time (D0 to E)	t_{HD}	0.79
Input Setup Time (D1 to CK)	t_{SU}	0.33
Input Hold Time (D1 to CK)	t_{HD}	0.76
Input Setup Time (D1 to E)	t_{SU}	0.33
Input Hold Time (D1 to E)	t_{HD}	0.76
Input Setup Time (D2 to CK)	t_{SU}	0.36
Input Hold Time (D2 to CK)	t_{HD}	0.76
Input Setup Time (D2 to E)	t_{SU}	0.74
Input Hold Time (D2 to E)	t_{HD}	0.76
Input Setup Time (D3 to CK)	t_{SU}	0.52
Input Hold Time (D3 to CK)	t_{HD}	0.74
Input Setup Time (D3 to E)	t_{SU}	0.33
Input Hold Time (D3 to E)	t_{HD}	0.76
Recovery Time (RN)	t_{RC}	0.33
Input Hold Time (RN to CK)	t_{HD}	1.09
Recovery Time (RN to E)	t_{RC}	0.33
Input Hold Time (RN to E)	t_{HD}	1.15

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q0	t_{PLH}	1.11	1.04 + 0.035*SL	1.05 + 0.030*SL	1.08 + 0.027*SL
	t_{PHL}	1.47	1.39 + 0.040*SL	1.40 + 0.035*SL	1.42 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.062*SL	0.09 + 0.065*SL
E to Q0	t_{PLH}	1.13	1.06 + 0.035*SL	1.07 + 0.030*SL	1.10 + 0.027*SL
	t_{PHL}	1.49	1.41 + 0.040*SL	1.42 + 0.035*SL	1.44 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q0	t_{PHL}	0.37	0.29 + 0.040*SL	0.31 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q1	t_{PLH}	1.11	1.04 + 0.035*SL	1.05 + 0.030*SL	1.08 + 0.027*SL
	t_{PHL}	1.47	1.38 + 0.040*SL	1.40 + 0.035*SL	1.42 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.062*SL	0.09 + 0.065*SL
E to Q1	t_{PLH}	1.13	1.06 + 0.035*SL	1.07 + 0.030*SL	1.10 + 0.027*SL
	t_{PHL}	1.49	1.41 + 0.040*SL	1.42 + 0.035*SL	1.44 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q1	t_{PHL}	0.37	0.29 + 0.040*SL	0.31 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q2	t_{PLH}	1.11	1.04 + 0.035*SL	1.05 + 0.030*SL	1.08 + 0.027*SL
	t_{PHL}	1.47	1.39 + 0.040*SL	1.40 + 0.035*SL	1.42 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.062*SL	0.09 + 0.065*SL
E to Q2	t_{PLH}	1.13	1.06 + 0.035*SL	1.07 + 0.030*SL	1.10 + 0.027*SL
	t_{PHL}	1.49	1.41 + 0.040*SL	1.42 + 0.035*SL	1.44 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.25	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q2	t_{PHL}	0.37	0.29 + 0.040*SL	0.31 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
CK to Q3	t_{PLH}	1.10	1.03 + 0.035*SL	1.05 + 0.030*SL	1.07 + 0.027*SL
	t_{PHL}	1.46	1.38 + 0.040*SL	1.40 + 0.035*SL	1.41 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
E to Q3	t_{PLH}	1.13	1.06 + 0.035*SL	1.07 + 0.030*SL	1.10 + 0.027*SL
	t_{PHL}	1.49	1.40 + 0.040*SL	1.42 + 0.035*SL	1.44 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q3	t_{PHL}	0.37	0.29 + 0.040*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

(Continued)

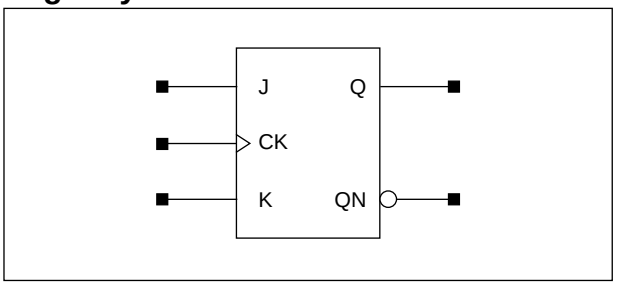
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to QN0	t_{PLH}	1.52	1.47 + 0.028*SL	1.47 + 0.027*SL	1.47 + 0.027*SL
	t_{PHL}	1.28	1.21 + 0.035*SL	1.21 + 0.033*SL	1.22 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.08 + 0.066*SL
E to QN0	t_{PLH}	1.54	1.49 + 0.028*SL	1.49 + 0.027*SL	1.49 + 0.027*SL
	t_{PHL}	1.30	1.23 + 0.035*SL	1.23 + 0.033*SL	1.24 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.23	0.10 + 0.061*SL	0.10 + 0.063*SL	0.08 + 0.066*SL
RN to QN0	t_{PLH}	0.43	0.38 + 0.028*SL	0.38 + 0.027*SL	0.38 + 0.027*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
CK to QN1	t_{PLH}	1.52	1.47 + 0.028*SL	1.47 + 0.027*SL	1.47 + 0.027*SL
	t_{PHL}	1.28	1.21 + 0.035*SL	1.21 + 0.033*SL	1.22 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.08 + 0.065*SL
E to QN1	t_{PLH}	1.54	1.49 + 0.028*SL	1.49 + 0.027*SL	1.49 + 0.027*SL
	t_{PHL}	1.30	1.23 + 0.035*SL	1.23 + 0.033*SL	1.24 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.08 + 0.065*SL
RN to QN1	t_{PLH}	0.43	0.38 + 0.028*SL	0.38 + 0.027*SL	0.38 + 0.027*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
CK to QN2	t_{PLH}	1.52	1.47 + 0.028*SL	1.47 + 0.027*SL	1.47 + 0.027*SL
	t_{PHL}	1.28	1.21 + 0.035*SL	1.21 + 0.033*SL	1.22 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.08 + 0.066*SL
E to QN2	t_{PLH}	1.54	1.49 + 0.028*SL	1.49 + 0.027*SL	1.49 + 0.027*SL
	t_{PHL}	1.30	1.23 + 0.035*SL	1.23 + 0.033*SL	1.24 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.23	0.10 + 0.061*SL	0.10 + 0.063*SL	0.08 + 0.066*SL
RN to QN2	t_{PLH}	0.43	0.38 + 0.028*SL	0.38 + 0.027*SL	0.38 + 0.027*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
CK to QN3	t_{PLH}	1.52	1.46 + 0.028*SL	1.47 + 0.027*SL	1.47 + 0.027*SL
	t_{PHL}	1.27	1.20 + 0.035*SL	1.21 + 0.033*SL	1.21 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.063*SL	0.08 + 0.066*SL
E to QN3	t_{PLH}	1.54	1.48 + 0.028*SL	1.49 + 0.027*SL	1.49 + 0.027*SL
	t_{PHL}	1.30	1.23 + 0.035*SL	1.23 + 0.033*SL	1.23 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.08 + 0.066*SL
RN to QN3	t_{PLH}	0.43	0.37 + 0.028*SL	0.37 + 0.027*SL	0.37 + 0.027*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.059*SL	0.07 + 0.060*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Logic Symbol



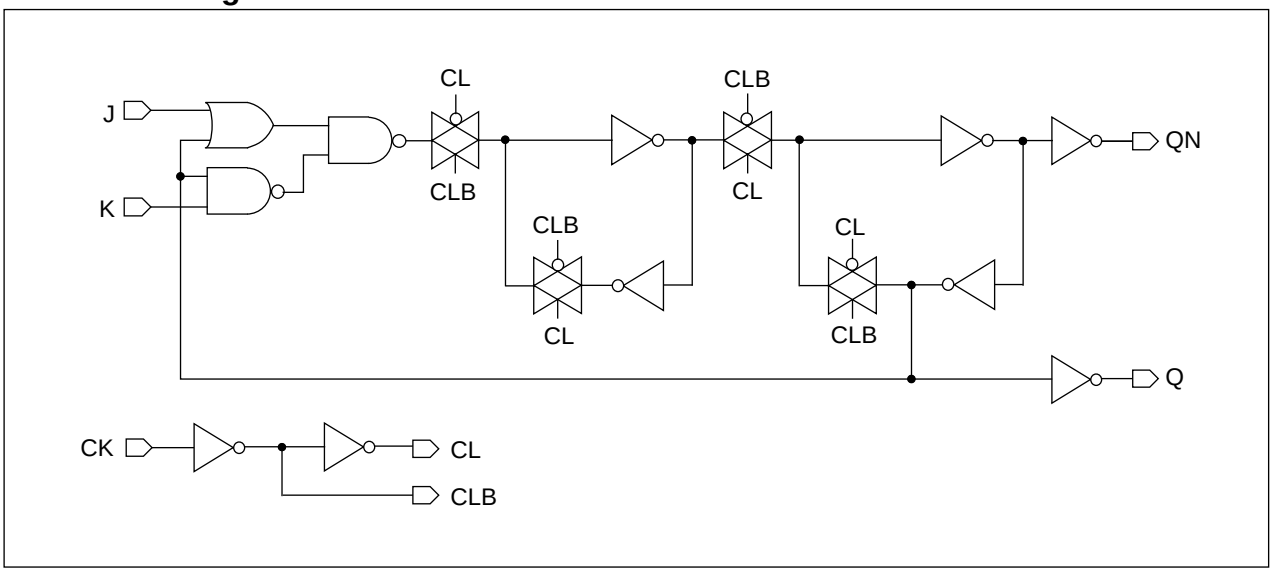
Truth Table

J	CK	K	Q (n+1)	QN (n+1)
0	↑	1	0	1
1	↑	0	1	0
0	↑	0	Q (n)	QN (n)
1	↑	1	QN (n)	Q (n)
x	↓	x	Q (n)	QN (n)

Cell Data

Input Load (SL)						Gate Count	
FJ1			*FJ1D2*			*FJ1*	*FJ1D2*
J	CK	K	J	CK	K		
0.6	0.6	0.4	0.6	0.6	0.4	7.0	7.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FJ1	FJ1D2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Input Setup Time (J to CK)	t_{SU}	0.68	0.68
Input Hold Time (J to CK)	t_{HD}	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.68	0.68
Input Hold Time (K to CK)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FJ1

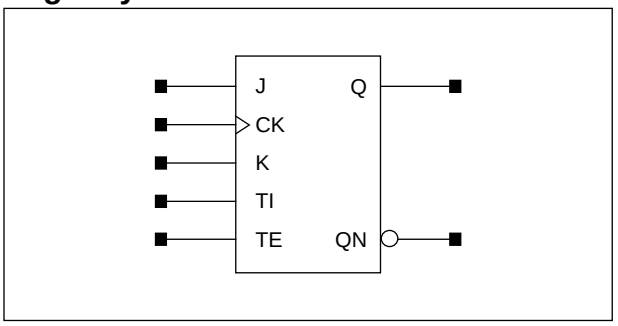
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.82	0.76 + 0.030*SL	0.77 + 0.027*SL	0.77 + 0.027*SL
	t_{PHL}	0.87	0.79 + 0.039*SL	0.81 + 0.034*SL	0.82 + 0.033*SL
	t_R	0.22	0.12 + 0.054*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
	t_F	0.25	0.12 + 0.063*SL	0.12 + 0.062*SL	0.10 + 0.065*SL
CK to QN	t_{PLH}	0.63	0.56 + 0.030*SL	0.57 + 0.028*SL	0.58 + 0.027*SL
	t_{PHL}	0.70	0.62 + 0.039*SL	0.63 + 0.035*SL	0.65 + 0.033*SL
	t_R	0.22	0.11 + 0.054*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

FJ1D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.88	0.85 + 0.016*SL	0.86 + 0.014*SL	0.87 + 0.013*SL
	t_{PHL}	0.93	0.89 + 0.022*SL	0.90 + 0.018*SL	0.92 + 0.017*SL
	t_R	0.17	0.12 + 0.026*SL	0.12 + 0.026*SL	0.10 + 0.029*SL
	t_F	0.19	0.13 + 0.033*SL	0.13 + 0.031*SL	0.13 + 0.032*SL
CK to QN	t_{PLH}	0.63	0.59 + 0.018*SL	0.60 + 0.015*SL	0.62 + 0.013*SL
	t_{PHL}	0.70	0.65 + 0.024*SL	0.66 + 0.019*SL	0.69 + 0.017*SL
	t_R	0.17	0.11 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Logic Symbol



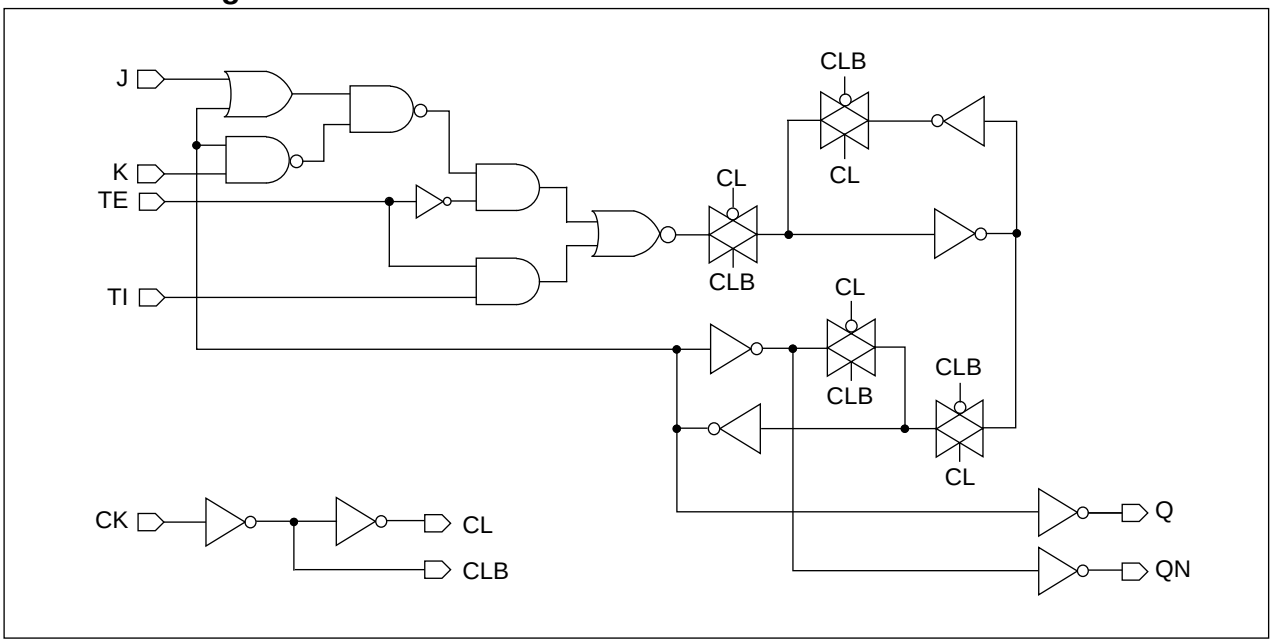
Truth Table

J	CK	K	TI	TE	Q (n+1)	QN (n+1)
0	↑	1	x	0	0	1
1	↑	0	x	0	1	0
0	↑	0	x	0	Q (n)	QN (n)
1	↑	1	x	0	QN (n)	Q (n)
x	↓	x	x	x	Q (n)	QN (n)
x	↑	x	0	1	0	1
x	↑	x	1	1	1	0

Cell Data

Input Load (SL)										Gate Count	
FJ1S					*FJ1SD2*					*FJ1S*	*FJ1S D2*
J	CK	K	TI	TE	J	CK	K	TI	TE		
0.6	0.6	0.6	0.6	1.1	0.6	0.6	0.6	0.6	1.1	9.3	10.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FJ1S	FJ1SD2
Pulse Width Low (CK)	t_{PWL}	0.85	0.85
Pulse Width High (CK)	t_{PWH}	0.77	0.77
Input Setup Time (J to CK)	t_{SU}	0.98	0.98
Input Hold Time (J to CK)	t_{HD}	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.98	0.98
Input Hold Time (K to CK)	t_{HD}	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.76	0.76
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.71	0.71
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FJ1S

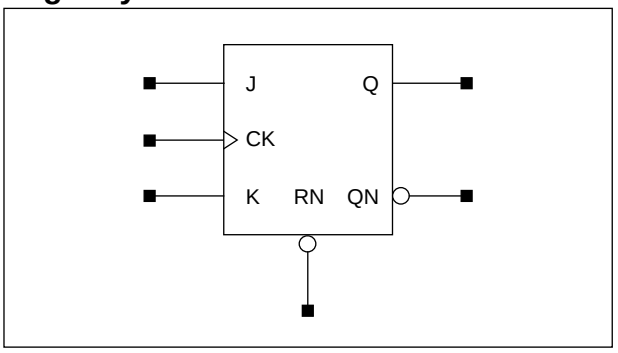
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.71	0.64 + 0.034*SL	0.65 + 0.029*SL	0.67 + 0.027*SL
	t_{PHL}	0.79	0.70 + 0.044*SL	0.72 + 0.036*SL	0.75 + 0.033*SL
	t_R	0.25	0.14 + 0.055*SL	0.13 + 0.057*SL	0.11 + 0.060*SL
	t_F	0.27	0.14 + 0.064*SL	0.15 + 0.062*SL	0.12 + 0.065*SL
CK to QN	t_{PLH}	0.84	0.78 + 0.028*SL	0.79 + 0.027*SL	0.79 + 0.027*SL
	t_{PHL}	0.88	0.80 + 0.036*SL	0.81 + 0.033*SL	0.82 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.063*SL	0.07 + 0.066*SL

FJ1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.70	0.66 + 0.020*SL	0.67 + 0.016*SL	0.69 + 0.013*SL
	t_{PHL}	0.78	0.73 + 0.026*SL	0.74 + 0.021*SL	0.78 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.026*SL	0.12 + 0.028*SL
	t_F	0.21	0.14 + 0.034*SL	0.15 + 0.031*SL	0.15 + 0.032*SL
CK to QN	t_{PLH}	0.91	0.88 + 0.014*SL	0.88 + 0.013*SL	0.88 + 0.013*SL
	t_{PHL}	0.94	0.90 + 0.019*SL	0.91 + 0.017*SL	0.92 + 0.016*SL
	t_R	0.16	0.11 + 0.025*SL	0.11 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.030*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



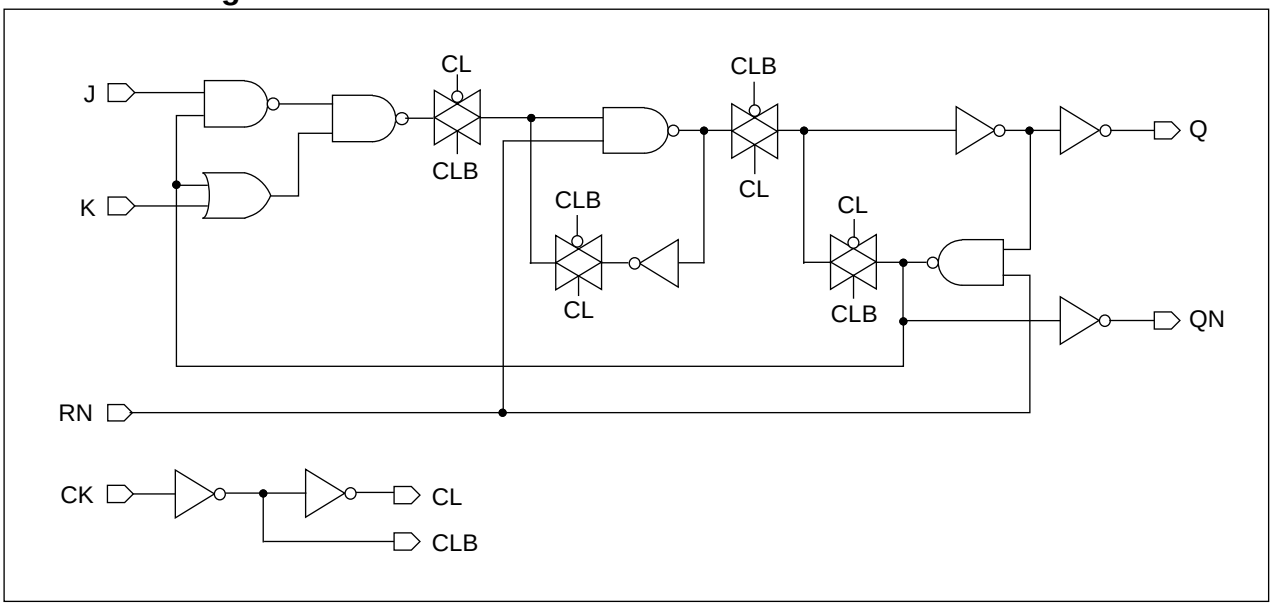
Truth Table

J	CK	K	RN	Q (n+1)	QN (n+1)
0	↑	1	1	0	1
1	↑	0	1	1	0
0	↑	0	1	Q (n)	QN (n)
1	↑	1	1	QN (n)	Q (n)
x	↓	x	1	Q (n)	QN (n)
x	x	x	0	0	1

Cell Data

Input Load (SL)								Gate Count	
FJ2				*FJ2D2*				*FJ2*	*FJ2D2*
J	CK	K	RN	J	CK	K	RN		
0.4	0.6	0.4	1.1	0.4	0.6	0.4	1.1	8.3	9.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FJ2	FJ2D2
Pulse Width Low (CK)	t_{PWL}	0.85	0.85
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Input Setup Time (J to CK)	t_{SU}	0.74	0.74
Input Hold Time (J to CK)	t_{HD}	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.74	0.74
Input Hold Time (K to CK)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FJ2

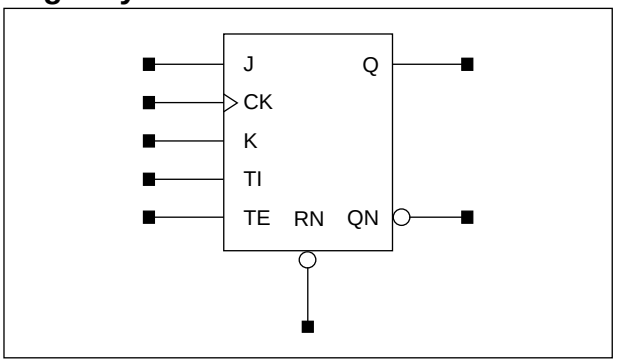
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.97	0.90 + 0.036*SL	0.92 + 0.030*SL	0.95 + 0.027*SL
	t_{PHL}	0.92	0.84 + 0.040*SL	0.86 + 0.035*SL	0.88 + 0.033*SL
	t_R	0.27	0.16 + 0.057*SL	0.16 + 0.057*SL	0.13 + 0.059*SL
	t_F	0.26	0.13 + 0.064*SL	0.14 + 0.062*SL	0.11 + 0.065*SL
RN to Q	t_{PHL}	0.44	0.35 + 0.042*SL	0.37 + 0.035*SL	0.39 + 0.033*SL
	t_F	0.26	0.13 + 0.062*SL	0.13 + 0.062*SL	0.10 + 0.065*SL
CK to QN	t_{PLH}	0.63	0.57 + 0.030*SL	0.58 + 0.028*SL	0.58 + 0.027*SL
	t_{PHL}	0.75	0.67 + 0.039*SL	0.68 + 0.035*SL	0.70 + 0.033*SL
	t_R	0.22	0.11 + 0.054*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to QN	t_{PLH}	0.68	0.62 + 0.030*SL	0.62 + 0.027*SL	0.63 + 0.027*SL
	t_R	0.23	0.12 + 0.053*SL	0.11 + 0.057*SL	0.08 + 0.060*SL

FJ2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.04	1.00 + 0.021*SL	1.01 + 0.017*SL	1.04 + 0.014*SL
	t_{PHL}	0.98	0.93 + 0.024*SL	0.94 + 0.019*SL	0.97 + 0.017*SL
	t_R	0.23	0.17 + 0.028*SL	0.17 + 0.027*SL	0.17 + 0.028*SL
	t_F	0.21	0.15 + 0.032*SL	0.15 + 0.031*SL	0.14 + 0.032*SL
RN to Q	t_{PHL}	0.43	0.38 + 0.026*SL	0.40 + 0.020*SL	0.43 + 0.017*SL
	t_F	0.21	0.14 + 0.032*SL	0.15 + 0.030*SL	0.13 + 0.032*SL
CK to QN	t_{PLH}	0.63	0.59 + 0.018*SL	0.60 + 0.015*SL	0.62 + 0.013*SL
	t_{PHL}	0.75	0.70 + 0.024*SL	0.72 + 0.019*SL	0.74 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.030*SL	0.11 + 0.032*SL
RN to QN	t_{PLH}	0.68	0.64 + 0.018*SL	0.65 + 0.015*SL	0.67 + 0.013*SL
	t_R	0.17	0.13 + 0.025*SL	0.12 + 0.026*SL	0.10 + 0.029*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



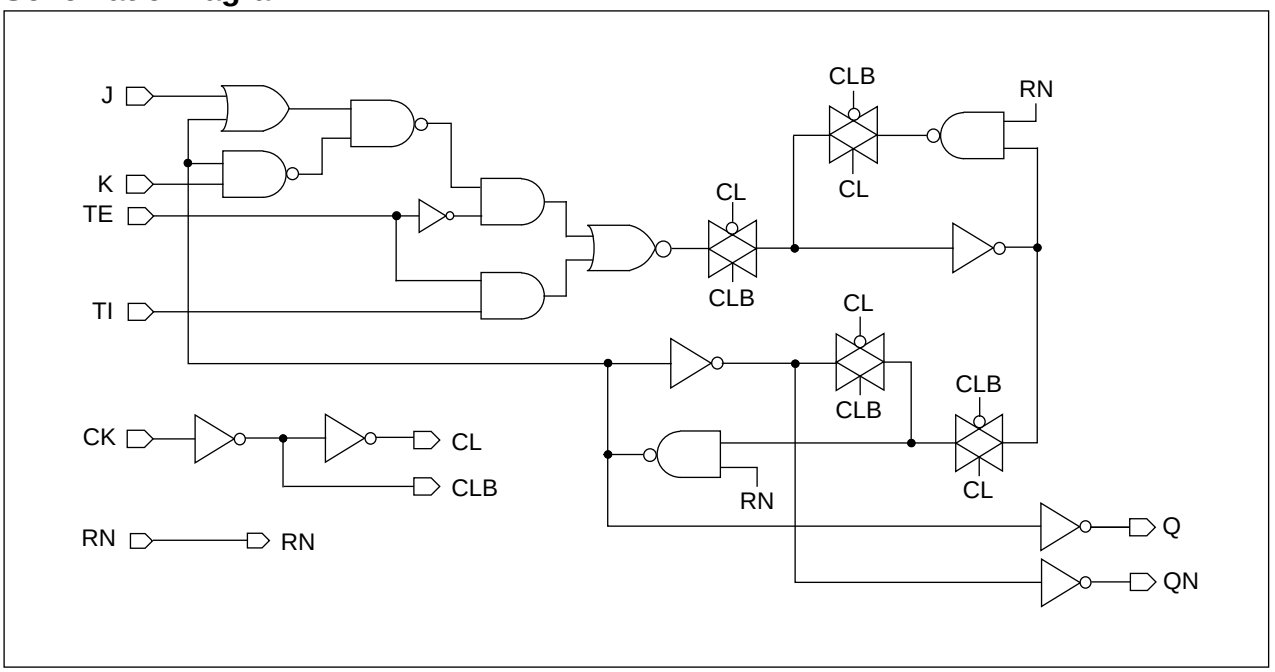
Truth Table

J	CK	K	TI	TE	RN	Q (n+1)	QN (n+1)
0	↑	1	x	0	1	0	1
1	↑	0	x	0	1	1	0
0	↑	0	x	0	1	Q (n)	QN (n)
1	↑	1	x	0	1	QN (n)	Q (n)
x	↓	x	x	0	1	Q (n)	QN (n)
x	x	x	x	x	0	0	1
x	↑	x	0	1	1	0	1
x	↑	x	1	1	1	1	0

Cell Data

Input Load (SL)												Gate Count	
FJ2S						*FJ2SD2*						*FJ2S*	*FJ2S D2*
J	CK	K	TI	TE	RN	J	CK	K	TI	TE	RN		
0.6	0.6	0.6	0.6	1.1	1.3	0.6	0.6	0.6	0.6	1.1	1.3	10.3	11.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FJ2S	FJ2SD2
Pulse Width Low (CK)	t_{PWL}	0.85	0.85
Pulse Width High (CK)	t_{PWH}	0.77	0.77
Pulse Width High (RN)	t_{PWH}	0.77	0.77
Input Setup Time (J to CK)	t_{SU}	1.01	1.01
Input Hold Time (J to CK)	t_{HD}	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	1.01	1.01
Input Hold Time (K to CK)	t_{HD}	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.76	0.76
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.71	0.71
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.71

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FJ2S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.79	0.71 + 0.039*SL	0.73 + 0.032*SL	0.78 + 0.027*SL
	t_{PHL}	0.82	0.74 + 0.044*SL	0.76 + 0.036*SL	0.79 + 0.033*SL
	t_R	0.29	0.18 + 0.058*SL	0.18 + 0.057*SL	0.16 + 0.059*SL
	t_F	0.28	0.15 + 0.064*SL	0.15 + 0.062*SL	0.13 + 0.065*SL
RN to Q	t_{PHL}	0.46	0.38 + 0.044*SL	0.40 + 0.035*SL	0.42 + 0.033*SL
	t_F	0.27	0.15 + 0.061*SL	0.15 + 0.061*SL	0.11 + 0.065*SL
CK to QN	t_{PLH}	0.88	0.82 + 0.028*SL	0.82 + 0.027*SL	0.82 + 0.027*SL
	t_{PHL}	0.98	0.91 + 0.035*SL	0.91 + 0.033*SL	0.92 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.23	0.11 + 0.061*SL	0.10 + 0.063*SL	0.08 + 0.065*SL
RN to QN	t_{PLH}	0.52	0.46 + 0.028*SL	0.46 + 0.027*SL	0.46 + 0.027*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.07 + 0.060*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FJ2SD2

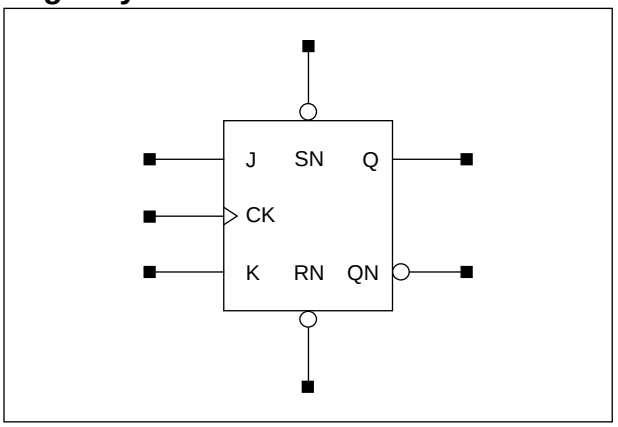
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.79	0.74 + 0.025*SL	0.76 + 0.018*SL	0.80 + 0.014*SL
	t_{PHL}	0.81	0.76 + 0.027*SL	0.78 + 0.021*SL	0.81 + 0.017*SL
	t_R	0.24	0.19 + 0.028*SL	0.19 + 0.028*SL	0.18 + 0.028*SL
	t_F	0.22	0.16 + 0.033*SL	0.16 + 0.031*SL	0.15 + 0.032*SL
RN to Q	t_{PHL}	0.45	0.40 + 0.027*SL	0.42 + 0.020*SL	0.45 + 0.017*SL
	t_F	0.22	0.15 + 0.031*SL	0.16 + 0.030*SL	0.14 + 0.031*SL
CK to QN	t_{PLH}	0.94	0.91 + 0.014*SL	0.92 + 0.013*SL	0.92 + 0.013*SL
	t_{PHL}	1.07	1.04 + 0.018*SL	1.04 + 0.017*SL	1.04 + 0.016*SL
	t_R	0.16	0.11 + 0.024*SL	0.11 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
RN to QN	t_{PLH}	0.58	0.55 + 0.014*SL	0.55 + 0.013*SL	0.56 + 0.013*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.026*SL	0.08 + 0.029*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

FJ4/FJ4D2

JK Flip-Flop with Reset, Set, 1X/2X Drive

Logic Symbol



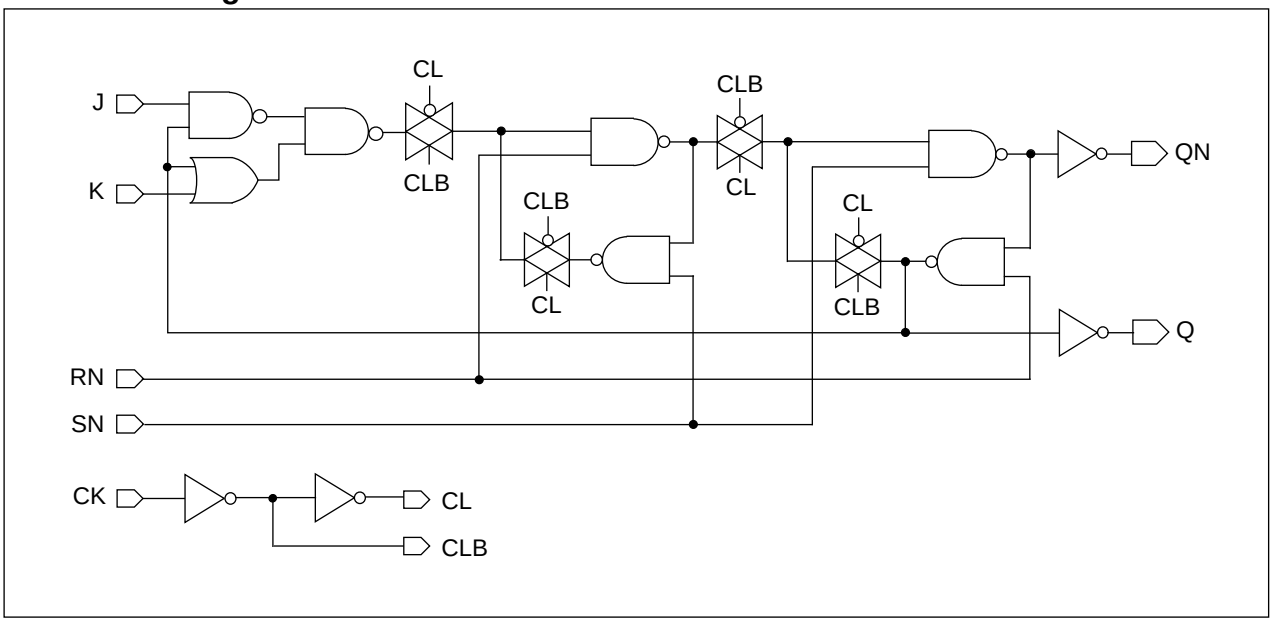
Truth Table

J	CK	K	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	1	1	0	1
1	↑	0	1	1	1	0
0	↑	0	1	1	Q (n)	QN (n)
1	↑	1	1	1	QN (n)	Q (n)
x	↓	x	1	1	Q (n)	QN (n)
x	x	x	0	1	0	1
x	x	x	1	0	1	0
x	x	x	0	0	0	0

Cell Data

Input Load (SL)										Gate Count	
FJ4					*FJ4D2*					*FJ4*	*FJ4D2*
J	CK	K	RN	SN	J	CK	K	RN	SN		
0.6	0.6	0.6	1.1	1.1	0.6	0.6	0.6	1.1	1.1	9.3	10.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FJ4	FJ4D2
Pulse Width Low (CK)	t_{PWL}	0.85	0.85
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Pulse Width Low (SN)	t_{PWL}	0.79	0.79
Input Setup Time (J to CK)	t_{SU}	0.74	0.74
Input Hold Time (J to CK)	t_{HD}	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	0.74	0.74
Input Hold Time (K to CK)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.44	0.44
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.71	0.71

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FJ4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.02	0.94 + 0.037*SL	0.96 + 0.030*SL	0.99 + 0.027*SL
	t_{PHL}	1.01	0.93 + 0.040*SL	0.95 + 0.035*SL	0.97 + 0.033*SL
	t_R	0.27	0.16 + 0.057*SL	0.16 + 0.057*SL	0.14 + 0.059*SL
	t_F	0.27	0.14 + 0.064*SL	0.15 + 0.061*SL	0.12 + 0.065*SL
RN to Q	t_{PLH}	0.42	0.35 + 0.037*SL	0.37 + 0.030*SL	0.40 + 0.027*SL
	t_{PHL}	0.45	0.36 + 0.043*SL	0.38 + 0.035*SL	0.40 + 0.033*SL
	t_R	0.27	0.16 + 0.057*SL	0.16 + 0.057*SL	0.13 + 0.059*SL
	t_F	0.26	0.14 + 0.062*SL	0.14 + 0.062*SL	0.11 + 0.065*SL
SN to Q	t_{PLH}	0.61	0.53 + 0.036*SL	0.55 + 0.030*SL	0.58 + 0.027*SL
	t_R	0.27	0.16 + 0.057*SL	0.16 + 0.056*SL	0.13 + 0.059*SL
CK to QN	t_{PLH}	0.70	0.63 + 0.034*SL	0.64 + 0.029*SL	0.66 + 0.027*SL
	t_{PHL}	0.78	0.70 + 0.040*SL	0.72 + 0.034*SL	0.73 + 0.033*SL
	t_R	0.25	0.14 + 0.055*SL	0.13 + 0.057*SL	0.11 + 0.060*SL
	t_F	0.25	0.13 + 0.060*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to QN	t_{PLH}	0.73	0.66 + 0.035*SL	0.67 + 0.029*SL	0.69 + 0.027*SL
	t_R	0.25	0.14 + 0.055*SL	0.14 + 0.057*SL	0.11 + 0.060*SL
SN to QN	t_{PLH}	0.33	0.26 + 0.034*SL	0.28 + 0.028*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.11 + 0.064*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

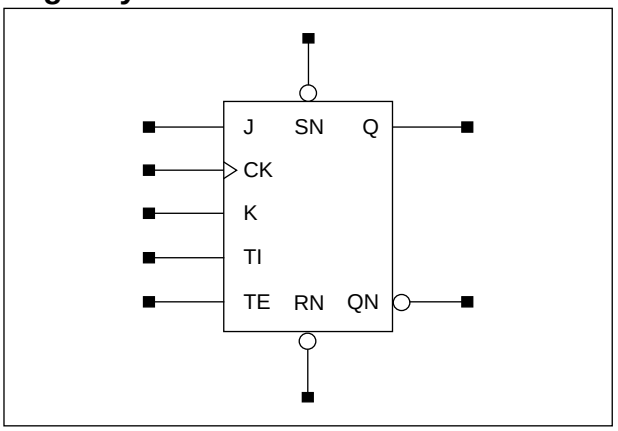
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FJ4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.08	1.04 + 0.022*SL	1.05 + 0.017*SL	1.08 + 0.014*SL
	t_{PHL}	1.10	1.05 + 0.023*SL	1.06 + 0.019*SL	1.08 + 0.017*SL
	t_R	0.23	0.17 + 0.028*SL	0.18 + 0.027*SL	0.17 + 0.028*SL
	t_F	0.22	0.16 + 0.033*SL	0.16 + 0.031*SL	0.16 + 0.031*SL
RN to Q	t_{PLH}	0.42	0.38 + 0.024*SL	0.39 + 0.018*SL	0.43 + 0.014*SL
	t_{PHL}	0.44	0.39 + 0.026*SL	0.40 + 0.020*SL	0.44 + 0.017*SL
	t_R	0.22	0.17 + 0.028*SL	0.17 + 0.027*SL	0.16 + 0.028*SL
	t_F	0.21	0.14 + 0.032*SL	0.15 + 0.031*SL	0.14 + 0.032*SL
SN to Q	t_{PLH}	0.66	0.62 + 0.022*SL	0.64 + 0.017*SL	0.67 + 0.014*SL
	t_R	0.23	0.17 + 0.028*SL	0.17 + 0.027*SL	0.16 + 0.028*SL
CK to QN	t_{PLH}	0.70	0.66 + 0.021*SL	0.68 + 0.017*SL	0.70 + 0.013*SL
	t_{PHL}	0.78	0.74 + 0.024*SL	0.75 + 0.019*SL	0.78 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.19	0.13 + 0.031*SL	0.13 + 0.031*SL	0.12 + 0.032*SL
RN to QN	t_{PLH}	0.74	0.70 + 0.021*SL	0.71 + 0.017*SL	0.74 + 0.013*SL
	t_R	0.21	0.16 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
SN to QN	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.34 + 0.013*SL
	t_{PHL}	0.36	0.32 + 0.023*SL	0.33 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



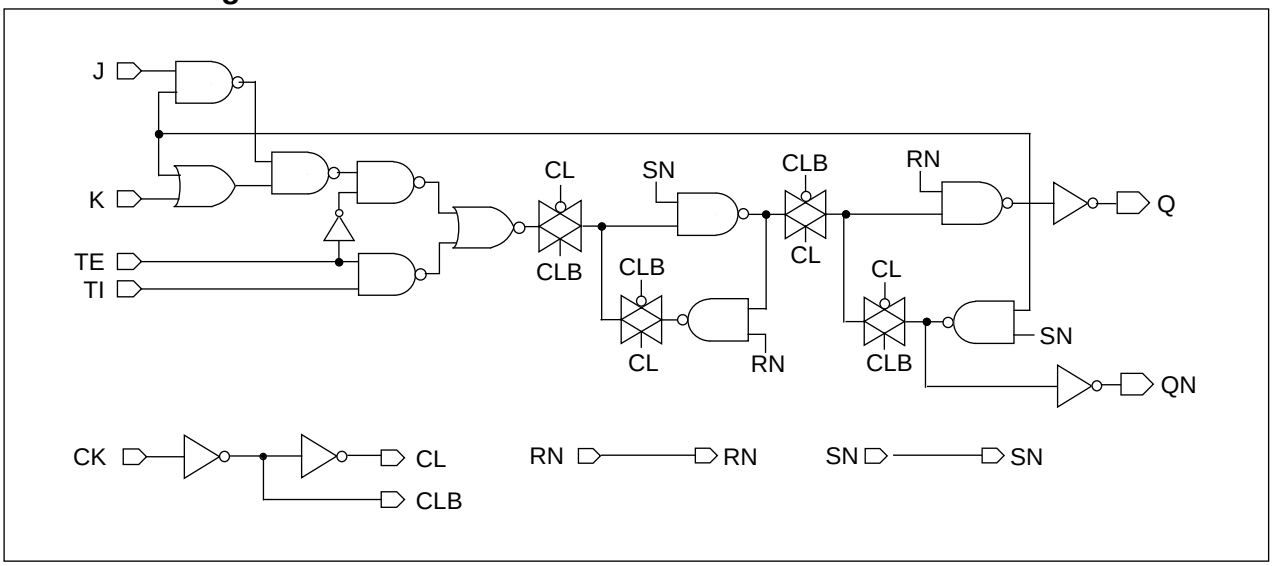
Truth Table

J	CK	K	TI	TE	RN	SN	Q (n+1)	QN (n+1)
0	↑	1	x	0	1	1	0	1
1	↑	0	x	0	1	1	1	0
0	↑	0	x	0	1	1	Q (n)	QN (n)
1	↑	1	x	0	1	1	QN (n)	Q (n)
x	↓	x	x	0	1	1	Q (n)	QN (n)
x	x	x	x	x	0	1	0	1
x	x	x	x	x	1	0	1	0
x	x	x	x	x	0	0	0	0
x	↑	x	0	1	1	1	0	1
x	↑	x	1	1	1	1	1	0

Cell Data

Input Load (SL)							Gate Count
FJ4S							*FJ4S*
J	CK	K	TI	TE	RN	SN	
0.6	0.6	0.6	0.5	1.1	1.6	1.6	11.7
FJ4SD2							*FJ4SD2*
J	CK	K	TI	TE	RN	SN	
0.6	0.6	0.6	0.5	1.1	1.6	1.6	12.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FJ4S	FJ4SD2
Pulse Width Low (CK)	t_{PWL}	0.90	0.90
Pulse Width High (CK)	t_{PWH}	0.77	0.77
Pulse Width High (RN)	t_{PWH}	0.77	0.78
Pulse Width High (SN)	t_{PWH}	0.87	0.87
Input Setup Time (J to CK)	t_{SU}	1.04	10.7
Input Hold Time (J to CK)	t_{HD}	0.33	0.33
Input Setup Time (K to CK)	t_{SU}	1.04	1.07
Input Hold Time (K to CK)	t_{HD}	0.33	0.33
Input Setup Time (TI to CK)	t_{SU}	0.82	0.82
Input Hold Time (TI to CK)	t_{HD}	0.33	0.33
Input Setup Time (TE to CK)	t_{SU}	0.76	0.76
Input Hold Time (TE to CK)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.71	0.71
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FJ4S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.80	0.73 + 0.039*SL	0.75 + 0.031*SL	0.79 + 0.027*SL
	t_{PHL}	0.88	0.79 + 0.044*SL	0.81 + 0.037*SL	0.85 + 0.033*SL
	t_R	0.29	0.18 + 0.058*SL	0.18 + 0.057*SL	0.16 + 0.059*SL
	t_F	0.28	0.15 + 0.064*SL	0.16 + 0.062*SL	0.13 + 0.065*SL
RN to Q	t_{PLH}	0.43	0.36 + 0.038*SL	0.38 + 0.030*SL	0.41 + 0.027*SL
	t_{PHL}	0.47	0.38 + 0.044*SL	0.40 + 0.036*SL	0.43 + 0.033*SL
	t_R	0.28	0.17 + 0.056*SL	0.16 + 0.056*SL	0.14 + 0.059*SL
	t_F	0.27	0.15 + 0.062*SL	0.15 + 0.062*SL	0.12 + 0.065*SL
SN to Q	t_{PLH}	0.84	0.76 + 0.038*SL	0.78 + 0.031*SL	0.82 + 0.027*SL
	t_R	0.29	0.18 + 0.056*SL	0.18 + 0.056*SL	0.15 + 0.059*SL
CK to QN	t_{PLH}	1.04	0.98 + 0.031*SL	0.99 + 0.028*SL	1.00 + 0.027*SL
	t_{PHL}	1.02	0.95 + 0.037*SL	0.95 + 0.034*SL	0.96 + 0.033*SL
	t_R	0.24	0.14 + 0.054*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to QN	t_{PLH}	0.62	0.56 + 0.032*SL	0.57 + 0.028*SL	0.58 + 0.027*SL
	t_R	0.24	0.13 + 0.057*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
SN to QN	t_{PLH}	0.30	0.24 + 0.033*SL	0.25 + 0.028*SL	0.26 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.31 + 0.034*SL	0.32 + 0.033*SL
	t_R	0.24	0.12 + 0.057*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.061*SL	0.10 + 0.064*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FJ4SD2

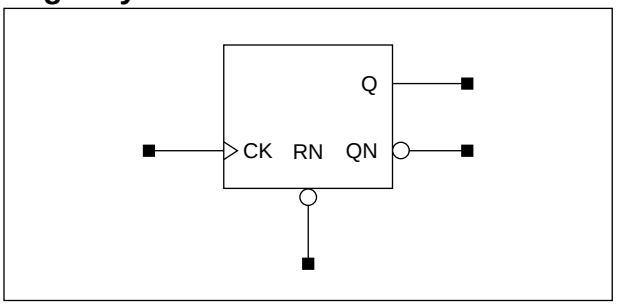
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.80	0.75 + 0.025*SL	0.77 + 0.018*SL	0.81 + 0.014*SL
	t_{PHL}	0.87	0.82 + 0.027*SL	0.84 + 0.021*SL	0.87 + 0.017*SL
	t_R	0.24	0.19 + 0.027*SL	0.19 + 0.028*SL	0.18 + 0.028*SL
	t_F	0.22	0.16 + 0.032*SL	0.16 + 0.031*SL	0.16 + 0.032*SL
RN to Q	t_{PLH}	0.43	0.38 + 0.024*SL	0.40 + 0.018*SL	0.44 + 0.014*SL
	t_{PHL}	0.46	0.40 + 0.026*SL	0.42 + 0.021*SL	0.46 + 0.017*SL
	t_R	0.23	0.18 + 0.027*SL	0.17 + 0.027*SL	0.17 + 0.028*SL
	t_F	0.22	0.15 + 0.032*SL	0.16 + 0.030*SL	0.15 + 0.031*SL
SN to Q	t_{PLH}	0.84	0.79 + 0.024*SL	0.81 + 0.018*SL	0.85 + 0.014*SL
	t_R	0.24	0.19 + 0.026*SL	0.18 + 0.027*SL	0.18 + 0.028*SL
CK to QN	t_{PLH}	1.13	1.09 + 0.018*SL	1.10 + 0.015*SL	1.12 + 0.013*SL
	t_{PHL}	1.11	1.07 + 0.020*SL	1.08 + 0.017*SL	1.08 + 0.016*SL
	t_R	0.20	0.15 + 0.027*SL	0.15 + 0.026*SL	0.13 + 0.028*SL
	t_F	0.19	0.13 + 0.030*SL	0.13 + 0.030*SL	0.12 + 0.032*SL
RN to QN	t_{PLH}	0.71	0.67 + 0.017*SL	0.68 + 0.015*SL	0.69 + 0.013*SL
	t_R	0.20	0.15 + 0.026*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
SN to QN	t_{PLH}	0.31	0.27 + 0.020*SL	0.29 + 0.016*SL	0.31 + 0.013*SL
	t_{PHL}	0.37	0.33 + 0.023*SL	0.34 + 0.019*SL	0.36 + 0.017*SL
	t_R	0.19	0.13 + 0.027*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

FT2/FT2D2

Toggle Flip-Flop with Reset, 1X/2X Drive

Logic Symbol



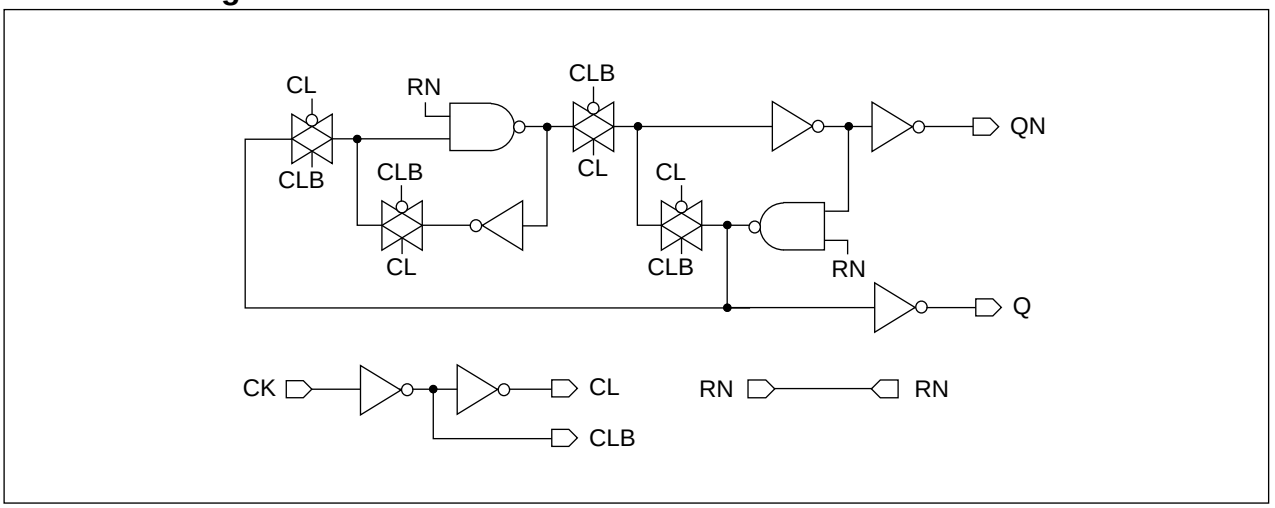
Truth Table

CK	RN	Q (n+1)	QN (n+1)
⎍	1	QN (n)	Q (n)
x	0	0	1

Cell Data

Input Load (SL)				Gate Count	
FT2		*FT2D2*		*FT2*	*FT2D2*
CK	RN	CK	RN		
0.6	1.1	0.6	1.1	6.3	7.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FT2	FT2D2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width High (RN)	t_{PWH}	0.79	0.79
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to CK)	t_{HD}	0.44	0.44

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FT2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.94	0.87 + 0.034*SL	0.88 + 0.029*SL	0.90 + 0.027*SL
	t_{PHL}	0.89	0.81 + 0.038*SL	0.82 + 0.034*SL	0.84 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.11 + 0.059*SL
	t_F	0.25	0.12 + 0.063*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
RN to Q	t_{PHL}	0.39	0.31 + 0.041*SL	0.33 + 0.035*SL	0.35 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
CK to QN	t_{PLH}	0.64	0.58 + 0.030*SL	0.58 + 0.027*SL	0.59 + 0.027*SL
	t_{PHL}	0.75	0.67 + 0.039*SL	0.68 + 0.035*SL	0.70 + 0.033*SL
	t_R	0.22	0.12 + 0.054*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to QN	t_{PLH}	0.67	0.61 + 0.030*SL	0.62 + 0.027*SL	0.63 + 0.027*SL
	t_R	0.23	0.12 + 0.053*SL	0.11 + 0.057*SL	0.08 + 0.060*SL

FT2D2

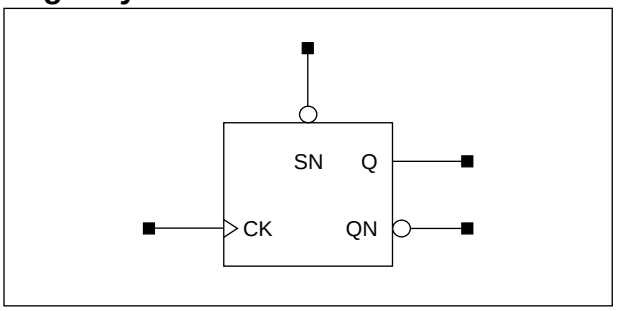
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	1.00	0.97 + 0.020*SL	0.98 + 0.016*SL	1.00 + 0.013*SL
	t_{PHL}	0.95	0.90 + 0.022*SL	0.91 + 0.019*SL	0.93 + 0.017*SL
	t_R	0.21	0.16 + 0.027*SL	0.16 + 0.027*SL	0.15 + 0.028*SL
	t_F	0.20	0.13 + 0.032*SL	0.14 + 0.031*SL	0.13 + 0.032*SL
RN to Q	t_{PHL}	0.39	0.34 + 0.025*SL	0.36 + 0.020*SL	0.39 + 0.017*SL
	t_F	0.19	0.12 + 0.033*SL	0.13 + 0.031*SL	0.12 + 0.032*SL
CK to QN	t_{PLH}	0.64	0.60 + 0.018*SL	0.61 + 0.015*SL	0.62 + 0.013*SL
	t_{PHL}	0.75	0.70 + 0.023*SL	0.72 + 0.019*SL	0.74 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.13 + 0.029*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
RN to QN	t_{PLH}	0.68	0.64 + 0.018*SL	0.65 + 0.014*SL	0.67 + 0.013*SL
	t_R	0.17	0.12 + 0.025*SL	0.12 + 0.026*SL	0.10 + 0.029*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

FT3/FT3D2

Toggle Flip-Flop with Set, 1X/2X Drive

Logic Symbol



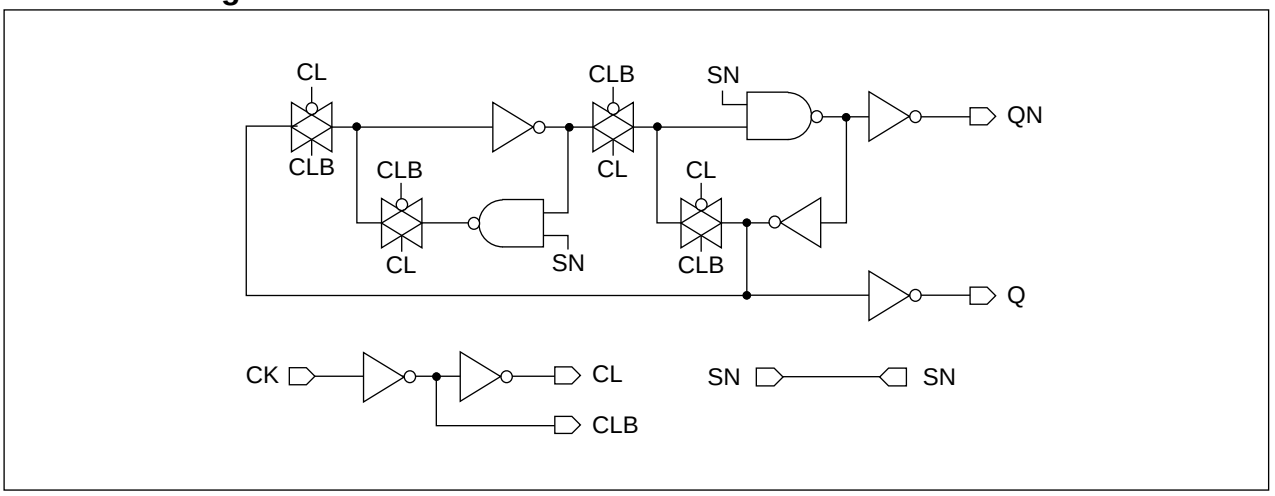
Truth Table

CK	SN	Q (n+1)	QN (n+1)
⎍	1	QN (n)	Q (n)
x	0	1	0

Cell Data

Input Load (SL)				Gate Count	
FT3		*FT3D2*		*FT3*	*FT3D2*
CK	SN	CK	SN		
0.6	1.1	0.6	1.1	6.0	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		FT3	FT3D2
Pulse Width Low (CK)	t_{PWL}	0.79	0.79
Pulse Width High (CK)	t_{PWH}	0.79	0.79
Pulse Width High (SN)	t_{PWH}	0.79	0.79
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (SN to CK)	t_{HD}	0.66	0.66

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FT3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.83	0.77 + 0.029*SL	0.78 + 0.027*SL	0.78 + 0.027*SL
	t_{PHL}	0.91	0.84 + 0.037*SL	0.85 + 0.034*SL	0.85 + 0.033*SL
	t_R	0.21	0.11 + 0.055*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
SN to Q	t_{PLH}	0.47	0.41 + 0.029*SL	0.41 + 0.027*SL	0.42 + 0.027*SL
	t_R	0.21	0.11 + 0.054*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
CK to QN	t_{PLH}	0.69	0.62 + 0.035*SL	0.63 + 0.029*SL	0.66 + 0.027*SL
	t_{PHL}	0.73	0.65 + 0.039*SL	0.67 + 0.035*SL	0.68 + 0.033*SL
	t_R	0.25	0.14 + 0.056*SL	0.13 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
SN to QN	t_{PHL}	0.37	0.29 + 0.039*SL	0.30 + 0.035*SL	0.32 + 0.033*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

FT3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
CK to Q	t_{PLH}	0.89	0.86 + 0.015*SL	0.87 + 0.013*SL	0.87 + 0.013*SL
	t_{PHL}	1.00	0.96 + 0.019*SL	0.97 + 0.017*SL	0.98 + 0.016*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.19	0.12 + 0.033*SL	0.13 + 0.030*SL	0.12 + 0.032*SL
SN to Q	t_{PLH}	0.53	0.50 + 0.015*SL	0.50 + 0.013*SL	0.51 + 0.013*SL
	t_R	0.17	0.12 + 0.023*SL	0.11 + 0.026*SL	0.09 + 0.029*SL
CK to QN	t_{PLH}	0.70	0.65 + 0.022*SL	0.67 + 0.016*SL	0.70 + 0.014*SL
	t_{PHL}	0.73	0.68 + 0.024*SL	0.69 + 0.019*SL	0.72 + 0.017*SL
	t_R	0.20	0.15 + 0.027*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.19	0.12 + 0.032*SL	0.13 + 0.031*SL	0.11 + 0.032*SL
SN to QN	t_{PHL}	0.36	0.32 + 0.024*SL	0.33 + 0.019*SL	0.35 + 0.017*SL
	t_F	0.18	0.11 + 0.033*SL	0.11 + 0.032*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

LATCHES

Cell Names & Function Descriptions

Cell Name	Function Description
LD1	D Latch with Active High
LD1D2	D Latch with Active High, 2X Drive
LD1S	D Latch with Active High, Scan
LD1SD2	D Latch with Active High, Scan, 2X Drive
LD1Q	D Latch with Active High, Q Output Only
LD1QD2	D Latch with Active High, Q Output Only, 2X Drive
LD1X4	4-Bit D Latch with Active High
LD1X4D2	4-Bit D Latch with Active High, 2X Drive
YLD1	Fast D Latch with Active High
YLD1D2	Fast D Latch with Active High, 2X Drive
LD1A	D Latch with Active High, Tri-State Output
LD1B	D Latch with Active High, Tri-State Output, Separate WR, WRN
LD2	D Latch with Active High, Reset
LD2D2	D Latch with Active High, Reset, 2X Drive
LD2Q	D Latch with Active High, Reset, Q Output Only
LD2QD2	D Latch with Active High, Reset, Q Output Only, 2X Drive
YLD2	Fast D Latch with Active High, Reset
YLD2D2	Fast D Latch with Active High, Reset, 2X Drive
LD3	D Latch with Active High, Set
LD3D2	D Latch with Active High, Set, 2X Drive
LD4	D Latch with Active High, Reset, Set
LD4D2	D Latch with Active High, Reset, Set, 2X Drive
LD5	D Latch with Active Low
LD5D2	D Latch with Active Low, 2X Drive
LD5S	D Latch with Active Low, Scan
LD5SD2	D Latch with Active Low, Scan, 2X Drive
LD5X4	4-Bit D Latch with Active Low
LD5X4D2	4-Bit D Latch with Active Low, 2X Drive
LD6	D Latch with Active Low, Reset
LD6D2	D Latch with Active Low, Reset, 2X Drive
LD7	D Latch with Active Low, Set
LD7D2	D Latch with Active Low, Set, 2X Drive
LD8	D Latch with Active Low, Reset, Set
LD8D2	D Latch with Active Low, Reset, Set, 2X Drive

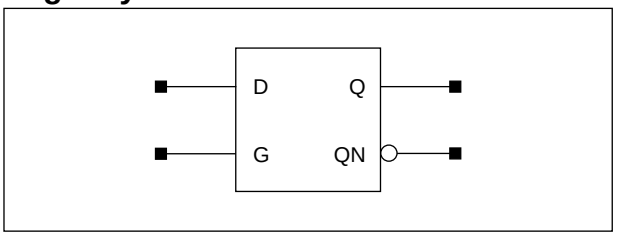
Cell Names & Function Descriptions (Continued)

Cell Name	Function Description
LDS2	D Latch with Active High, Synchronous Clear
LDS6	D Latch with Active Low, Synchronous Clear
LS0	SR Latch
LS0D2	SR Latch with 2X Drive
LS1	SR Latch with Separate Inputs
LS2	SR Latch with Common Inputs

LD1/LD1D2

D Latch with Active High, 1X/2X Drive

Logic Symbol



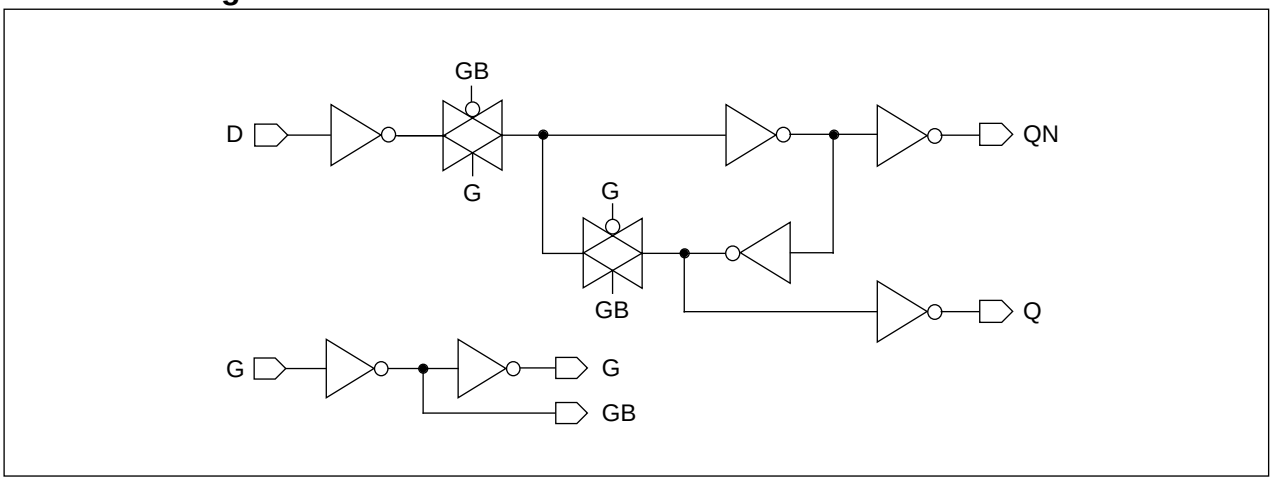
Truth Table

D	G	Q (n+1)	QN (n+1)
0	1	0	1
1	1	1	0
x	0	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
LD1		*LD1D2*		*LD1*	*LD1D2*
D	G	D	G		
0.6	0.6	0.6	0.6	4.0	4.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD1	LD1D2
Pulse Width High (G)	t_{PWH}	0.79	0.79
Input Setup Time (D to G)	t_{SU}	0.55	0.60
Input Hold Time (D to G)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.53	0.47 + 0.027*SL	0.47 + 0.027*SL	0.47 + 0.027*SL
	t_{PHL}	0.74	0.67 + 0.035*SL	0.67 + 0.033*SL	0.67 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
G to Q	t_{PLH}	0.68	0.62 + 0.028*SL	0.63 + 0.027*SL	0.63 + 0.027*SL
	t_{PHL}	0.74	0.67 + 0.036*SL	0.68 + 0.033*SL	0.68 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.063*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
D to QN	t_{PLH}	0.57	0.51 + 0.031*SL	0.52 + 0.028*SL	0.53 + 0.027*SL
	t_{PHL}	0.47	0.39 + 0.039*SL	0.40 + 0.034*SL	0.42 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
G to QN	t_{PLH}	0.58	0.52 + 0.030*SL	0.53 + 0.028*SL	0.53 + 0.027*SL
	t_{PHL}	0.62	0.54 + 0.040*SL	0.56 + 0.034*SL	0.57 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

LD1D2

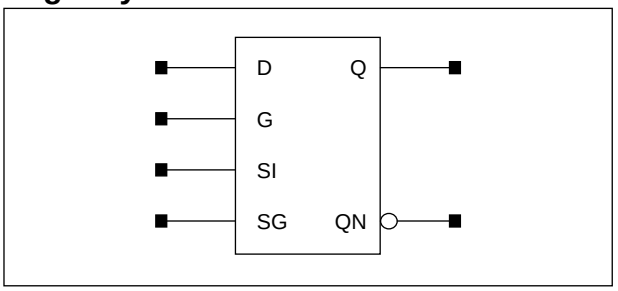
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.59	0.56 + 0.014*SL	0.57 + 0.013*SL	0.57 + 0.013*SL
	t_{PHL}	0.80	0.77 + 0.019*SL	0.77 + 0.017*SL	0.78 + 0.016*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
G to Q	t_{PLH}	0.75	0.72 + 0.014*SL	0.72 + 0.013*SL	0.72 + 0.013*SL
	t_{PHL}	0.81	0.77 + 0.019*SL	0.78 + 0.017*SL	0.78 + 0.016*SL
	t_R	0.15	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D to QN	t_{PLH}	0.57	0.54 + 0.018*SL	0.55 + 0.015*SL	0.56 + 0.013*SL
	t_{PHL}	0.47	0.42 + 0.023*SL	0.43 + 0.019*SL	0.46 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.11 + 0.032*SL
G to QN	t_{PLH}	0.58	0.54 + 0.018*SL	0.55 + 0.015*SL	0.57 + 0.013*SL
	t_{PHL}	0.62	0.57 + 0.024*SL	0.59 + 0.019*SL	0.61 + 0.017*SL
	t_R	0.17	0.11 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

LD1S/LD1SD2

D Latch with Active High, Scan, 1X/2X Drive

Logic Symbol



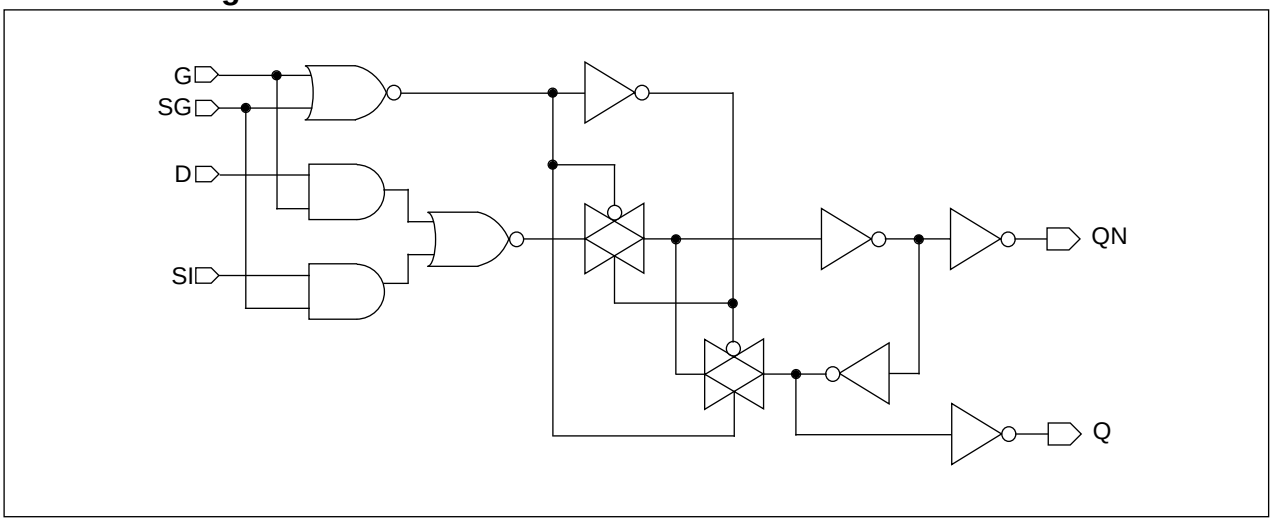
Truth Table

D	G	SI	SG	Q (n+1)	QN (n+1)
x	0	x	0	Q (n)	QN (n)
x	x	1	1	1	0
x	0	0	1	0	1
1	1	x	x	1	0
0	1	x	0	0	1
0	1	0	1	0	1

Cell Data

Input Load (SL)								Gate Count	
LD1S				*LD1SD2*				*LD1S*	*LD1SD2*
D	G	SI	SG	D	G	SI	SG		
0.4	0.9	0.5	1.0	0.4	0.9	0.5	1.0	5.7	6.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD1S	LD1SD2
Pulse Width High (G)	t_{PWH}	0.79	0.79
Pulse Width High (SG)	t_{PWH}	0.79	0.79
Input Setup Time (D to G)	t_{SU}	0.63	0.68
Input Hold Time (D to G)	t_{HD}	0.33	0.33
Input Setup Time (SI to SG)	t_{SU}	0.60	0.68
Input Hold Time (SI to SG)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD1S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.65	0.59 + 0.027*SL	0.59 + 0.027*SL	0.59 + 0.027*SL
	t_{PHL}	0.89	0.82 + 0.035*SL	0.83 + 0.033*SL	0.83 + 0.033*SL
	t_R	0.21	0.10 + 0.053*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
SI to Q	t_{PLH}	0.70	0.64 + 0.028*SL	0.65 + 0.027*SL	0.65 + 0.027*SL
	t_{PHL}	0.94	0.88 + 0.035*SL	0.88 + 0.033*SL	0.88 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
G to Q	t_{PLH}	0.75	0.70 + 0.028*SL	0.70 + 0.027*SL	0.70 + 0.027*SL
	t_{PHL}	0.78	0.71 + 0.035*SL	0.72 + 0.033*SL	0.72 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
SG to Q	t_{PLH}	0.78	0.72 + 0.028*SL	0.73 + 0.027*SL	0.73 + 0.027*SL
	t_{PHL}	0.79	0.72 + 0.035*SL	0.72 + 0.033*SL	0.73 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
D to QN	t_{PLH}	0.73	0.66 + 0.031*SL	0.67 + 0.028*SL	0.68 + 0.027*SL
	t_{PHL}	0.59	0.51 + 0.040*SL	0.53 + 0.035*SL	0.54 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
SI to QN	t_{PLH}	0.78	0.71 + 0.032*SL	0.72 + 0.028*SL	0.73 + 0.027*SL
	t_{PHL}	0.65	0.57 + 0.040*SL	0.58 + 0.035*SL	0.60 + 0.033*SL
	t_R	0.24	0.13 + 0.053*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
G to QN	t_{PLH}	0.62	0.55 + 0.031*SL	0.56 + 0.028*SL	0.57 + 0.027*SL
	t_{PHL}	0.70	0.62 + 0.039*SL	0.63 + 0.035*SL	0.65 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
SG to QN	t_{PLH}	0.62	0.56 + 0.031*SL	0.57 + 0.028*SL	0.58 + 0.027*SL
	t_{PHL}	0.72	0.64 + 0.040*SL	0.66 + 0.035*SL	0.67 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.063*SL	0.12 + 0.063*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

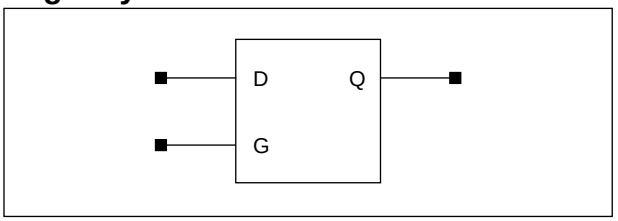
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD1SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.72	0.69 + 0.014*SL	0.69 + 0.013*SL	0.69 + 0.013*SL
	t_{PHL}	0.97	0.93 + 0.018*SL	0.94 + 0.017*SL	0.94 + 0.016*SL
	t_R	0.16	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
SI to Q	t_{PLH}	0.77	0.74 + 0.014*SL	0.74 + 0.013*SL	0.75 + 0.013*SL
	t_{PHL}	1.02	0.99 + 0.018*SL	0.99 + 0.017*SL	1.00 + 0.016*SL
	t_R	0.16	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.030*SL	0.09 + 0.032*SL
G to Q	t_{PLH}	0.82	0.80 + 0.014*SL	0.80 + 0.013*SL	0.80 + 0.013*SL
	t_{PHL}	0.85	0.82 + 0.018*SL	0.82 + 0.017*SL	0.83 + 0.016*SL
	t_R	0.16	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
SG to Q	t_{PLH}	0.85	0.82 + 0.014*SL	0.82 + 0.013*SL	0.82 + 0.013*SL
	t_{PHL}	0.86	0.82 + 0.018*SL	0.83 + 0.017*SL	0.83 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D to QN	t_{PLH}	0.73	0.69 + 0.019*SL	0.71 + 0.015*SL	0.72 + 0.013*SL
	t_{PHL}	0.59	0.54 + 0.024*SL	0.56 + 0.019*SL	0.58 + 0.017*SL
	t_R	0.18	0.13 + 0.025*SL	0.13 + 0.026*SL	0.11 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SI to QN	t_{PLH}	0.78	0.75 + 0.019*SL	0.76 + 0.015*SL	0.78 + 0.013*SL
	t_{PHL}	0.65	0.60 + 0.023*SL	0.61 + 0.019*SL	0.64 + 0.017*SL
	t_R	0.19	0.14 + 0.024*SL	0.14 + 0.025*SL	0.11 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
G to QN	t_{PLH}	0.62	0.58 + 0.018*SL	0.59 + 0.015*SL	0.61 + 0.013*SL
	t_{PHL}	0.70	0.65 + 0.023*SL	0.66 + 0.019*SL	0.69 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.12 + 0.026*SL	0.10 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SG to QN	t_{PLH}	0.63	0.59 + 0.018*SL	0.60 + 0.015*SL	0.62 + 0.013*SL
	t_{PHL}	0.72	0.68 + 0.024*SL	0.69 + 0.019*SL	0.71 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.12 + 0.027*SL	0.10 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



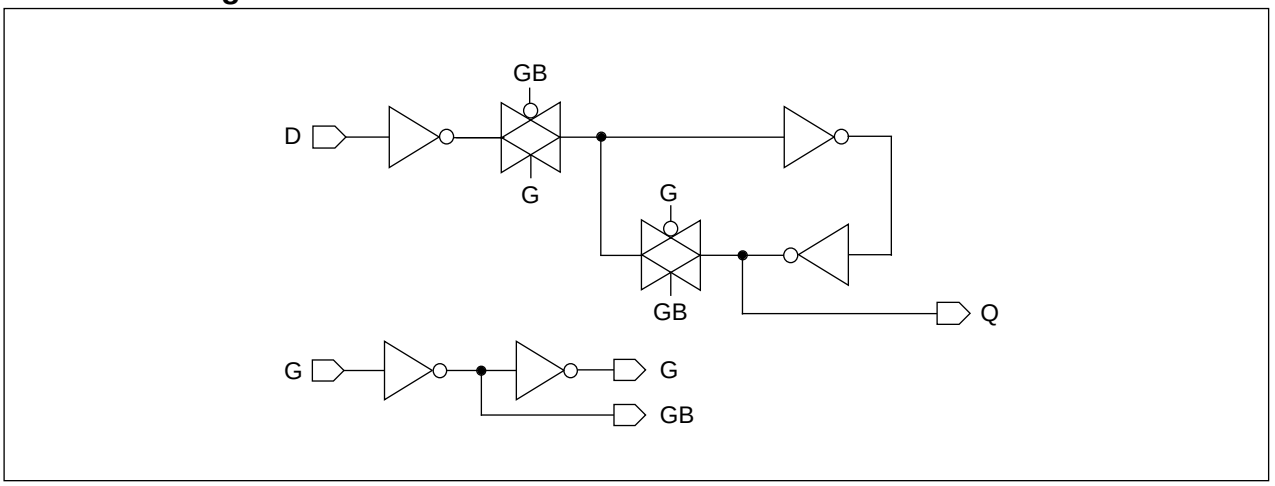
Truth Table

D	G	Q (n+1)
0	1	0
1	1	1
x	0	Q (n)

Cell Data

Input Load (SL)				Gate Count	
LD1Q		*LD1QD2*		*LD1Q*	*LD1QD2*
D	G	D	G		
0.6	0.6	0.6	0.6	3.7	4.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD1Q	LD1QD2
Pulse Width High (G)	t_{PWH}	0.79	0.79
Input Setup Time (D to G)	t_{SU}	0.46	0.47
Input Hold Time (D to G)	t_{HD}	0.35	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD1Q

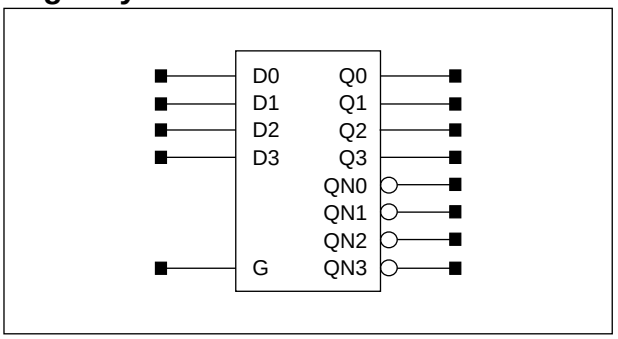
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.51	0.45 + 0.029*SL	0.45 + 0.027*SL	0.46 + 0.027*SL
	t_{PHL}	0.63	0.56 + 0.037*SL	0.57 + 0.033*SL	0.57 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.063*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
G to Q	t_{PLH}	0.66	0.60 + 0.029*SL	0.61 + 0.027*SL	0.61 + 0.027*SL
	t_{PHL}	0.64	0.56 + 0.037*SL	0.58 + 0.033*SL	0.58 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.063*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

LD1QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.51	0.48 + 0.017*SL	0.48 + 0.014*SL	0.49 + 0.013*SL
	t_{PHL}	0.63	0.59 + 0.022*SL	0.60 + 0.019*SL	0.62 + 0.017*SL
	t_R	0.15	0.09 + 0.027*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
G to Q	t_{PLH}	0.66	0.63 + 0.017*SL	0.64 + 0.014*SL	0.65 + 0.013*SL
	t_{PHL}	0.64	0.60 + 0.023*SL	0.61 + 0.018*SL	0.63 + 0.017*SL
	t_R	0.14	0.09 + 0.026*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.031*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

Dn	G	Qn (n+1)	QNn (n+1)
0	1	0	1
1	1	1	0
x	0	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
LD1X4/LD1XD2		*LD1X4/LD1XD2*		*LD1X4*	*LD1X4D2*
Dn	G	Dn	G		
0.6	0.6	0.6	0.6	13.0	15.3

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD1X4	LD1X4D2
Pulse Width High (G)	t_{PWH}	0.79	0.79
Input Setup Time (D0 to G)	t_{SU}	3.80	3.80
Input Hold Time (D0 to G)	t_{HD}	0.55	0.55
Input Setup Time (D1 to G)	t_{SU}	0.44	0.44
Input Hold Time (D1 to G)	t_{HD}	0.55	0.55
Input Setup Time (D2 to G)	t_{SU}	0.44	0.44
Input Hold Time (D2 to G)	t_{HD}	0.55	0.55
Input Setup Time (D3 to G)	t_{SU}	0.52	0.52
Input Hold Time (D3 to G)	t_{HD}	0.55	0.55

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.52	0.47 + 0.028*SL	0.47 + 0.027*SL	0.47 + 0.027*SL
	t_{PHL}	0.74	0.67 + 0.035*SL	0.67 + 0.033*SL	0.67 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
G to Q0	t_{PLH}	0.94	0.88 + 0.028*SL	0.89 + 0.027*SL	0.89 + 0.027*SL
	t_{PHL}	0.87	0.80 + 0.036*SL	0.81 + 0.033*SL	0.81 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
D1 to Q1	t_{PLH}	0.53	0.47 + 0.028*SL	0.48 + 0.027*SL	0.47 + 0.027*SL
	t_{PHL}	0.74	0.67 + 0.035*SL	0.67 + 0.033*SL	0.68 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.08 + 0.066*SL
G to Q1	t_{PLH}	0.94	0.89 + 0.028*SL	0.89 + 0.027*SL	0.89 + 0.027*SL
	t_{PHL}	0.88	0.80 + 0.036*SL	0.81 + 0.033*SL	0.81 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.08 + 0.066*SL
D2 to Q2	t_{PLH}	0.53	0.47 + 0.028*SL	0.47 + 0.027*SL	0.47 + 0.027*SL
	t_{PHL}	0.74	0.67 + 0.035*SL	0.67 + 0.033*SL	0.68 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.08 + 0.066*SL
G to Q2	t_{PLH}	0.94	0.89 + 0.028*SL	0.89 + 0.027*SL	0.89 + 0.027*SL
	t_{PHL}	0.88	0.81 + 0.035*SL	0.81 + 0.033*SL	0.81 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.08 + 0.066*SL
D3 to Q3	t_{PLH}	0.52	0.47 + 0.028*SL	0.47 + 0.027*SL	0.47 + 0.027*SL
	t_{PHL}	0.74	0.66 + 0.036*SL	0.67 + 0.033*SL	0.67 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
G to Q3	t_{PLH}	0.94	0.88 + 0.027*SL	0.89 + 0.027*SL	0.89 + 0.027*SL
	t_{PHL}	0.88	0.81 + 0.035*SL	0.81 + 0.033*SL	0.82 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
D0 to QN0	t_{PLH}	0.57	0.51 + 0.030*SL	0.52 + 0.028*SL	0.53 + 0.027*SL
	t_{PHL}	0.47	0.39 + 0.040*SL	0.40 + 0.034*SL	0.42 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
G to QN0	t_{PLH}	0.71	0.65 + 0.030*SL	0.66 + 0.028*SL	0.67 + 0.027*SL
	t_{PHL}	0.88	0.81 + 0.040*SL	0.82 + 0.034*SL	0.83 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

LD1X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.57	0.51 + 0.031*SL	0.52 + 0.028*SL	0.53 + 0.027*SL
	t_{PHL}	0.47	0.39 + 0.040*SL	0.41 + 0.034*SL	0.42 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
G to QN1	t_{PLH}	0.71	0.65 + 0.030*SL	0.66 + 0.028*SL	0.67 + 0.027*SL
	t_{PHL}	0.88	0.81 + 0.040*SL	0.82 + 0.034*SL	0.84 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
D2 to QN2	t_{PLH}	0.57	0.51 + 0.030*SL	0.52 + 0.028*SL	0.53 + 0.027*SL
	t_{PHL}	0.47	0.39 + 0.040*SL	0.40 + 0.034*SL	0.42 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
G to QN2	t_{PLH}	0.71	0.65 + 0.030*SL	0.66 + 0.028*SL	0.67 + 0.027*SL
	t_{PHL}	0.88	0.81 + 0.040*SL	0.82 + 0.034*SL	0.83 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
D3 to QN3	t_{PLH}	0.57	0.51 + 0.030*SL	0.52 + 0.028*SL	0.53 + 0.027*SL
	t_{PHL}	0.47	0.39 + 0.040*SL	0.40 + 0.034*SL	0.42 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
G to QN3	t_{PLH}	0.71	0.65 + 0.030*SL	0.66 + 0.028*SL	0.67 + 0.027*SL
	t_{PHL}	0.88	0.80 + 0.040*SL	0.82 + 0.034*SL	0.83 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

LD1X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.59	0.56 + 0.014*SL	0.56 + 0.013*SL	0.57 + 0.013*SL
	t_{PHL}	0.80	0.77 + 0.019*SL	0.77 + 0.017*SL	0.78 + 0.016*SL
	t_R	0.15	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.034*SL	0.11 + 0.030*SL	0.09 + 0.032*SL
G to Q0	t_{PLH}	1.01	0.99 + 0.014*SL	0.99 + 0.013*SL	0.99 + 0.013*SL
	t_{PHL}	0.94	0.91 + 0.019*SL	0.91 + 0.017*SL	0.92 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D1 to Q1	t_{PLH}	0.59	0.56 + 0.014*SL	0.57 + 0.013*SL	0.57 + 0.013*SL
	t_{PHL}	0.81	0.77 + 0.019*SL	0.77 + 0.017*SL	0.78 + 0.016*SL
	t_R	0.16	0.11 + 0.024*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.11 + 0.031*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
G to Q1	t_{PLH}	1.02	0.99 + 0.013*SL	0.99 + 0.013*SL	0.99 + 0.013*SL
	t_{PHL}	0.94	0.91 + 0.019*SL	0.91 + 0.017*SL	0.92 + 0.016*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D2 to Q2	t_{PLH}	0.59	0.56 + 0.014*SL	0.57 + 0.013*SL	0.57 + 0.013*SL
	t_{PHL}	0.81	0.77 + 0.019*SL	0.78 + 0.017*SL	0.78 + 0.016*SL
	t_R	0.15	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
G to Q2	t_{PLH}	1.02	0.99 + 0.013*SL	0.99 + 0.013*SL	0.99 + 0.013*SL
	t_{PHL}	0.94	0.91 + 0.019*SL	0.91 + 0.017*SL	0.92 + 0.016*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D3 to Q3	t_{PLH}	0.59	0.56 + 0.014*SL	0.56 + 0.013*SL	0.57 + 0.013*SL
	t_{PHL}	0.80	0.77 + 0.019*SL	0.77 + 0.017*SL	0.78 + 0.016*SL
	t_R	0.15	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.034*SL	0.11 + 0.030*SL	0.09 + 0.032*SL
G to Q3	t_{PLH}	1.01	0.98 + 0.014*SL	0.99 + 0.013*SL	0.99 + 0.013*SL
	t_{PHL}	0.95	0.91 + 0.019*SL	0.91 + 0.017*SL	0.92 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D0 to QN0	t_{PLH}	0.57	0.54 + 0.018*SL	0.55 + 0.015*SL	0.56 + 0.013*SL
	t_{PHL}	0.46	0.42 + 0.024*SL	0.43 + 0.019*SL	0.46 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
G to QN0	t_{PLH}	0.71	0.68 + 0.018*SL	0.69 + 0.015*SL	0.70 + 0.013*SL
	t_{PHL}	0.89	0.84 + 0.024*SL	0.85 + 0.019*SL	0.88 + 0.017*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

LD1X4D2

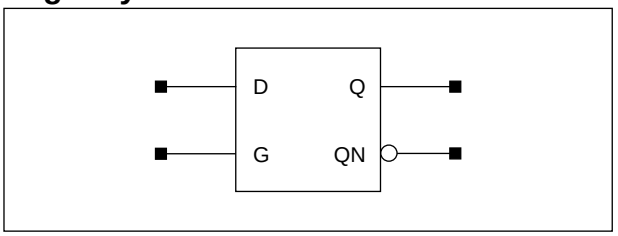
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.57	0.54 + 0.018*SL	0.55 + 0.015*SL	0.56 + 0.013*SL
	t_{PHL}	0.47	0.42 + 0.023*SL	0.43 + 0.019*SL	0.46 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
G to QN1	t_{PLH}	0.71	0.68 + 0.018*SL	0.69 + 0.015*SL	0.70 + 0.013*SL
	t_{PHL}	0.89	0.84 + 0.023*SL	0.85 + 0.019*SL	0.88 + 0.017*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
D2 to QN2	t_{PLH}	0.57	0.54 + 0.018*SL	0.55 + 0.015*SL	0.56 + 0.013*SL
	t_{PHL}	0.46	0.42 + 0.024*SL	0.43 + 0.019*SL	0.46 + 0.017*SL
	t_R	0.17	0.12 + 0.026*SL	0.12 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
G to QN2	t_{PLH}	0.71	0.68 + 0.018*SL	0.69 + 0.015*SL	0.70 + 0.013*SL
	t_{PHL}	0.89	0.84 + 0.023*SL	0.85 + 0.019*SL	0.88 + 0.017*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
D3 to QN3	t_{PLH}	0.57	0.54 + 0.018*SL	0.55 + 0.015*SL	0.56 + 0.013*SL
	t_{PHL}	0.46	0.42 + 0.024*SL	0.43 + 0.019*SL	0.46 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
G to QN3	t_{PLH}	0.72	0.68 + 0.018*SL	0.69 + 0.015*SL	0.71 + 0.013*SL
	t_{PHL}	0.89	0.84 + 0.023*SL	0.85 + 0.019*SL	0.88 + 0.017*SL
	t_R	0.16	0.11 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

YLD1/YLD1D2

Fast D Latch with Active High, 1X/2X Drive

Logic Symbol



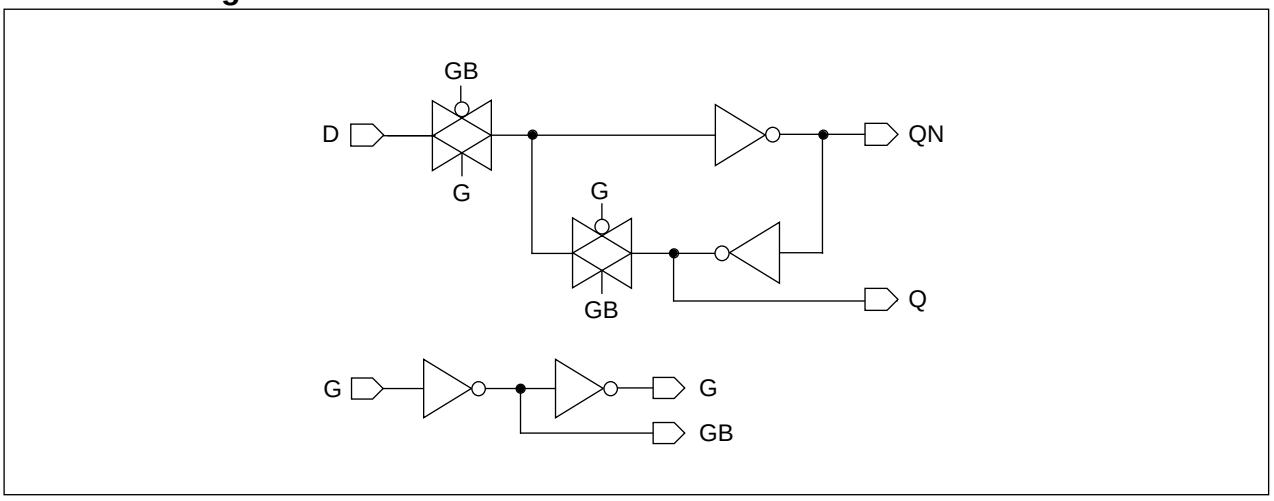
Truth Table

D	G	Q (n+1)	QN (n+1)
0	1	0	1
1	1	1	0
x	0	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
YLD1		*YLD1D2*		*YLD1*	*YLD1D2*
D	G	D	G		
2.3	0.6	3.3	0.6	2.7	3.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		YLD1	YLD1D2
Pulse Width High (G)	t_{PWH}	0.79	0.79
Input Setup Time (D to G)	t_{SU}	0.33	0.38
Input Hold Time (D to G)	t_{HD}	0.44	0.40

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

YLD1

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.42	0.25 + 0.082*SL	0.27 + 0.077*SL	0.28 + 0.076*SL
	t_{PHL}	0.40	0.25 + 0.075*SL	0.26 + 0.073*SL	0.26 + 0.073*SL
	t_R	0.25	0.11 + 0.069*SL	0.10 + 0.071*SL	0.10 + 0.071*SL
	t_F	0.24	0.09 + 0.072*SL	0.08 + 0.075*SL	0.08 + 0.075*SL
G to Q	t_{PLH}	0.61	0.45 + 0.080*SL	0.45 + 0.077*SL	0.46 + 0.076*SL
	t_{PHL}	0.57	0.42 + 0.073*SL	0.43 + 0.073*SL	0.43 + 0.073*SL
	t_R	0.24	0.10 + 0.069*SL	0.10 + 0.071*SL	0.10 + 0.071*SL
	t_F	0.23	0.08 + 0.075*SL	0.08 + 0.075*SL	0.08 + 0.075*SL
D to QN	t_{PLH}	0.24	0.18 + 0.029*SL	0.19 + 0.027*SL	0.19 + 0.027*SL
	t_{PHL}	0.27	0.19 + 0.039*SL	0.20 + 0.034*SL	0.22 + 0.033*SL
	t_R	0.29	0.19 + 0.049*SL	0.17 + 0.056*SL	0.13 + 0.060*SL
	t_F	0.34	0.23 + 0.056*SL	0.21 + 0.060*SL	0.17 + 0.065*SL
G to QN	t_{PLH}	0.41	0.35 + 0.028*SL	0.36 + 0.027*SL	0.36 + 0.027*SL
	t_{PHL}	0.46	0.39 + 0.037*SL	0.39 + 0.034*SL	0.41 + 0.033*SL
	t_R	0.26	0.15 + 0.054*SL	0.14 + 0.059*SL	0.12 + 0.060*SL
	t_F	0.30	0.19 + 0.059*SL	0.17 + 0.063*SL	0.15 + 0.065*SL

YLD1D2

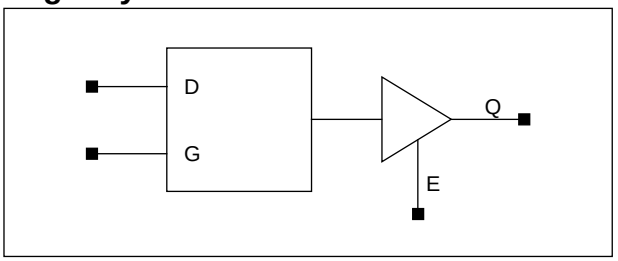
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.35	0.26 + 0.044*SL	0.27 + 0.040*SL	0.30 + 0.038*SL
	t_{PHL}	0.34	0.26 + 0.038*SL	0.27 + 0.036*SL	0.28 + 0.036*SL
	t_R	0.16	0.10 + 0.033*SL	0.09 + 0.034*SL	0.09 + 0.035*SL
	t_F	0.15	0.07 + 0.037*SL	0.07 + 0.037*SL	0.07 + 0.037*SL
G to Q	t_{PLH}	0.57	0.48 + 0.044*SL	0.49 + 0.040*SL	0.51 + 0.038*SL
	t_{PHL}	0.52	0.44 + 0.038*SL	0.44 + 0.036*SL	0.45 + 0.036*SL
	t_R	0.16	0.09 + 0.034*SL	0.09 + 0.034*SL	0.09 + 0.035*SL
	t_F	0.15	0.07 + 0.036*SL	0.07 + 0.037*SL	0.07 + 0.038*SL
D to QN	t_{PLH}	0.23	0.21 + 0.015*SL	0.21 + 0.014*SL	0.21 + 0.013*SL
	t_{PHL}	0.25	0.21 + 0.023*SL	0.22 + 0.019*SL	0.24 + 0.017*SL
	t_R	0.22	0.18 + 0.021*SL	0.17 + 0.026*SL	0.14 + 0.029*SL
	t_F	0.29	0.24 + 0.026*SL	0.23 + 0.029*SL	0.21 + 0.032*SL
G to QN	t_{PLH}	0.41	0.38 + 0.015*SL	0.38 + 0.014*SL	0.39 + 0.013*SL
	t_{PHL}	0.47	0.43 + 0.022*SL	0.43 + 0.019*SL	0.46 + 0.017*SL
	t_R	0.20	0.16 + 0.023*SL	0.15 + 0.027*SL	0.13 + 0.029*SL
	t_F	0.26	0.21 + 0.027*SL	0.20 + 0.031*SL	0.19 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

LD1A

D Latch with Active High, Tri-State Output

Logic Symbol



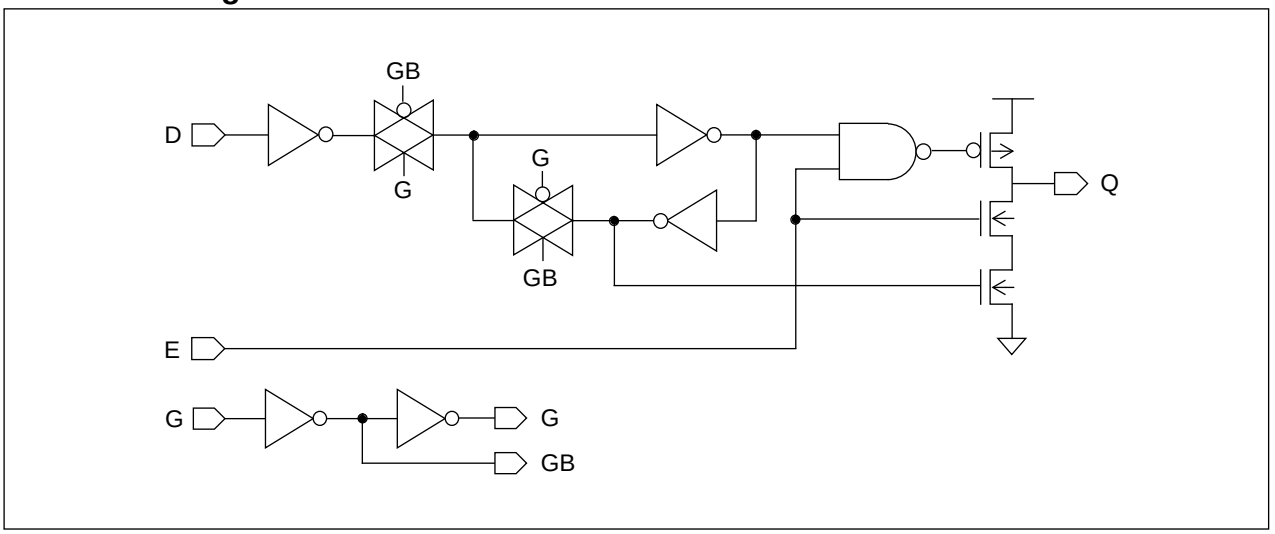
Truth Table

D	G	E	Q (n+1)
x	x	0	Hi-Z
0	1	1	0
1	1	1	1
x	0	1	Q (n)

Cell Data

Input Load (SL)			Output Load (SL)	Gate Count
D	G	E	Q	
0.6	0.6	0.9	1.0	4.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width High (G)	t_{PWH}	0.79
Input Setup Time (D to G)	t_{SU}	0.49
Input Hold Time (D to G)	t_{HD}	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

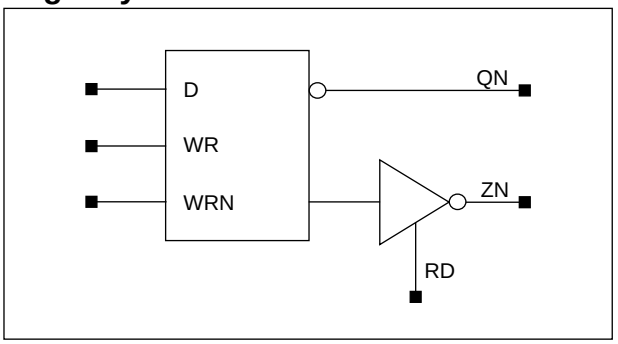
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.62	0.57 + 0.021*SL	0.59 + 0.016*SL	0.61 + 0.014*SL
	t_{PHL}	0.69	0.62 + 0.036*SL	0.62 + 0.037*SL	0.61 + 0.037*SL
	t_R	0.18	0.12 + 0.030*SL	0.12 + 0.028*SL	0.11 + 0.030*SL
	t_F	0.27	0.12 + 0.075*SL	0.11 + 0.079*SL	0.10 + 0.081*SL
G to Q	t_{PLH}	0.77	0.73 + 0.022*SL	0.74 + 0.016*SL	0.76 + 0.014*SL
	t_{PHL}	0.70	0.63 + 0.037*SL	0.63 + 0.037*SL	0.62 + 0.037*SL
	t_R	0.18	0.12 + 0.029*SL	0.12 + 0.029*SL	0.11 + 0.030*SL
	t_F	0.28	0.13 + 0.072*SL	0.11 + 0.079*SL	0.10 + 0.081*SL
E to Q	t_{PLH}	0.22	0.18 + 0.022*SL	0.19 + 0.016*SL	0.22 + 0.014*SL
	t_{PHL}	0.16	0.06 + 0.047*SL	0.09 + 0.038*SL	0.09 + 0.037*SL
	t_R	0.19	0.14 + 0.026*SL	0.13 + 0.028*SL	0.11 + 0.030*SL
	t_F	0.32	0.18 + 0.070*SL	0.17 + 0.075*SL	0.11 + 0.081*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.35	0.35 + 0.001*SL	0.35 + 0.000*SL	0.35 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

LD1B

D Latch with Active High, Tri-State Output, Separate WR, WRN

Logic Symbol



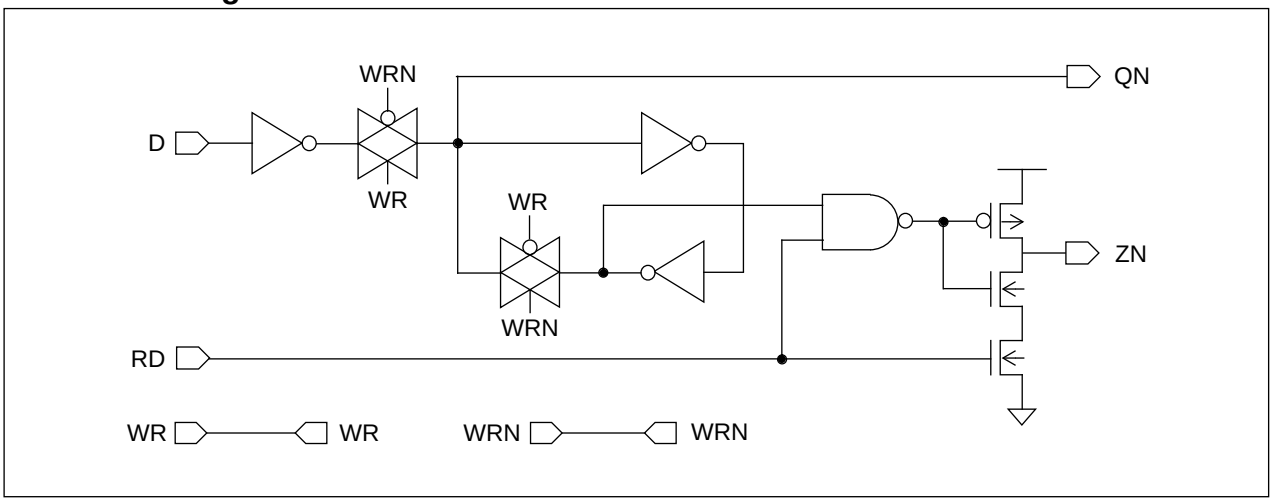
Truth Table

D	WR	WRN	RD	QN (n+1)	ZN (n+1)
0	1	0	0	1	Hi-Z
1	1	0	0	0	Hi-Z
0	1	0	1	1	1
1	1	0	1	0	0
x	0	1	0	QN (n)	Hi-Z
x	0	1	1	QN (n)	QN (n)

Cell Data

Input Load (SL)				Output Load (SL)	Gate Count
D	WR	WRN	RD	ZN	
0.5	0.5	0.6	1.0	1.0	4.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width High (WR)	t_{PWH}	0.79
Pulse Width Low (WRN)	t_{PWL}	0.79
Input Setup Time (D to WR)	t_{SU}	0.85
Input Hold Time (D to WR)	t_{HD}	0.33
Input Setup Time (D to WRN)	t_{SU}	0.82
Input Hold Time (D to WRN)	t_{HD}	0.85
Skew Time (WR to WRN)	t_{SK}	0.74
Skew Time (WRN to WR)	t_{SK}	0.94

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

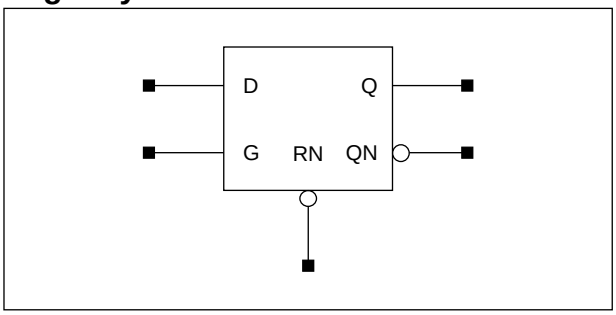
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to QN	t_{PLH}	0.47	0.29 + 0.092*SL	0.29 + 0.091*SL	0.30 + 0.090*SL
	t_{PHL}	0.23	0.14 + 0.048*SL	0.14 + 0.046*SL	0.14 + 0.046*SL
	t_R	1.07	0.50 + 0.284*SL	0.48 + 0.292*SL	0.47 + 0.293*SL
	t_F	0.41	0.21 + 0.100*SL	0.19 + 0.106*SL	0.17 + 0.108*SL
WR to QN	t_{PLH}	0.33	0.17 + 0.079*SL	0.15 + 0.087*SL	0.12 + 0.090*SL
	t_{PHL}	0.20	0.11 + 0.047*SL	0.12 + 0.045*SL	0.11 + 0.046*SL
	t_R	1.04	0.49 + 0.278*SL	0.45 + 0.293*SL	0.44 + 0.293*SL
	t_F	0.43	0.23 + 0.097*SL	0.21 + 0.104*SL	0.17 + 0.108*SL
WRN to QN	t_{PLH}	0.33	0.17 + 0.079*SL	0.15 + 0.087*SL	0.12 + 0.090*SL
	t_{PHL}	0.20	0.11 + 0.047*SL	0.12 + 0.045*SL	0.11 + 0.046*SL
	t_R	1.04	0.49 + 0.278*SL	0.45 + 0.293*SL	0.44 + 0.293*SL
	t_F	0.43	0.23 + 0.097*SL	0.21 + 0.104*SL	0.17 + 0.108*SL
D to ZN	t_{PLH}	0.97	0.76 + 0.104*SL	0.80 + 0.093*SL	0.89 + 0.084*SL
	t_{PHL}	0.85	0.62 + 0.114*SL	0.64 + 0.109*SL	0.69 + 0.103*SL
	t_R	0.19	0.13 + 0.029*SL	0.13 + 0.028*SL	0.11 + 0.030*SL
	t_F	0.28	0.12 + 0.077*SL	0.12 + 0.079*SL	0.10 + 0.081*SL
WR to ZN	t_{PLH}	0.83	0.65 + 0.090*SL	0.65 + 0.089*SL	0.70 + 0.083*SL
	t_{PHL}	0.82	0.59 + 0.114*SL	0.61 + 0.108*SL	0.66 + 0.103*SL
	t_R	0.19	0.13 + 0.027*SL	0.13 + 0.028*SL	0.11 + 0.030*SL
	t_F	0.28	0.12 + 0.077*SL	0.12 + 0.079*SL	0.10 + 0.081*SL
WRN to ZN	t_{PLH}	0.83	0.65 + 0.090*SL	0.65 + 0.089*SL	0.70 + 0.083*SL
	t_{PHL}	0.82	0.59 + 0.114*SL	0.61 + 0.108*SL	0.66 + 0.103*SL
	t_R	0.19	0.13 + 0.027*SL	0.13 + 0.028*SL	0.11 + 0.030*SL
	t_F	0.28	0.12 + 0.077*SL	0.12 + 0.079*SL	0.10 + 0.081*SL
RD to ZN	t_{PLH}	0.26	0.22 + 0.019*SL	0.23 + 0.016*SL	0.25 + 0.014*SL
	t_{PHL}	0.16	0.06 + 0.047*SL	0.09 + 0.038*SL	0.09 + 0.037*SL
	t_R	0.19	0.14 + 0.026*SL	0.13 + 0.028*SL	0.12 + 0.030*SL
	t_F	0.32	0.18 + 0.070*SL	0.16 + 0.075*SL	0.11 + 0.081*SL
	t_{PLZ}	0.18	0.18 + 0.000*SL	0.18 + 0.000*SL	0.18 + 0.000*SL
	t_{PHZ}	0.39	0.39 + 0.000*SL	0.39 + 0.000*SL	0.39 + 0.000*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

LD2/LD2D2

D Latch with Active High, Reset, 1X/2X Drive

Logic Symbol



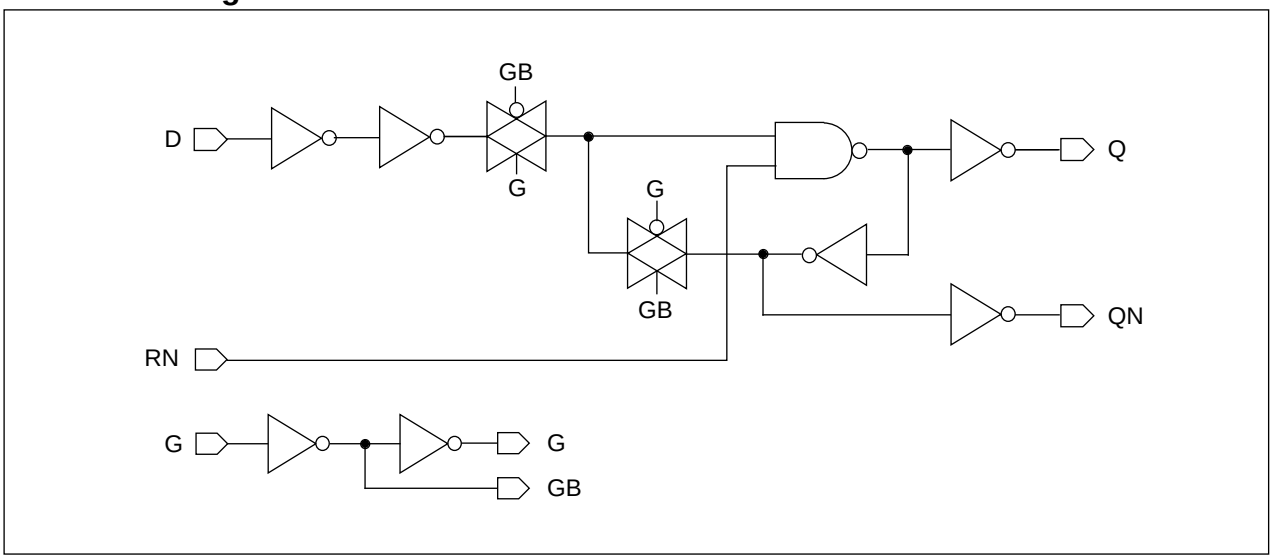
Truth Table

D	G	RN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
LD2/LD2D2			*LD2/LD2D2*			*LD2*	*LD2D2*
D	G	RN	D	G	RN		
0.6	0.6	0.8	0.6	0.6	0.8	4.7	5.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD2	LD2D2
Pulse Width High (G)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Input Setup Time (D to G)	t_{SU}	0.55	0.74
Input Hold Time (D to G)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RM to G)	t_{RC}	0.44	0.38

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.62	0.55 + 0.035*SL	0.57 + 0.030*SL	0.59 + 0.027*SL
	t_{PHL}	0.68	0.60 + 0.040*SL	0.62 + 0.035*SL	0.63 + 0.033*SL
	t_R	0.25	0.14 + 0.058*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
G to Q	t_{PLH}	0.64	0.57 + 0.035*SL	0.58 + 0.029*SL	0.61 + 0.027*SL
	t_{PHL}	0.65	0.57 + 0.040*SL	0.59 + 0.035*SL	0.60 + 0.033*SL
	t_R	0.25	0.13 + 0.058*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q	t_{PLH}	0.33	0.26 + 0.034*SL	0.28 + 0.029*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.30 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.24	0.13 + 0.058*SL	0.13 + 0.058*SL	0.11 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
D to QN	t_{PLH}	0.74	0.68 + 0.028*SL	0.68 + 0.027*SL	0.68 + 0.027*SL
	t_{PHL}	0.80	0.73 + 0.035*SL	0.73 + 0.033*SL	0.74 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.10 + 0.063*SL	0.07 + 0.066*SL
G to QN	t_{PLH}	0.71	0.65 + 0.028*SL	0.66 + 0.027*SL	0.66 + 0.027*SL
	t_{PHL}	0.81	0.74 + 0.035*SL	0.75 + 0.033*SL	0.75 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
RN to QN	t_{PLH}	0.49	0.42 + 0.032*SL	0.44 + 0.028*SL	0.45 + 0.027*SL
	t_{PHL}	0.50	0.43 + 0.035*SL	0.44 + 0.033*SL	0.44 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.063*SL	0.07 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

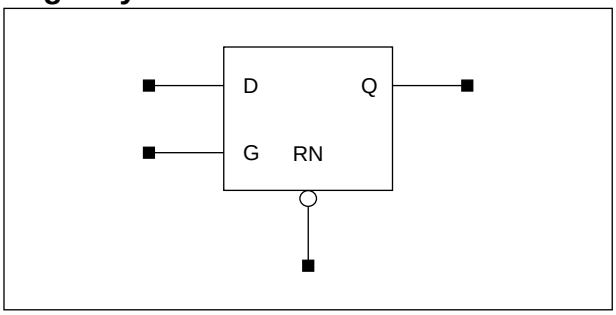
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.63	0.59 + 0.021*SL	0.60 + 0.016*SL	0.63 + 0.013*SL
	t_{PHL}	0.68	0.63 + 0.024*SL	0.64 + 0.019*SL	0.67 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
G to Q	t_{PLH}	0.65	0.60 + 0.022*SL	0.62 + 0.016*SL	0.65 + 0.013*SL
	t_{PHL}	0.65	0.60 + 0.024*SL	0.61 + 0.019*SL	0.64 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.14 + 0.028*SL	0.14 + 0.028*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
RN to Q	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.34 + 0.013*SL
	t_{PHL}	0.36	0.32 + 0.024*SL	0.33 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.18	0.11 + 0.033*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
D to QN	t_{PLH}	0.80	0.78 + 0.014*SL	0.78 + 0.013*SL	0.78 + 0.013*SL
	t_{PHL}	0.89	0.86 + 0.017*SL	0.86 + 0.016*SL	0.86 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
G to QN	t_{PLH}	0.77	0.75 + 0.014*SL	0.75 + 0.013*SL	0.75 + 0.013*SL
	t_{PHL}	0.91	0.87 + 0.017*SL	0.87 + 0.016*SL	0.88 + 0.016*SL
	t_R	0.16	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
RN to QN	t_{PLH}	0.55	0.52 + 0.017*SL	0.52 + 0.014*SL	0.54 + 0.013*SL
	t_{PHL}	0.59	0.56 + 0.018*SL	0.56 + 0.017*SL	0.57 + 0.016*SL
	t_R	0.18	0.13 + 0.026*SL	0.13 + 0.026*SL	0.11 + 0.028*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.030*SL	0.10 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



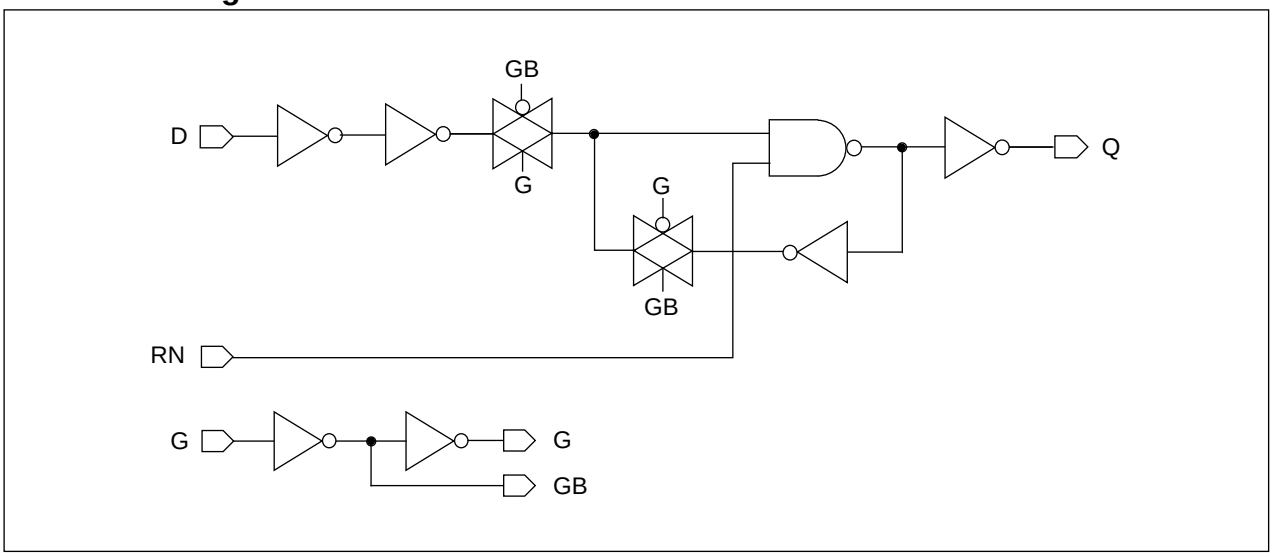
Truth Table

D	G	RN	Q (n+1)
0	1	1	0
1	1	1	1
x	0	1	Q (n)
x	x	0	0

Cell Data

Input Load (SL)						Gate Count	
LD2Q			*LD2QD2*			*LD2Q*	*LD2QD2*
D	G	RN	D	G	RN		
0.6	0.6	0.8	0.6	0.6	0.8	4.3	4.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD2Q	LD2QD2
Pulse Width High (G)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Input Setup Time (D to G)	t_{SU}	0.55	0.57
Input Hold Time (D to G)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to G)	t_{RC}	0.44	0.38

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD2Q

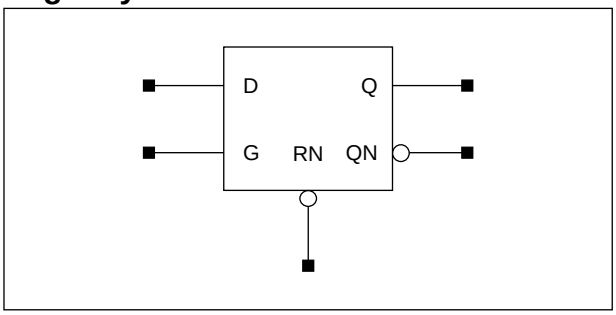
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.62	0.55 + 0.035*SL	0.56 + 0.029*SL	0.58 + 0.027*SL
	t_{PHL}	0.67	0.59 + 0.039*SL	0.61 + 0.034*SL	0.62 + 0.033*SL
	t_R	0.25	0.14 + 0.056*SL	0.13 + 0.057*SL	0.11 + 0.060*SL
	t_F	0.24	0.11 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
G to Q	t_{PLH}	0.63	0.56 + 0.035*SL	0.58 + 0.029*SL	0.60 + 0.027*SL
	t_{PHL}	0.64	0.56 + 0.039*SL	0.58 + 0.034*SL	0.59 + 0.033*SL
	t_R	0.25	0.13 + 0.057*SL	0.13 + 0.057*SL	0.11 + 0.060*SL
	t_F	0.24	0.12 + 0.061*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
RN to Q	t_{PLH}	0.32	0.25 + 0.034*SL	0.27 + 0.029*SL	0.29 + 0.027*SL
	t_{PHL}	0.36	0.28 + 0.038*SL	0.29 + 0.034*SL	0.30 + 0.033*SL
	t_R	0.24	0.13 + 0.057*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.23	0.11 + 0.061*SL	0.11 + 0.063*SL	0.08 + 0.065*SL

LD2QD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.62	0.58 + 0.021*SL	0.60 + 0.016*SL	0.63 + 0.013*SL
	t_{PHL}	0.67	0.62 + 0.024*SL	0.64 + 0.019*SL	0.66 + 0.017*SL
	t_R	0.20	0.15 + 0.027*SL	0.14 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.030*SL	0.11 + 0.032*SL
G to Q	t_{PLH}	0.64	0.60 + 0.021*SL	0.61 + 0.016*SL	0.64 + 0.013*SL
	t_{PHL}	0.64	0.59 + 0.024*SL	0.61 + 0.019*SL	0.63 + 0.017*SL
	t_R	0.20	0.14 + 0.026*SL	0.14 + 0.028*SL	0.13 + 0.028*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.030*SL	0.11 + 0.032*SL
RN to Q	t_{PLH}	0.33	0.29 + 0.020*SL	0.30 + 0.016*SL	0.33 + 0.013*SL
	t_{PHL}	0.36	0.31 + 0.023*SL	0.32 + 0.019*SL	0.34 + 0.016*SL
	t_R	0.19	0.14 + 0.027*SL	0.13 + 0.028*SL	0.13 + 0.028*SL
	t_F	0.17	0.11 + 0.033*SL	0.12 + 0.030*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



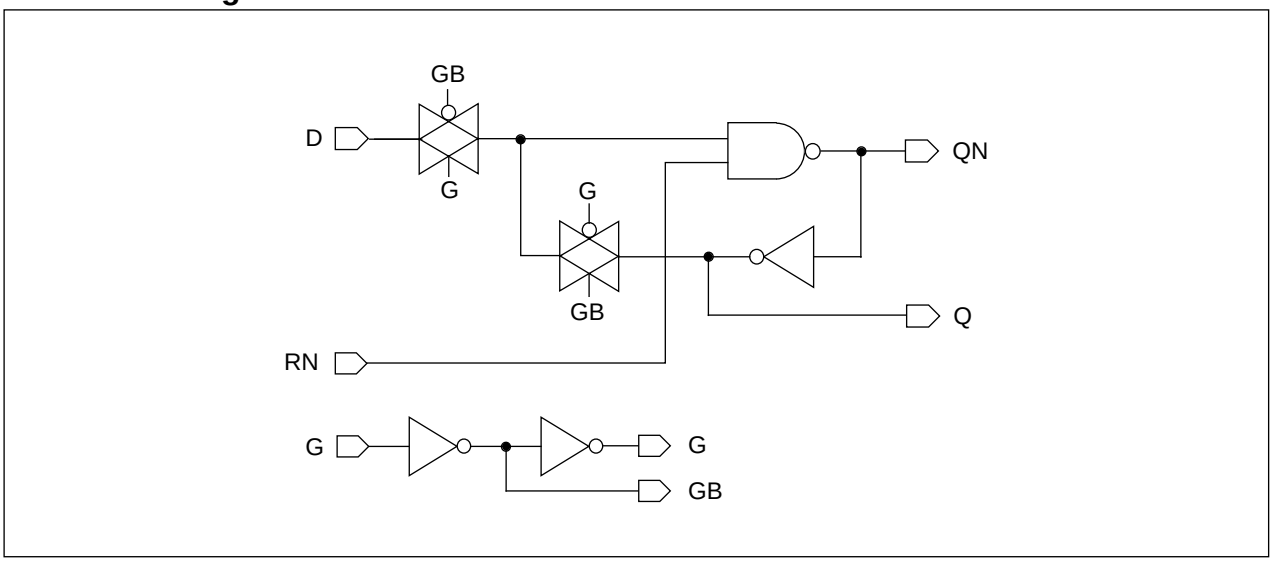
Truth Table

D	G	RN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
YLD2			*YLD2D2*			*YLD2*	*YLD2D2*
D	G	RN	D	G	RN		
2.4	0.6	0.8	3.5	0.6	1.5	3.0	3.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		YLD2	YLD2D2
Pulse Width High (G)	t_{PWH}	0.79	0.79
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Input Setup Time (D to G)	t_{SU}	0.33	0.33
Input Hold Time (D to G)	t_{HD}	0.38	0.38
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to G)	t_{RC}	0.49	0.55

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

YLD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.42	0.25 + 0.086*SL	0.26 + 0.084*SL	0.26 + 0.084*SL
	t_{PHL}	0.44	0.29 + 0.076*SL	0.29 + 0.074*SL	0.29 + 0.074*SL
	t_R	0.26	0.11 + 0.074*SL	0.11 + 0.075*SL	0.11 + 0.076*SL
	t_F	0.24	0.09 + 0.075*SL	0.09 + 0.076*SL	0.09 + 0.076*SL
G to Q	t_{PLH}	0.63	0.46 + 0.086*SL	0.46 + 0.085*SL	0.47 + 0.084*SL
	t_{PHL}	0.61	0.45 + 0.076*SL	0.46 + 0.075*SL	0.46 + 0.074*SL
	t_R	0.26	0.11 + 0.075*SL	0.11 + 0.075*SL	0.11 + 0.076*SL
	t_F	0.24	0.09 + 0.075*SL	0.09 + 0.076*SL	0.09 + 0.076*SL
RN to Q	t_{PLH}	0.38	0.21 + 0.085*SL	0.21 + 0.084*SL	0.21 + 0.084*SL
	t_{PHL}	0.40	0.24 + 0.081*SL	0.26 + 0.076*SL	0.28 + 0.074*SL
	t_R	0.26	0.11 + 0.076*SL	0.11 + 0.075*SL	0.11 + 0.076*SL
	t_F	0.38	0.24 + 0.070*SL	0.23 + 0.074*SL	0.21 + 0.075*SL
D to QN	t_{PLH}	0.27	0.22 + 0.028*SL	0.22 + 0.028*SL	0.21 + 0.028*SL
	t_{PHL}	0.26	0.18 + 0.040*SL	0.19 + 0.038*SL	0.19 + 0.037*SL
	t_R	0.33	0.22 + 0.052*SL	0.20 + 0.059*SL	0.17 + 0.063*SL
	t_F	0.40	0.27 + 0.068*SL	0.24 + 0.076*SL	0.20 + 0.080*SL
G to QN	t_{PLH}	0.44	0.38 + 0.028*SL	0.38 + 0.028*SL	0.38 + 0.028*SL
	t_{PHL}	0.47	0.39 + 0.039*SL	0.40 + 0.038*SL	0.40 + 0.037*SL
	t_R	0.30	0.19 + 0.056*SL	0.17 + 0.061*SL	0.16 + 0.063*SL
	t_F	0.37	0.23 + 0.074*SL	0.21 + 0.078*SL	0.19 + 0.081*SL
RN to QN	t_{PLH}	0.20	0.14 + 0.030*SL	0.15 + 0.028*SL	0.14 + 0.028*SL
	t_{PHL}	0.22	0.14 + 0.039*SL	0.15 + 0.037*SL	0.14 + 0.037*SL
	t_R	0.32	0.21 + 0.052*SL	0.19 + 0.058*SL	0.17 + 0.061*SL
	t_F	0.39	0.25 + 0.069*SL	0.23 + 0.076*SL	0.19 + 0.081*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

YLD2D2

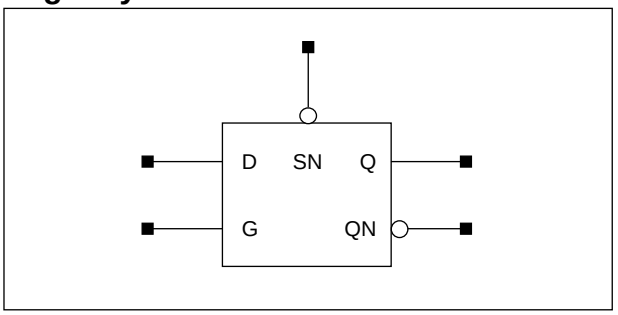
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.38	0.27 + 0.060*SL	0.27 + 0.058*SL	0.28 + 0.057*SL
	t_{PHL}	0.41	0.30 + 0.056*SL	0.30 + 0.054*SL	0.31 + 0.054*SL
	t_R	0.24	0.11 + 0.064*SL	0.10 + 0.066*SL	0.10 + 0.066*SL
	t_F	0.22	0.09 + 0.067*SL	0.08 + 0.069*SL	0.08 + 0.069*SL
G to Q	t_{PLH}	0.61	0.49 + 0.060*SL	0.50 + 0.058*SL	0.51 + 0.057*SL
	t_{PHL}	0.59	0.47 + 0.056*SL	0.48 + 0.054*SL	0.49 + 0.054*SL
	t_R	0.23	0.10 + 0.065*SL	0.10 + 0.066*SL	0.10 + 0.066*SL
	t_F	0.22	0.09 + 0.068*SL	0.08 + 0.069*SL	0.08 + 0.069*SL
RN to Q	t_{PLH}	0.30	0.18 + 0.059*SL	0.18 + 0.057*SL	0.19 + 0.057*SL
	t_{PHL}	0.34	0.21 + 0.064*SL	0.23 + 0.058*SL	0.27 + 0.054*SL
	t_R	0.23	0.11 + 0.061*SL	0.10 + 0.066*SL	0.09 + 0.066*SL
	t_F	0.45	0.33 + 0.060*SL	0.31 + 0.066*SL	0.29 + 0.068*SL
D to QN	t_{PLH}	0.26	0.23 + 0.015*SL	0.23 + 0.014*SL	0.24 + 0.014*SL
	t_{PHL}	0.24	0.20 + 0.022*SL	0.20 + 0.020*SL	0.21 + 0.019*SL
	t_R	0.24	0.19 + 0.023*SL	0.18 + 0.027*SL	0.15 + 0.030*SL
	t_F	0.30	0.23 + 0.032*SL	0.22 + 0.036*SL	0.19 + 0.040*SL
G to QN	t_{PLH}	0.43	0.41 + 0.015*SL	0.41 + 0.014*SL	0.41 + 0.014*SL
	t_{PHL}	0.47	0.42 + 0.022*SL	0.43 + 0.020*SL	0.44 + 0.019*SL
	t_R	0.22	0.17 + 0.025*SL	0.16 + 0.028*SL	0.14 + 0.030*SL
	t_F	0.27	0.20 + 0.035*SL	0.19 + 0.037*SL	0.17 + 0.040*SL
RN to QN	t_{PLH}	0.14	0.11 + 0.018*SL	0.12 + 0.014*SL	0.13 + 0.014*SL
	t_{PHL}	0.16	0.11 + 0.023*SL	0.12 + 0.019*SL	0.13 + 0.019*SL
	t_R	0.23	0.18 + 0.023*SL	0.17 + 0.026*SL	0.14 + 0.030*SL
	t_F	0.27	0.21 + 0.029*SL	0.19 + 0.036*SL	0.16 + 0.040*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

LD3/LD3D2

D Latch with Active High, Set, 1X/2X Drive

Logic Symbol



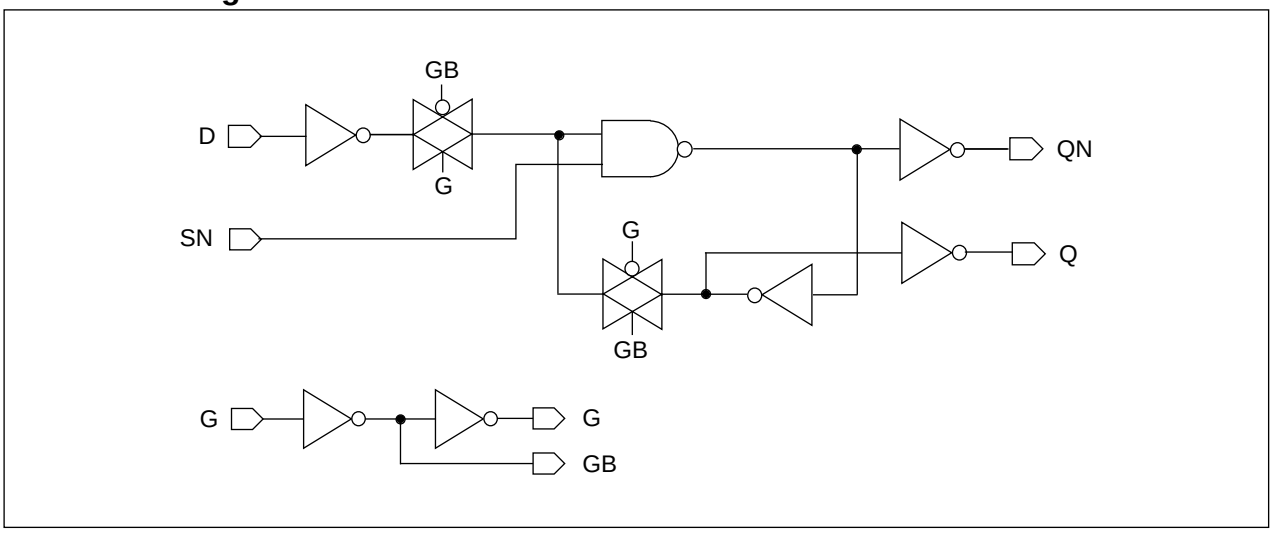
Truth Table

D	G	SN	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	0	1	Q (n)	QN (n)
x	x	0	1	0

Cell Data

Input Load (SL)						Gate Count	
LD3			*LD3D2*			*LD3*	*LD3D2*
D	G	SN	D	G	SN		
0.6	0.6	0.5	0.6	0.6	0.5	4.3	5.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD3	LD3D2
Pulse Width High (G)	t_{PWH}	0.79	0.79
Pulse Width Low (SN)	t_{PWL}	0.79	0.79
Input Setup Time (D to G)	t_{SU}	0.57	0.66
Input Hold Time (D to G)	t_{HD}	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time(SN to G)	t_{RC}	0.44	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD3

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.55	0.49 + 0.028*SL	0.50 + 0.027*SL	0.50 + 0.027*SL
	t_{PHL}	0.80	0.73 + 0.035*SL	0.74 + 0.033*SL	0.74 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
G to Q	t_{PLH}	0.70	0.65 + 0.028*SL	0.65 + 0.027*SL	0.65 + 0.027*SL
	t_{PHL}	0.81	0.74 + 0.035*SL	0.74 + 0.033*SL	0.75 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
SN to Q	t_{PLH}	0.49	0.42 + 0.032*SL	0.44 + 0.028*SL	0.45 + 0.027*SL
	t_{PHL}	0.50	0.43 + 0.035*SL	0.44 + 0.033*SL	0.44 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
D to QN	t_{PLH}	0.63	0.56 + 0.035*SL	0.57 + 0.029*SL	0.60 + 0.027*SL
	t_{PHL}	0.49	0.41 + 0.040*SL	0.43 + 0.035*SL	0.44 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.061*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
G to QN	t_{PLH}	0.63	0.56 + 0.035*SL	0.58 + 0.030*SL	0.60 + 0.027*SL
	t_{PHL}	0.65	0.57 + 0.040*SL	0.58 + 0.035*SL	0.60 + 0.033*SL
	t_R	0.25	0.14 + 0.056*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
SN to QN	t_{PLH}	0.33	0.26 + 0.034*SL	0.28 + 0.029*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.30 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.24	0.13 + 0.058*SL	0.13 + 0.058*SL	0.11 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

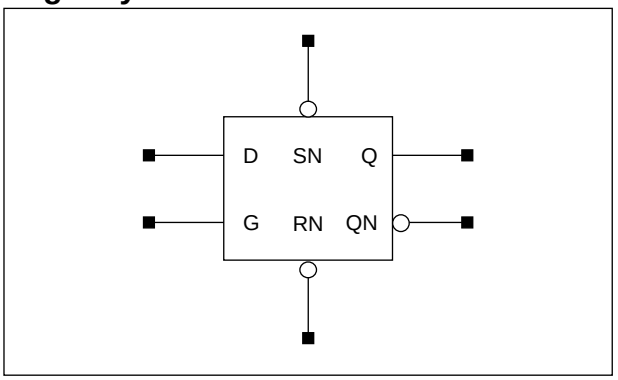
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD3D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.62	0.59 + 0.014*SL	0.59 + 0.013*SL	0.59 + 0.013*SL
	t_{PHL}	0.90	0.86 + 0.017*SL	0.86 + 0.016*SL	0.86 + 0.016*SL
	t_R	0.16	0.11 + 0.025*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.18	0.11 + 0.033*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
G to Q	t_{PLH}	0.77	0.74 + 0.014*SL	0.74 + 0.013*SL	0.75 + 0.013*SL
	t_{PHL}	0.90	0.87 + 0.017*SL	0.87 + 0.016*SL	0.87 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
SN to Q	t_{PLH}	0.55	0.52 + 0.017*SL	0.53 + 0.014*SL	0.54 + 0.013*SL
	t_{PHL}	0.59	0.56 + 0.018*SL	0.56 + 0.017*SL	0.57 + 0.016*SL
	t_R	0.18	0.13 + 0.026*SL	0.13 + 0.026*SL	0.11 + 0.028*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
D to QN	t_{PLH}	0.63	0.59 + 0.022*SL	0.61 + 0.016*SL	0.63 + 0.013*SL
	t_{PHL}	0.49	0.44 + 0.024*SL	0.45 + 0.020*SL	0.48 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.19	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
G to QN	t_{PLH}	0.64	0.60 + 0.022*SL	0.61 + 0.016*SL	0.64 + 0.013*SL
	t_{PHL}	0.64	0.60 + 0.024*SL	0.61 + 0.019*SL	0.64 + 0.017*SL
	t_R	0.20	0.15 + 0.027*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.19	0.12 + 0.031*SL	0.13 + 0.031*SL	0.11 + 0.032*SL
SN to QN	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.34 + 0.013*SL
	t_{PHL}	0.36	0.32 + 0.024*SL	0.33 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.028*SL	0.13 + 0.028*SL
	t_F	0.18	0.11 + 0.033*SL	0.12 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



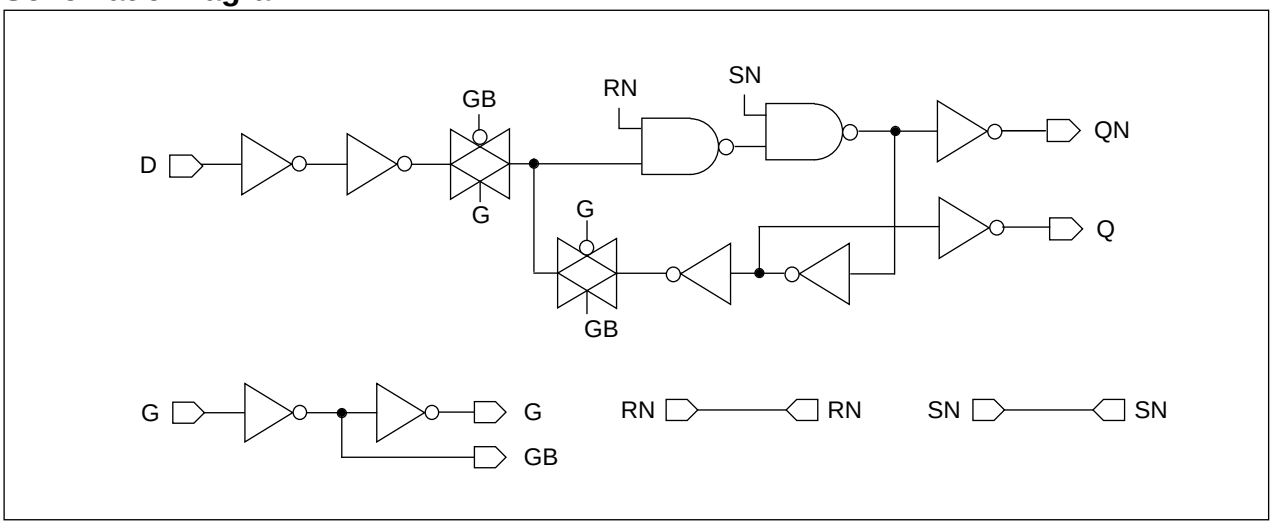
Truth Table

D	G	RN	SN	Q (n+1)	QN (n+1)
0	1	1	1	0	1
1	1	1	1	1	0
x	0	1	1	Q (n)	QN (n)
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0

Cell Data

Input Load (SL)								Gate Count	
LD4				*LD4D2*				*LD4*	*LD4D2*
D	G	SN	RN	D	G	SN	RN		
0.6	0.6	0.8	0.6	0.6	0.6	0.8	0.6	6.0	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD4	LD4D2
Pulse Width High (G)	t_{PWH}	0.79	0.74
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Pulse Width Low (SN)	t_{PWL}	0.79	0.87
Input Setup Time (D to G)	t_{SU}	0.66	0.76
Input Hold Time (D to G)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (SN to G)	t_{HD}	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.33
Input Hold Time (RN to G)	t_{HD}	0.38	0.38

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.80	0.75 + 0.029*SL	0.75 + 0.027*SL	0.76 + 0.027*SL
	t_{PHL}	1.05	0.97 + 0.037*SL	0.98 + 0.034*SL	0.99 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.12 + 0.060*SL	0.11 + 0.062*SL	0.08 + 0.065*SL
G to Q	t_{PLH}	0.82	0.76 + 0.030*SL	0.77 + 0.027*SL	0.77 + 0.027*SL
	t_{PHL}	1.02	0.94 + 0.037*SL	0.95 + 0.034*SL	0.96 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.12 + 0.060*SL	0.11 + 0.062*SL	0.08 + 0.065*SL
SN to Q	t_{PLH}	0.47	0.41 + 0.029*SL	0.41 + 0.027*SL	0.42 + 0.027*SL
	t_{PHL}	0.52	0.45 + 0.037*SL	0.46 + 0.034*SL	0.46 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.11 + 0.061*SL	0.11 + 0.062*SL	0.08 + 0.065*SL
RN to Q	t_{PLH}	0.53	0.47 + 0.029*SL	0.47 + 0.027*SL	0.48 + 0.027*SL
	t_{PHL}	0.73	0.65 + 0.037*SL	0.66 + 0.034*SL	0.67 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
D to QN	t_{PLH}	0.84	0.77 + 0.034*SL	0.78 + 0.029*SL	0.80 + 0.027*SL
	t_{PHL}	0.72	0.64 + 0.039*SL	0.65 + 0.035*SL	0.67 + 0.033*SL
	t_R	0.24	0.13 + 0.057*SL	0.13 + 0.058*SL	0.11 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
G to QN	t_{PLH}	0.81	0.74 + 0.034*SL	0.75 + 0.029*SL	0.77 + 0.027*SL
	t_{PHL}	0.73	0.65 + 0.039*SL	0.67 + 0.035*SL	0.68 + 0.033*SL
	t_R	0.24	0.13 + 0.057*SL	0.13 + 0.058*SL	0.11 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
SN to QN	t_{PLH}	0.31	0.24 + 0.034*SL	0.26 + 0.029*SL	0.28 + 0.027*SL
	t_{PHL}	0.38	0.30 + 0.039*SL	0.31 + 0.035*SL	0.33 + 0.033*SL
	t_R	0.24	0.13 + 0.057*SL	0.13 + 0.058*SL	0.11 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.064*SL	0.10 + 0.065*SL
RN to QN	t_{PLH}	0.52	0.46 + 0.034*SL	0.47 + 0.029*SL	0.49 + 0.027*SL
	t_{PHL}	0.44	0.36 + 0.039*SL	0.37 + 0.035*SL	0.39 + 0.033*SL
	t_R	0.24	0.13 + 0.058*SL	0.13 + 0.058*SL	0.11 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD4D2

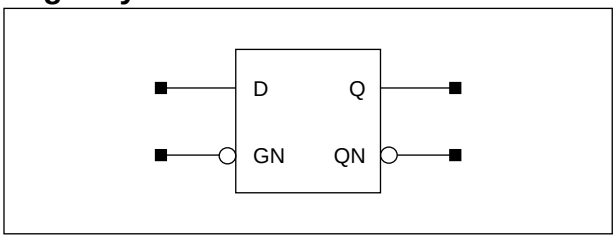
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.87	0.84 + 0.015*SL	0.84 + 0.014*SL	0.85 + 0.013*SL
	t_{PHL}	1.14	1.10 + 0.019*SL	1.11 + 0.017*SL	1.12 + 0.016*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.19	0.13 + 0.032*SL	0.13 + 0.030*SL	0.12 + 0.032*SL
G to Q	t_{PLH}	0.89	0.86 + 0.014*SL	0.86 + 0.014*SL	0.87 + 0.013*SL
	t_{PHL}	1.11	1.07 + 0.020*SL	1.08 + 0.017*SL	1.08 + 0.016*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.19	0.13 + 0.032*SL	0.13 + 0.030*SL	0.12 + 0.032*SL
SN to Q	t_{PLH}	0.53	0.50 + 0.015*SL	0.50 + 0.013*SL	0.51 + 0.013*SL
	t_{PHL}	0.61	0.57 + 0.019*SL	0.58 + 0.017*SL	0.59 + 0.016*SL
	t_R	0.16	0.11 + 0.025*SL	0.11 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.19	0.13 + 0.032*SL	0.13 + 0.030*SL	0.12 + 0.032*SL
RN to Q	t_{PLH}	0.59	0.56 + 0.015*SL	0.57 + 0.014*SL	0.57 + 0.013*SL
	t_{PHL}	0.82	0.79 + 0.019*SL	0.79 + 0.017*SL	0.80 + 0.016*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.19	0.12 + 0.033*SL	0.13 + 0.031*SL	0.12 + 0.032*SL
D to QN	t_{PLH}	0.85	0.80 + 0.021*SL	0.82 + 0.016*SL	0.84 + 0.013*SL
	t_{PHL}	0.72	0.67 + 0.024*SL	0.68 + 0.019*SL	0.71 + 0.017*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.18	0.11 + 0.034*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
G to QN	t_{PLH}	0.82	0.77 + 0.021*SL	0.79 + 0.016*SL	0.81 + 0.013*SL
	t_{PHL}	0.74	0.69 + 0.023*SL	0.70 + 0.019*SL	0.73 + 0.017*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SN to QN	t_{PLH}	0.32	0.28 + 0.021*SL	0.29 + 0.016*SL	0.32 + 0.013*SL
	t_{PHL}	0.38	0.33 + 0.024*SL	0.34 + 0.019*SL	0.37 + 0.017*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.028*SL	0.13 + 0.028*SL
	t_F	0.18	0.12 + 0.033*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
RN to QN	t_{PLH}	0.53	0.49 + 0.021*SL	0.51 + 0.016*SL	0.53 + 0.013*SL
	t_{PHL}	0.44	0.39 + 0.024*SL	0.41 + 0.019*SL	0.43 + 0.017*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

LD5/LD5D2

D Latch with Active Low, 1X/2X Drive

Logic Symbol



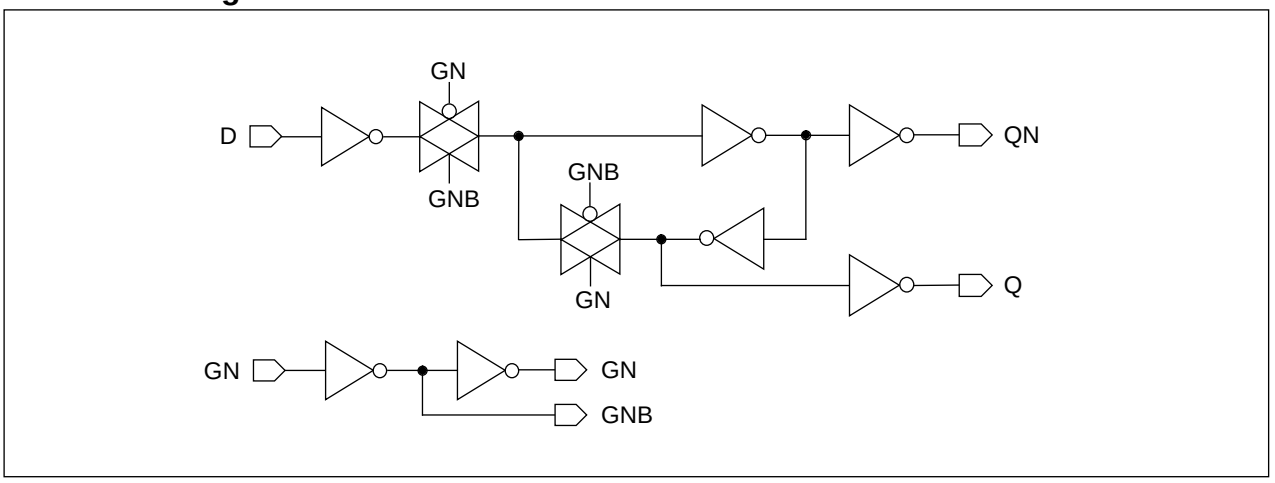
Truth Table

D	GN	Q (n+1)	QN (n+1)
0	0	0	1
1	0	1	0
x	1	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
LD5		*LD5D2*		*LD5*	*LD5D2*
D	GN	D	GN		
0.6	0.6	0.6	0.6	4.0	4.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD5	LD5D2
Pulse Width Low (GN)	t_{PWL}	0.79	0.82
Input Setup Time (D to GN)	t_{SU}	0.60	0.66
Input Hold Time (D to GN)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.52	0.47 + 0.028*SL	0.47 + 0.027*SL	0.47 + 0.027*SL
	t_{PHL}	0.74	0.67 + 0.035*SL	0.67 + 0.033*SL	0.67 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
GN to Q	t_{PLH}	0.73	0.68 + 0.028*SL	0.68 + 0.027*SL	0.68 + 0.027*SL
	t_{PHL}	0.87	0.80 + 0.035*SL	0.81 + 0.033*SL	0.81 + 0.033*SL
	t_R	0.20	0.10 + 0.055*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
D to QN	t_{PLH}	0.57	0.51 + 0.030*SL	0.52 + 0.028*SL	0.53 + 0.027*SL
	t_{PHL}	0.47	0.39 + 0.040*SL	0.40 + 0.034*SL	0.42 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
GN to QN	t_{PLH}	0.71	0.65 + 0.030*SL	0.65 + 0.028*SL	0.66 + 0.027*SL
	t_{PHL}	0.67	0.60 + 0.040*SL	0.61 + 0.035*SL	0.63 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

LD5D2

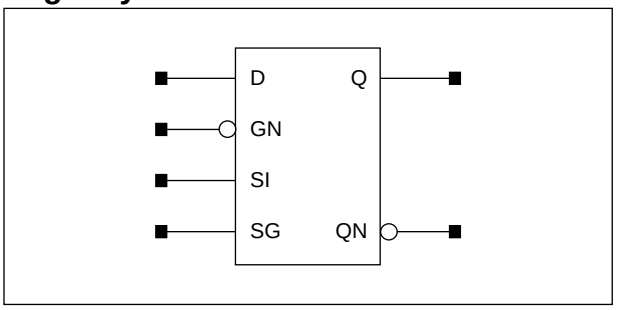
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.59	0.56 + 0.013*SL	0.56 + 0.013*SL	0.57 + 0.013*SL
	t_{PHL}	0.80	0.77 + 0.019*SL	0.77 + 0.017*SL	0.78 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
GN to Q	t_{PLH}	0.80	0.77 + 0.014*SL	0.77 + 0.013*SL	0.77 + 0.013*SL
	t_{PHL}	0.94	0.90 + 0.019*SL	0.91 + 0.017*SL	0.92 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D to QN	t_{PLH}	0.57	0.54 + 0.018*SL	0.55 + 0.015*SL	0.56 + 0.013*SL
	t_{PHL}	0.47	0.42 + 0.024*SL	0.43 + 0.019*SL	0.46 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.031*SL	0.11 + 0.031*SL	0.11 + 0.032*SL
GN to QN	t_{PLH}	0.71	0.67 + 0.018*SL	0.68 + 0.015*SL	0.70 + 0.013*SL
	t_{PHL}	0.67	0.63 + 0.023*SL	0.64 + 0.019*SL	0.66 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.031*SL	0.11 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

LD5S/LD5SD2

D Latch with Active Low, Scan, 1X/2X Drive

Logic Symbol



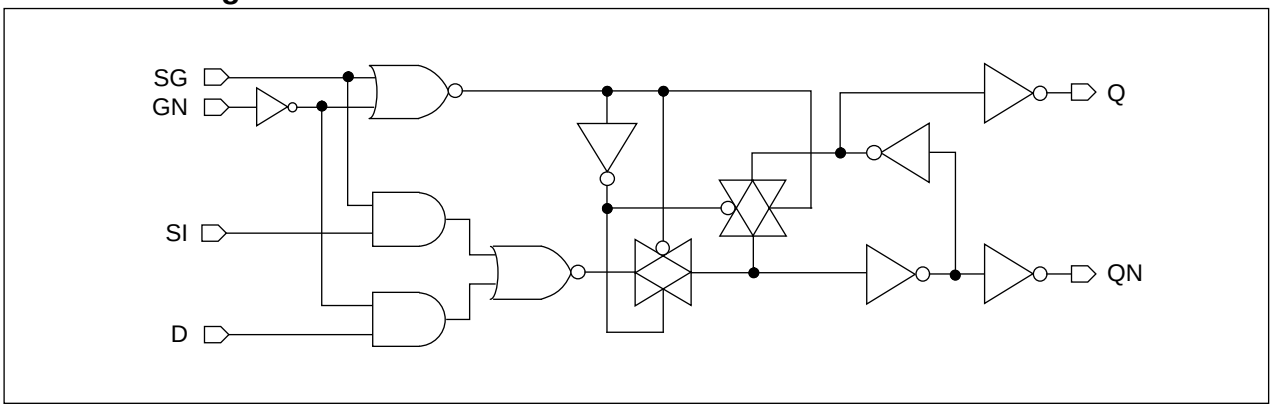
Truth Table

D	GN	SI	SG	Q (n+1)	QN (n+1)
x	1	x	0	Q(n)	QN(n)
x	x	1	1	1	0
x	1	0	1	0	1
1	0	x	x	1	0
0	0	x	0	0	1
0	0	0	1	0	1

Cell Data

Input Load (SL)								Gate Count	
LD5S				*LD5SD2*				*LD5S*	*LD5SD2*
D	GN	SI	SG	D	GN	SI	SG		
0.4	0.6	0.6	1.1	0.4	0.6	0.6	1.1	6.0	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD5S	LD5SD2
Pulse Width Low (GN)	t_{PWL}	0.93	0.96
Pulse Width High (SG)	t_{PWH}	0.79	0.79
Input Setup Time (D to GN)	t_{SU}	0.74	0.66
Input Hold Time (D to GN)	t_{HD}	0.33	0.33
Input Setup Time (SI to SG)	t_{SU}	0.49	0.68
Input Hold Time (SI to SG)	t_{HD}	0.33	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD5S

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.65	0.59 + 0.027*SL	0.60 + 0.027*SL	0.60 + 0.027*SL
	t_{PHL}	0.90	0.83 + 0.035*SL	0.83 + 0.033*SL	0.83 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
SI to Q	t_{PLH}	0.70	0.65 + 0.028*SL	0.65 + 0.027*SL	0.65 + 0.027*SL
	t_{PHL}	0.95	0.88 + 0.035*SL	0.88 + 0.033*SL	0.89 + 0.033*SL
	t_R	0.20	0.09 + 0.055*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
GN to Q	t_{PLH}	1.01	0.95 + 0.028*SL	0.95 + 0.027*SL	0.95 + 0.027*SL
	t_{PHL}	1.03	0.96 + 0.035*SL	0.97 + 0.033*SL	0.97 + 0.033*SL
	t_R	0.20	0.10 + 0.054*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
SG to Q	t_{PLH}	0.78	0.73 + 0.027*SL	0.73 + 0.027*SL	0.73 + 0.027*SL
	t_{PHL}	0.79	0.72 + 0.035*SL	0.73 + 0.033*SL	0.73 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
D to QN	t_{PLH}	0.73	0.67 + 0.032*SL	0.68 + 0.028*SL	0.69 + 0.027*SL
	t_{PHL}	0.59	0.51 + 0.040*SL	0.53 + 0.034*SL	0.54 + 0.033*SL
	t_R	0.24	0.13 + 0.054*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
SI to QN	t_{PLH}	0.78	0.72 + 0.031*SL	0.73 + 0.028*SL	0.74 + 0.027*SL
	t_{PHL}	0.65	0.57 + 0.040*SL	0.58 + 0.035*SL	0.60 + 0.033*SL
	t_R	0.24	0.13 + 0.053*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
GN to QN	t_{PLH}	0.87	0.81 + 0.031*SL	0.82 + 0.028*SL	0.83 + 0.027*SL
	t_{PHL}	0.95	0.87 + 0.040*SL	0.89 + 0.035*SL	0.90 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
SG to QN	t_{PLH}	0.63	0.57 + 0.030*SL	0.57 + 0.028*SL	0.58 + 0.027*SL
	t_{PHL}	0.73	0.65 + 0.039*SL	0.66 + 0.035*SL	0.68 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.12 + 0.063*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

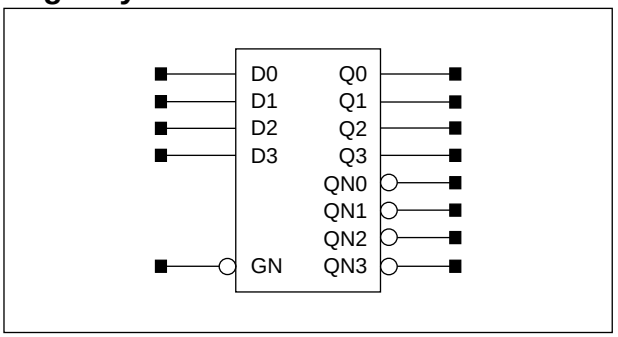
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD5SD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.72	0.69 + 0.014*SL	0.69 + 0.013*SL	0.69 + 0.013*SL
	t_{PHL}	0.97	0.94 + 0.018*SL	0.94 + 0.017*SL	0.95 + 0.016*SL
	t_R	0.16	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
SI to Q	t_{PLH}	0.77	0.75 + 0.014*SL	0.75 + 0.013*SL	0.75 + 0.013*SL
	t_{PHL}	1.03	0.99 + 0.018*SL	1.00 + 0.017*SL	1.00 + 0.016*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.11 + 0.032*SL	0.11 + 0.030*SL	0.09 + 0.032*SL
GN to Q	t_{PLH}	1.08	1.05 + 0.013*SL	1.05 + 0.013*SL	1.05 + 0.013*SL
	t_{PHL}	1.11	1.07 + 0.018*SL	1.07 + 0.017*SL	1.08 + 0.016*SL
	t_R	0.16	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
SG to Q	t_{PLH}	0.85	0.83 + 0.013*SL	0.83 + 0.013*SL	0.83 + 0.013*SL
	t_{PHL}	0.86	0.83 + 0.018*SL	0.83 + 0.017*SL	0.84 + 0.016*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D to QN	t_{PLH}	0.74	0.70 + 0.019*SL	0.71 + 0.015*SL	0.73 + 0.013*SL
	t_{PHL}	0.59	0.55 + 0.023*SL	0.56 + 0.019*SL	0.58 + 0.017*SL
	t_R	0.18	0.13 + 0.025*SL	0.13 + 0.026*SL	0.11 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SI to QN	t_{PLH}	0.79	0.75 + 0.019*SL	0.76 + 0.015*SL	0.78 + 0.013*SL
	t_{PHL}	0.65	0.60 + 0.023*SL	0.61 + 0.019*SL	0.64 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.025*SL	0.11 + 0.028*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
GN to QN	t_{PLH}	0.87	0.84 + 0.018*SL	0.85 + 0.015*SL	0.86 + 0.013*SL
	t_{PHL}	0.95	0.90 + 0.024*SL	0.92 + 0.019*SL	0.94 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.12 + 0.026*SL	0.10 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SG to QN	t_{PLH}	0.63	0.59 + 0.019*SL	0.61 + 0.015*SL	0.62 + 0.013*SL
	t_{PHL}	0.73	0.68 + 0.024*SL	0.69 + 0.019*SL	0.72 + 0.017*SL
	t_R	0.17	0.12 + 0.026*SL	0.12 + 0.026*SL	0.10 + 0.029*SL
	t_F	0.18	0.13 + 0.029*SL	0.12 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

Dn	GN	Qn (n+1)	QNn (n+1)
0	0	0	1
1	0	1	0
x	1	Q (n)	QN (n)

Cell Data

Input Load (SL)				Gate Count	
LD5X4		*LD5X4D2*		*LD5X4*	*LD5X4D2*
Dn	GN	Dn	GN		
0.6	0.6	0.6	0.6	13.0	15.3

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD5X4	LD5X4D2
Pulse Width Low (GN)	t_{PWL}	0.96	0.98
Input Setup Time (D0 to GN)	t_{SU}	0.46	0.49
Input Hold Time (D0 to GN)	t_{HD}	0.33	0.33
Input Setup Time (D1 to GN)	t_{SU}	0.46	0.46
Input Hold Time (D1 to GN)	t_{HD}	0.33	0.33
Input Setup Time (D2 to GN)	t_{SU}	0.46	0.46
Input Hold Time (D2 to GN)	t_{HD}	0.33	0.33
Input Setup Time (D3 to GN)	t_{SU}	0.74	0.49
Input Hold Time (D3 to GN)	t_{HD}	0.33	0.36

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD5X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.52	0.47 + 0.028*SL	0.47 + 0.027*SL	0.47 + 0.027*SL
	t_{PHL}	0.74	0.66 + 0.036*SL	0.67 + 0.033*SL	0.68 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
GN to Q0	t_{PLH}	0.90	0.84 + 0.028*SL	0.85 + 0.027*SL	0.85 + 0.027*SL
	t_{PHL}	1.16	1.08 + 0.036*SL	1.09 + 0.033*SL	1.09 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
D1 to Q1	t_{PLH}	0.53	0.47 + 0.028*SL	0.47 + 0.027*SL	0.47 + 0.027*SL
	t_{PHL}	0.74	0.67 + 0.035*SL	0.67 + 0.033*SL	0.68 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.08 + 0.066*SL
GN to Q1	t_{PLH}	0.90	0.85 + 0.028*SL	0.85 + 0.027*SL	0.85 + 0.027*SL
	t_{PHL}	1.16	1.09 + 0.036*SL	1.10 + 0.033*SL	1.10 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.064*SL	0.10 + 0.063*SL	0.08 + 0.066*SL
D2 to Q2	t_{PLH}	0.53	0.47 + 0.028*SL	0.47 + 0.027*SL	0.47 + 0.027*SL
	t_{PHL}	0.74	0.67 + 0.036*SL	0.67 + 0.033*SL	0.68 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.08 + 0.066*SL
GN to Q2	t_{PLH}	0.90	0.85 + 0.027*SL	0.85 + 0.027*SL	0.85 + 0.027*SL
	t_{PHL}	1.16	1.09 + 0.035*SL	1.09 + 0.033*SL	1.10 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.09 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.08 + 0.066*SL
D3 to Q3	t_{PLH}	0.52	0.47 + 0.028*SL	0.47 + 0.027*SL	0.47 + 0.027*SL
	t_{PHL}	0.74	0.66 + 0.036*SL	0.67 + 0.033*SL	0.68 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
GN to Q3	t_{PLH}	0.90	0.84 + 0.028*SL	0.85 + 0.027*SL	0.85 + 0.027*SL
	t_{PHL}	1.16	1.09 + 0.035*SL	1.09 + 0.033*SL	1.10 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
D0 to QN0	t_{PLH}	0.57	0.51 + 0.031*SL	0.52 + 0.028*SL	0.53 + 0.027*SL
	t_{PHL}	0.47	0.39 + 0.040*SL	0.40 + 0.034*SL	0.42 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
GN to QN0	t_{PLH}	0.99	0.93 + 0.031*SL	0.94 + 0.028*SL	0.95 + 0.027*SL
	t_{PHL}	0.84	0.76 + 0.039*SL	0.78 + 0.034*SL	0.79 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD5X4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.57	0.51 + 0.030*SL	0.52 + 0.028*SL	0.53 + 0.027*SL
	t_{PHL}	0.47	0.39 + 0.040*SL	0.40 + 0.034*SL	0.42 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
GN to QN1	t_{PLH}	0.99	0.93 + 0.030*SL	0.94 + 0.028*SL	0.95 + 0.027*SL
	t_{PHL}	0.84	0.76 + 0.040*SL	0.78 + 0.034*SL	0.79 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
D2 to QN2	t_{PLH}	0.57	0.51 + 0.030*SL	0.52 + 0.028*SL	0.53 + 0.027*SL
	t_{PHL}	0.47	0.39 + 0.040*SL	0.40 + 0.034*SL	0.42 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
GN to QN2	t_{PLH}	0.99	0.93 + 0.030*SL	0.94 + 0.028*SL	0.95 + 0.027*SL
	t_{PHL}	0.85	0.77 + 0.039*SL	0.78 + 0.035*SL	0.80 + 0.033*SL
	t_R	0.23	0.12 + 0.054*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
D3 to QN3	t_{PLH}	0.57	0.51 + 0.031*SL	0.52 + 0.028*SL	0.53 + 0.027*SL
	t_{PHL}	0.47	0.39 + 0.040*SL	0.40 + 0.034*SL	0.42 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
GN to QN3	t_{PLH}	0.99	0.93 + 0.030*SL	0.94 + 0.028*SL	0.95 + 0.027*SL
	t_{PHL}	0.84	0.76 + 0.039*SL	0.78 + 0.034*SL	0.79 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD5X4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Q0	t_{PLH}	0.59	0.56 + 0.014*SL	0.56 + 0.013*SL	0.57 + 0.013*SL
	t_{PHL}	0.81	0.77 + 0.019*SL	0.77 + 0.017*SL	0.78 + 0.016*SL
	t_R	0.15	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
GN to Q0	t_{PLH}	0.97	0.94 + 0.014*SL	0.94 + 0.013*SL	0.95 + 0.013*SL
	t_{PHL}	1.23	1.20 + 0.018*SL	1.20 + 0.017*SL	1.21 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D1 to Q1	t_{PLH}	0.59	0.56 + 0.014*SL	0.57 + 0.013*SL	0.57 + 0.013*SL
	t_{PHL}	0.81	0.77 + 0.019*SL	0.77 + 0.017*SL	0.78 + 0.016*SL
	t_R	0.15	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
GN to Q1	t_{PLH}	0.97	0.95 + 0.014*SL	0.95 + 0.013*SL	0.95 + 0.013*SL
	t_{PHL}	1.24	1.20 + 0.019*SL	1.20 + 0.017*SL	1.21 + 0.016*SL
	t_R	0.16	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D2 to Q2	t_{PLH}	0.59	0.56 + 0.014*SL	0.57 + 0.013*SL	0.57 + 0.013*SL
	t_{PHL}	0.81	0.77 + 0.019*SL	0.77 + 0.017*SL	0.78 + 0.016*SL
	t_R	0.16	0.11 + 0.024*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
GN to Q2	t_{PLH}	0.97	0.95 + 0.014*SL	0.95 + 0.013*SL	0.95 + 0.013*SL
	t_{PHL}	1.23	1.20 + 0.019*SL	1.20 + 0.017*SL	1.21 + 0.016*SL
	t_R	0.16	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D3 to Q3	t_{PLH}	0.59	0.56 + 0.014*SL	0.56 + 0.013*SL	0.57 + 0.013*SL
	t_{PHL}	0.81	0.77 + 0.019*SL	0.77 + 0.017*SL	0.78 + 0.016*SL
	t_R	0.15	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.033*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
GN to Q3	t_{PLH}	0.97	0.94 + 0.014*SL	0.94 + 0.013*SL	0.95 + 0.013*SL
	t_{PHL}	1.23	1.20 + 0.019*SL	1.20 + 0.017*SL	1.21 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.032*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D0 to QN0	t_{PLH}	0.57	0.54 + 0.018*SL	0.55 + 0.015*SL	0.56 + 0.013*SL
	t_{PHL}	0.46	0.42 + 0.024*SL	0.43 + 0.019*SL	0.46 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
GN to QN0	t_{PLH}	1.00	0.97 + 0.018*SL	0.98 + 0.015*SL	0.99 + 0.013*SL
	t_{PHL}	0.85	0.80 + 0.023*SL	0.81 + 0.019*SL	0.84 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD5X4D2

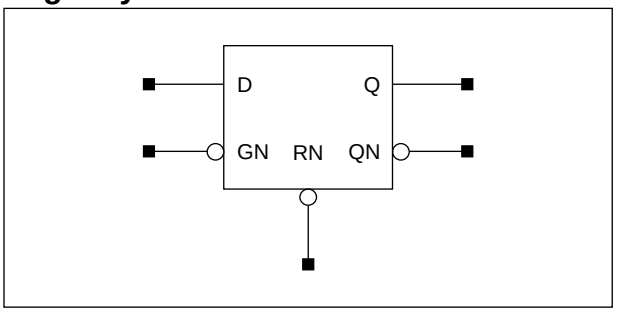
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D1 to QN1	t_{PLH}	0.57	0.54 + 0.018*SL	0.55 + 0.015*SL	0.56 + 0.013*SL
	t_{PHL}	0.46	0.42 + 0.024*SL	0.43 + 0.019*SL	0.46 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
GN to QN1	t_{PLH}	1.00	0.97 + 0.018*SL	0.98 + 0.015*SL	0.99 + 0.013*SL
	t_{PHL}	0.85	0.80 + 0.023*SL	0.81 + 0.019*SL	0.84 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.11 + 0.032*SL
D2 to QN2	t_{PLH}	0.57	0.54 + 0.018*SL	0.55 + 0.015*SL	0.56 + 0.013*SL
	t_{PHL}	0.46	0.42 + 0.024*SL	0.43 + 0.019*SL	0.46 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
GN to QN2	t_{PLH}	1.00	0.97 + 0.018*SL	0.97 + 0.015*SL	0.99 + 0.013*SL
	t_{PHL}	0.85	0.80 + 0.024*SL	0.81 + 0.019*SL	0.84 + 0.017*SL
	t_R	0.17	0.12 + 0.026*SL	0.11 + 0.027*SL	0.10 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.11 + 0.031*SL	0.11 + 0.032*SL
D3 to QN3	t_{PLH}	0.57	0.54 + 0.018*SL	0.55 + 0.015*SL	0.56 + 0.013*SL
	t_{PHL}	0.46	0.42 + 0.024*SL	0.43 + 0.019*SL	0.46 + 0.017*SL
	t_R	0.17	0.12 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
GN to QN3	t_{PLH}	1.00	0.97 + 0.018*SL	0.98 + 0.015*SL	0.99 + 0.013*SL
	t_{PHL}	0.85	0.80 + 0.023*SL	0.81 + 0.019*SL	0.84 + 0.017*SL
	t_R	0.17	0.12 + 0.025*SL	0.11 + 0.027*SL	0.10 + 0.029*SL
	t_F	0.18	0.11 + 0.033*SL	0.12 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

LD6/LD6D2

D Latch with Active Low, Reset, 1X/2X Drive

Logic Symbol



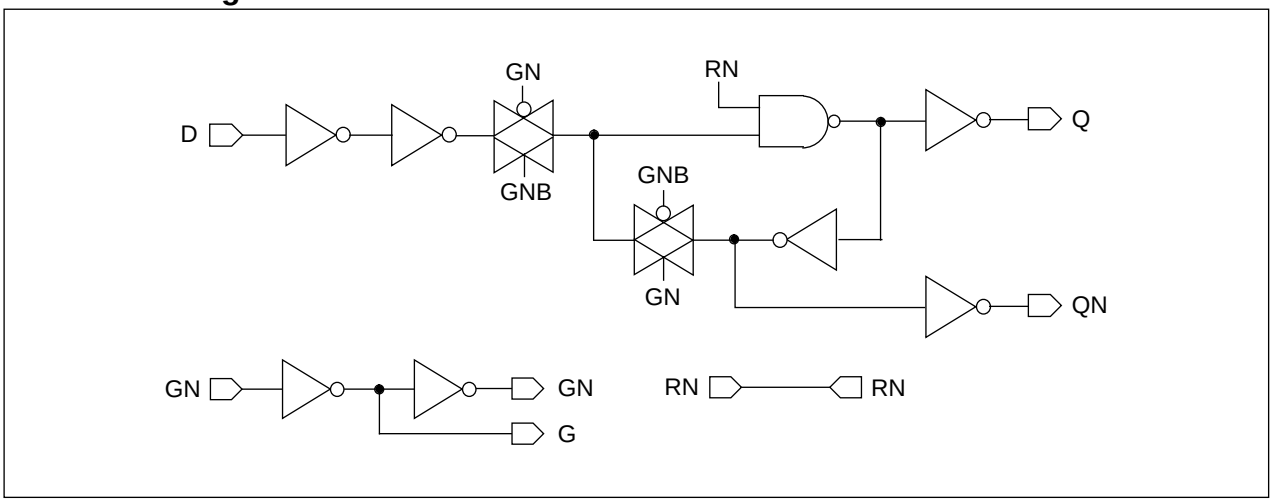
Truth Table

D	GN	RN	Q (n+1)	QN (n+1)
0	0	1	0	1
1	0	1	1	0
x	1	1	Q (n)	QN (n)
x	x	0	0	1

Cell Data

Input Load (SL)						Gate Count	
LD6			*LD6D2*			*LD6*	*LD6D2*
D	GN	RN	D	GN	RN		
0.6	0.6	0.5	0.6	0.6	0.5	4.7	5.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD6	LD6D2
Pulse Width Low (GN)	t_{PWL}	0.79	0.82
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Input Setup Time (D to GN)	t_{SU}	0.68	0.71
Input Hold Time (D to GN)	t_{HD}	0.38	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to GN)	t_{HD}	0.38	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD6

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.62	0.55 + 0.035*SL	0.57 + 0.030*SL	0.59 + 0.027*SL
	t_{PHL}	0.68	0.60 + 0.040*SL	0.61 + 0.035*SL	0.63 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
GN to Q	t_{PLH}	0.77	0.70 + 0.035*SL	0.71 + 0.030*SL	0.74 + 0.027*SL
	t_{PHL}	0.70	0.62 + 0.040*SL	0.64 + 0.035*SL	0.65 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
RN to Q	t_{PLH}	0.33	0.26 + 0.034*SL	0.28 + 0.029*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.30 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.24	0.13 + 0.058*SL	0.13 + 0.058*SL	0.11 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
D to QN	t_{PLH}	0.74	0.68 + 0.027*SL	0.68 + 0.027*SL	0.68 + 0.027*SL
	t_{PHL}	0.80	0.73 + 0.035*SL	0.73 + 0.033*SL	0.74 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
GN to QN	t_{PLH}	0.76	0.70 + 0.028*SL	0.71 + 0.027*SL	0.71 + 0.027*SL
	t_{PHL}	0.94	0.87 + 0.035*SL	0.87 + 0.033*SL	0.88 + 0.033*SL
	t_R	0.20	0.09 + 0.055*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
RN to QN	t_{PLH}	0.49	0.42 + 0.032*SL	0.44 + 0.028*SL	0.45 + 0.027*SL
	t_{PHL}	0.50	0.43 + 0.035*SL	0.44 + 0.033*SL	0.44 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.063*SL	0.07 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

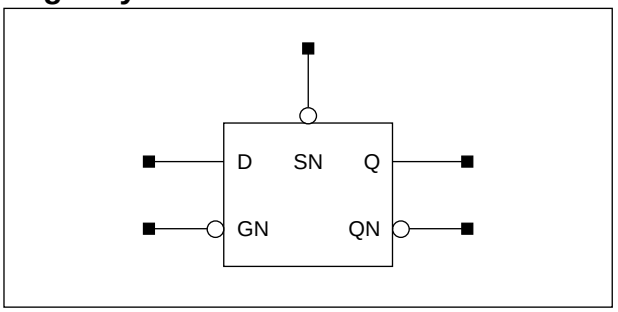
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD6D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.63	0.59 + 0.021*SL	0.60 + 0.016*SL	0.63 + 0.013*SL
	t_{PHL}	0.68	0.63 + 0.024*SL	0.64 + 0.019*SL	0.67 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
GN to Q	t_{PLH}	0.77	0.73 + 0.021*SL	0.75 + 0.017*SL	0.77 + 0.013*SL
	t_{PHL}	0.70	0.65 + 0.024*SL	0.66 + 0.020*SL	0.69 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
RN to Q	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.34 + 0.013*SL
	t_{PHL}	0.36	0.32 + 0.024*SL	0.33 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.028*SL	0.13 + 0.028*SL
	t_F	0.18	0.11 + 0.033*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
D to QN	t_{PLH}	0.80	0.77 + 0.014*SL	0.78 + 0.013*SL	0.78 + 0.013*SL
	t_{PHL}	0.89	0.86 + 0.017*SL	0.86 + 0.016*SL	0.86 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
GN to QN	t_{PLH}	0.83	0.80 + 0.014*SL	0.80 + 0.013*SL	0.80 + 0.013*SL
	t_{PHL}	1.04	1.00 + 0.017*SL	1.00 + 0.016*SL	1.00 + 0.016*SL
	t_R	0.15	0.11 + 0.024*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
RN to QN	t_{PLH}	0.55	0.52 + 0.016*SL	0.52 + 0.014*SL	0.54 + 0.013*SL
	t_{PHL}	0.59	0.56 + 0.018*SL	0.56 + 0.016*SL	0.56 + 0.016*SL
	t_R	0.18	0.13 + 0.026*SL	0.13 + 0.027*SL	0.11 + 0.028*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.030*SL	0.10 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



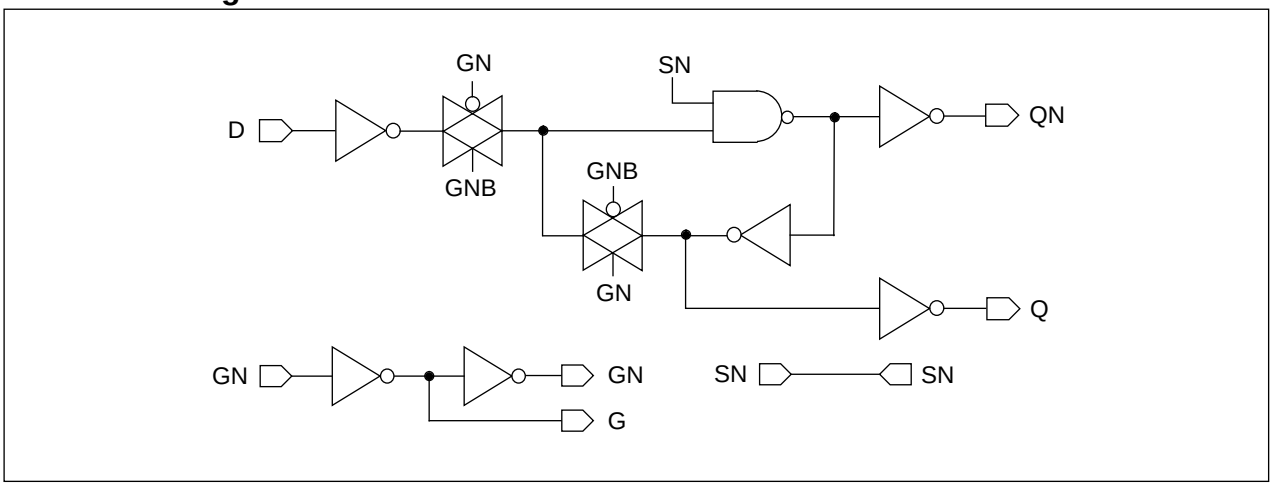
Truth Table

D	GN	SN	Q (n+1)	QN (n+1)
0	0	1	0	1
1	0	1	1	0
x	1	1	Q (n)	QN (n)
x	x	0	1	0

Cell Data

Input Load (SL)						Gate Count	
LD7			*LD7D2*			*LD7*	*LD7D2*
D	GN	SN	D	GN	SN		
0.6	0.6	0.8	0.6	0.6	0.8	4.3	5.0

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD7	LD7D2
Pulse Width Low (GN)	t_{PWL}	0.79	0.85
Pulse Width Low (SN)	t_{PWL}	0.79	0.79
Input Setup Time (D to GN)	t_{SU}	0.63	0.68
Input Hold Time (D to GN)	t_{HD}	0.33	0.33
Recovery Time (SN)	t_{RC}	0.33	0.36
Input Hold Time (SN to GN)	t_{HD}	0.38	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD7

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.55	0.49 + 0.028*SL	0.50 + 0.027*SL	0.50 + 0.027*SL
	t_{PHL}	0.80	0.73 + 0.035*SL	0.73 + 0.033*SL	0.74 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
GN to Q	t_{PLH}	0.76	0.70 + 0.028*SL	0.70 + 0.027*SL	0.70 + 0.027*SL
	t_{PHL}	0.94	0.87 + 0.035*SL	0.87 + 0.033*SL	0.87 + 0.033*SL
	t_R	0.21	0.09 + 0.056*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
SN to Q	t_{PLH}	0.49	0.42 + 0.032*SL	0.44 + 0.028*SL	0.45 + 0.027*SL
	t_{PHL}	0.50	0.43 + 0.035*SL	0.44 + 0.033*SL	0.44 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
D to QN	t_{PLH}	0.63	0.56 + 0.035*SL	0.57 + 0.030*SL	0.60 + 0.027*SL
	t_{PHL}	0.49	0.41 + 0.040*SL	0.43 + 0.035*SL	0.44 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
GN to QN	t_{PLH}	0.76	0.69 + 0.035*SL	0.71 + 0.029*SL	0.73 + 0.027*SL
	t_{PHL}	0.70	0.62 + 0.040*SL	0.63 + 0.035*SL	0.65 + 0.033*SL
	t_R	0.25	0.14 + 0.057*SL	0.14 + 0.057*SL	0.12 + 0.059*SL
	t_F	0.24	0.12 + 0.062*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
SN to QN	t_{PLH}	0.33	0.26 + 0.034*SL	0.28 + 0.029*SL	0.30 + 0.027*SL
	t_{PHL}	0.37	0.29 + 0.039*SL	0.30 + 0.034*SL	0.31 + 0.033*SL
	t_R	0.24	0.13 + 0.058*SL	0.13 + 0.058*SL	0.11 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD7D2

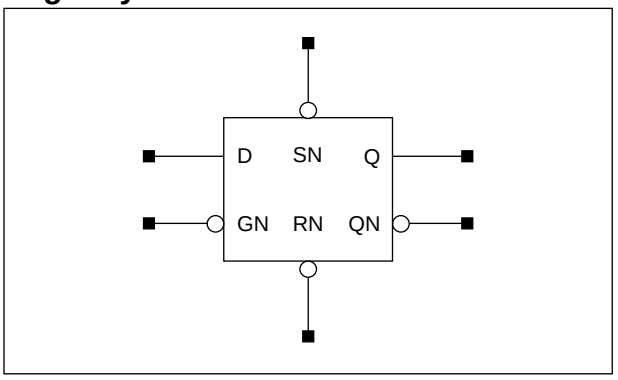
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.62	0.59 + 0.014*SL	0.59 + 0.013*SL	0.59 + 0.013*SL
	t_{PHL}	0.90	0.86 + 0.018*SL	0.86 + 0.016*SL	0.86 + 0.016*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
GN to Q	t_{PLH}	0.82	0.79 + 0.014*SL	0.80 + 0.013*SL	0.80 + 0.013*SL
	t_{PHL}	1.03	1.00 + 0.017*SL	1.00 + 0.016*SL	1.00 + 0.016*SL
	t_R	0.16	0.10 + 0.026*SL	0.10 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.18	0.11 + 0.033*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
SN to Q	t_{PLH}	0.55	0.52 + 0.016*SL	0.52 + 0.014*SL	0.54 + 0.013*SL
	t_{PHL}	0.59	0.56 + 0.018*SL	0.56 + 0.016*SL	0.56 + 0.016*SL
	t_R	0.18	0.13 + 0.026*SL	0.13 + 0.027*SL	0.11 + 0.028*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.030*SL	0.10 + 0.032*SL
D to QN	t_{PLH}	0.63	0.59 + 0.022*SL	0.61 + 0.016*SL	0.63 + 0.013*SL
	t_{PHL}	0.49	0.44 + 0.024*SL	0.45 + 0.020*SL	0.48 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.19	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
GN to QN	t_{PLH}	0.77	0.73 + 0.022*SL	0.74 + 0.017*SL	0.77 + 0.013*SL
	t_{PHL}	0.70	0.65 + 0.024*SL	0.66 + 0.020*SL	0.69 + 0.017*SL
	t_R	0.20	0.15 + 0.024*SL	0.14 + 0.028*SL	0.14 + 0.028*SL
	t_F	0.18	0.12 + 0.031*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SN to QN	t_{PLH}	0.34	0.30 + 0.020*SL	0.31 + 0.016*SL	0.34 + 0.013*SL
	t_{PHL}	0.36	0.32 + 0.024*SL	0.33 + 0.019*SL	0.35 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.028*SL	0.13 + 0.028*SL
	t_F	0.18	0.11 + 0.033*SL	0.12 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

LD8/LD8D2

D Latch with Active Low, Reset, Set, 1X/2X Drive

Logic Symbol



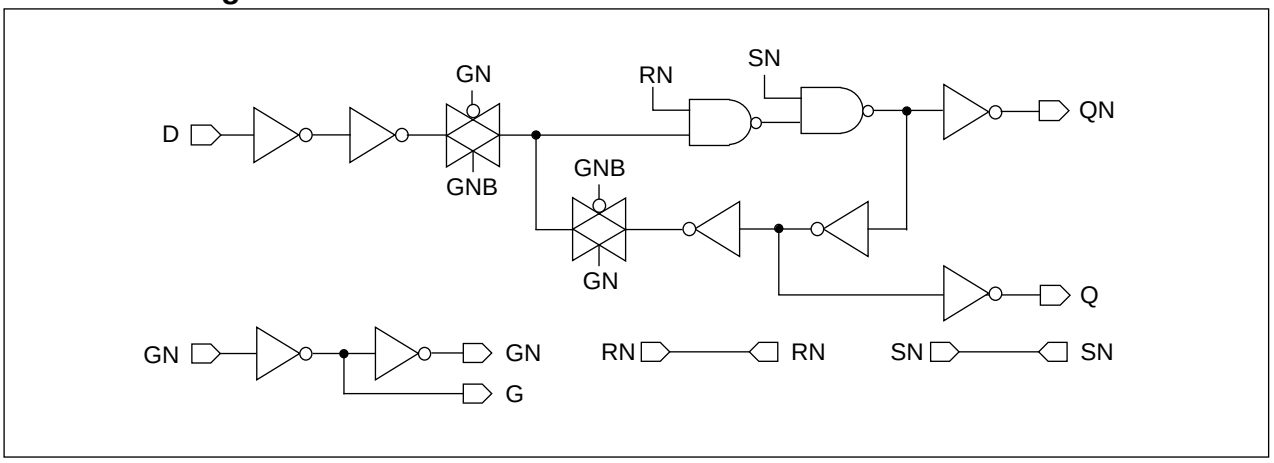
Truth Table

D	GN	RN	SN	Q (n+1)	QN (n+1)
0	0	1	1	0	1
1	0	1	1	1	0
x	1	1	1	Q (n)	QN (n)
x	x	1	0	1	0
x	x	0	1	0	1
x	x	0	0	1	0

Cell Data

Input Load (SL)								Gate Count	
LD8				*LD8D2*				*LD8*	*LD8D2*
D	GN	RN	SN	D	GN	RN	SN		
0.6	0.6	0.4	0.8	0.6	0.6	0.4	0.8	6.0	6.7

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)	
		LD8	LD8D2
Pulse Width Low (GN)	t_{PWL}	0.85	0.93
Pulse Width Low (RN)	t_{PWL}	0.79	0.79
Pulse Width Low (SN)	t_{PWL}	0.79	0.87
Input Setup Time (D to GN)	t_{SU}	0.82	0.90
Input Hold Time (D to GN)	t_{HD}	0.33	0.33
Recovery Time (RN)	t_{RC}	0.33	0.33
Input Hold Time (RN to GN)	t_{HD}	0.33	0.33
Recovery Time (SN)	t_{RC}	0.36	0.33
Input Hold Time (SN to GN)	t_{HD}	0.38	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.81	0.75 + 0.029*SL	0.75 + 0.027*SL	0.76 + 0.027*SL
	t_{PHL}	1.05	0.97 + 0.037*SL	0.98 + 0.034*SL	0.99 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.12 + 0.060*SL	0.11 + 0.062*SL	0.08 + 0.065*SL
GN to Q	t_{PLH}	0.95	0.89 + 0.030*SL	0.90 + 0.027*SL	0.90 + 0.027*SL
	t_{PHL}	1.07	0.99 + 0.037*SL	1.00 + 0.034*SL	1.01 + 0.033*SL
	t_R	0.21	0.10 + 0.056*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.12 + 0.060*SL	0.11 + 0.062*SL	0.08 + 0.065*SL
SN to Q	t_{PLH}	0.47	0.41 + 0.029*SL	0.41 + 0.027*SL	0.42 + 0.027*SL
	t_{PHL}	0.52	0.45 + 0.037*SL	0.46 + 0.034*SL	0.46 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.24	0.11 + 0.061*SL	0.11 + 0.062*SL	0.08 + 0.065*SL
RN to Q	t_{PLH}	0.53	0.47 + 0.029*SL	0.47 + 0.027*SL	0.48 + 0.027*SL
	t_{PHL}	0.73	0.66 + 0.037*SL	0.67 + 0.034*SL	0.68 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
D to QN	t_{PLH}	0.84	0.77 + 0.034*SL	0.78 + 0.029*SL	0.80 + 0.027*SL
	t_{PHL}	0.72	0.64 + 0.039*SL	0.65 + 0.035*SL	0.67 + 0.033*SL
	t_R	0.24	0.13 + 0.057*SL	0.13 + 0.058*SL	0.11 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
GN to QN	t_{PLH}	0.85	0.79 + 0.034*SL	0.80 + 0.029*SL	0.82 + 0.027*SL
	t_{PHL}	0.86	0.78 + 0.039*SL	0.80 + 0.035*SL	0.81 + 0.033*SL
	t_R	0.24	0.13 + 0.057*SL	0.13 + 0.058*SL	0.11 + 0.060*SL
	t_F	0.24	0.11 + 0.065*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
SN to QN	t_{PLH}	0.31	0.24 + 0.034*SL	0.26 + 0.029*SL	0.28 + 0.027*SL
	t_{PHL}	0.38	0.30 + 0.039*SL	0.31 + 0.035*SL	0.33 + 0.033*SL
	t_R	0.24	0.13 + 0.057*SL	0.13 + 0.058*SL	0.11 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.11 + 0.064*SL	0.10 + 0.065*SL
RN to QN	t_{PLH}	0.52	0.46 + 0.034*SL	0.47 + 0.029*SL	0.49 + 0.027*SL
	t_{PHL}	0.44	0.36 + 0.039*SL	0.38 + 0.034*SL	0.39 + 0.033*SL
	t_R	0.24	0.13 + 0.057*SL	0.12 + 0.058*SL	0.11 + 0.060*SL
	t_F	0.23	0.11 + 0.065*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

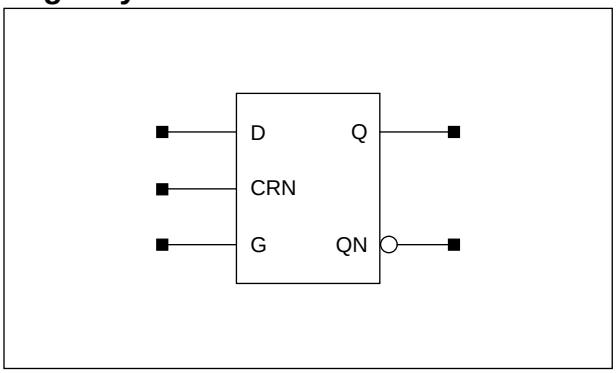
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LD8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.87	0.84 + 0.015*SL	0.84 + 0.014*SL	0.85 + 0.013*SL
	t_{PHL}	1.14	1.10 + 0.019*SL	1.11 + 0.017*SL	1.11 + 0.016*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.19	0.13 + 0.032*SL	0.13 + 0.030*SL	0.12 + 0.032*SL
GN to Q	t_{PLH}	1.01	0.99 + 0.014*SL	0.99 + 0.014*SL	1.00 + 0.013*SL
	t_{PHL}	1.16	1.12 + 0.019*SL	1.13 + 0.017*SL	1.13 + 0.016*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.19	0.13 + 0.032*SL	0.13 + 0.030*SL	0.12 + 0.032*SL
SN to Q	t_{PLH}	0.53	0.50 + 0.015*SL	0.50 + 0.013*SL	0.51 + 0.013*SL
	t_{PHL}	0.61	0.57 + 0.019*SL	0.58 + 0.017*SL	0.59 + 0.016*SL
	t_R	0.16	0.11 + 0.025*SL	0.11 + 0.026*SL	0.08 + 0.029*SL
	t_F	0.19	0.13 + 0.032*SL	0.13 + 0.030*SL	0.12 + 0.032*SL
RN to Q	t_{PLH}	0.59	0.56 + 0.015*SL	0.57 + 0.014*SL	0.57 + 0.013*SL
	t_{PHL}	0.82	0.79 + 0.019*SL	0.79 + 0.017*SL	0.80 + 0.016*SL
	t_R	0.16	0.11 + 0.026*SL	0.11 + 0.027*SL	0.09 + 0.029*SL
	t_F	0.19	0.12 + 0.033*SL	0.13 + 0.031*SL	0.12 + 0.032*SL
D to QN	t_{PLH}	0.85	0.80 + 0.021*SL	0.82 + 0.016*SL	0.84 + 0.013*SL
	t_{PHL}	0.72	0.67 + 0.024*SL	0.68 + 0.019*SL	0.71 + 0.017*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.18	0.11 + 0.034*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
GN to QN	t_{PLH}	0.87	0.82 + 0.021*SL	0.84 + 0.016*SL	0.86 + 0.013*SL
	t_{PHL}	0.86	0.82 + 0.024*SL	0.83 + 0.019*SL	0.85 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.028*SL	0.13 + 0.028*SL
	t_F	0.18	0.12 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
SN to QN	t_{PLH}	0.32	0.28 + 0.021*SL	0.29 + 0.016*SL	0.32 + 0.013*SL
	t_{PHL}	0.38	0.33 + 0.024*SL	0.34 + 0.019*SL	0.37 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.028*SL	0.13 + 0.028*SL
	t_F	0.18	0.12 + 0.033*SL	0.12 + 0.031*SL	0.11 + 0.032*SL
RN to QN	t_{PLH}	0.53	0.49 + 0.021*SL	0.51 + 0.016*SL	0.53 + 0.013*SL
	t_{PHL}	0.44	0.39 + 0.023*SL	0.41 + 0.019*SL	0.43 + 0.017*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.18	0.11 + 0.032*SL	0.12 + 0.031*SL	0.11 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



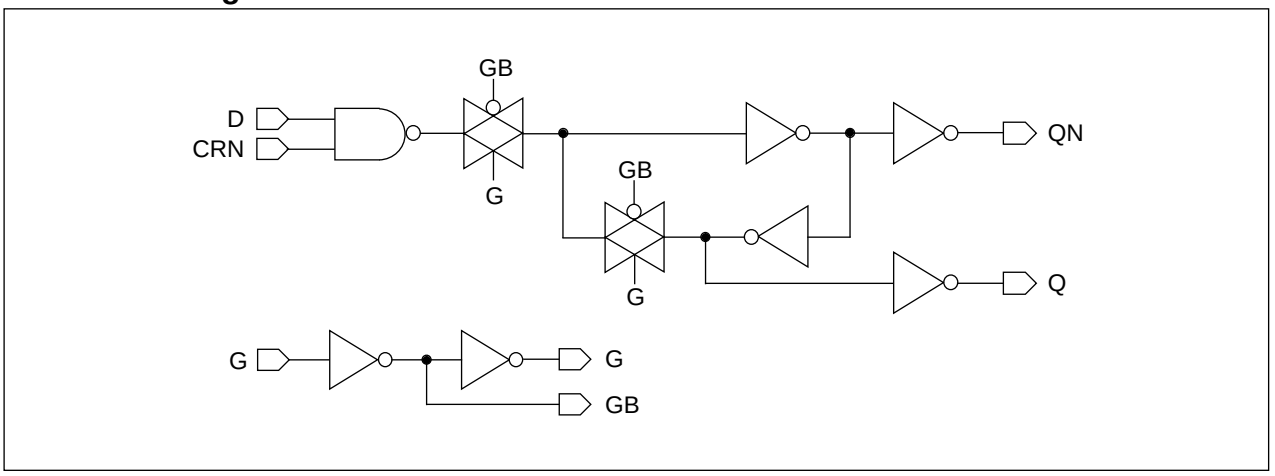
Truth Table

D	CRN	G	Q (n+1)	QN (n+1)
0	1	1	0	1
1	1	1	1	0
x	x	0	Q (n)	QN (n)
x	0	1	0	1

Cell Data

Input Load (SL)			Gate Count
D	CRN	G	
0.6	0.6	0.6	4.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width High (G)	t_{PWH}	0.79
Input Setup Time (D to G)	t_{SU}	0.46
Input Hold Time (D to G)	t_{HD}	0.33
Input Setup Time (CRN to G)	t_{SU}	0.46
Input Hold Time (CRN to G)	t_{HD}	0.33

LDS2

D Latch with Active High, Synchronous Clear

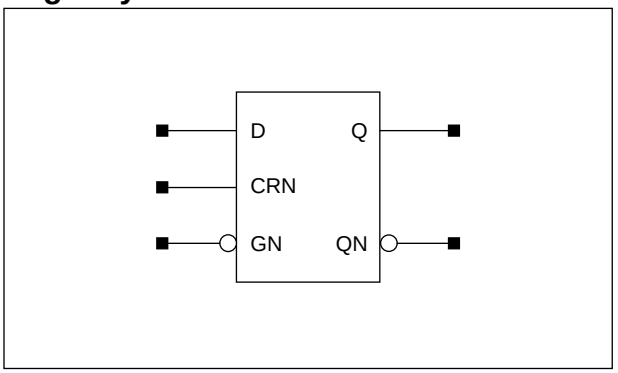
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.61	0.55 + 0.028*SL	0.55 + 0.027*SL	0.55 + 0.027*SL
	t_{PHL}	0.79	0.72 + 0.036*SL	0.72 + 0.033*SL	0.73 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
CRN to Q	t_{PLH}	0.63	0.57 + 0.028*SL	0.57 + 0.027*SL	0.57 + 0.027*SL
	t_{PHL}	0.76	0.69 + 0.035*SL	0.69 + 0.033*SL	0.70 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
G to Q	t_{PLH}	0.72	0.67 + 0.028*SL	0.67 + 0.027*SL	0.67 + 0.027*SL
	t_{PHL}	0.71	0.64 + 0.036*SL	0.64 + 0.033*SL	0.65 + 0.033*SL
	t_R	0.20	0.09 + 0.055*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
D to QN	t_{PLH}	0.62	0.56 + 0.030*SL	0.57 + 0.028*SL	0.58 + 0.027*SL
	t_{PHL}	0.55	0.47 + 0.040*SL	0.49 + 0.034*SL	0.50 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.063*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
CRN to QN	t_{PLH}	0.59	0.53 + 0.030*SL	0.54 + 0.028*SL	0.55 + 0.027*SL
	t_{PHL}	0.57	0.49 + 0.040*SL	0.51 + 0.034*SL	0.52 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
G to QN	t_{PLH}	0.54	0.48 + 0.030*SL	0.49 + 0.028*SL	0.50 + 0.027*SL
	t_{PHL}	0.67	0.59 + 0.040*SL	0.60 + 0.035*SL	0.62 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.12 + 0.063*SL	0.12 + 0.063*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



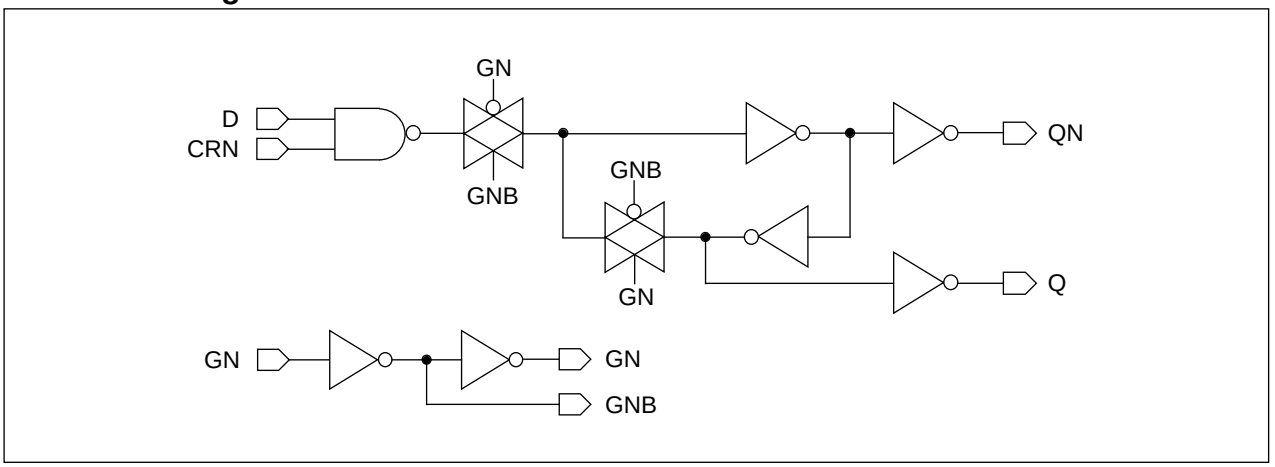
Truth Table

D	CRN	GN	Q (n+1)	QN (n+1)
0	1	0	0	1
1	1	0	1	0
x	x	1	Q (n)	QN (n)
x	0	0	0	1

Cell Data

Input Load (SL)			Gate Count
D	CRN	GN	
0.5	0.6	0.6	4.3

Schematic Diagram



Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Pulse Width Low (GN)	t_{PWL}	0.79
Input Setup Time (D to GN)	t_{SU}	0.60
Input Hold Time (D to GN)	t_{HD}	0.33
Input Setup Time (CRN to GN)	t_{SU}	0.60
Input Hold Time (CRN to GN)	t_{HD}	0.33

LDS6

D Latch with Active Low, Synchronous Clear

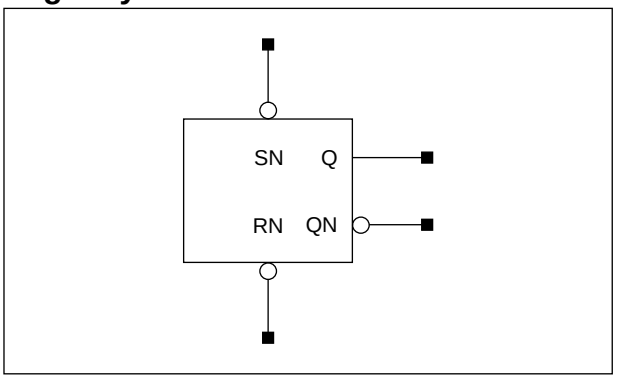
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D to Q	t_{PLH}	0.61	0.55 + 0.028*SL	0.55 + 0.027*SL	0.55 + 0.027*SL
	t_{PHL}	0.79	0.72 + 0.035*SL	0.72 + 0.033*SL	0.73 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
CRN to Q	t_{PLH}	0.63	0.57 + 0.028*SL	0.57 + 0.027*SL	0.57 + 0.027*SL
	t_{PHL}	0.76	0.69 + 0.036*SL	0.69 + 0.033*SL	0.70 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
GN to Q	t_{PLH}	0.77	0.71 + 0.028*SL	0.72 + 0.027*SL	0.72 + 0.027*SL
	t_{PHL}	0.83	0.76 + 0.036*SL	0.77 + 0.033*SL	0.77 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
D to QN	t_{PLH}	0.62	0.56 + 0.030*SL	0.57 + 0.028*SL	0.58 + 0.027*SL
	t_{PHL}	0.55	0.47 + 0.040*SL	0.49 + 0.034*SL	0.50 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
CRN to QN	t_{PLH}	0.59	0.53 + 0.031*SL	0.54 + 0.028*SL	0.55 + 0.027*SL
	t_{PHL}	0.57	0.49 + 0.040*SL	0.51 + 0.034*SL	0.52 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.064*SL	0.12 + 0.063*SL	0.09 + 0.065*SL
GN to QN	t_{PLH}	0.67	0.61 + 0.030*SL	0.62 + 0.028*SL	0.63 + 0.027*SL
	t_{PHL}	0.72	0.64 + 0.040*SL	0.65 + 0.034*SL	0.67 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

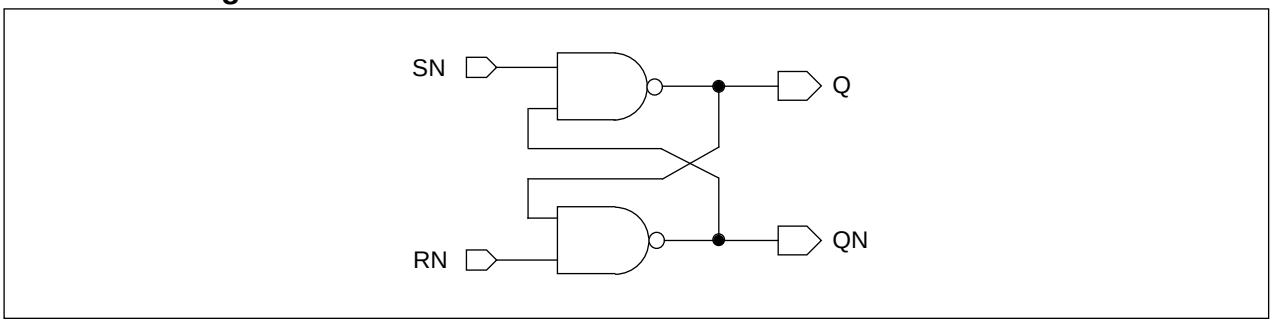
RN	SN	Q (n+1)	QN (n+1)
0	0	*	*
1	0	1	0
0	1	0	1
1	1	Q (n)	QN (n)

* Both Q and QN outputs will remain high during RN and SN are low. However, if RN and SN go high simultaneously, the output states are unpredictable.

Cell Data

Input Load (SL)				Gate Count	
LS0		*LS0D2*		*LS0*	*LS0D2*
RN	SN	RN	SN		
1.1	1.1	2.2	2.2	1.7	3.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LS0

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.20	0.14 + 0.030*SL	0.15 + 0.028*SL	0.15 + 0.028*SL
	t_{PHL}	0.22	0.15 + 0.039*SL	0.15 + 0.037*SL	0.15 + 0.037*SL
	t_R	0.31	0.21 + 0.053*SL	0.19 + 0.058*SL	0.15 + 0.063*SL
	t_F	0.38	0.23 + 0.072*SL	0.22 + 0.077*SL	0.18 + 0.081*SL
RN to Q	t_{PHL}	0.41	0.26 + 0.073*SL	0.27 + 0.070*SL	0.27 + 0.070*SL
	t_F	0.36	0.19 + 0.084*SL	0.19 + 0.085*SL	0.18 + 0.085*SL
SN to QN	t_{PHL}	0.41	0.26 + 0.073*SL	0.27 + 0.071*SL	0.27 + 0.070*SL
	t_F	0.36	0.19 + 0.085*SL	0.19 + 0.085*SL	0.18 + 0.085*SL
RN to QN	t_{PLH}	0.20	0.14 + 0.030*SL	0.15 + 0.028*SL	0.15 + 0.028*SL
	t_{PHL}	0.22	0.15 + 0.039*SL	0.15 + 0.037*SL	0.15 + 0.037*SL
	t_R	0.31	0.21 + 0.054*SL	0.19 + 0.058*SL	0.15 + 0.063*SL
	t_F	0.38	0.23 + 0.072*SL	0.22 + 0.077*SL	0.18 + 0.081*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

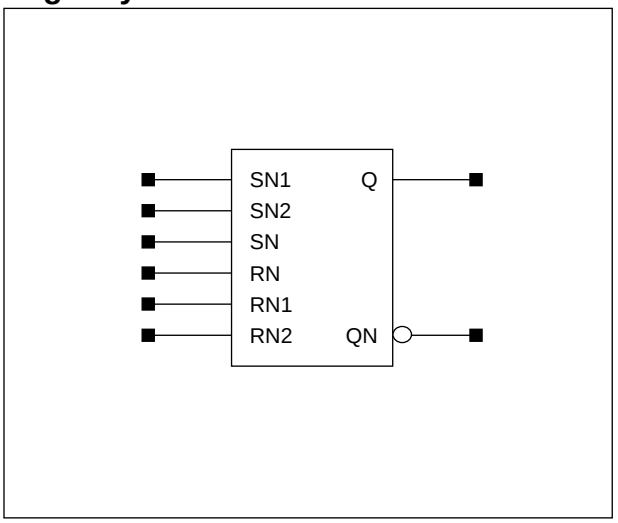
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

LS0D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.17	0.14 + 0.016*SL	0.14 + 0.014*SL	0.15 + 0.014*SL
	t_{PHL}	0.17	0.12 + 0.021*SL	0.13 + 0.019*SL	0.13 + 0.019*SL
	t_R	0.26	0.21 + 0.024*SL	0.20 + 0.026*SL	0.17 + 0.030*SL
	t_F	0.29	0.22 + 0.034*SL	0.21 + 0.037*SL	0.19 + 0.040*SL
RN to Q	t_{PHL}	0.33	0.25 + 0.039*SL	0.26 + 0.037*SL	0.27 + 0.036*SL
	t_F	0.26	0.18 + 0.042*SL	0.17 + 0.043*SL	0.17 + 0.044*SL
SN to QN	t_{PHL}	0.33	0.25 + 0.039*SL	0.26 + 0.037*SL	0.27 + 0.036*SL
	t_F	0.26	0.17 + 0.043*SL	0.17 + 0.043*SL	0.17 + 0.044*SL
RN to QN	t_{PLH}	0.17	0.14 + 0.016*SL	0.14 + 0.014*SL	0.15 + 0.014*SL
	t_{PHL}	0.17	0.12 + 0.021*SL	0.13 + 0.019*SL	0.13 + 0.019*SL
	t_R	0.26	0.21 + 0.024*SL	0.20 + 0.026*SL	0.17 + 0.030*SL
	t_F	0.29	0.22 + 0.035*SL	0.21 + 0.037*SL	0.18 + 0.040*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

RN	SN	RN*	SN*	Q (n+1)	QN (n+1)
0	0	x	x	*	*
x	0	0	x	*	*
x	x	0	0	*	*
0	x	x	0	*	*
1	0	1	x	1	0
0	1	x	1	0	1
1	x	1	0	1	0
x	1	0	1	0	1
1	1	1	1	Q (n)	QN (n)

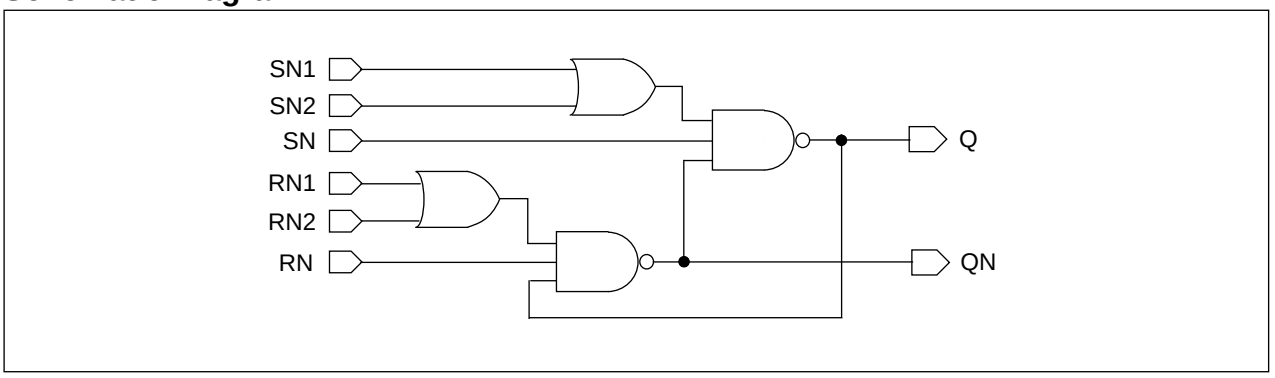
RN* = RN1 + RN2, SN* = SN1 + SN2

* Both Q and QN outputs will be unknown when RN (RN*) and SN (SN*) are low.

Cell Data

Input Load (SL)						Gate Count
RN	RN1	RN2	SN	SN1	SN2	
0.9	0.8	0.8	0.9	0.8	0.8	3.0

Schematic Diagram



LS1

SR Latch with Separate Inputs

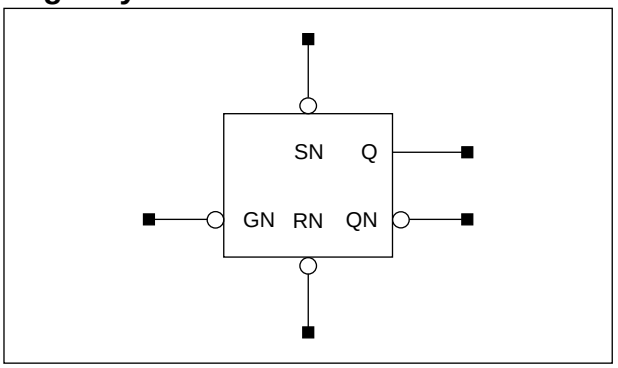
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN1 to Q	t_{PLH}	0.32	0.22 + 0.051*SL	0.22 + 0.051*SL	0.22 + 0.051*SL
	t_{PHL}	0.42	0.27 + 0.074*SL	0.28 + 0.073*SL	0.28 + 0.073*SL
	t_R	0.60	0.38 + 0.109*SL	0.37 + 0.114*SL	0.34 + 0.117*SL
	t_F	0.77	0.46 + 0.157*SL	0.45 + 0.161*SL	0.44 + 0.162*SL
SN2 to Q	t_{PLH}	0.32	0.22 + 0.051*SL	0.22 + 0.051*SL	0.22 + 0.051*SL
	t_{PHL}	0.48	0.33 + 0.074*SL	0.34 + 0.073*SL	0.34 + 0.073*SL
	t_R	0.59	0.37 + 0.112*SL	0.36 + 0.115*SL	0.34 + 0.117*SL
	t_F	0.87	0.56 + 0.156*SL	0.55 + 0.161*SL	0.54 + 0.162*SL
SN to Q	t_{PLH}	0.22	0.17 + 0.028*SL	0.17 + 0.027*SL	0.17 + 0.027*SL
	t_{PHL}	0.42	0.28 + 0.074*SL	0.28 + 0.073*SL	0.28 + 0.073*SL
	t_R	0.36	0.26 + 0.051*SL	0.25 + 0.055*SL	0.20 + 0.060*SL
	t_F	0.78	0.46 + 0.158*SL	0.45 + 0.161*SL	0.44 + 0.162*SL
RN1 to Q	t_{PHL}	0.76	0.50 + 0.130*SL	0.50 + 0.129*SL	0.50 + 0.129*SL
	t_F	0.80	0.47 + 0.167*SL	0.46 + 0.168*SL	0.46 + 0.169*SL
RN2 to Q	t_{PHL}	0.76	0.50 + 0.130*SL	0.50 + 0.129*SL	0.50 + 0.129*SL
	t_F	0.80	0.46 + 0.169*SL	0.46 + 0.168*SL	0.46 + 0.169*SL
RN to Q	t_{PHL}	0.65	0.44 + 0.104*SL	0.45 + 0.102*SL	0.45 + 0.102*SL
	t_F	0.78	0.45 + 0.164*SL	0.45 + 0.164*SL	0.45 + 0.164*SL
SN1 to QN	t_{PHL}	0.76	0.50 + 0.130*SL	0.50 + 0.129*SL	0.50 + 0.129*SL
	t_F	0.80	0.47 + 0.167*SL	0.46 + 0.168*SL	0.46 + 0.169*SL
SN2 to QN	t_{PHL}	0.76	0.50 + 0.131*SL	0.50 + 0.129*SL	0.50 + 0.129*SL
	t_F	0.80	0.46 + 0.168*SL	0.46 + 0.168*SL	0.46 + 0.169*SL
SN to QN	t_{PHL}	0.65	0.44 + 0.104*SL	0.45 + 0.102*SL	0.45 + 0.102*SL
	t_F	0.78	0.45 + 0.164*SL	0.45 + 0.164*SL	0.45 + 0.164*SL
RN1 to QN	t_{PLH}	0.32	0.22 + 0.051*SL	0.22 + 0.051*SL	0.22 + 0.051*SL
	t_{PHL}	0.42	0.27 + 0.074*SL	0.28 + 0.073*SL	0.28 + 0.073*SL
	t_R	0.60	0.38 + 0.110*SL	0.37 + 0.114*SL	0.34 + 0.117*SL
	t_F	0.77	0.46 + 0.158*SL	0.45 + 0.161*SL	0.44 + 0.162*SL
RN2 to QN	t_{PLH}	0.32	0.22 + 0.051*SL	0.22 + 0.051*SL	0.22 + 0.051*SL
	t_{PHL}	0.48	0.33 + 0.074*SL	0.34 + 0.073*SL	0.34 + 0.073*SL
	t_R	0.59	0.37 + 0.112*SL	0.36 + 0.115*SL	0.34 + 0.117*SL
	t_F	0.87	0.56 + 0.156*SL	0.55 + 0.161*SL	0.54 + 0.162*SL
RN to QN	t_{PLH}	0.22	0.17 + 0.028*SL	0.17 + 0.027*SL	0.17 + 0.027*SL
	t_{PHL}	0.42	0.28 + 0.074*SL	0.28 + 0.073*SL	0.28 + 0.073*SL
	t_R	0.36	0.26 + 0.051*SL	0.25 + 0.055*SL	0.20 + 0.060*SL
	t_F	0.78	0.46 + 0.158*SL	0.45 + 0.161*SL	0.44 + 0.162*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

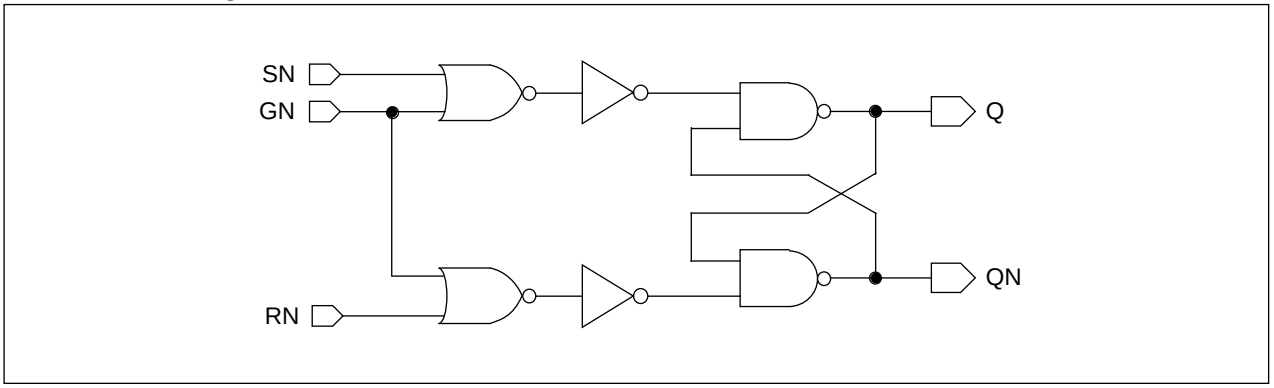
GN	RN	SN	Q (n+1)	QN (n+1)
1	x	x	Q (n)	QN (n)
0	1	1	Q (n)	QN (n)
0	0	1	0	1
0	1	0	1	0
0	0	0	*	*

* Both Q and QN outputs will be unknown when GN, RN, and SN are low.
However, if GN goes high, or RN and SN go high simultaneously, the output states are unpredictable.

Cell Data

Input Load (SL)			Gate Count
GN	RN	SN	
1.4	0.6	0.6	4.3

Schematic Diagram



LS2

SR Latch with Common Inputs

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

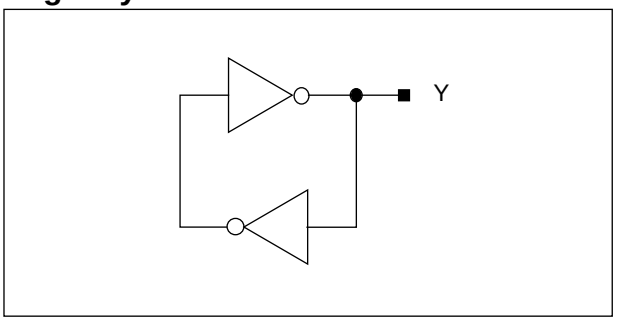
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
SN to Q	t_{PLH}	0.53	0.48 + 0.029*SL	0.48 + 0.028*SL	0.48 + 0.028*SL
	t_{PHL}	0.45	0.37 + 0.040*SL	0.37 + 0.038*SL	0.38 + 0.037*SL
	t_R	0.28	0.16 + 0.059*SL	0.16 + 0.062*SL	0.15 + 0.063*SL
	t_F	0.38	0.22 + 0.078*SL	0.22 + 0.078*SL	0.20 + 0.081*SL
RN to Q	t_{PHL}	0.75	0.61 + 0.072*SL	0.61 + 0.071*SL	0.61 + 0.070*SL
	t_F	0.37	0.20 + 0.086*SL	0.20 + 0.085*SL	0.20 + 0.085*SL
GN to Q	t_{PLH}	0.53	0.47 + 0.029*SL	0.48 + 0.028*SL	0.48 + 0.028*SL
	t_{PHL}	0.75	0.60 + 0.072*SL	0.61 + 0.071*SL	0.61 + 0.070*SL
	t_R	0.29	0.18 + 0.057*SL	0.17 + 0.059*SL	0.16 + 0.060*SL
	t_F	0.37	0.20 + 0.085*SL	0.20 + 0.085*SL	0.19 + 0.085*SL
SN to QN	t_{PHL}	0.75	0.60 + 0.072*SL	0.61 + 0.071*SL	0.61 + 0.070*SL
	t_F	0.37	0.20 + 0.086*SL	0.20 + 0.085*SL	0.20 + 0.085*SL
RN to QN	t_{PLH}	0.54	0.48 + 0.029*SL	0.48 + 0.028*SL	0.48 + 0.028*SL
	t_{PHL}	0.45	0.37 + 0.041*SL	0.37 + 0.038*SL	0.38 + 0.037*SL
	t_R	0.28	0.16 + 0.059*SL	0.16 + 0.062*SL	0.14 + 0.063*SL
	t_F	0.38	0.22 + 0.077*SL	0.22 + 0.079*SL	0.20 + 0.081*SL
GN to QN	t_{PLH}	0.53	0.48 + 0.029*SL	0.48 + 0.028*SL	0.48 + 0.028*SL
	t_{PHL}	0.75	0.60 + 0.072*SL	0.61 + 0.071*SL	0.61 + 0.070*SL
	t_R	0.29	0.18 + 0.057*SL	0.17 + 0.059*SL	0.16 + 0.060*SL
	t_F	0.37	0.20 + 0.086*SL	0.20 + 0.085*SL	0.19 + 0.085*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Cell Name & Function Description

Cell Name	Function Description
BUSHOLDER	Bus Holder

Logic Symbol



Cell Data

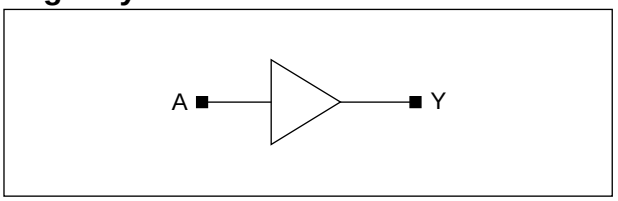
Input Load (SL)	Gate Count
Y	
3.7	1.3

INTERNAL CLOCK DRIVERS

Cell Names & Function Descriptions

Cell Name	Function Description
CK2	Internal Clock Driver CMOS 2mA
CK4	Internal Clock Driver CMOS 4mA
CK6	Internal Clock Driver CMOS 6mA
CK8	Internal Clock Driver CMOS 8mA

Logic Symbol



Truth Table

A	Y
0	0
1	1

Cell Data

Input Load (SL)				Gate Count			
CK2	*CK4*	*CK6*	*CK8*	*CK2*	*CK4*	*CK6*	*CK8*
A	A	A	A				
6.2	6.2	10.8	10.8	1.0	1.0	1.0	1.0

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

CK2

Path	Parameter	Delay [ns] SL = 103	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.51	0.22 + 0.003*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.49	0.19 + 0.003*SL	0.19 + 0.003*SL	0.19 + 0.003*SL
	t_R	0.72	0.09 + 0.006*SL	0.08 + 0.006*SL	0.08 + 0.006*SL
	t_F	0.65	0.08 + 0.006*SL	0.07 + 0.006*SL	0.06 + 0.006*SL

*Group1 : SL < 69, *Group2 : 69 ≤ SL ≤ 103, *Group3 : 103 < SL

CK4

Path	Parameter	Delay [ns] SL = 202	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.57	0.29 + 0.001*SL	0.29 + 0.001*SL	0.29 + 0.001*SL
	t_{PHL}	0.53	0.24 + 0.001*SL	0.24 + 0.001*SL	0.25 + 0.001*SL
	t_R	0.72	0.12 + 0.003*SL	0.10 + 0.003*SL	0.10 + 0.003*SL
	t_F	0.65	0.09 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.003*SL

*Group1 : SL < 135, *Group2 : 135 ≤ SL ≤ 202, *Group3 : 202 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.40ns, SL: Standard Load)

CK6

Path	Parameter	Delay [ns] SL = 307	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.53	0.25 + 0.001*SL	0.25 + 0.001*SL	0.25 + 0.001*SL
	t_{PHL}	0.53	0.23 + 0.001*SL	0.24 + 0.001*SL	0.24 + 0.001*SL
	t_R	0.72	0.10 + 0.002*SL	0.09 + 0.002*SL	0.08 + 0.002*SL
	t_F	0.65	0.09 + 0.002*SL	0.08 + 0.002*SL	0.07 + 0.002*SL

*Group1 : SL < 204, *Group2 : 204 ≦SL≦ 307, *Group3 : 307 < SL

CK8

Path	Parameter	Delay [ns] SL = 405	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.56	0.28 + 0.001*SL	0.28 + 0.001*SL	0.28 + 0.001*SL
	t_{PHL}	0.56	0.26 + 0.001*SL	0.27 + 0.001*SL	0.27 + 0.001*SL
	t_R	0.72	0.11 + 0.001*SL	0.11 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.65	0.10 + 0.001*SL	0.09 + 0.001*SL	0.08 + 0.001*SL

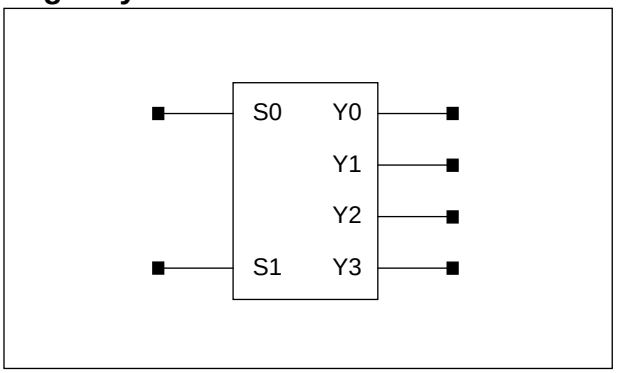
*Group1 : SL < 270, *Group2 : 270 ≦SL≦ 405, *Group3 : 405 < SL

DECODERS

Cell Names & Function Descriptions

Cell Name	Function Description
DC4	2 > 4 Non-Inverting Decoder
DC4I	2 > 4 Inverting Decoder
DC8I	3 > 8 Inverting Decoder

Logic Symbol



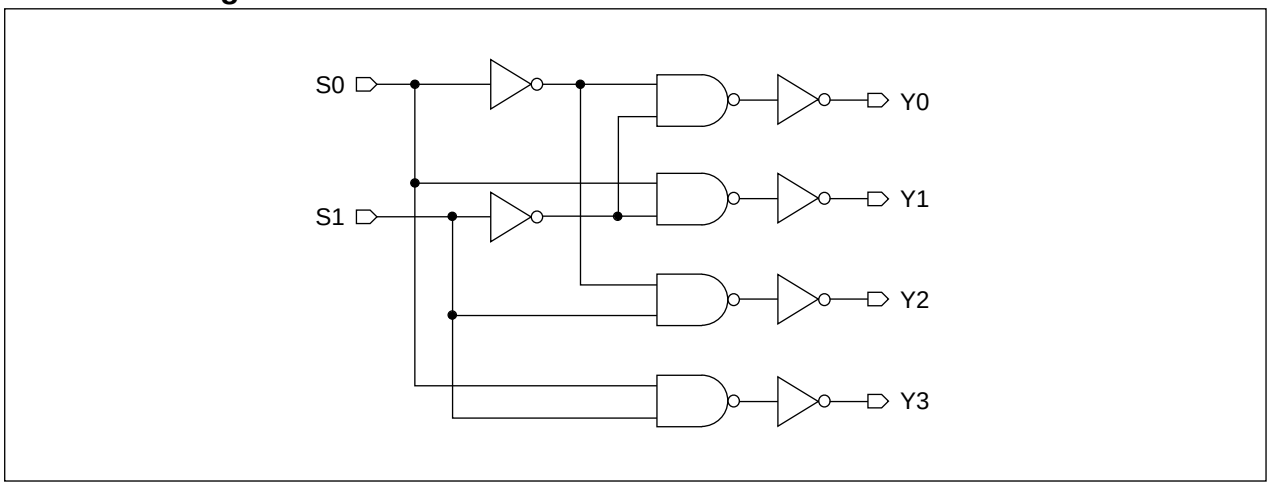
Truth Table

S1	S0	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Cell Data

Input Load (SL)		Gate Count
S0	S1	
1.8	1.9	6.3

Schematic Diagram



DC4

2 > 4 Non-Inverting Decoder

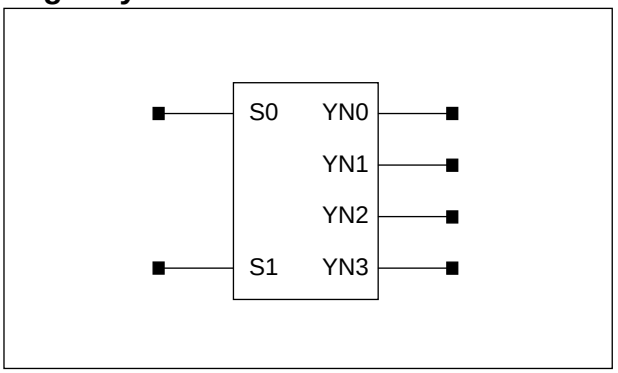
Switching Characteristics

(Typical process, 25℃, 3.3V, tR/tF = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to Y0	t_{PLH}	0.46	0.40 + 0.032*SL	0.41 + 0.028*SL	0.42 + 0.027*SL
	t_{PHL}	0.43	0.36 + 0.037*SL	0.37 + 0.034*SL	0.37 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.10 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
S1 to Y0	t_{PLH}	0.45	0.39 + 0.032*SL	0.40 + 0.028*SL	0.41 + 0.027*SL
	t_{PHL}	0.39	0.32 + 0.037*SL	0.33 + 0.034*SL	0.34 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
S0 to Y1	t_{PLH}	0.26	0.20 + 0.032*SL	0.21 + 0.028*SL	0.22 + 0.027*SL
	t_{PHL}	0.34	0.26 + 0.037*SL	0.27 + 0.034*SL	0.28 + 0.033*SL
	t_R	0.23	0.11 + 0.057*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
S1 to Y1	t_{PLH}	0.45	0.39 + 0.032*SL	0.40 + 0.028*SL	0.41 + 0.027*SL
	t_{PHL}	0.40	0.32 + 0.037*SL	0.33 + 0.033*SL	0.34 + 0.033*SL
	t_R	0.22	0.11 + 0.057*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
S0 to Y2	t_{PLH}	0.46	0.40 + 0.032*SL	0.41 + 0.028*SL	0.42 + 0.027*SL
	t_{PHL}	0.43	0.36 + 0.037*SL	0.37 + 0.033*SL	0.37 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.10 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.22	0.09 + 0.063*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
S1 to Y2	t_{PLH}	0.28	0.22 + 0.032*SL	0.23 + 0.028*SL	0.23 + 0.027*SL
	t_{PHL}	0.32	0.24 + 0.037*SL	0.25 + 0.034*SL	0.26 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.22	0.09 + 0.061*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
S0 to Y3	t_{PLH}	0.26	0.20 + 0.032*SL	0.21 + 0.028*SL	0.22 + 0.027*SL
	t_{PHL}	0.34	0.26 + 0.037*SL	0.28 + 0.033*SL	0.28 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
S1 to Y3	t_{PLH}	0.28	0.22 + 0.031*SL	0.22 + 0.028*SL	0.23 + 0.027*SL
	t_{PHL}	0.32	0.24 + 0.037*SL	0.25 + 0.033*SL	0.26 + 0.033*SL
	t_R	0.23	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



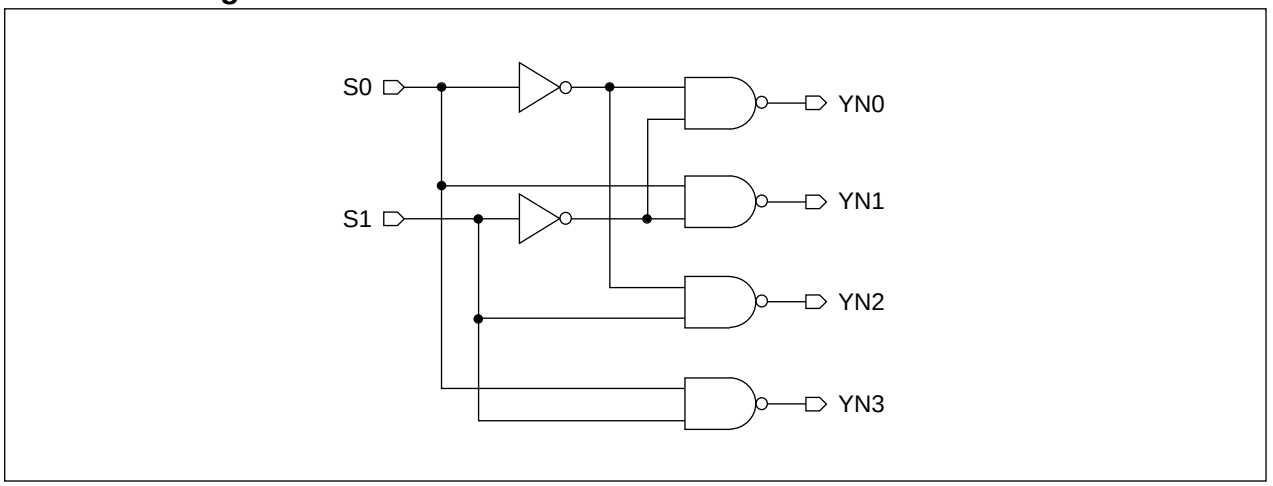
Truth Table

S1	S0	YN0	YN1	YN2	YN3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Cell Data

Input Load (SL)		Gate Count
S0	S1	
2.4	2.6	4.3

Schematic Diagram



DC4I

2 > 4 Inverting Decoder

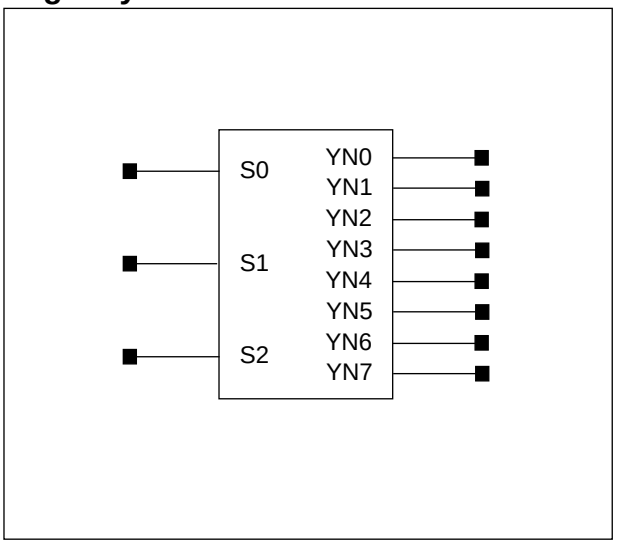
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	t_{PLH}	0.29	0.23 + 0.032*SL	0.24 + 0.028*SL	0.24 + 0.028*SL
	t_{PHL}	0.41	0.32 + 0.043*SL	0.33 + 0.038*SL	0.34 + 0.037*SL
	t_R	0.23	0.12 + 0.058*SL	0.11 + 0.061*SL	0.09 + 0.063*SL
	t_F	0.30	0.14 + 0.077*SL	0.14 + 0.078*SL	0.12 + 0.080*SL
S1 to YN0	t_{PLH}	0.30	0.24 + 0.031*SL	0.24 + 0.028*SL	0.24 + 0.028*SL
	t_{PHL}	0.38	0.30 + 0.040*SL	0.31 + 0.038*SL	0.31 + 0.037*SL
	t_R	0.25	0.14 + 0.056*SL	0.13 + 0.061*SL	0.11 + 0.063*SL
	t_F	0.29	0.14 + 0.075*SL	0.13 + 0.078*SL	0.11 + 0.081*SL
S0 to YN1	t_{PLH}	0.17	0.10 + 0.034*SL	0.12 + 0.028*SL	0.12 + 0.028*SL
	t_{PHL}	0.19	0.10 + 0.042*SL	0.12 + 0.037*SL	0.12 + 0.037*SL
	t_R	0.26	0.16 + 0.051*SL	0.14 + 0.058*SL	0.10 + 0.063*SL
	t_F	0.31	0.17 + 0.069*SL	0.15 + 0.076*SL	0.11 + 0.081*SL
S1 to YN1	t_{PLH}	0.30	0.24 + 0.030*SL	0.24 + 0.028*SL	0.25 + 0.028*SL
	t_{PHL}	0.39	0.31 + 0.040*SL	0.31 + 0.038*SL	0.32 + 0.037*SL
	t_R	0.25	0.14 + 0.057*SL	0.13 + 0.061*SL	0.11 + 0.063*SL
	t_F	0.29	0.13 + 0.076*SL	0.13 + 0.078*SL	0.11 + 0.081*SL
S0 to YN2	t_{PLH}	0.29	0.22 + 0.033*SL	0.24 + 0.028*SL	0.24 + 0.028*SL
	t_{PHL}	0.41	0.32 + 0.043*SL	0.33 + 0.039*SL	0.34 + 0.037*SL
	t_R	0.24	0.12 + 0.057*SL	0.11 + 0.061*SL	0.09 + 0.063*SL
	t_F	0.30	0.14 + 0.077*SL	0.14 + 0.078*SL	0.12 + 0.081*SL
S1 to YN2	t_{PLH}	0.19	0.12 + 0.032*SL	0.13 + 0.027*SL	0.13 + 0.028*SL
	t_{PHL}	0.17	0.08 + 0.041*SL	0.10 + 0.037*SL	0.09 + 0.037*SL
	t_R	0.28	0.19 + 0.048*SL	0.16 + 0.057*SL	0.11 + 0.063*SL
	t_F	0.30	0.16 + 0.070*SL	0.14 + 0.077*SL	0.10 + 0.081*SL
S0 to YN3	t_{PLH}	0.17	0.10 + 0.034*SL	0.12 + 0.028*SL	0.12 + 0.028*SL
	t_{PHL}	0.19	0.10 + 0.041*SL	0.12 + 0.037*SL	0.11 + 0.037*SL
	t_R	0.26	0.16 + 0.050*SL	0.14 + 0.058*SL	0.10 + 0.063*SL
	t_F	0.31	0.17 + 0.069*SL	0.15 + 0.076*SL	0.11 + 0.081*SL
S1 to YN3	t_{PLH}	0.19	0.12 + 0.032*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_R	0.28	0.19 + 0.049*SL	0.16 + 0.057*SL	0.11 + 0.063*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

Logic Symbol



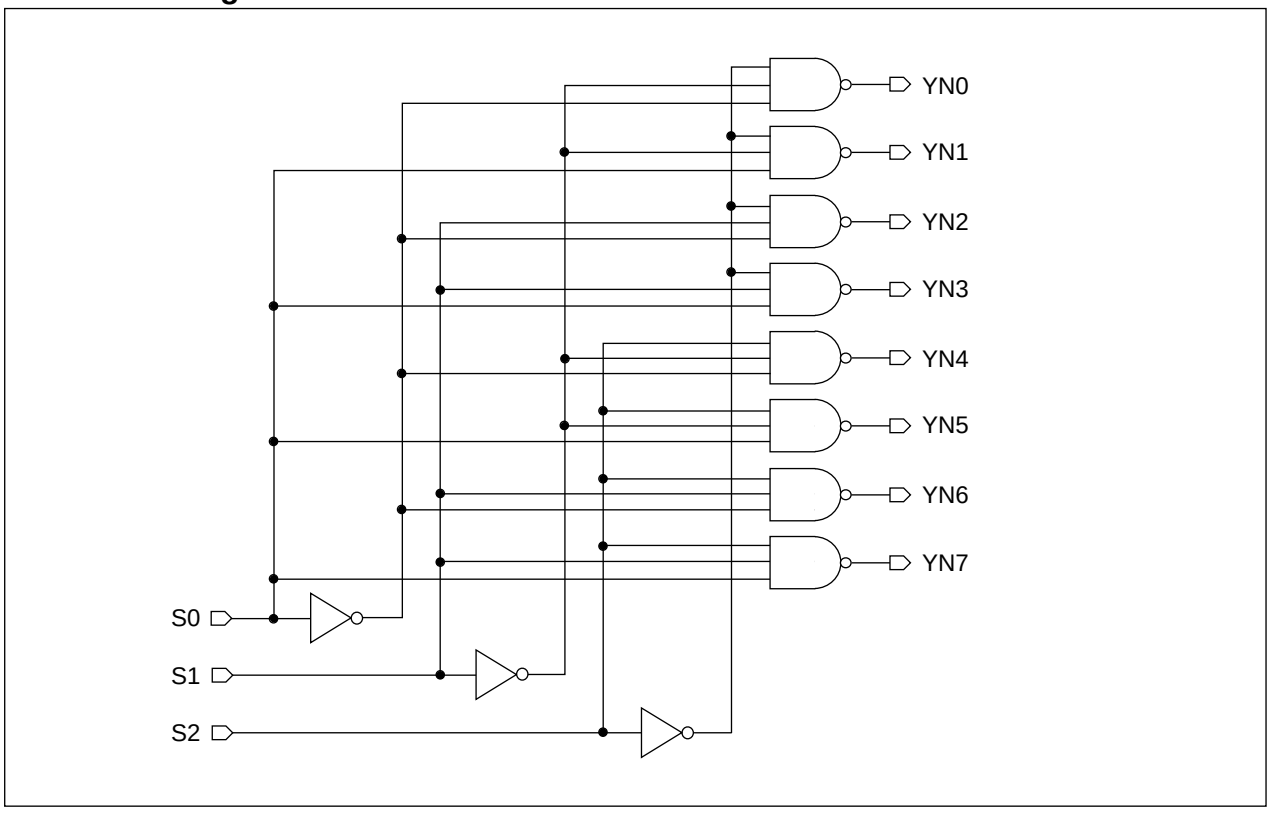
Truth Table

S0	S1	S2	YN 0	YN 1	YN 2	YN 3	YN 4	YN 5	YN 6	YN 7
0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
1	1	0	1	1	1	0	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Cell Data

Input Load (SL)			Gate Count
S0	S1	S2	
5.1	4.9	5.0	11.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S0 to YN0	t_{PLH}	0.42	0.35 + 0.033*SL	0.36 + 0.029*SL	0.37 + 0.028*SL
	t_{PHL}	0.60	0.49 + 0.055*SL	0.50 + 0.052*SL	0.51 + 0.052*SL
	t_R	0.32	0.21 + 0.058*SL	0.20 + 0.060*SL	0.18 + 0.062*SL
	t_F	0.50	0.28 + 0.108*SL	0.27 + 0.112*SL	0.25 + 0.115*SL
S1 to YN0	t_{PLH}	0.39	0.33 + 0.034*SL	0.34 + 0.030*SL	0.35 + 0.028*SL
	t_{PHL}	0.61	0.50 + 0.057*SL	0.51 + 0.052*SL	0.52 + 0.052*SL
	t_R	0.30	0.19 + 0.058*SL	0.18 + 0.060*SL	0.16 + 0.062*SL
	t_F	0.51	0.29 + 0.110*SL	0.29 + 0.111*SL	0.25 + 0.115*SL
S2 to YN0	t_{PLH}	0.42	0.35 + 0.032*SL	0.36 + 0.029*SL	0.37 + 0.028*SL
	t_{PHL}	0.57	0.47 + 0.053*SL	0.47 + 0.051*SL	0.47 + 0.052*SL
	t_R	0.34	0.23 + 0.056*SL	0.22 + 0.059*SL	0.19 + 0.062*SL
	t_F	0.49	0.27 + 0.109*SL	0.26 + 0.112*SL	0.23 + 0.115*SL
S0 to YN1	t_{PLH}	0.20	0.14 + 0.030*SL	0.15 + 0.028*SL	0.15 + 0.028*SL
	t_{PHL}	0.27	0.16 + 0.053*SL	0.17 + 0.052*SL	0.17 + 0.052*SL
	t_R	0.32	0.21 + 0.053*SL	0.20 + 0.058*SL	0.16 + 0.063*SL
	t_F	0.48	0.27 + 0.108*SL	0.26 + 0.112*SL	0.23 + 0.115*SL
S1 to YN1	t_{PLH}	0.39	0.33 + 0.034*SL	0.34 + 0.029*SL	0.35 + 0.028*SL
	t_{PHL}	0.61	0.50 + 0.057*SL	0.51 + 0.053*SL	0.52 + 0.052*SL
	t_R	0.30	0.19 + 0.057*SL	0.18 + 0.060*SL	0.16 + 0.062*SL
	t_F	0.51	0.30 + 0.108*SL	0.29 + 0.112*SL	0.26 + 0.115*SL
S2 to YN1	t_{PLH}	0.42	0.35 + 0.032*SL	0.36 + 0.029*SL	0.37 + 0.028*SL
	t_{PHL}	0.57	0.47 + 0.053*SL	0.47 + 0.052*SL	0.47 + 0.052*SL
	t_R	0.34	0.23 + 0.055*SL	0.22 + 0.059*SL	0.19 + 0.062*SL
	t_F	0.49	0.27 + 0.108*SL	0.26 + 0.112*SL	0.24 + 0.115*SL
S0 to YN2	t_{PLH}	0.42	0.35 + 0.033*SL	0.36 + 0.029*SL	0.38 + 0.028*SL
	t_{PHL}	0.60	0.49 + 0.055*SL	0.50 + 0.052*SL	0.51 + 0.052*SL
	t_R	0.32	0.20 + 0.057*SL	0.20 + 0.059*SL	0.17 + 0.062*SL
	t_F	0.49	0.28 + 0.108*SL	0.27 + 0.112*SL	0.24 + 0.115*SL
S1 to YN2	t_{PLH}	0.21	0.15 + 0.030*SL	0.16 + 0.028*SL	0.15 + 0.028*SL
	t_{PHL}	0.25	0.15 + 0.052*SL	0.15 + 0.052*SL	0.15 + 0.052*SL
	t_R	0.34	0.24 + 0.050*SL	0.22 + 0.057*SL	0.17 + 0.062*SL
	t_F	0.46	0.24 + 0.110*SL	0.23 + 0.113*SL	0.21 + 0.115*SL
S2 to YN2	t_{PLH}	0.40	0.33 + 0.034*SL	0.34 + 0.030*SL	0.36 + 0.028*SL
	t_{PHL}	0.61	0.50 + 0.058*SL	0.51 + 0.053*SL	0.52 + 0.052*SL
	t_R	0.29	0.18 + 0.058*SL	0.17 + 0.060*SL	0.15 + 0.062*SL
	t_F	0.51	0.28 + 0.111*SL	0.28 + 0.111*SL	0.25 + 0.115*SL
S0 to YN3	t_{PLH}	0.20	0.14 + 0.030*SL	0.15 + 0.028*SL	0.15 + 0.028*SL
	t_{PHL}	0.26	0.16 + 0.053*SL	0.16 + 0.051*SL	0.16 + 0.052*SL
	t_R	0.32	0.21 + 0.051*SL	0.19 + 0.058*SL	0.15 + 0.063*SL
	t_F	0.47	0.26 + 0.107*SL	0.24 + 0.113*SL	0.22 + 0.115*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S1 to YN3	t_{PLH}	0.21	0.15 + 0.029*SL	0.16 + 0.028*SL	0.16 + 0.028*SL
	t_{PHL}	0.25	0.15 + 0.053*SL	0.15 + 0.052*SL	0.15 + 0.052*SL
	t_R	0.34	0.24 + 0.050*SL	0.22 + 0.058*SL	0.17 + 0.062*SL
	t_F	0.46	0.24 + 0.111*SL	0.23 + 0.114*SL	0.22 + 0.115*SL
S2 to YN3	t_{PLH}	0.40	0.33 + 0.034*SL	0.34 + 0.029*SL	0.36 + 0.028*SL
	t_{PHL}	0.61	0.50 + 0.057*SL	0.51 + 0.053*SL	0.52 + 0.052*SL
	t_R	0.30	0.18 + 0.057*SL	0.18 + 0.060*SL	0.15 + 0.062*SL
	t_F	0.51	0.29 + 0.110*SL	0.29 + 0.111*SL	0.25 + 0.115*SL
S0 to YN4	t_{PLH}	0.42	0.36 + 0.033*SL	0.37 + 0.029*SL	0.38 + 0.028*SL
	t_{PHL}	0.61	0.50 + 0.055*SL	0.50 + 0.052*SL	0.51 + 0.052*SL
	t_R	0.32	0.21 + 0.058*SL	0.20 + 0.059*SL	0.17 + 0.062*SL
	t_F	0.49	0.28 + 0.108*SL	0.27 + 0.112*SL	0.24 + 0.115*SL
S1 to YN4	t_{PLH}	0.39	0.32 + 0.034*SL	0.33 + 0.029*SL	0.35 + 0.028*SL
	t_{PHL}	0.61	0.49 + 0.057*SL	0.50 + 0.053*SL	0.51 + 0.052*SL
	t_R	0.30	0.18 + 0.057*SL	0.17 + 0.060*SL	0.15 + 0.062*SL
	t_F	0.50	0.28 + 0.109*SL	0.28 + 0.111*SL	0.25 + 0.115*SL
S2 to YN4	t_{PLH}	0.21	0.15 + 0.029*SL	0.16 + 0.028*SL	0.16 + 0.028*SL
	t_{PHL}	0.25	0.15 + 0.052*SL	0.15 + 0.051*SL	0.15 + 0.051*SL
	t_R	0.34	0.24 + 0.051*SL	0.22 + 0.057*SL	0.17 + 0.062*SL
	t_F	0.46	0.25 + 0.108*SL	0.24 + 0.113*SL	0.21 + 0.115*SL
S0 to YN5	t_{PLH}	0.20	0.14 + 0.030*SL	0.15 + 0.028*SL	0.15 + 0.028*SL
	t_{PHL}	0.26	0.16 + 0.053*SL	0.16 + 0.052*SL	0.16 + 0.052*SL
	t_R	0.31	0.21 + 0.051*SL	0.19 + 0.058*SL	0.15 + 0.063*SL
	t_F	0.47	0.26 + 0.108*SL	0.24 + 0.112*SL	0.22 + 0.115*SL
S1 to YN5	t_{PLH}	0.39	0.32 + 0.034*SL	0.33 + 0.029*SL	0.35 + 0.028*SL
	t_{PHL}	0.61	0.49 + 0.057*SL	0.50 + 0.053*SL	0.52 + 0.052*SL
	t_R	0.30	0.18 + 0.057*SL	0.17 + 0.060*SL	0.15 + 0.062*SL
	t_F	0.50	0.29 + 0.110*SL	0.28 + 0.111*SL	0.25 + 0.115*SL
S2 to YN5	t_{PLH}	0.21	0.15 + 0.030*SL	0.16 + 0.028*SL	0.16 + 0.028*SL
	t_{PHL}	0.25	0.15 + 0.053*SL	0.15 + 0.051*SL	0.15 + 0.052*SL
	t_R	0.34	0.24 + 0.050*SL	0.22 + 0.058*SL	0.17 + 0.062*SL
	t_F	0.46	0.25 + 0.108*SL	0.23 + 0.113*SL	0.21 + 0.115*SL
S0 to YN6	t_{PLH}	0.43	0.36 + 0.034*SL	0.37 + 0.029*SL	0.39 + 0.028*SL
	t_{PHL}	0.61	0.50 + 0.055*SL	0.51 + 0.053*SL	0.52 + 0.052*SL
	t_R	0.32	0.21 + 0.056*SL	0.20 + 0.059*SL	0.17 + 0.062*SL
	t_F	0.50	0.28 + 0.108*SL	0.27 + 0.111*SL	0.24 + 0.115*SL
S1 to YN6	t_{PLH}	0.19	0.12 + 0.033*SL	0.14 + 0.028*SL	0.13 + 0.028*SL
	t_{PHL}	0.27	0.17 + 0.051*SL	0.16 + 0.051*SL	0.16 + 0.052*SL
	t_R	0.29	0.19 + 0.052*SL	0.17 + 0.058*SL	0.13 + 0.063*SL
	t_F	0.47	0.25 + 0.107*SL	0.24 + 0.112*SL	0.21 + 0.115*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

(Continued)

DC8I

3 > 8 Inverting Decoder

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
S2 to YN6	t_{PLH}	0.21	0.15 + 0.029*SL	0.16 + 0.028*SL	0.16 + 0.028*SL
	t_{PHL}	0.25	0.14 + 0.053*SL	0.15 + 0.052*SL	0.15 + 0.052*SL
	t_R	0.34	0.24 + 0.050*SL	0.22 + 0.057*SL	0.17 + 0.063*SL
	t_F	0.46	0.24 + 0.109*SL	0.23 + 0.114*SL	0.22 + 0.115*SL
S0 to YN7	t_{PLH}	0.20	0.14 + 0.030*SL	0.15 + 0.028*SL	0.15 + 0.028*SL
	t_{PHL}	0.26	0.16 + 0.051*SL	0.16 + 0.052*SL	0.16 + 0.052*SL
	t_R	0.31	0.21 + 0.051*SL	0.19 + 0.058*SL	0.15 + 0.063*SL
	t_F	0.46	0.24 + 0.109*SL	0.23 + 0.113*SL	0.21 + 0.115*SL
S1 to YN7	t_{PLH}	0.19	0.12 + 0.033*SL	0.14 + 0.028*SL	0.13 + 0.028*SL
	t_{PHL}	0.27	0.17 + 0.051*SL	0.17 + 0.051*SL	0.16 + 0.052*SL
	t_R	0.30	0.19 + 0.053*SL	0.18 + 0.058*SL	0.13 + 0.063*SL
	t_F	0.47	0.26 + 0.108*SL	0.24 + 0.112*SL	0.21 + 0.115*SL
S2 to YN7	t_{PLH}	0.21	0.15 + 0.029*SL	0.16 + 0.028*SL	0.16 + 0.028*SL
	t_{PHL}	0.25	0.15 + 0.052*SL	0.15 + 0.052*SL	0.15 + 0.052*SL
	t_R	0.34	0.24 + 0.052*SL	0.22 + 0.057*SL	0.17 + 0.063*SL
	t_F	0.46	0.24 + 0.111*SL	0.23 + 0.114*SL	0.22 + 0.115*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

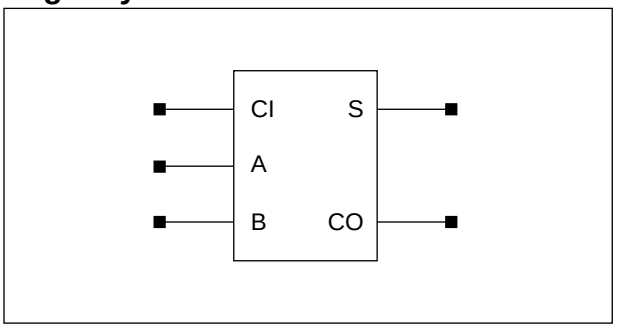
Cell Names & Function Descriptions

Cell Name	Function Description
FA	Full Adder
FAD2	Full Adder with 2X Drive
HA	Half Adder
HAD2	Half Adder with 2X Drive

FA/FAD2

Full Adder with 1X/2X Drive

Logic Symbol



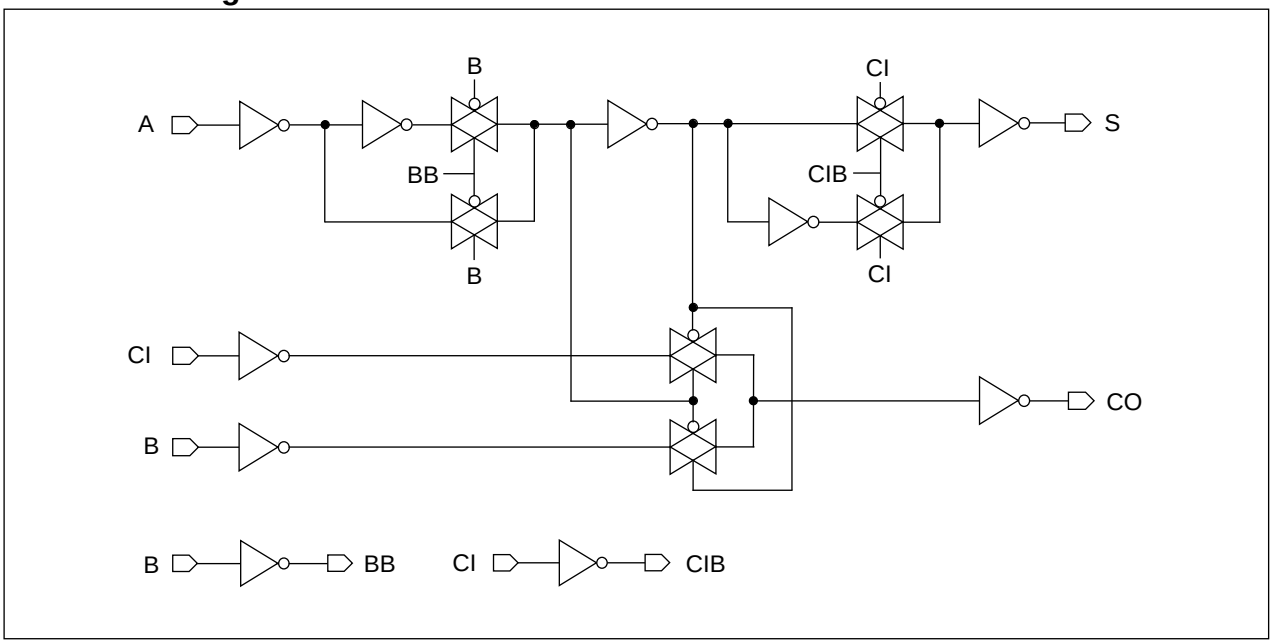
Truth Table

CI	A	B	S	CO
0	0	0	0	0
1	0	0	1	0
0	0	1	1	0
1	0	1	0	1
0	1	0	1	0
1	1	0	0	1
0	1	1	0	1
1	1	1	1	1

Cell Data

Input Load (SL)						Gate Count	
FA			*FAD2*			*FA*	*FAD2*
CI	A	B	CI	A	B		
1.5	0.7	1.6	1.5	0.7	1.6	6.3	6.7

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.89	0.83 + 0.032*SL	0.84 + 0.028*SL	0.85 + 0.027*SL
	t_{PHL}	0.92	0.83 + 0.047*SL	0.86 + 0.038*SL	0.90 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.32	0.19 + 0.064*SL	0.20 + 0.061*SL	0.17 + 0.064*SL
B to S	t_{PLH}	0.81	0.74 + 0.033*SL	0.75 + 0.028*SL	0.77 + 0.027*SL
	t_{PHL}	0.86	0.78 + 0.044*SL	0.80 + 0.036*SL	0.83 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.064*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
CI to S	t_{PLH}	0.47	0.41 + 0.033*SL	0.42 + 0.029*SL	0.44 + 0.027*SL
	t_{PHL}	0.46	0.38 + 0.044*SL	0.40 + 0.036*SL	0.43 + 0.033*SL
	t_R	0.25	0.14 + 0.054*SL	0.14 + 0.057*SL	0.11 + 0.060*SL
	t_F	0.27	0.15 + 0.065*SL	0.15 + 0.062*SL	0.13 + 0.065*SL
A to CO	t_{PLH}	0.76	0.70 + 0.032*SL	0.71 + 0.028*SL	0.72 + 0.027*SL
	t_{PHL}	0.89	0.80 + 0.045*SL	0.82 + 0.037*SL	0.86 + 0.033*SL
	t_R	0.26	0.15 + 0.052*SL	0.14 + 0.056*SL	0.11 + 0.060*SL
	t_F	0.29	0.16 + 0.065*SL	0.17 + 0.063*SL	0.15 + 0.065*SL
B to CO	t_{PLH}	0.65	0.58 + 0.033*SL	0.60 + 0.028*SL	0.61 + 0.027*SL
	t_{PHL}	0.72	0.63 + 0.043*SL	0.65 + 0.037*SL	0.68 + 0.033*SL
	t_R	0.26	0.15 + 0.053*SL	0.14 + 0.056*SL	0.11 + 0.060*SL
	t_F	0.27	0.13 + 0.066*SL	0.14 + 0.064*SL	0.13 + 0.065*SL
CI to CO	t_{PLH}	0.38	0.31 + 0.034*SL	0.33 + 0.029*SL	0.34 + 0.027*SL
	t_{PHL}	0.51	0.42 + 0.047*SL	0.44 + 0.038*SL	0.49 + 0.033*SL
	t_R	0.24	0.13 + 0.057*SL	0.13 + 0.057*SL	0.11 + 0.060*SL
	t_F	0.30	0.17 + 0.066*SL	0.17 + 0.063*SL	0.16 + 0.064*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

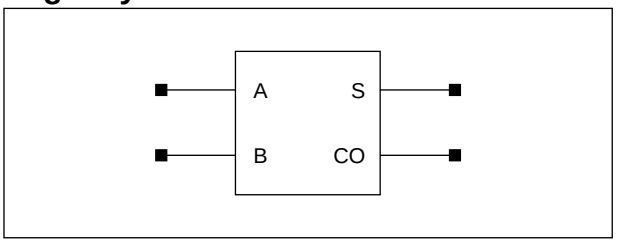
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

FAD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.90	0.86 + 0.020*SL	0.87 + 0.016*SL	0.90 + 0.013*SL
	t_{PHL}	0.94	0.88 + 0.027*SL	0.90 + 0.022*SL	0.94 + 0.017*SL
	t_R	0.18	0.13 + 0.027*SL	0.13 + 0.027*SL	0.11 + 0.028*SL
	t_F	0.23	0.17 + 0.033*SL	0.17 + 0.032*SL	0.17 + 0.032*SL
B to S	t_{PLH}	0.82	0.78 + 0.020*SL	0.79 + 0.016*SL	0.81 + 0.013*SL
	t_{PHL}	0.88	0.83 + 0.027*SL	0.84 + 0.022*SL	0.89 + 0.017*SL
	t_R	0.18	0.13 + 0.026*SL	0.13 + 0.027*SL	0.11 + 0.028*SL
	t_F	0.23	0.16 + 0.033*SL	0.16 + 0.032*SL	0.17 + 0.032*SL
CI to S	t_{PLH}	0.50	0.46 + 0.020*SL	0.47 + 0.016*SL	0.50 + 0.013*SL
	t_{PHL}	0.47	0.42 + 0.028*SL	0.44 + 0.022*SL	0.48 + 0.017*SL
	t_R	0.22	0.17 + 0.025*SL	0.17 + 0.026*SL	0.14 + 0.028*SL
	t_F	0.24	0.18 + 0.032*SL	0.18 + 0.032*SL	0.18 + 0.032*SL
A to CO	t_{PLH}	0.80	0.76 + 0.020*SL	0.77 + 0.016*SL	0.80 + 0.013*SL
	t_{PHL}	0.90	0.84 + 0.028*SL	0.86 + 0.022*SL	0.91 + 0.017*SL
	t_R	0.23	0.18 + 0.024*SL	0.17 + 0.025*SL	0.15 + 0.028*SL
	t_F	0.26	0.19 + 0.033*SL	0.19 + 0.032*SL	0.20 + 0.031*SL
B to CO	t_{PLH}	0.68	0.64 + 0.020*SL	0.66 + 0.016*SL	0.68 + 0.013*SL
	t_{PHL}	0.75	0.70 + 0.027*SL	0.71 + 0.022*SL	0.75 + 0.017*SL
	t_R	0.23	0.18 + 0.023*SL	0.17 + 0.025*SL	0.15 + 0.028*SL
	t_F	0.23	0.17 + 0.033*SL	0.17 + 0.032*SL	0.17 + 0.032*SL
CI to CO	t_{PLH}	0.38	0.34 + 0.020*SL	0.35 + 0.016*SL	0.38 + 0.013*SL
	t_{PHL}	0.51	0.46 + 0.029*SL	0.47 + 0.023*SL	0.53 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.25	0.19 + 0.033*SL	0.19 + 0.032*SL	0.20 + 0.031*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



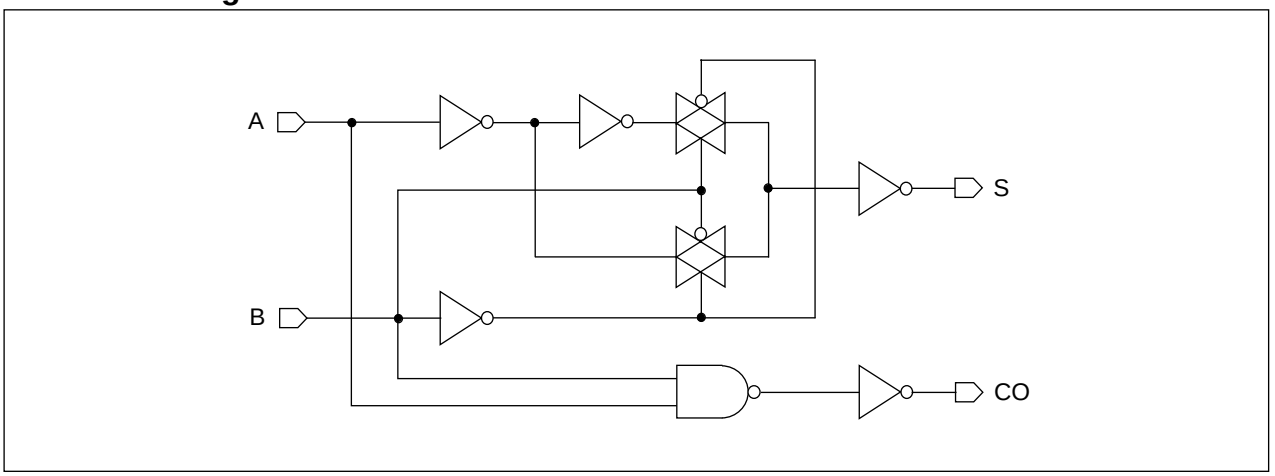
Truth Table

A	B	S	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Cell Data

Input Load (SL)				Gate Count	
HA		*HAD2*		*HA*	*HAD2*
A	B	A	B		
1.5	2.3	1.5	2.3	4.0	4.7

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

HA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.49	0.42 + 0.033*SL	0.43 + 0.028*SL	0.45 + 0.027*SL
	t_{PHL}	0.51	0.42 + 0.045*SL	0.45 + 0.037*SL	0.48 + 0.033*SL
	t_R	0.23	0.12 + 0.056*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.28	0.15 + 0.066*SL	0.16 + 0.062*SL	0.14 + 0.065*SL
B to S	t_{PLH}	0.37	0.31 + 0.033*SL	0.32 + 0.028*SL	0.33 + 0.027*SL
	t_{PHL}	0.40	0.31 + 0.044*SL	0.33 + 0.037*SL	0.36 + 0.033*SL
	t_R	0.23	0.12 + 0.056*SL	0.11 + 0.058*SL	0.10 + 0.060*SL
	t_F	0.26	0.12 + 0.068*SL	0.14 + 0.063*SL	0.12 + 0.065*SL
A to CO	t_{PLH}	0.28	0.21 + 0.031*SL	0.22 + 0.028*SL	0.23 + 0.027*SL
	t_{PHL}	0.32	0.24 + 0.037*SL	0.25 + 0.033*SL	0.26 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.22	0.09 + 0.061*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
B to CO	t_{PLH}	0.26	0.19 + 0.032*SL	0.20 + 0.028*SL	0.21 + 0.027*SL
	t_{PHL}	0.34	0.26 + 0.037*SL	0.27 + 0.034*SL	0.28 + 0.033*SL
	t_R	0.22	0.12 + 0.053*SL	0.10 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

HAD2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to S	t_{PLH}	0.49	0.45 + 0.020*SL	0.46 + 0.016*SL	0.49 + 0.013*SL
	t_{PHL}	0.52	0.46 + 0.028*SL	0.48 + 0.022*SL	0.53 + 0.017*SL
	t_R	0.18	0.13 + 0.026*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.24	0.17 + 0.033*SL	0.17 + 0.032*SL	0.18 + 0.032*SL
B to S	t_{PLH}	0.37	0.33 + 0.020*SL	0.34 + 0.016*SL	0.37 + 0.013*SL
	t_{PHL}	0.40	0.35 + 0.028*SL	0.36 + 0.022*SL	0.41 + 0.017*SL
	t_R	0.18	0.13 + 0.025*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.22	0.15 + 0.034*SL	0.16 + 0.033*SL	0.16 + 0.032*SL
A to CO	t_{PLH}	0.30	0.26 + 0.019*SL	0.27 + 0.015*SL	0.29 + 0.013*SL
	t_{PHL}	0.32	0.28 + 0.022*SL	0.29 + 0.018*SL	0.31 + 0.017*SL
	t_R	0.18	0.12 + 0.026*SL	0.12 + 0.027*SL	0.11 + 0.029*SL
	t_F	0.16	0.10 + 0.032*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
B to CO	t_{PLH}	0.27	0.23 + 0.019*SL	0.24 + 0.015*SL	0.27 + 0.013*SL
	t_{PHL}	0.34	0.30 + 0.022*SL	0.31 + 0.018*SL	0.33 + 0.017*SL
	t_R	0.18	0.13 + 0.023*SL	0.12 + 0.027*SL	0.11 + 0.029*SL
	t_F	0.17	0.10 + 0.031*SL	0.10 + 0.031*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

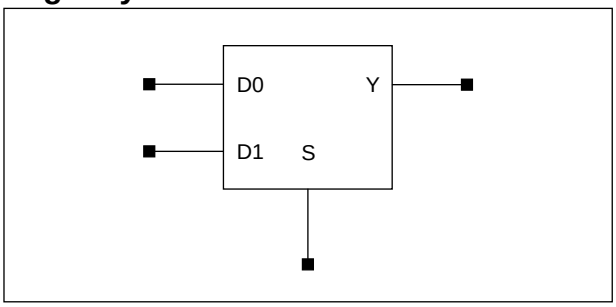
Cell Names & Function Descriptions

Cell Name	Function Description
MX2	2 > 1 Non-Inverting Mux
MX2D3	2 > 1 Non-Inverting Mux with 3X Drive
MX2X4	4-Bit 2 > 1 Non-Inverting Mux
YMX2	Fast 2 > 1 Non-Inverting Mux
YMX2D2	Fast 2 > 1 Non-Inverting Mux with 2X Drive
MX2I	2 > 1 Inverting Mux
MX2ID2	2 > 1 Inverting Mux with 2X Drive
MX2IA	2 > 1 Inverting Mux with Separate S and SN Inputs
MX2ID2A	2 > 1 Inverting Mux with Separate S and SN Inputs, 2X Drive
MX2IX4	4-Bit 2 > 1 Inverting Mux
MX3I	3 > 1 Inverting Mux
MX3ID2	3 > 1 Inverting Mux with 2X Drive
MX4	4 > 1 Non-Inverting Mux
MX4D2	4 > 1 Non-Inverting Mux with 2X Drive
YMX4	Fast 4 > 1 Non-Inverting Mux
YMX4D2	Fast 4 > 1 Non-Inverting Mux with 2X Drive
MX5	5 > 1 Non-Inverting Mux
MX5D2	5 > 1 Non-Inverting Mux with 2X Drive
MX8	8 > 1 Non-Inverting Mux
MX8D2	8 > 1 Non-Inverting Mux with 2X Drive
YMX8	Fast 8 > 1 Non-Inverting Mux
YMX8D2	Fast 8 > 1 Non-Inverting Mux with 2X Drive

MX2/MX2D3

2 > 1 Non-Inverting MUX with 1X/3X Drive

Logic Symbol



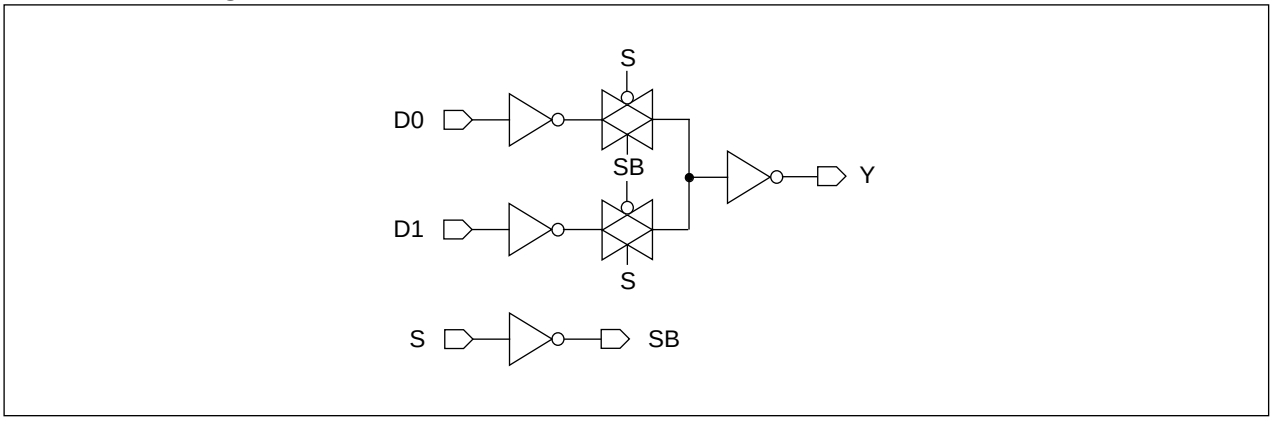
Truth Table

D0	D1	S	Y
0	x	0	0
1	x	0	1
x	0	1	0
x	1	1	1

Cell Data

Input Load (SL)						Gate Count	
MX2			*MX2D3*			*MX2*	*MX2D3*
D0	D1	S	D0	D1	S		
0.7	0.7	1.3	0.7	0.7	1.3	2.7	3.3

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

MX2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.31	0.25 + 0.032*SL	0.26 + 0.028*SL	0.27 + 0.027*SL
	t_{PHL}	0.43	0.34 + 0.043*SL	0.36 + 0.036*SL	0.39 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.065*SL	0.15 + 0.063*SL	0.12 + 0.065*SL
D1 to Y	t_{PLH}	0.31	0.25 + 0.033*SL	0.26 + 0.028*SL	0.27 + 0.027*SL
	t_{PHL}	0.43	0.34 + 0.044*SL	0.36 + 0.036*SL	0.39 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.066*SL	0.15 + 0.062*SL	0.12 + 0.065*SL
S to Y	t_{PLH}	0.37	0.31 + 0.032*SL	0.32 + 0.028*SL	0.33 + 0.027*SL
	t_{PHL}	0.40	0.31 + 0.043*SL	0.33 + 0.036*SL	0.36 + 0.033*SL
	t_R	0.23	0.12 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.26	0.12 + 0.068*SL	0.14 + 0.063*SL	0.12 + 0.065*SL

MX2D3

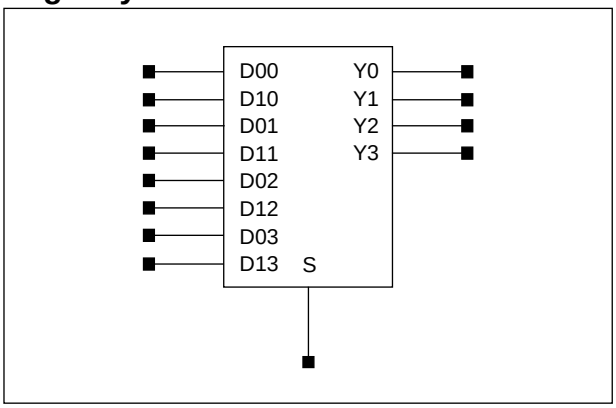
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.36	0.33 + 0.015*SL	0.34 + 0.012*SL	0.36 + 0.009*SL
	t_{PHL}	0.49	0.45 + 0.020*SL	0.46 + 0.016*SL	0.50 + 0.012*SL
	t_R	0.20	0.16 + 0.017*SL	0.16 + 0.017*SL	0.15 + 0.018*SL
	t_F	0.25	0.20 + 0.023*SL	0.21 + 0.022*SL	0.22 + 0.021*SL
D1 to Y	t_{PLH}	0.35	0.32 + 0.015*SL	0.33 + 0.012*SL	0.36 + 0.009*SL
	t_{PHL}	0.49	0.45 + 0.020*SL	0.46 + 0.016*SL	0.50 + 0.012*SL
	t_R	0.20	0.16 + 0.018*SL	0.16 + 0.017*SL	0.15 + 0.018*SL
	t_F	0.25	0.21 + 0.023*SL	0.21 + 0.021*SL	0.21 + 0.021*SL
S to Y	t_{PLH}	0.40	0.37 + 0.015*SL	0.38 + 0.012*SL	0.41 + 0.009*SL
	t_{PHL}	0.46	0.42 + 0.020*SL	0.43 + 0.017*SL	0.47 + 0.012*SL
	t_R	0.20	0.17 + 0.015*SL	0.16 + 0.018*SL	0.16 + 0.018*SL
	t_F	0.25	0.20 + 0.024*SL	0.21 + 0.021*SL	0.21 + 0.021*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

MX2X4

4-Bit 2 > 1 Non-Inverting MUX

Logic Symbol



Truth Table

S	Y0	Y1	Y2	Y3
0	D00	D01	D02	D03
1	D10	D11	D12	D13

Cell Data

Input Load (SL)		Gate Count
Dxy	S	
0.7	2.9	8.7

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to Y0	t_{PLH}	0.31	0.25 + 0.032*SL	0.26 + 0.028*SL	0.27 + 0.027*SL
	t_{PHL}	0.43	0.34 + 0.043*SL	0.36 + 0.036*SL	0.39 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.065*SL	0.15 + 0.062*SL	0.12 + 0.065*SL
D10 to Y0	t_{PLH}	0.31	0.25 + 0.032*SL	0.26 + 0.028*SL	0.27 + 0.027*SL
	t_{PHL}	0.43	0.34 + 0.043*SL	0.36 + 0.036*SL	0.39 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.066*SL	0.15 + 0.063*SL	0.12 + 0.065*SL
S to Y0	t_{PLH}	0.47	0.41 + 0.032*SL	0.42 + 0.028*SL	0.43 + 0.027*SL
	t_{PHL}	0.46	0.37 + 0.044*SL	0.39 + 0.036*SL	0.42 + 0.033*SL
	t_R	0.25	0.14 + 0.052*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.27	0.14 + 0.065*SL	0.15 + 0.063*SL	0.13 + 0.065*SL
D01 to Y1	t_{PLH}	0.31	0.25 + 0.032*SL	0.26 + 0.028*SL	0.27 + 0.027*SL
	t_{PHL}	0.43	0.34 + 0.043*SL	0.36 + 0.036*SL	0.39 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.065*SL	0.15 + 0.063*SL	0.13 + 0.065*SL
D11 to Y1	t_{PLH}	0.31	0.25 + 0.032*SL	0.26 + 0.028*SL	0.27 + 0.027*SL
	t_{PHL}	0.43	0.35 + 0.043*SL	0.37 + 0.036*SL	0.40 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.066*SL	0.15 + 0.062*SL	0.13 + 0.065*SL
S to Y1	t_{PLH}	0.48	0.41 + 0.033*SL	0.42 + 0.028*SL	0.44 + 0.027*SL
	t_{PHL}	0.46	0.37 + 0.044*SL	0.39 + 0.036*SL	0.42 + 0.033*SL
	t_R	0.25	0.14 + 0.052*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.27	0.15 + 0.065*SL	0.15 + 0.063*SL	0.13 + 0.065*SL
D02 to Y2	t_{PLH}	0.31	0.25 + 0.032*SL	0.26 + 0.028*SL	0.27 + 0.027*SL
	t_{PHL}	0.43	0.34 + 0.043*SL	0.36 + 0.036*SL	0.39 + 0.033*SL
	t_R	0.23	0.13 + 0.053*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.066*SL	0.15 + 0.063*SL	0.13 + 0.065*SL
D12 to Y2	t_{PLH}	0.31	0.25 + 0.032*SL	0.26 + 0.028*SL	0.27 + 0.027*SL
	t_{PHL}	0.43	0.35 + 0.044*SL	0.37 + 0.036*SL	0.40 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.066*SL	0.15 + 0.063*SL	0.13 + 0.065*SL
S to Y2	t_{PLH}	0.48	0.41 + 0.032*SL	0.42 + 0.028*SL	0.43 + 0.027*SL
	t_{PHL}	0.46	0.37 + 0.043*SL	0.39 + 0.036*SL	0.42 + 0.033*SL
	t_R	0.25	0.14 + 0.052*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.28	0.15 + 0.065*SL	0.15 + 0.062*SL	0.13 + 0.065*SL
D03 to Y3	t_{PLH}	0.31	0.25 + 0.032*SL	0.26 + 0.028*SL	0.27 + 0.027*SL
	t_{PHL}	0.43	0.34 + 0.043*SL	0.36 + 0.036*SL	0.39 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.065*SL	0.15 + 0.063*SL	0.12 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

(Continued)

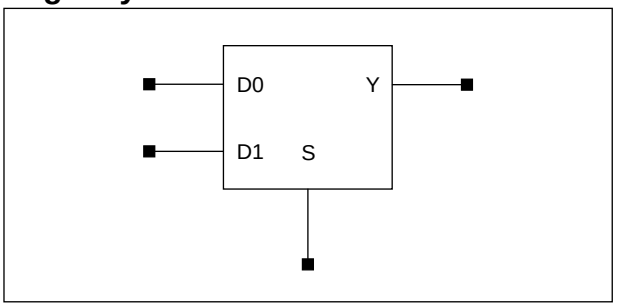
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D13 to Y3	t_{PLH}	0.31	0.25 + 0.032*SL	0.26 + 0.028*SL	0.27 + 0.027*SL
	t_{PHL}	0.43	0.34 + 0.043*SL	0.36 + 0.036*SL	0.39 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.066*SL	0.15 + 0.063*SL	0.12 + 0.065*SL
S to Y3	t_{PLH}	0.47	0.41 + 0.033*SL	0.42 + 0.028*SL	0.43 + 0.027*SL
	t_{PHL}	0.46	0.37 + 0.043*SL	0.39 + 0.036*SL	0.42 + 0.033*SL
	t_R	0.24	0.14 + 0.052*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.27	0.14 + 0.065*SL	0.15 + 0.063*SL	0.13 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



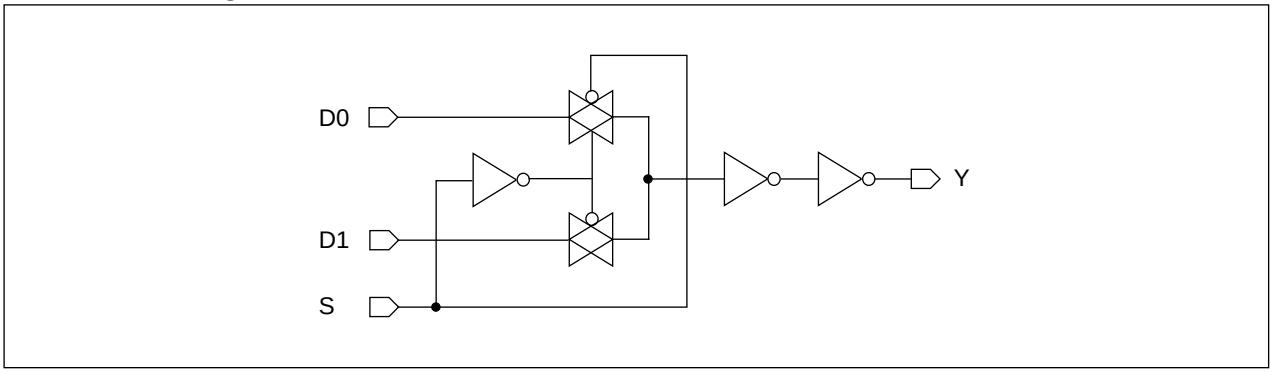
Truth Table

D0	D1	S	Y
0	x	0	0
1	x	0	1
x	0	1	0
x	1	1	1

Cell Data

Input Load (SL)						Gate Count	
YMX2			*YMX2D2*			*YMX2*	*YMX2D2*
D0	D1	S	D0	D1	S		
2.4	2.3	1.3	2.4	2.4	1.3	2.7	3.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

YMX2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.26	0.21 + 0.029*SL	0.21 + 0.027*SL	0.21 + 0.027*SL
	t_{PHL}	0.36	0.29 + 0.037*SL	0.30 + 0.033*SL	0.30 + 0.033*SL
	t_R	0.21	0.09 + 0.059*SL	0.10 + 0.057*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
D1 to Y	t_{PLH}	0.26	0.21 + 0.029*SL	0.21 + 0.027*SL	0.21 + 0.027*SL
	t_{PHL}	0.36	0.28 + 0.036*SL	0.29 + 0.033*SL	0.30 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.064*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
S to Y	t_{PLH}	0.36	0.30 + 0.028*SL	0.30 + 0.027*SL	0.30 + 0.027*SL
	t_{PHL}	0.47	0.39 + 0.037*SL	0.40 + 0.033*SL	0.41 + 0.033*SL
	t_R	0.20	0.09 + 0.056*SL	0.08 + 0.059*SL	0.07 + 0.060*SL
	t_F	0.21	0.09 + 0.062*SL	0.08 + 0.064*SL	0.07 + 0.066*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

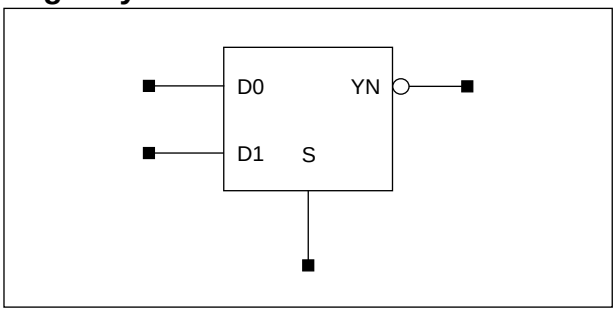
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

YMX2D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.27	0.24 + 0.016*SL	0.25 + 0.014*SL	0.25 + 0.013*SL
	t_{PHL}	0.36	0.32 + 0.021*SL	0.33 + 0.018*SL	0.35 + 0.017*SL
	t_R	0.15	0.10 + 0.027*SL	0.10 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.09 + 0.034*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
D1 to Y	t_{PLH}	0.27	0.24 + 0.017*SL	0.25 + 0.014*SL	0.25 + 0.013*SL
	t_{PHL}	0.36	0.32 + 0.022*SL	0.33 + 0.018*SL	0.34 + 0.017*SL
	t_R	0.16	0.12 + 0.016*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.029*SL	0.10 + 0.031*SL	0.08 + 0.032*SL
S to Y	t_{PLH}	0.36	0.32 + 0.016*SL	0.33 + 0.014*SL	0.34 + 0.013*SL
	t_{PHL}	0.47	0.43 + 0.022*SL	0.44 + 0.018*SL	0.46 + 0.017*SL
	t_R	0.14	0.09 + 0.027*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.030*SL	0.09 + 0.031*SL	0.08 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



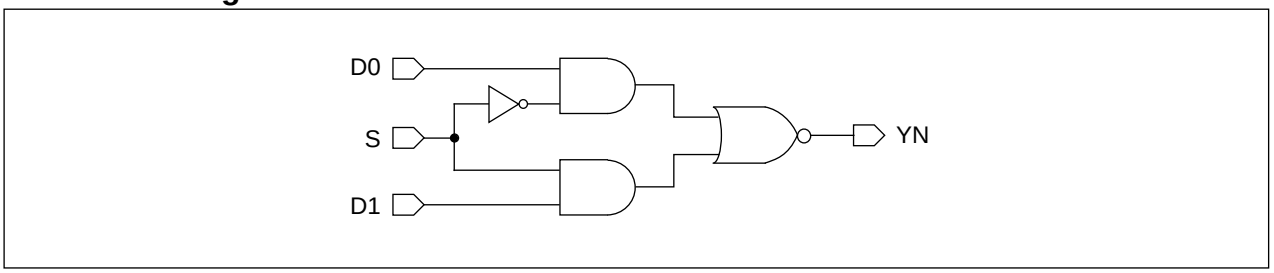
Truth Table

D0	D1	S	YN
0	x	0	1
1	x	0	0
x	0	1	1
x	1	1	0

Cell Data

Input Load (SL)						Gate Count	
MX2I			*MX2ID2*			*MX2I*	*MX2ID2*
D0	D1	S	D0	D1	S		
0.6	1.0	1.7	0.7	0.7	1.3	2.3	3.7

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

MX2I

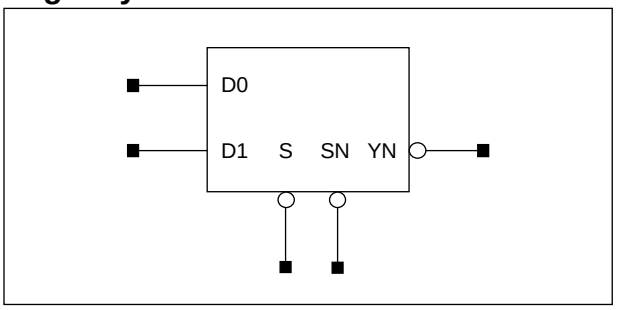
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.26	0.17 + 0.049*SL	0.16 + 0.051*SL	0.16 + 0.051*SL
	t_{PHL}	0.24	0.13 + 0.055*SL	0.13 + 0.053*SL	0.13 + 0.053*SL
	t_R	0.50	0.29 + 0.107*SL	0.27 + 0.114*SL	0.23 + 0.117*SL
	t_F	0.42	0.21 + 0.104*SL	0.19 + 0.111*SL	0.17 + 0.114*SL
D1 to YN	t_{PLH}	0.29	0.19 + 0.054*SL	0.19 + 0.052*SL	0.19 + 0.051*SL
	t_{PHL}	0.38	0.27 + 0.055*SL	0.28 + 0.054*SL	0.28 + 0.053*SL
	t_R	0.45	0.23 + 0.110*SL	0.22 + 0.115*SL	0.19 + 0.117*SL
	t_F	0.57	0.36 + 0.106*SL	0.35 + 0.111*SL	0.32 + 0.114*SL
S to YN	t_{PLH}	0.29	0.19 + 0.050*SL	0.19 + 0.051*SL	0.19 + 0.051*SL
	t_{PHL}	0.39	0.28 + 0.055*SL	0.29 + 0.053*SL	0.29 + 0.053*SL
	t_R	0.48	0.25 + 0.113*SL	0.24 + 0.117*SL	0.23 + 0.117*SL
	t_F	0.37	0.15 + 0.110*SL	0.15 + 0.112*SL	0.13 + 0.114*SL

MX2ID2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.46	0.42 + 0.016*SL	0.43 + 0.014*SL	0.44 + 0.013*SL
	t_{PHL}	0.46	0.41 + 0.022*SL	0.42 + 0.018*SL	0.44 + 0.017*SL
	t_R	0.15	0.10 + 0.024*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
D1 to YN	t_{PLH}	0.46	0.42 + 0.017*SL	0.43 + 0.014*SL	0.44 + 0.013*SL
	t_{PHL}	0.45	0.41 + 0.022*SL	0.42 + 0.018*SL	0.44 + 0.017*SL
	t_R	0.15	0.10 + 0.025*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
S to YN	t_{PLH}	0.42	0.39 + 0.016*SL	0.40 + 0.014*SL	0.41 + 0.013*SL
	t_{PHL}	0.51	0.47 + 0.022*SL	0.48 + 0.018*SL	0.50 + 0.017*SL
	t_R	0.15	0.09 + 0.026*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.08 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



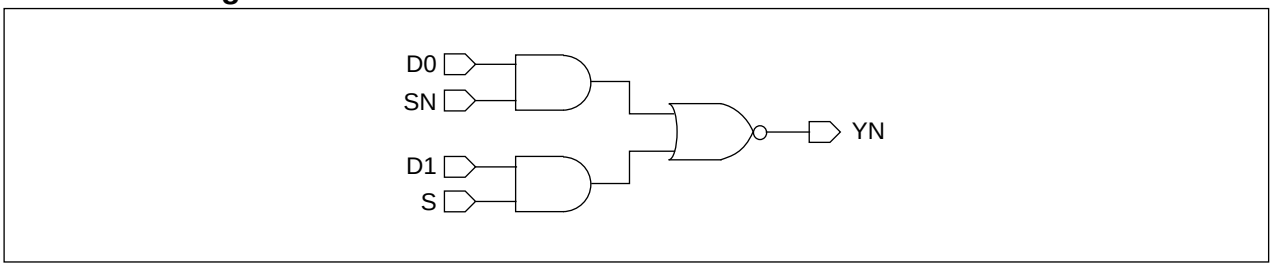
Truth Table

D0	D1	S	SN	YN
0	x	0	1	1
1	x	0	1	0
x	0	1	0	1
x	1	1	0	0

Cell Data

Input Load (SL)								Gate Count	
MX2IA				*MX2ID2A*				*MX2IA*	*MX2ID2A*
D0	D1	S	SN	D0	D1	S	SN		
0.6	0.9	0.9	0.6	0.7	0.7	0.7	0.6	1.7	3.3

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

MX2IA

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.23	0.13 + 0.051*SL	0.13 + 0.051*SL	0.12 + 0.051*SL
	t_{PHL}	0.25	0.14 + 0.054*SL	0.14 + 0.053*SL	0.14 + 0.053*SL
	t_R	0.46	0.24 + 0.105*SL	0.22 + 0.114*SL	0.18 + 0.117*SL
	t_F	0.38	0.18 + 0.104*SL	0.16 + 0.110*SL	0.13 + 0.114*SL
D1 to YN	t_{PLH}	0.33	0.22 + 0.052*SL	0.22 + 0.051*SL	0.22 + 0.051*SL
	t_{PHL}	0.36	0.25 + 0.055*SL	0.26 + 0.054*SL	0.26 + 0.053*SL
	t_R	0.49	0.27 + 0.110*SL	0.26 + 0.115*SL	0.24 + 0.117*SL
	t_F	0.57	0.35 + 0.108*SL	0.34 + 0.111*SL	0.32 + 0.113*SL
S to YN	t_{PLH}	0.28	0.17 + 0.053*SL	0.17 + 0.051*SL	0.17 + 0.051*SL
	t_{PHL}	0.34	0.23 + 0.055*SL	0.23 + 0.053*SL	0.24 + 0.053*SL
	t_R	0.45	0.23 + 0.109*SL	0.21 + 0.115*SL	0.19 + 0.117*SL
	t_F	0.57	0.36 + 0.105*SL	0.34 + 0.110*SL	0.31 + 0.114*SL
SN to YN	t_{PLH}	0.28	0.17 + 0.053*SL	0.17 + 0.051*SL	0.17 + 0.051*SL
	t_{PHL}	0.34	0.23 + 0.055*SL	0.23 + 0.053*SL	0.24 + 0.053*SL
	t_R	0.45	0.23 + 0.109*SL	0.21 + 0.115*SL	0.19 + 0.117*SL
	t_F	0.57	0.36 + 0.105*SL	0.34 + 0.110*SL	0.31 + 0.114*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

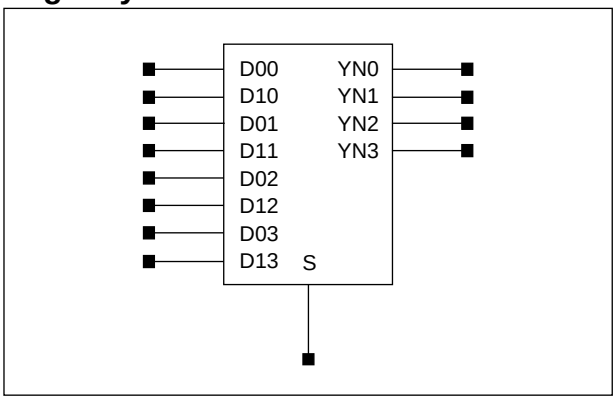
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

MX2ID2A

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.46	0.42 + 0.017*SL	0.43 + 0.014*SL	0.44 + 0.013*SL
	t_{PHL}	0.46	0.41 + 0.022*SL	0.42 + 0.018*SL	0.44 + 0.017*SL
	t_R	0.15	0.10 + 0.024*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.031*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
D1 to YN	t_{PLH}	0.46	0.42 + 0.017*SL	0.43 + 0.014*SL	0.44 + 0.013*SL
	t_{PHL}	0.46	0.41 + 0.022*SL	0.42 + 0.018*SL	0.44 + 0.017*SL
	t_R	0.15	0.10 + 0.025*SL	0.10 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.030*SL	0.10 + 0.031*SL	0.09 + 0.032*SL
S to YN	t_{PLH}	0.39	0.35 + 0.016*SL	0.36 + 0.014*SL	0.37 + 0.013*SL
	t_{PHL}	0.41	0.36 + 0.022*SL	0.37 + 0.018*SL	0.39 + 0.017*SL
	t_R	0.15	0.10 + 0.025*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.033*SL	0.10 + 0.030*SL	0.09 + 0.032*SL
SN to YN	t_{PLH}	0.39	0.35 + 0.016*SL	0.36 + 0.014*SL	0.37 + 0.013*SL
	t_{PHL}	0.41	0.36 + 0.022*SL	0.37 + 0.018*SL	0.39 + 0.017*SL
	t_R	0.15	0.10 + 0.025*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.033*SL	0.10 + 0.030*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Truth Table

S	YN0	YN1	YN2	YN3
0	$\overline{D00}$	$\overline{D01}$	$\overline{D02}$	$\overline{D03}$
1	$\overline{D10}$	$\overline{D11}$	$\overline{D12}$	$\overline{D13}$

Cell Data

Input Load (SL)									Gate Count
MX2IX4									*MX2IX4*
D00	D10	D01	D11	D02	D12	D03	D13	S	
1.0	0.9	1.0	0.9	1.0	0.9	1.0	0.9	4.2	7.3

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D00 to YN0	t_{PLH}	0.21	0.13 + 0.040*SL	0.14 + 0.038*SL	0.13 + 0.039*SL
	t_{PHL}	0.23	0.12 + 0.055*SL	0.12 + 0.053*SL	0.12 + 0.053*SL
	t_R	0.37	0.22 + 0.074*SL	0.20 + 0.083*SL	0.15 + 0.088*SL
	t_F	0.38	0.17 + 0.106*SL	0.15 + 0.112*SL	0.13 + 0.114*SL
D10 to YN0	t_{PLH}	0.26	0.18 + 0.041*SL	0.19 + 0.039*SL	0.19 + 0.039*SL
	t_{PHL}	0.36	0.25 + 0.055*SL	0.26 + 0.054*SL	0.26 + 0.053*SL
	t_R	0.42	0.26 + 0.080*SL	0.25 + 0.085*SL	0.22 + 0.088*SL
	t_F	0.57	0.35 + 0.108*SL	0.35 + 0.111*SL	0.32 + 0.113*SL
S to YN0	t_{PLH}	0.42	0.32 + 0.053*SL	0.32 + 0.051*SL	0.32 + 0.051*SL
	t_{PHL}	0.56	0.44 + 0.060*SL	0.46 + 0.054*SL	0.47 + 0.053*SL
	t_R	0.48	0.26 + 0.112*SL	0.25 + 0.115*SL	0.22 + 0.117*SL
	t_F	0.42	0.20 + 0.109*SL	0.20 + 0.109*SL	0.16 + 0.113*SL
D01 to YN1	t_{PLH}	0.21	0.13 + 0.040*SL	0.14 + 0.038*SL	0.13 + 0.039*SL
	t_{PHL}	0.23	0.12 + 0.055*SL	0.12 + 0.053*SL	0.12 + 0.053*SL
	t_R	0.37	0.22 + 0.074*SL	0.20 + 0.083*SL	0.15 + 0.088*SL
	t_F	0.38	0.17 + 0.106*SL	0.15 + 0.112*SL	0.13 + 0.114*SL
D11 to YN1	t_{PLH}	0.27	0.18 + 0.040*SL	0.19 + 0.039*SL	0.19 + 0.039*SL
	t_{PHL}	0.36	0.25 + 0.056*SL	0.26 + 0.054*SL	0.26 + 0.053*SL
	t_R	0.42	0.26 + 0.080*SL	0.25 + 0.085*SL	0.22 + 0.088*SL
	t_F	0.57	0.35 + 0.108*SL	0.35 + 0.111*SL	0.32 + 0.113*SL
S to YN1	t_{PLH}	0.42	0.32 + 0.053*SL	0.32 + 0.051*SL	0.32 + 0.051*SL
	t_{PHL}	0.56	0.44 + 0.060*SL	0.46 + 0.054*SL	0.47 + 0.053*SL
	t_R	0.48	0.26 + 0.112*SL	0.25 + 0.115*SL	0.23 + 0.117*SL
	t_F	0.42	0.20 + 0.109*SL	0.20 + 0.109*SL	0.16 + 0.113*SL
D02 to YN2	t_{PLH}	0.21	0.13 + 0.040*SL	0.14 + 0.038*SL	0.13 + 0.039*SL
	t_{PHL}	0.23	0.12 + 0.054*SL	0.12 + 0.053*SL	0.12 + 0.053*SL
	t_R	0.37	0.22 + 0.074*SL	0.20 + 0.083*SL	0.15 + 0.088*SL
	t_F	0.38	0.17 + 0.106*SL	0.15 + 0.112*SL	0.13 + 0.114*SL
D12 to YN2	t_{PLH}	0.27	0.18 + 0.040*SL	0.19 + 0.039*SL	0.19 + 0.039*SL
	t_{PHL}	0.36	0.25 + 0.056*SL	0.26 + 0.054*SL	0.26 + 0.053*SL
	t_R	0.42	0.26 + 0.080*SL	0.25 + 0.085*SL	0.22 + 0.088*SL
	t_F	0.57	0.35 + 0.108*SL	0.35 + 0.111*SL	0.32 + 0.113*SL
S to YN2	t_{PLH}	0.42	0.32 + 0.053*SL	0.32 + 0.051*SL	0.32 + 0.051*SL
	t_{PHL}	0.56	0.44 + 0.060*SL	0.46 + 0.054*SL	0.47 + 0.053*SL
	t_R	0.48	0.26 + 0.112*SL	0.25 + 0.115*SL	0.23 + 0.117*SL
	t_F	0.42	0.20 + 0.109*SL	0.20 + 0.109*SL	0.16 + 0.113*SL
D03 to YN3	t_{PLH}	0.21	0.13 + 0.040*SL	0.14 + 0.038*SL	0.13 + 0.039*SL
	t_{PHL}	0.23	0.12 + 0.055*SL	0.12 + 0.053*SL	0.12 + 0.053*SL
	t_R	0.37	0.22 + 0.074*SL	0.20 + 0.083*SL	0.15 + 0.088*SL
	t_F	0.38	0.17 + 0.106*SL	0.15 + 0.112*SL	0.13 + 0.114*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

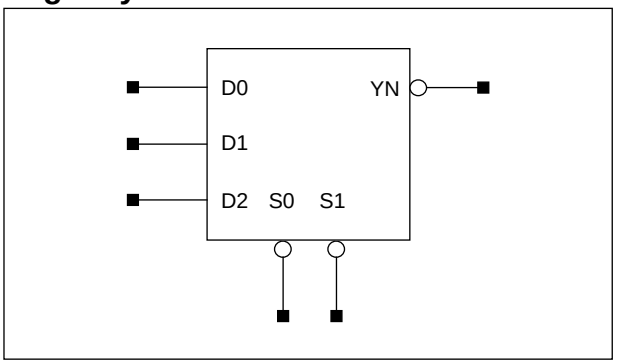
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D13 to YN3	t_{PLH}	0.26	0.18 + 0.041*SL	0.19 + 0.039*SL	0.19 + 0.039*SL
	t_{PHL}	0.36	0.25 + 0.055*SL	0.26 + 0.054*SL	0.26 + 0.053*SL
	t_R	0.42	0.26 + 0.080*SL	0.25 + 0.085*SL	0.22 + 0.088*SL
	t_F	0.57	0.35 + 0.108*SL	0.35 + 0.111*SL	0.32 + 0.113*SL
S to YN3	t_{PLH}	0.42	0.32 + 0.053*SL	0.32 + 0.051*SL	0.32 + 0.051*SL
	t_{PHL}	0.56	0.44 + 0.060*SL	0.46 + 0.054*SL	0.47 + 0.053*SL
	t_R	0.48	0.26 + 0.112*SL	0.25 + 0.115*SL	0.22 + 0.117*SL
	t_F	0.42	0.20 + 0.109*SL	0.20 + 0.109*SL	0.16 + 0.113*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

MX3I/MX3ID2

3 > 1 Inverting MUX with 1X/2X Drive

Logic Symbol



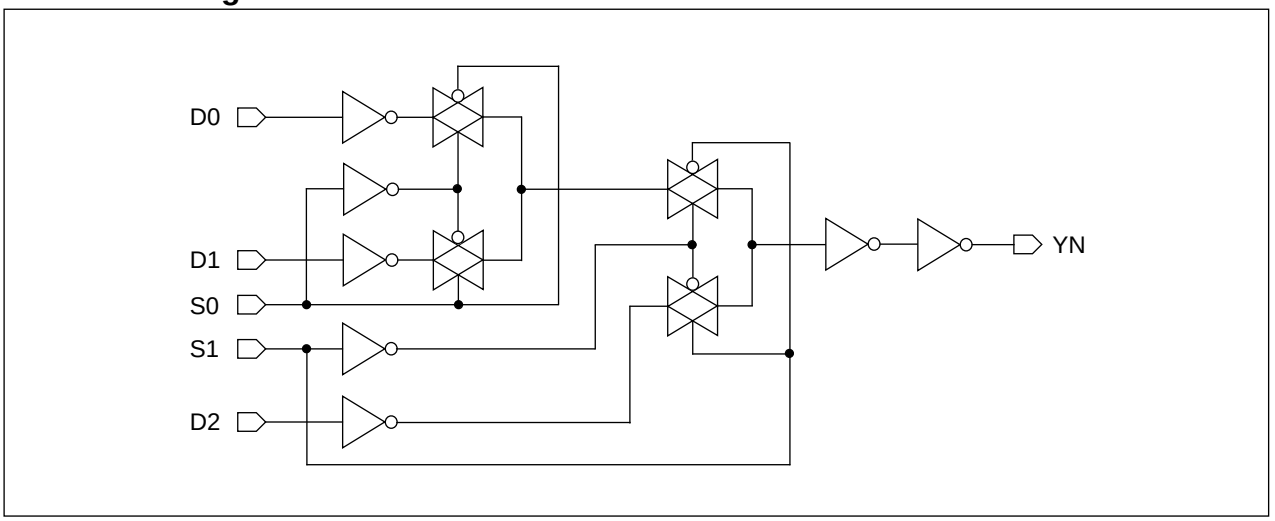
Truth Table

S0	S1	YN
0	0	$\overline{D0}$
1	0	$\overline{D1}$
x	1	$\overline{D2}$

Cell Data

Input Load (SL)										Gate Count	
MX3I					*MX3ID2*					*MX3I*	*MX3ID2*
D0	D1	D2	S0	S1	D0	D1	D2	S0	S1		
0.7	0.7	0.7	1.3	1.3	0.7	0.7	0.7	1.3	1.3	5.3	5.7

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

MX3I

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.59	0.53 + 0.029*SL	0.54 + 0.027*SL	0.54 + 0.027*SL
	t_{PHL}	0.60	0.53 + 0.037*SL	0.54 + 0.034*SL	0.55 + 0.033*SL
	t_R	0.22	0.11 + 0.054*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.22	0.10 + 0.061*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
D1 to YN	t_{PLH}	0.60	0.54 + 0.030*SL	0.54 + 0.027*SL	0.55 + 0.027*SL
	t_{PHL}	0.60	0.53 + 0.037*SL	0.54 + 0.034*SL	0.54 + 0.033*SL
	t_R	0.22	0.11 + 0.054*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.22	0.10 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL
D2 to YN	t_{PLH}	0.45	0.39 + 0.028*SL	0.40 + 0.027*SL	0.40 + 0.027*SL
	t_{PHL}	0.44	0.37 + 0.035*SL	0.38 + 0.033*SL	0.38 + 0.033*SL
	t_R	0.21	0.10 + 0.054*SL	0.08 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.066*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
S0 to YN	t_{PLH}	0.56	0.50 + 0.029*SL	0.51 + 0.027*SL	0.51 + 0.027*SL
	t_{PHL}	0.65	0.58 + 0.037*SL	0.59 + 0.034*SL	0.59 + 0.033*SL
	t_R	0.21	0.11 + 0.054*SL	0.10 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.063*SL	0.09 + 0.063*SL	0.07 + 0.066*SL
S1 to YN	t_{PLH}	0.43	0.38 + 0.029*SL	0.38 + 0.027*SL	0.38 + 0.027*SL
	t_{PHL}	0.54	0.47 + 0.037*SL	0.47 + 0.034*SL	0.48 + 0.033*SL
	t_R	0.21	0.10 + 0.055*SL	0.09 + 0.058*SL	0.07 + 0.060*SL
	t_F	0.22	0.09 + 0.062*SL	0.09 + 0.064*SL	0.07 + 0.066*SL

MX3ID2

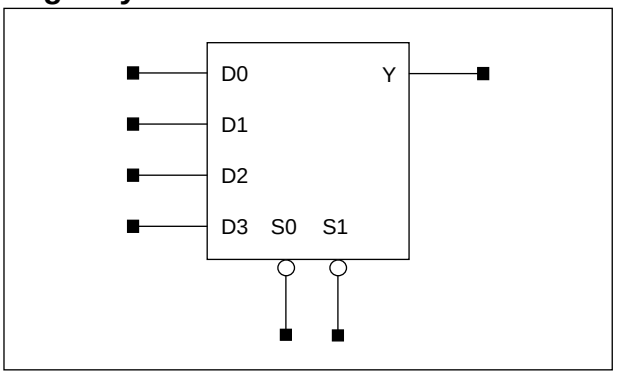
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to YN	t_{PLH}	0.61	0.58 + 0.017*SL	0.59 + 0.014*SL	0.60 + 0.013*SL
	t_{PHL}	0.62	0.57 + 0.022*SL	0.58 + 0.018*SL	0.60 + 0.017*SL
	t_R	0.17	0.12 + 0.023*SL	0.11 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.17	0.10 + 0.031*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D1 to YN	t_{PLH}	0.62	0.58 + 0.017*SL	0.59 + 0.014*SL	0.60 + 0.013*SL
	t_{PHL}	0.62	0.57 + 0.022*SL	0.58 + 0.018*SL	0.60 + 0.017*SL
	t_R	0.17	0.12 + 0.023*SL	0.11 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.17	0.10 + 0.031*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
D2 to YN	t_{PLH}	0.46	0.43 + 0.016*SL	0.43 + 0.014*SL	0.44 + 0.013*SL
	t_{PHL}	0.45	0.41 + 0.022*SL	0.42 + 0.018*SL	0.44 + 0.017*SL
	t_R	0.15	0.10 + 0.025*SL	0.09 + 0.027*SL	0.07 + 0.029*SL
	t_F	0.16	0.10 + 0.029*SL	0.10 + 0.031*SL	0.08 + 0.032*SL
S0 to YN	t_{PLH}	0.58	0.55 + 0.017*SL	0.56 + 0.014*SL	0.57 + 0.013*SL
	t_{PHL}	0.67	0.62 + 0.022*SL	0.63 + 0.018*SL	0.65 + 0.017*SL
	t_R	0.17	0.12 + 0.023*SL	0.11 + 0.026*SL	0.09 + 0.029*SL
	t_F	0.17	0.10 + 0.031*SL	0.11 + 0.031*SL	0.09 + 0.032*SL
S1 to YN	t_{PLH}	0.45	0.41 + 0.017*SL	0.42 + 0.014*SL	0.43 + 0.013*SL
	t_{PHL}	0.55	0.51 + 0.022*SL	0.52 + 0.018*SL	0.54 + 0.017*SL
	t_R	0.15	0.11 + 0.025*SL	0.10 + 0.027*SL	0.08 + 0.029*SL
	t_F	0.17	0.10 + 0.030*SL	0.10 + 0.031*SL	0.09 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

MX4/MX4D2

4 > 1 Non-Inverting MUX with 1X/2X Drive

Logic Symbol



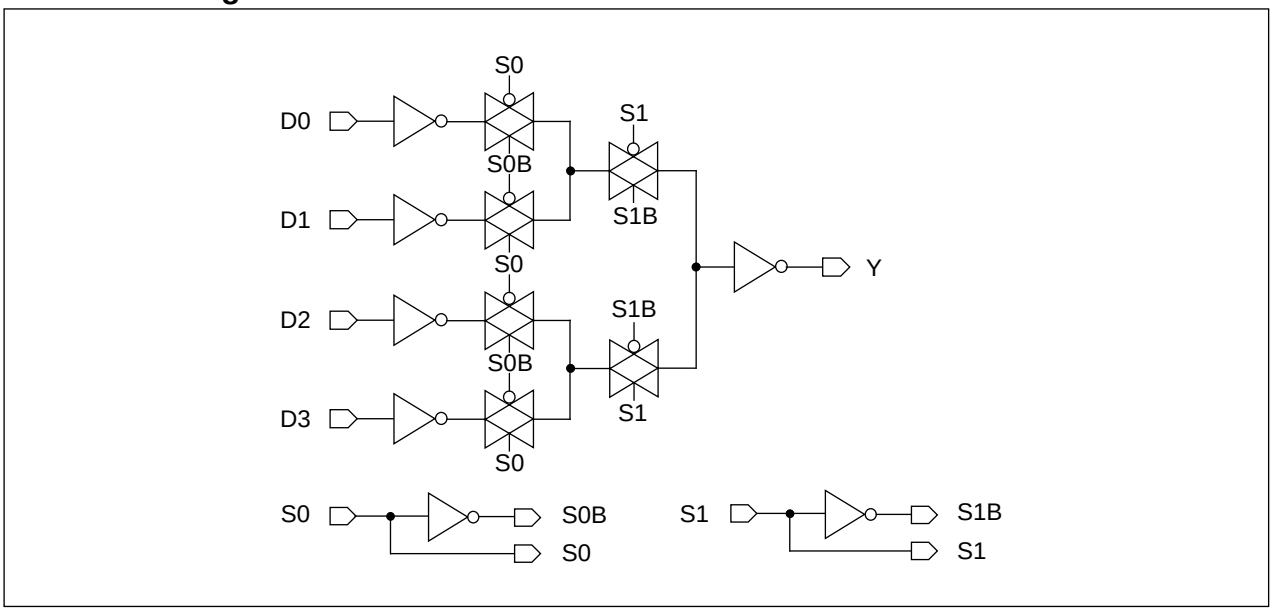
Truth Table

S0	S1	Y
0	0	D0
1	0	D1
0	1	D2
1	1	D3

Cell Data

Input Load (SL)												Gate Count	
MX4						*MX4D2*						*MX4*	*MX4D2*
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1		
0.7	0.6	0.7	0.7	1.8	1.5	0.7	0.6	0.7	0.7	2.0	1.5	6.3	6.7

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

MX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.47	0.39 + 0.037*SL	0.41 + 0.030*SL	0.44 + 0.027*SL
	t_{PHL}	0.60	0.50 + 0.053*SL	0.53 + 0.041*SL	0.60 + 0.034*SL
	t_R	0.28	0.16 + 0.057*SL	0.16 + 0.057*SL	0.14 + 0.059*SL
	t_F	0.35	0.22 + 0.068*SL	0.23 + 0.064*SL	0.23 + 0.064*SL
D1 to Y	t_{PLH}	0.47	0.39 + 0.037*SL	0.41 + 0.030*SL	0.44 + 0.027*SL
	t_{PHL}	0.60	0.50 + 0.053*SL	0.53 + 0.041*SL	0.60 + 0.034*SL
	t_R	0.28	0.17 + 0.056*SL	0.16 + 0.057*SL	0.14 + 0.059*SL
	t_F	0.36	0.22 + 0.066*SL	0.23 + 0.064*SL	0.23 + 0.064*SL
D2 to Y	t_{PLH}	0.46	0.39 + 0.037*SL	0.41 + 0.030*SL	0.44 + 0.027*SL
	t_{PHL}	0.60	0.50 + 0.052*SL	0.53 + 0.041*SL	0.60 + 0.034*SL
	t_R	0.28	0.17 + 0.055*SL	0.16 + 0.057*SL	0.14 + 0.059*SL
	t_F	0.35	0.22 + 0.068*SL	0.23 + 0.064*SL	0.23 + 0.064*SL
D3 to Y	t_{PLH}	0.46	0.39 + 0.037*SL	0.41 + 0.030*SL	0.44 + 0.027*SL
	t_{PHL}	0.60	0.50 + 0.053*SL	0.53 + 0.041*SL	0.60 + 0.034*SL
	t_R	0.28	0.17 + 0.056*SL	0.16 + 0.057*SL	0.14 + 0.059*SL
	t_F	0.36	0.22 + 0.068*SL	0.23 + 0.064*SL	0.23 + 0.064*SL
S0 to Y	t_{PLH}	0.55	0.47 + 0.037*SL	0.49 + 0.030*SL	0.53 + 0.027*SL
	t_{PHL}	0.61	0.50 + 0.052*SL	0.53 + 0.041*SL	0.60 + 0.034*SL
	t_R	0.28	0.17 + 0.055*SL	0.17 + 0.057*SL	0.14 + 0.059*SL
	t_F	0.35	0.22 + 0.067*SL	0.23 + 0.064*SL	0.23 + 0.064*SL
S1 to Y	t_{PLH}	0.40	0.33 + 0.037*SL	0.34 + 0.030*SL	0.38 + 0.027*SL
	t_{PHL}	0.42	0.32 + 0.050*SL	0.35 + 0.040*SL	0.41 + 0.034*SL
	t_R	0.26	0.15 + 0.058*SL	0.15 + 0.058*SL	0.13 + 0.059*SL
	t_F	0.30	0.15 + 0.072*SL	0.17 + 0.067*SL	0.19 + 0.064*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

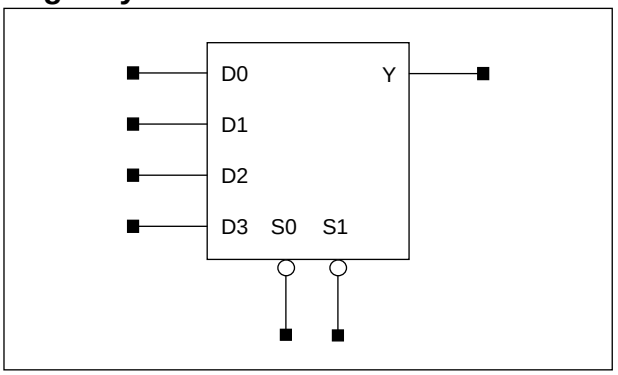
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

MX4D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.48	0.43 + 0.024*SL	0.45 + 0.018*SL	0.49 + 0.014*SL
	t_{PHL}	0.61	0.55 + 0.033*SL	0.57 + 0.025*SL	0.64 + 0.018*SL
	t_R	0.24	0.19 + 0.026*SL	0.19 + 0.027*SL	0.18 + 0.028*SL
	t_F	0.33	0.25 + 0.038*SL	0.27 + 0.032*SL	0.28 + 0.031*SL
D1 to Y	t_{PLH}	0.48	0.43 + 0.024*SL	0.45 + 0.018*SL	0.48 + 0.014*SL
	t_{PHL}	0.62	0.55 + 0.033*SL	0.57 + 0.025*SL	0.64 + 0.018*SL
	t_R	0.24	0.19 + 0.027*SL	0.18 + 0.027*SL	0.18 + 0.028*SL
	t_F	0.33	0.25 + 0.038*SL	0.27 + 0.033*SL	0.28 + 0.031*SL
D2 to Y	t_{PLH}	0.47	0.42 + 0.024*SL	0.44 + 0.018*SL	0.48 + 0.014*SL
	t_{PHL}	0.61	0.54 + 0.033*SL	0.57 + 0.026*SL	0.63 + 0.018*SL
	t_R	0.24	0.19 + 0.027*SL	0.19 + 0.027*SL	0.18 + 0.028*SL
	t_F	0.32	0.25 + 0.038*SL	0.26 + 0.033*SL	0.27 + 0.031*SL
D3 to Y	t_{PLH}	0.47	0.42 + 0.024*SL	0.44 + 0.018*SL	0.48 + 0.014*SL
	t_{PHL}	0.61	0.55 + 0.033*SL	0.57 + 0.025*SL	0.64 + 0.018*SL
	t_R	0.24	0.19 + 0.027*SL	0.18 + 0.027*SL	0.18 + 0.028*SL
	t_F	0.33	0.25 + 0.038*SL	0.27 + 0.033*SL	0.28 + 0.031*SL
S0 to Y	t_{PLH}	0.56	0.51 + 0.024*SL	0.53 + 0.018*SL	0.57 + 0.014*SL
	t_{PHL}	0.62	0.55 + 0.033*SL	0.58 + 0.025*SL	0.64 + 0.018*SL
	t_R	0.25	0.20 + 0.026*SL	0.19 + 0.027*SL	0.18 + 0.028*SL
	t_F	0.33	0.25 + 0.036*SL	0.26 + 0.033*SL	0.28 + 0.031*SL
S1 to Y	t_{PLH}	0.41	0.36 + 0.024*SL	0.38 + 0.018*SL	0.41 + 0.014*SL
	t_{PHL}	0.44	0.37 + 0.033*SL	0.39 + 0.025*SL	0.46 + 0.018*SL
	t_R	0.23	0.17 + 0.028*SL	0.17 + 0.028*SL	0.17 + 0.028*SL
	t_F	0.28	0.20 + 0.040*SL	0.21 + 0.034*SL	0.24 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



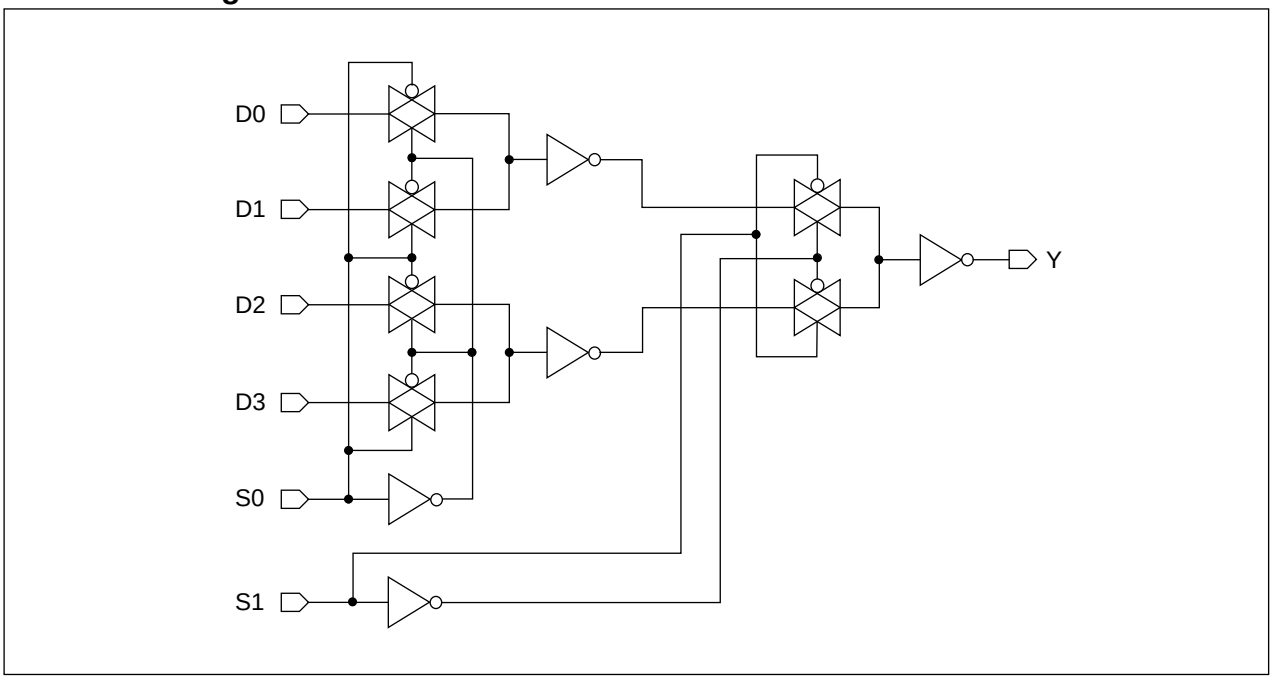
Truth Table

S0	S1	Y
0	0	D0
1	0	D1
0	1	D2
1	1	D3

Cell Data

Input Load (SL)												Gate Count	
YMX4						*YMX4D2*						*YMX4*	*YMX4D2*
D0	D1	D2	D3	S0	S1	D0	D1	D2	D3	S0	S1		
2.0	2.0	2.0	2.0	1.5	1.2	2.0	2.0	2.0	2.0	1.5	1.2	5.7	6.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

YMX4

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.39	0.32 + 0.033*SL	0.34 + 0.028*SL	0.35 + 0.027*SL
	t_{PHL}	0.50	0.41 + 0.045*SL	0.43 + 0.037*SL	0.47 + 0.033*SL
	t_R	0.23	0.12 + 0.056*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.29	0.16 + 0.065*SL	0.16 + 0.063*SL	0.14 + 0.065*SL
D1 to Y	t_{PLH}	0.39	0.33 + 0.033*SL	0.34 + 0.028*SL	0.35 + 0.027*SL
	t_{PHL}	0.50	0.41 + 0.045*SL	0.43 + 0.037*SL	0.47 + 0.033*SL
	t_R	0.23	0.12 + 0.056*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.29	0.16 + 0.065*SL	0.16 + 0.063*SL	0.14 + 0.065*SL
D2 to Y	t_{PLH}	0.38	0.32 + 0.033*SL	0.33 + 0.028*SL	0.34 + 0.027*SL
	t_{PHL}	0.50	0.41 + 0.045*SL	0.43 + 0.037*SL	0.47 + 0.033*SL
	t_R	0.23	0.13 + 0.054*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.29	0.16 + 0.064*SL	0.16 + 0.063*SL	0.14 + 0.065*SL
D3 to Y	t_{PLH}	0.39	0.32 + 0.033*SL	0.34 + 0.028*SL	0.35 + 0.027*SL
	t_{PHL}	0.50	0.41 + 0.045*SL	0.43 + 0.037*SL	0.47 + 0.033*SL
	t_R	0.23	0.13 + 0.054*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.29	0.16 + 0.065*SL	0.16 + 0.063*SL	0.14 + 0.065*SL
S0 to Y	t_{PLH}	0.54	0.47 + 0.033*SL	0.48 + 0.028*SL	0.49 + 0.027*SL
	t_{PHL}	0.68	0.59 + 0.045*SL	0.62 + 0.037*SL	0.66 + 0.033*SL
	t_R	0.23	0.12 + 0.056*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.28	0.15 + 0.066*SL	0.16 + 0.063*SL	0.14 + 0.065*SL
S1 to Y	t_{PLH}	0.35	0.29 + 0.032*SL	0.30 + 0.028*SL	0.31 + 0.027*SL
	t_{PHL}	0.41	0.32 + 0.044*SL	0.34 + 0.037*SL	0.38 + 0.033*SL
	t_R	0.23	0.11 + 0.057*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.068*SL	0.15 + 0.063*SL	0.14 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

YMX4D2

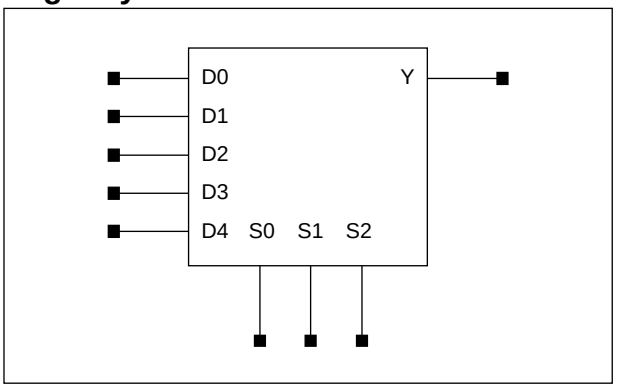
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.40	0.36 + 0.020*SL	0.37 + 0.016*SL	0.39 + 0.013*SL
	t_{PHL}	0.51	0.45 + 0.029*SL	0.47 + 0.023*SL	0.52 + 0.017*SL
	t_R	0.18	0.13 + 0.025*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.25	0.18 + 0.034*SL	0.18 + 0.032*SL	0.19 + 0.032*SL
D1 to Y	t_{PLH}	0.40	0.36 + 0.019*SL	0.37 + 0.016*SL	0.39 + 0.013*SL
	t_{PHL}	0.51	0.45 + 0.029*SL	0.47 + 0.023*SL	0.52 + 0.017*SL
	t_R	0.18	0.13 + 0.028*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.25	0.18 + 0.036*SL	0.19 + 0.032*SL	0.19 + 0.032*SL
D2 to Y	t_{PLH}	0.39	0.35 + 0.019*SL	0.36 + 0.016*SL	0.38 + 0.013*SL
	t_{PHL}	0.51	0.45 + 0.029*SL	0.47 + 0.023*SL	0.52 + 0.017*SL
	t_R	0.18	0.13 + 0.026*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.25	0.18 + 0.034*SL	0.19 + 0.032*SL	0.19 + 0.032*SL
D3 to Y	t_{PLH}	0.39	0.35 + 0.020*SL	0.37 + 0.016*SL	0.39 + 0.013*SL
	t_{PHL}	0.51	0.45 + 0.029*SL	0.47 + 0.023*SL	0.52 + 0.017*SL
	t_R	0.18	0.13 + 0.027*SL	0.13 + 0.027*SL	0.11 + 0.028*SL
	t_F	0.25	0.18 + 0.035*SL	0.19 + 0.032*SL	0.19 + 0.032*SL
S0 to Y	t_{PLH}	0.54	0.50 + 0.019*SL	0.52 + 0.016*SL	0.54 + 0.013*SL
	t_{PHL}	0.69	0.63 + 0.029*SL	0.65 + 0.023*SL	0.70 + 0.017*SL
	t_R	0.18	0.13 + 0.026*SL	0.12 + 0.027*SL	0.11 + 0.029*SL
	t_F	0.25	0.18 + 0.035*SL	0.18 + 0.032*SL	0.19 + 0.032*SL
S1 to Y	t_{PLH}	0.36	0.32 + 0.019*SL	0.33 + 0.016*SL	0.35 + 0.013*SL
	t_{PHL}	0.42	0.36 + 0.028*SL	0.38 + 0.023*SL	0.43 + 0.017*SL
	t_R	0.18	0.12 + 0.027*SL	0.12 + 0.027*SL	0.11 + 0.029*SL
	t_F	0.23	0.16 + 0.037*SL	0.17 + 0.033*SL	0.18 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

MX5/MX5D2

5 > 1 Non-Inverting MUX with 1X/2X Drive

Logic Symbol



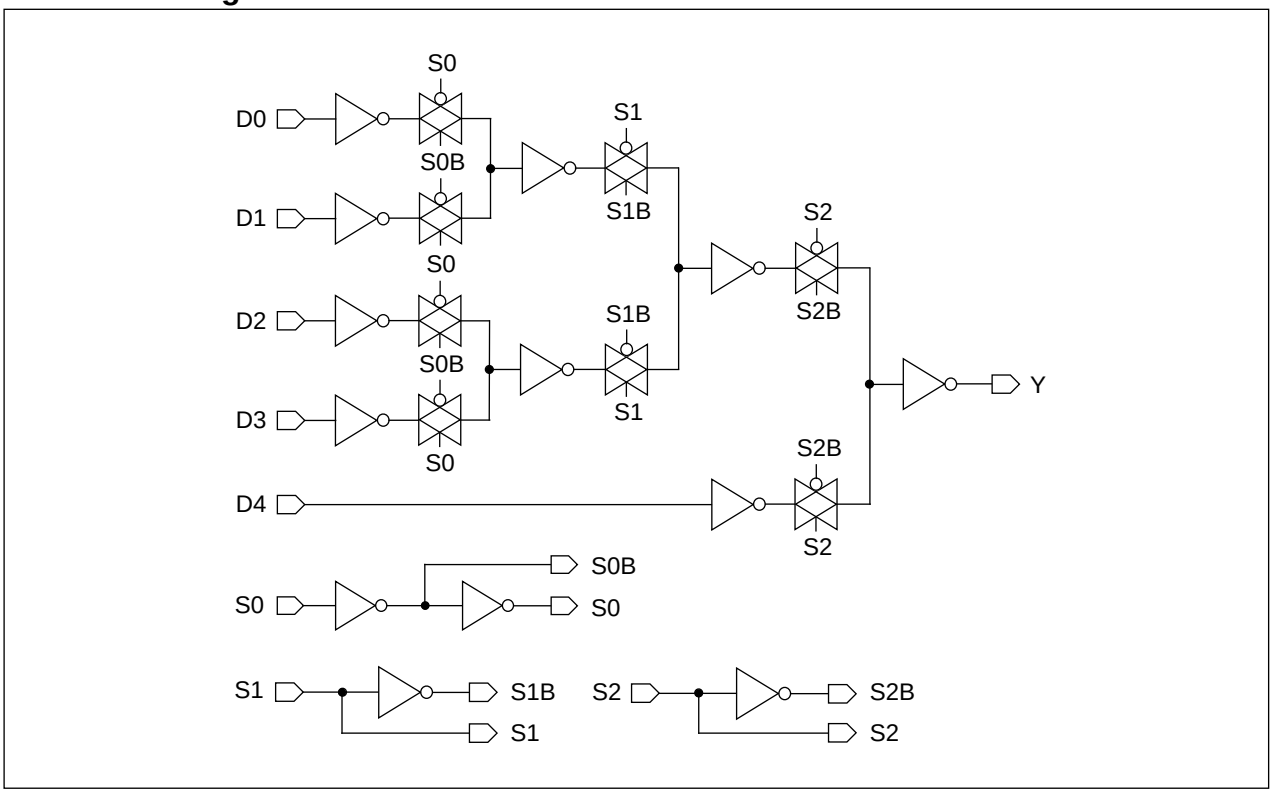
Truth Table

S0	S1	S2	Y
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
x	x	1	D4

Cell Data

Input Load (SL)								Gate Count
MX5								*MX5*
D0	D1	D2	D3	D4	S0	S1	S2	
0.7	0.7	0.7	0.7	0.7	0.8	1.4	1.3	9.3
MX5D2								*MX5D2*
D0	D1	D2	D3	D4	S0	S1	S2	
0.7	0.7	0.7	0.7	0.7	0.8	1.4	1.3	9.7

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

MX5

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.76	0.70 + 0.033*SL	0.71 + 0.028*SL	0.72 + 0.027*SL
	t_{PHL}	0.88	0.79 + 0.045*SL	0.82 + 0.037*SL	0.85 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.28	0.15 + 0.065*SL	0.16 + 0.062*SL	0.13 + 0.065*SL
D1 to Y	t_{PLH}	0.76	0.70 + 0.033*SL	0.71 + 0.028*SL	0.72 + 0.027*SL
	t_{PHL}	0.88	0.79 + 0.045*SL	0.82 + 0.037*SL	0.85 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.28	0.15 + 0.065*SL	0.16 + 0.062*SL	0.13 + 0.065*SL
D2 to Y	t_{PLH}	0.73	0.67 + 0.033*SL	0.68 + 0.028*SL	0.70 + 0.027*SL
	t_{PHL}	0.85	0.76 + 0.045*SL	0.78 + 0.037*SL	0.82 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.28	0.15 + 0.065*SL	0.15 + 0.063*SL	0.13 + 0.065*SL
D3 to Y	t_{PLH}	0.73	0.67 + 0.033*SL	0.68 + 0.028*SL	0.70 + 0.027*SL
	t_{PHL}	0.85	0.76 + 0.045*SL	0.78 + 0.037*SL	0.82 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.28	0.15 + 0.065*SL	0.15 + 0.063*SL	0.13 + 0.065*SL
D4 to Y	t_{PLH}	0.31	0.25 + 0.032*SL	0.26 + 0.028*SL	0.27 + 0.027*SL
	t_{PHL}	0.43	0.34 + 0.044*SL	0.36 + 0.036*SL	0.39 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.065*SL	0.15 + 0.063*SL	0.12 + 0.065*SL
S0 to Y	t_{PLH}	0.92	0.85 + 0.033*SL	0.86 + 0.028*SL	0.88 + 0.027*SL
	t_{PHL}	0.94	0.85 + 0.045*SL	0.87 + 0.037*SL	0.91 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.28	0.15 + 0.065*SL	0.15 + 0.063*SL	0.13 + 0.065*SL
S1 to Y	t_{PLH}	0.55	0.48 + 0.033*SL	0.49 + 0.028*SL	0.51 + 0.027*SL
	t_{PHL}	0.55	0.46 + 0.045*SL	0.48 + 0.037*SL	0.52 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.28	0.15 + 0.066*SL	0.16 + 0.062*SL	0.13 + 0.065*SL
S2 to Y	t_{PLH}	0.37	0.30 + 0.032*SL	0.31 + 0.028*SL	0.33 + 0.027*SL
	t_{PHL}	0.38	0.29 + 0.044*SL	0.31 + 0.036*SL	0.34 + 0.033*SL
	t_R	0.23	0.12 + 0.057*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.26	0.13 + 0.066*SL	0.14 + 0.063*SL	0.12 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

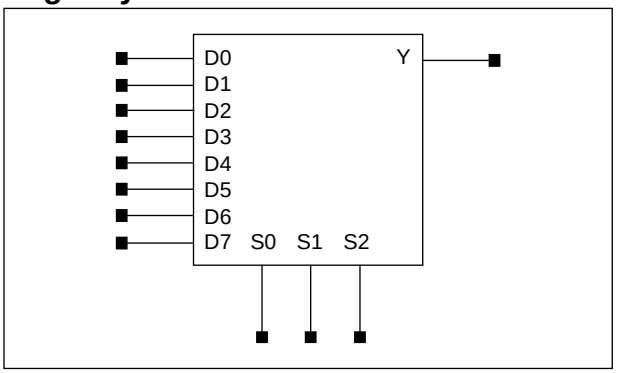
(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

MX5D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.77	0.73 + 0.020*SL	0.74 + 0.016*SL	0.77 + 0.013*SL
	t_{PHL}	0.89	0.83 + 0.028*SL	0.85 + 0.022*SL	0.90 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.23	0.17 + 0.033*SL	0.17 + 0.032*SL	0.17 + 0.032*SL
D1 to Y	t_{PLH}	0.77	0.73 + 0.020*SL	0.74 + 0.016*SL	0.77 + 0.013*SL
	t_{PHL}	0.89	0.83 + 0.028*SL	0.85 + 0.022*SL	0.90 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.23	0.17 + 0.033*SL	0.17 + 0.032*SL	0.17 + 0.032*SL
D2 to Y	t_{PLH}	0.74	0.70 + 0.020*SL	0.71 + 0.016*SL	0.74 + 0.013*SL
	t_{PHL}	0.86	0.80 + 0.028*SL	0.82 + 0.022*SL	0.86 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.23	0.17 + 0.033*SL	0.17 + 0.032*SL	0.17 + 0.032*SL
D3 to Y	t_{PLH}	0.74	0.70 + 0.020*SL	0.71 + 0.016*SL	0.74 + 0.013*SL
	t_{PHL}	0.86	0.80 + 0.028*SL	0.82 + 0.022*SL	0.86 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.23	0.17 + 0.033*SL	0.17 + 0.032*SL	0.17 + 0.032*SL
D4 to Y	t_{PLH}	0.32	0.28 + 0.019*SL	0.29 + 0.016*SL	0.31 + 0.013*SL
	t_{PHL}	0.44	0.38 + 0.027*SL	0.40 + 0.021*SL	0.44 + 0.017*SL
	t_R	0.18	0.13 + 0.027*SL	0.12 + 0.027*SL	0.11 + 0.028*SL
	t_F	0.22	0.16 + 0.033*SL	0.16 + 0.032*SL	0.16 + 0.032*SL
S0 to Y	t_{PLH}	0.92	0.88 + 0.020*SL	0.89 + 0.016*SL	0.92 + 0.013*SL
	t_{PHL}	0.95	0.89 + 0.028*SL	0.91 + 0.022*SL	0.95 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.23	0.17 + 0.034*SL	0.17 + 0.032*SL	0.17 + 0.032*SL
S1 to Y	t_{PLH}	0.55	0.51 + 0.020*SL	0.53 + 0.016*SL	0.55 + 0.013*SL
	t_{PHL}	0.56	0.50 + 0.027*SL	0.52 + 0.022*SL	0.56 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.24	0.17 + 0.034*SL	0.17 + 0.032*SL	0.17 + 0.032*SL
S2 to Y	t_{PLH}	0.37	0.33 + 0.020*SL	0.34 + 0.016*SL	0.36 + 0.013*SL
	t_{PHL}	0.38	0.32 + 0.027*SL	0.34 + 0.022*SL	0.38 + 0.017*SL
	t_R	0.18	0.13 + 0.026*SL	0.13 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.22	0.15 + 0.035*SL	0.16 + 0.032*SL	0.16 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



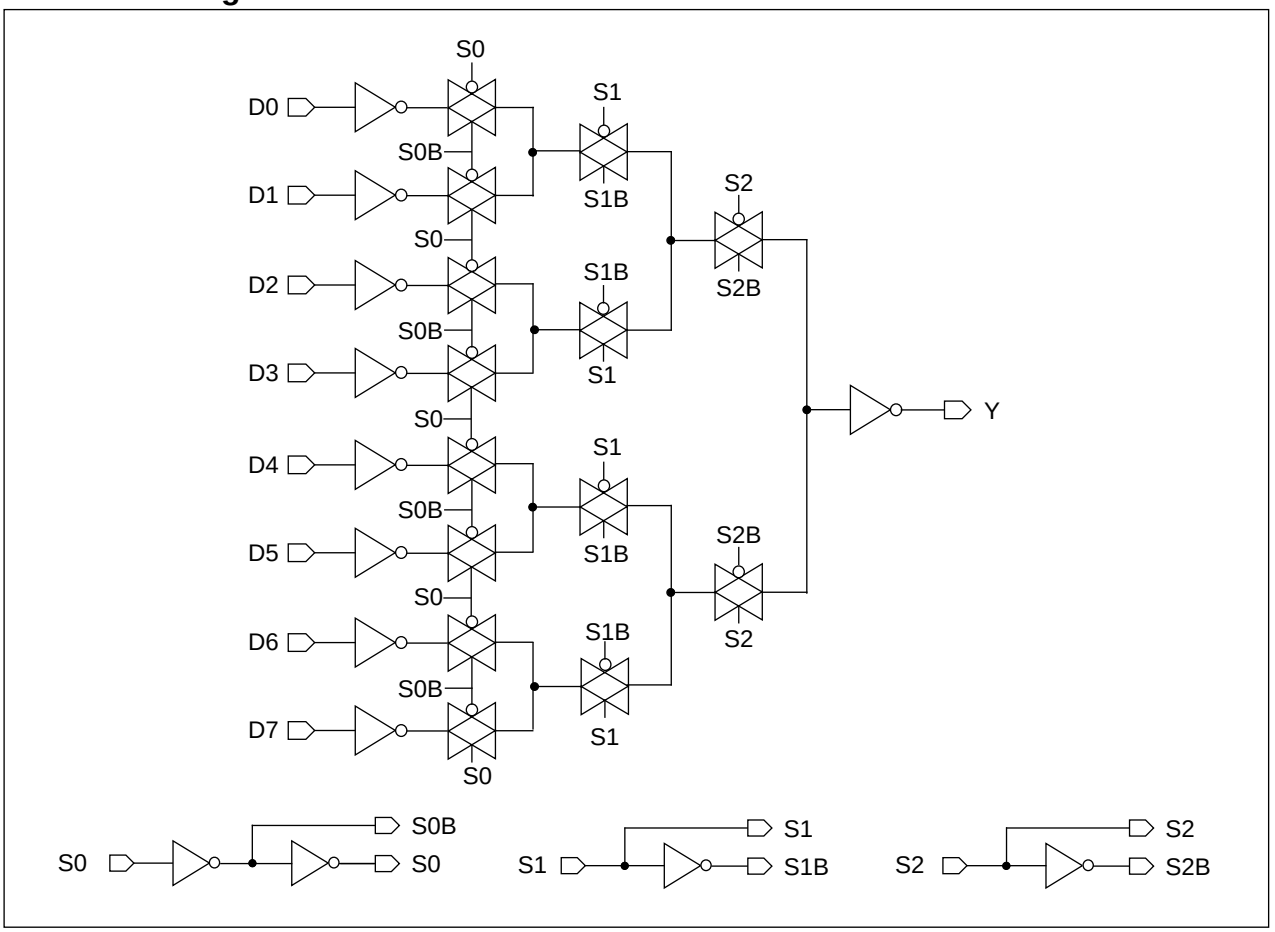
Truth Table

S0	S1	S2	Y
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D7

Cell Data

Input Load (SL)											Gate Count
MX8											*MX8*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	1.9	1.3	12.7
MX8D2											*MX8D2*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7	1.6	1.3	13.0

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

MX8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.69	0.61 + 0.044*SL	0.63 + 0.034*SL	0.70 + 0.028*SL
	t_{PHL}	0.85	0.72 + 0.063*SL	0.77 + 0.048*SL	0.89 + 0.036*SL
	t_R	0.36	0.24 + 0.058*SL	0.24 + 0.057*SL	0.23 + 0.058*SL
	t_F	0.49	0.33 + 0.076*SL	0.36 + 0.066*SL	0.39 + 0.063*SL
D1 to Y	t_{PLH}	0.70	0.61 + 0.044*SL	0.64 + 0.034*SL	0.70 + 0.028*SL
	t_{PHL}	0.85	0.73 + 0.062*SL	0.77 + 0.048*SL	0.89 + 0.036*SL
	t_R	0.36	0.24 + 0.057*SL	0.24 + 0.057*SL	0.23 + 0.058*SL
	t_F	0.48	0.33 + 0.075*SL	0.36 + 0.066*SL	0.39 + 0.063*SL
D2 to Y	t_{PLH}	0.68	0.59 + 0.044*SL	0.62 + 0.034*SL	0.68 + 0.028*SL
	t_{PHL}	0.83	0.71 + 0.062*SL	0.75 + 0.048*SL	0.87 + 0.035*SL
	t_R	0.35	0.24 + 0.056*SL	0.24 + 0.057*SL	0.22 + 0.058*SL
	t_F	0.48	0.33 + 0.074*SL	0.35 + 0.066*SL	0.38 + 0.063*SL
D3 to Y	t_{PLH}	0.68	0.59 + 0.044*SL	0.62 + 0.034*SL	0.68 + 0.028*SL
	t_{PHL}	0.83	0.71 + 0.062*SL	0.75 + 0.048*SL	0.87 + 0.035*SL
	t_R	0.35	0.24 + 0.056*SL	0.24 + 0.057*SL	0.22 + 0.058*SL
	t_F	0.48	0.33 + 0.074*SL	0.35 + 0.066*SL	0.38 + 0.063*SL
D4 to Y	t_{PLH}	0.69	0.60 + 0.044*SL	0.63 + 0.034*SL	0.69 + 0.028*SL
	t_{PHL}	0.84	0.72 + 0.062*SL	0.76 + 0.048*SL	0.88 + 0.036*SL
	t_R	0.35	0.24 + 0.057*SL	0.24 + 0.057*SL	0.23 + 0.058*SL
	t_F	0.48	0.34 + 0.074*SL	0.36 + 0.066*SL	0.39 + 0.063*SL
D5 to Y	t_{PLH}	0.69	0.60 + 0.044*SL	0.63 + 0.034*SL	0.69 + 0.028*SL
	t_{PHL}	0.84	0.72 + 0.062*SL	0.76 + 0.048*SL	0.88 + 0.036*SL
	t_R	0.35	0.24 + 0.057*SL	0.24 + 0.057*SL	0.23 + 0.058*SL
	t_F	0.48	0.34 + 0.074*SL	0.36 + 0.066*SL	0.39 + 0.063*SL
D6 to Y	t_{PLH}	0.68	0.59 + 0.044*SL	0.62 + 0.034*SL	0.68 + 0.028*SL
	t_{PHL}	0.84	0.71 + 0.062*SL	0.76 + 0.048*SL	0.87 + 0.035*SL
	t_R	0.35	0.24 + 0.056*SL	0.24 + 0.057*SL	0.23 + 0.058*SL
	t_F	0.48	0.33 + 0.075*SL	0.36 + 0.066*SL	0.38 + 0.063*SL
D7 to Y	t_{PLH}	0.68	0.59 + 0.044*SL	0.62 + 0.034*SL	0.68 + 0.028*SL
	t_{PHL}	0.84	0.71 + 0.062*SL	0.76 + 0.048*SL	0.87 + 0.035*SL
	t_R	0.35	0.24 + 0.056*SL	0.24 + 0.057*SL	0.23 + 0.058*SL
	t_F	0.48	0.33 + 0.075*SL	0.36 + 0.066*SL	0.38 + 0.063*SL
S0 to Y	t_{PLH}	1.00	0.92 + 0.044*SL	0.95 + 0.034*SL	1.01 + 0.028*SL
	t_{PHL}	1.09	0.96 + 0.062*SL	1.00 + 0.048*SL	1.12 + 0.035*SL
	t_R	0.36	0.25 + 0.057*SL	0.25 + 0.057*SL	0.23 + 0.058*SL
	t_F	0.49	0.34 + 0.074*SL	0.36 + 0.066*SL	0.39 + 0.063*SL
S1 to Y	t_{PLH}	0.64	0.55 + 0.044*SL	0.58 + 0.034*SL	0.64 + 0.028*SL
	t_{PHL}	0.68	0.55 + 0.062*SL	0.60 + 0.048*SL	0.71 + 0.036*SL
	t_R	0.35	0.23 + 0.058*SL	0.24 + 0.057*SL	0.23 + 0.058*SL
	t_F	0.47	0.32 + 0.076*SL	0.35 + 0.066*SL	0.38 + 0.063*SL
S2 to Y	t_{PLH}	0.42	0.33 + 0.041*SL	0.36 + 0.033*SL	0.41 + 0.028*SL
	t_{PHL}	0.42	0.31 + 0.057*SL	0.34 + 0.046*SL	0.44 + 0.035*SL
	t_R	0.29	0.16 + 0.062*SL	0.17 + 0.060*SL	0.19 + 0.059*SL
	t_F	0.35	0.19 + 0.081*SL	0.21 + 0.071*SL	0.28 + 0.064*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

MX8D2

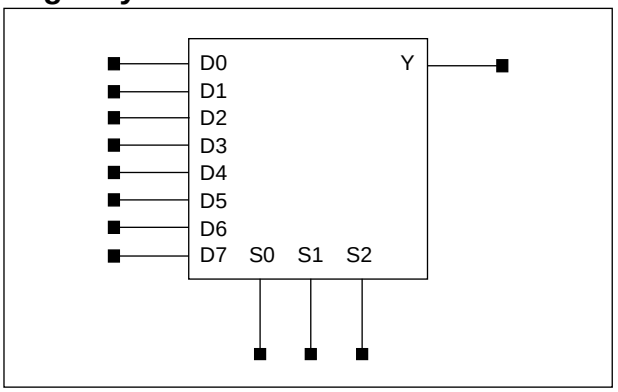
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.71	0.65 + 0.029*SL	0.68 + 0.021*SL	0.73 + 0.015*SL
	t_{PHL}	0.87	0.79 + 0.039*SL	0.82 + 0.030*SL	0.91 + 0.020*SL
	t_R	0.33	0.27 + 0.030*SL	0.28 + 0.027*SL	0.27 + 0.028*SL
	t_F	0.47	0.38 + 0.043*SL	0.40 + 0.035*SL	0.44 + 0.032*SL
D1 to Y	t_{PLH}	0.71	0.65 + 0.029*SL	0.68 + 0.021*SL	0.74 + 0.015*SL
	t_{PHL}	0.87	0.79 + 0.039*SL	0.82 + 0.030*SL	0.91 + 0.020*SL
	t_R	0.33	0.27 + 0.030*SL	0.28 + 0.027*SL	0.27 + 0.028*SL
	t_F	0.47	0.38 + 0.043*SL	0.40 + 0.035*SL	0.44 + 0.032*SL
D2 to Y	t_{PLH}	0.69	0.64 + 0.028*SL	0.66 + 0.021*SL	0.72 + 0.015*SL
	t_{PHL}	0.86	0.78 + 0.039*SL	0.81 + 0.030*SL	0.89 + 0.020*SL
	t_R	0.32	0.26 + 0.029*SL	0.27 + 0.027*SL	0.26 + 0.028*SL
	t_F	0.46	0.37 + 0.043*SL	0.39 + 0.035*SL	0.43 + 0.032*SL
D3 to Y	t_{PLH}	0.69	0.64 + 0.028*SL	0.66 + 0.021*SL	0.72 + 0.015*SL
	t_{PHL}	0.86	0.78 + 0.039*SL	0.80 + 0.030*SL	0.89 + 0.020*SL
	t_R	0.32	0.26 + 0.029*SL	0.27 + 0.027*SL	0.26 + 0.028*SL
	t_F	0.46	0.37 + 0.043*SL	0.39 + 0.035*SL	0.43 + 0.032*SL
D4 to Y	t_{PLH}	0.70	0.64 + 0.028*SL	0.66 + 0.021*SL	0.72 + 0.015*SL
	t_{PHL}	0.86	0.78 + 0.039*SL	0.81 + 0.030*SL	0.90 + 0.020*SL
	t_R	0.33	0.27 + 0.029*SL	0.27 + 0.027*SL	0.27 + 0.028*SL
	t_F	0.46	0.38 + 0.041*SL	0.40 + 0.035*SL	0.43 + 0.032*SL
D5 to Y	t_{PLH}	0.70	0.64 + 0.029*SL	0.66 + 0.021*SL	0.72 + 0.015*SL
	t_{PHL}	0.86	0.78 + 0.039*SL	0.81 + 0.030*SL	0.90 + 0.020*SL
	t_R	0.33	0.27 + 0.029*SL	0.27 + 0.027*SL	0.27 + 0.028*SL
	t_F	0.46	0.38 + 0.041*SL	0.40 + 0.036*SL	0.43 + 0.032*SL
D6 to Y	t_{PLH}	0.69	0.63 + 0.029*SL	0.66 + 0.021*SL	0.71 + 0.015*SL
	t_{PHL}	0.86	0.78 + 0.039*SL	0.81 + 0.030*SL	0.90 + 0.020*SL
	t_R	0.32	0.26 + 0.029*SL	0.27 + 0.027*SL	0.27 + 0.028*SL
	t_F	0.46	0.37 + 0.043*SL	0.40 + 0.035*SL	0.43 + 0.032*SL
D7 to Y	t_{PLH}	0.69	0.63 + 0.028*SL	0.66 + 0.021*SL	0.71 + 0.015*SL
	t_{PHL}	0.86	0.78 + 0.039*SL	0.81 + 0.030*SL	0.90 + 0.020*SL
	t_R	0.32	0.26 + 0.029*SL	0.27 + 0.027*SL	0.27 + 0.028*SL
	t_F	0.46	0.38 + 0.043*SL	0.40 + 0.035*SL	0.43 + 0.032*SL
S0 to Y	t_{PLH}	1.02	0.96 + 0.029*SL	0.98 + 0.021*SL	1.04 + 0.015*SL
	t_{PHL}	1.11	1.03 + 0.039*SL	1.05 + 0.030*SL	1.14 + 0.020*SL
	t_R	0.33	0.27 + 0.028*SL	0.27 + 0.027*SL	0.27 + 0.028*SL
	t_F	0.46	0.38 + 0.042*SL	0.40 + 0.035*SL	0.44 + 0.032*SL
S1 to Y	t_{PLH}	0.65	0.59 + 0.029*SL	0.61 + 0.021*SL	0.67 + 0.015*SL
	t_{PHL}	0.70	0.62 + 0.039*SL	0.64 + 0.030*SL	0.74 + 0.020*SL
	t_R	0.32	0.26 + 0.028*SL	0.27 + 0.027*SL	0.26 + 0.028*SL
	t_F	0.45	0.37 + 0.043*SL	0.39 + 0.035*SL	0.42 + 0.032*SL
S2 to Y	t_{PLH}	0.42	0.37 + 0.027*SL	0.39 + 0.021*SL	0.45 + 0.015*SL
	t_{PHL}	0.43	0.36 + 0.037*SL	0.38 + 0.030*SL	0.47 + 0.020*SL
	t_R	0.27	0.21 + 0.030*SL	0.21 + 0.029*SL	0.22 + 0.028*SL
	t_F	0.34	0.25 + 0.046*SL	0.27 + 0.039*SL	0.32 + 0.033*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

YMX8/YMX8D2

Fast 8 > 1 Non-Inverting MUX with 1X/2X Drive

Logic Symbol



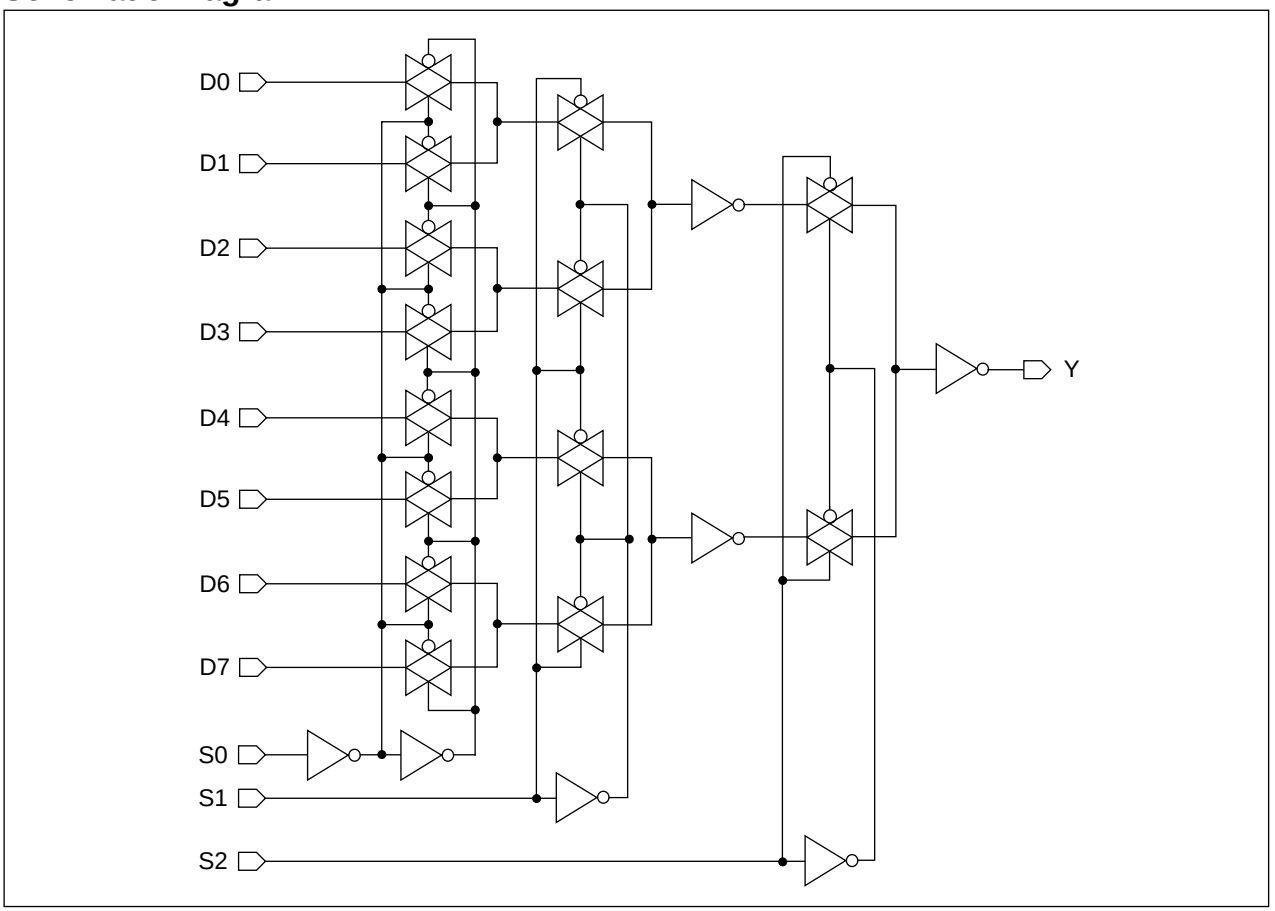
Truth Table

S0	S1	S2	Y
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D7

Cell Data

Input Load (SL)											Gate Count
YMX8/											*YMX8*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
3.4	3.4	3.3	3.3	3.4	3.4	3.2	3.2	0.6	1.7	1.2	11.0
YMX8D2											*YMX8D2*
D0	D1	D2	D3	D4	D5	D6	D7	S0	S1	S2	
3.4	3.4	3.3	3.3	3.4	3.4	3.2	3.2	0.6	1.7	1.2	11.3

Schematic Diagram



Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

YMX8

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.51	0.44 + 0.033*SL	0.46 + 0.028*SL	0.47 + 0.027*SL
	t_{PHL}	0.61	0.52 + 0.046*SL	0.54 + 0.038*SL	0.59 + 0.033*SL
	t_R	0.24	0.13 + 0.054*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.29	0.16 + 0.067*SL	0.17 + 0.063*SL	0.15 + 0.065*SL
D1 to Y	t_{PLH}	0.51	0.44 + 0.033*SL	0.46 + 0.028*SL	0.47 + 0.027*SL
	t_{PHL}	0.61	0.52 + 0.046*SL	0.55 + 0.037*SL	0.59 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.29	0.16 + 0.066*SL	0.17 + 0.063*SL	0.15 + 0.065*SL
D2 to Y	t_{PLH}	0.51	0.44 + 0.033*SL	0.46 + 0.028*SL	0.47 + 0.027*SL
	t_{PHL}	0.61	0.51 + 0.046*SL	0.54 + 0.038*SL	0.58 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.29	0.16 + 0.066*SL	0.17 + 0.063*SL	0.15 + 0.065*SL
D3 to Y	t_{PLH}	0.51	0.44 + 0.033*SL	0.46 + 0.028*SL	0.47 + 0.027*SL
	t_{PHL}	0.61	0.51 + 0.046*SL	0.54 + 0.037*SL	0.58 + 0.033*SL
	t_R	0.24	0.14 + 0.052*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.29	0.16 + 0.067*SL	0.17 + 0.062*SL	0.15 + 0.065*SL
D4 to Y	t_{PLH}	0.50	0.43 + 0.033*SL	0.44 + 0.028*SL	0.46 + 0.027*SL
	t_{PHL}	0.60	0.51 + 0.046*SL	0.54 + 0.037*SL	0.58 + 0.033*SL
	t_R	0.24	0.13 + 0.054*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.29	0.16 + 0.065*SL	0.16 + 0.063*SL	0.15 + 0.065*SL
D5 to Y	t_{PLH}	0.50	0.43 + 0.033*SL	0.44 + 0.028*SL	0.46 + 0.027*SL
	t_{PHL}	0.60	0.51 + 0.046*SL	0.53 + 0.037*SL	0.58 + 0.033*SL
	t_R	0.24	0.14 + 0.054*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.29	0.16 + 0.065*SL	0.16 + 0.063*SL	0.15 + 0.065*SL
D6 to Y	t_{PLH}	0.49	0.43 + 0.033*SL	0.44 + 0.028*SL	0.45 + 0.027*SL
	t_{PHL}	0.59	0.50 + 0.046*SL	0.53 + 0.037*SL	0.57 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.29	0.16 + 0.066*SL	0.16 + 0.063*SL	0.15 + 0.065*SL
D7 to Y	t_{PLH}	0.49	0.43 + 0.033*SL	0.44 + 0.028*SL	0.45 + 0.027*SL
	t_{PHL}	0.59	0.50 + 0.046*SL	0.53 + 0.037*SL	0.57 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.29	0.16 + 0.066*SL	0.16 + 0.063*SL	0.15 + 0.065*SL
S0 to Y	t_{PLH}	1.06	0.99 + 0.033*SL	1.01 + 0.028*SL	1.02 + 0.027*SL
	t_{PHL}	1.02	0.92 + 0.046*SL	0.95 + 0.037*SL	0.99 + 0.033*SL
	t_R	0.24	0.13 + 0.055*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.29	0.16 + 0.065*SL	0.16 + 0.063*SL	0.15 + 0.065*SL
S1 to Y	t_{PLH}	0.62	0.56 + 0.033*SL	0.57 + 0.028*SL	0.59 + 0.027*SL
	t_{PHL}	0.53	0.44 + 0.046*SL	0.46 + 0.037*SL	0.50 + 0.033*SL
	t_R	0.24	0.13 + 0.054*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.29	0.16 + 0.066*SL	0.17 + 0.063*SL	0.15 + 0.065*SL
S2 to Y	t_{PLH}	0.35	0.29 + 0.031*SL	0.30 + 0.028*SL	0.31 + 0.027*SL
	t_{PHL}	0.38	0.29 + 0.045*SL	0.31 + 0.037*SL	0.35 + 0.033*SL
	t_R	0.22	0.11 + 0.057*SL	0.11 + 0.058*SL	0.09 + 0.060*SL
	t_F	0.27	0.14 + 0.067*SL	0.15 + 0.064*SL	0.14 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

YMX8D2

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
D0 to Y	t_{PLH}	0.52	0.48 + 0.020*SL	0.50 + 0.016*SL	0.52 + 0.013*SL
	t_{PHL}	0.62	0.56 + 0.029*SL	0.58 + 0.023*SL	0.63 + 0.017*SL
	t_R	0.20	0.15 + 0.026*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.26	0.19 + 0.034*SL	0.19 + 0.032*SL	0.20 + 0.032*SL
D1 to Y	t_{PLH}	0.52	0.48 + 0.020*SL	0.50 + 0.016*SL	0.52 + 0.013*SL
	t_{PHL}	0.62	0.57 + 0.029*SL	0.58 + 0.023*SL	0.64 + 0.017*SL
	t_R	0.20	0.15 + 0.025*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.25	0.18 + 0.035*SL	0.19 + 0.032*SL	0.20 + 0.032*SL
D2 to Y	t_{PLH}	0.52	0.48 + 0.020*SL	0.49 + 0.016*SL	0.52 + 0.013*SL
	t_{PHL}	0.62	0.56 + 0.029*SL	0.57 + 0.023*SL	0.63 + 0.017*SL
	t_R	0.20	0.14 + 0.026*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.25	0.18 + 0.035*SL	0.19 + 0.032*SL	0.20 + 0.032*SL
D3 to Y	t_{PLH}	0.52	0.48 + 0.020*SL	0.49 + 0.016*SL	0.52 + 0.013*SL
	t_{PHL}	0.62	0.56 + 0.029*SL	0.58 + 0.023*SL	0.63 + 0.017*SL
	t_R	0.20	0.14 + 0.026*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.26	0.19 + 0.035*SL	0.19 + 0.032*SL	0.20 + 0.032*SL
D4 to Y	t_{PLH}	0.51	0.47 + 0.020*SL	0.48 + 0.016*SL	0.51 + 0.013*SL
	t_{PHL}	0.61	0.56 + 0.029*SL	0.57 + 0.023*SL	0.63 + 0.017*SL
	t_R	0.19	0.14 + 0.025*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.25	0.18 + 0.036*SL	0.19 + 0.032*SL	0.20 + 0.032*SL
D5 to Y	t_{PLH}	0.51	0.47 + 0.020*SL	0.48 + 0.016*SL	0.51 + 0.013*SL
	t_{PHL}	0.61	0.56 + 0.029*SL	0.57 + 0.023*SL	0.63 + 0.017*SL
	t_R	0.19	0.14 + 0.025*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.25	0.18 + 0.034*SL	0.19 + 0.032*SL	0.20 + 0.032*SL
D6 to Y	t_{PLH}	0.50	0.46 + 0.020*SL	0.48 + 0.016*SL	0.50 + 0.013*SL
	t_{PHL}	0.60	0.55 + 0.029*SL	0.56 + 0.023*SL	0.62 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.25	0.19 + 0.033*SL	0.19 + 0.032*SL	0.20 + 0.032*SL
D7 to Y	t_{PLH}	0.50	0.46 + 0.020*SL	0.48 + 0.016*SL	0.50 + 0.013*SL
	t_{PHL}	0.61	0.55 + 0.029*SL	0.56 + 0.023*SL	0.62 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.25	0.19 + 0.034*SL	0.19 + 0.032*SL	0.20 + 0.032*SL
S0 to Y	t_{PLH}	1.07	1.03 + 0.020*SL	1.04 + 0.016*SL	1.07 + 0.013*SL
	t_{PHL}	1.03	0.97 + 0.029*SL	0.99 + 0.023*SL	1.04 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.25	0.18 + 0.034*SL	0.19 + 0.032*SL	0.20 + 0.032*SL
S1 to Y	t_{PLH}	0.64	0.60 + 0.020*SL	0.61 + 0.016*SL	0.63 + 0.013*SL
	t_{PHL}	0.54	0.48 + 0.029*SL	0.50 + 0.023*SL	0.55 + 0.017*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.25	0.18 + 0.036*SL	0.19 + 0.032*SL	0.20 + 0.032*SL
S2 to Y	t_{PLH}	0.36	0.32 + 0.019*SL	0.33 + 0.016*SL	0.35 + 0.013*SL
	t_{PHL}	0.38	0.32 + 0.029*SL	0.34 + 0.023*SL	0.39 + 0.017*SL
	t_R	0.18	0.12 + 0.027*SL	0.12 + 0.028*SL	0.11 + 0.029*SL
	t_F	0.24	0.17 + 0.035*SL	0.18 + 0.033*SL	0.19 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Input/Output Cells 4

Contents

OVERVIEW

The fourth chapter describes various kinds of Input/Output cells (3.3V Normal and 5V tolerant operations) in STDL80 library.

The switching characteristics of each cell are attached to its basic cell information. The AC characteristics of bi-directional buffers are not included in this data sheet, however, they can be derived from different combinations of input and output buffers.

There are so many possible combinations of input/output cells, therefore, the naming conventions are adopted to help you memorize and use this cell library efficiently. You can refer to the naming conventions contained in “Summary Tables” section.

The “Summary Tables” section shows the list of 3.3V and 5V tolerant I/O cells seperated by the category (input, output, bi-directional, etc.), and the more detailed description tables can be found on the leading part of each category.

SUMMARY TABLES

Input Buffers

Cell Type	Cell Name	Page
CMOS Level	PIC/PICD/PICU	4-7
	PHIC/PHICD/PHICU	
CMOS Schmitt Trigger Level	PIS/PISD/PISU	4-10
	PHIS/PHISD/PHISU	

<Naming Convention of Input Buffers>

P v I a b			
v		**b**	
None	3.3V normal operation	None	No resistor
H	5V tolerant operation	D	Pull-down resistor
a		U	Pull-up resistor
C	CMOS level		
S	CMOS Schmitt trigger level		

Output Buffers

Cell Type	Cell Name	Current Drive (mA)	Page
Normal	POBy	1/2/4/8/12/16/20/24	4-14
	POBySM	4/8/12/16/20/24	
Open Drain	PODy	1/2/4/8/12/16/20/24	4-19
	PODySM	4/8/12/16/20/24	
	PHODy	1/2/4/6	
Tri-State	POTy	1/2/4/8/12/16/20/24	4-26
	POTySM	4/8/12/16/20/24	
	PHOTy	1/2/4/6	

<Naming Convention of Output Buffers>

P v O x y z			
v		**y**	
None	3.3V normal operation	1	1mA drive
H	5V tolerant operation	2	2mA drive
x		4	4mA drive
B	Normal buffer	6	6mA drive
D	Open drain buffer	8	8mA drive
T	Tri-state buffer	12	12mA drive
z		16	16mA drive
None	No slew-rate control	20	20mA drive
SM	Medium slew-rate control	24	24mA drive

Bi-Directional Buffers

Cell Type	Cell Name	Page
Open Drain	PBaDyz/PBaUDyz	4-37
	PHBaDyz/PHBaUDyz	
Tri-State	PBaTyz/PBaDTyz/PBaUTyz	
	PHBaTyz/PHBaDTyz/PHBaUTyz	

<Naming Convention of Bi-Directional Buffers>

P v B a b x y z			
v		**a**	
None	3.3V normal operation	C	CMOS level
H	5V tolerant operation	S	CMOS Schmitt trigger level
b		**y**	
None	No resistor	1	1mA drive
D	Pull-down resistor	2	2mA drive
U	Pull-up resistor	4	4mA drive
x		6	6mA drive
D	Open drain buffer	8	8mA drive
T	Tri-state buffer	12	12mA drive
z		16	16mA drive
None	No slew-rate control	20	20mA drive
SM	Medium slew-rate control	24	24mA drive

Input Clock Drivers

Cell Type	Cell Name	Current Drive (mA)	Page
CMOS Level	PSCKDCy/PSCKDCDy/PSCKDCUy	2/4/6/8	4-39
	PHSCKDCy/PHSCKDCDy/PHSCKDCUy	2/4/6/8	
CMOS Schmitt Trigger Level	PSCKDSy/PSCKDSDy/PSCKDSUy	2/4/6/8	4-46
	PHSCKDSy/PHSCKDSDy/PHSCKDSUy	2/4/6/8	

<Naming Convention of Input Clock Drivers>

PvSCKD a b y			
v		**a**	
None	3.3V normal operation	C	CMOS level
H	5V tolerant operation	S	CMOS Schmitt trigger level
b		**y**	
None	No resistor	2	2mA drive
D	Pull-down resistor	4	4mA drive
U	Pull-up resistor	6	6mA drive
		8	8mA drive

Oscillators

Cell Type	Cell Name	Page
Oscillator	PSOSCK(1/2) PSOSCK(16/26)	4-54
	PSOSCM(1/2/3/4/5/6) PSOSCM(16/26/36/46/56/66)	4-59

PCI Buffers

Cell Type	Cell Name	Page
3.3V PCI	PSPCIA3	4-68
5V Tolerant PCI	PHSPCIA	

CardBus I/O Buffers

Cell Type	Cell Name	Page
CardBus Input	PITCBU	4-71
CardBus Output	POTCBU/ POTCCKCBU/ POTCVSCBU	4-72
	PODCCKCBU	4-73
CardBus Bi-Directional I/O Buffers	PBTTCBU/ PBTCCKCBU/ PBTCVSCBU	4-74
	PBDCCKCBU	4-75

USB I/O Buffers

Cell Type	Cell Name	Page
USB	PBUSB/PBUSB1	4-78

Power Pads

Cell Type	Cell Name	Page
3.3V VDD	VDD3(I/P/O/IP/OI/OP/T)	4-84
5V VDD	VDD5O	
3.3V VSS	VSS3(I/P/O/IP/OI/OP/T)	
5V VSS	VSS5O	

INPUT BUFFERS

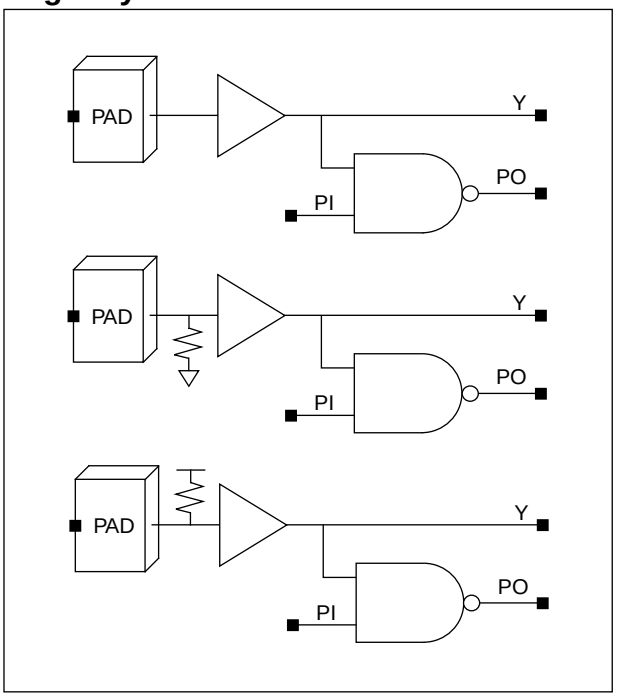
Cell List

Cell Name	Function Description
PIC/PICD/PICU	3.3V CMOS Level Input Buffers
PIS/PISD/PISU	3.3V CMOS Schmitt Trigger Level Input Buffers
PHIC/PHICD/PHICU	5V Tolerant CMOS Level Input Buffers
PHIS/PHISD/PHISU	5V Tolerant CMOS Schmitt Trigger Level Input Buffers

Cell Availability

3.3V Normal	5V Tolerant
PIC/PICD/PICU	PHIC/PHICD/PHICU

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Input Load (SL)

	PIC/PICD/PICU	PHIC/PHICD/PHICU
PI	3.0	3.0

I/O Slot

PvIC/PvICD/PvICU	1.0

STDL80 PIC Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.26	0.25 + 0.007*SL	0.26 + 0.005*SL	0.26 + 0.004*SL
	t_{PHL}	0.26	0.25 + 0.006*SL	0.25 + 0.007*SL	0.25 + 0.007*SL
	t_R	0.13	0.12 + 0.004*SL	0.11 + 0.008*SL	0.11 + 0.008*SL
	t_F	0.13	0.11 + 0.011*SL	0.11 + 0.011*SL	0.10 + 0.012*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 5, *Group3 : 5 < SL

STDL80 PICD Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.28	0.27 + 0.005*SL	0.27 + 0.004*SL	0.27 + 0.005*SL
	t_{PHL}	0.27	0.25 + 0.006*SL	0.25 + 0.007*SL	0.25 + 0.006*SL
	t_R	0.12	0.11 + 0.007*SL	0.10 + 0.010*SL	0.11 + 0.007*SL
	t_F	0.13	0.11 + 0.012*SL	0.11 + 0.011*SL	0.11 + 0.011*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 5, *Group3 : 5 < SL

STDL80 PICU Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.26	0.25 + 0.007*SL	0.26 + 0.005*SL	0.26 + 0.004*SL
	t_{PHL}	0.27	0.25 + 0.007*SL	0.26 + 0.007*SL	0.26 + 0.007*SL
	t_R	0.13	0.11 + 0.008*SL	0.12 + 0.006*SL	0.11 + 0.008*SL
	t_F	0.13	0.11 + 0.011*SL	0.11 + 0.011*SL	0.11 + 0.011*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 5, *Group3 : 5 < SL

STDL80 PHIC Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.66	0.64 + 0.007*SL	0.64 + 0.006*SL	0.65 + 0.006*SL
	t_{PHL}	0.46	0.45 + 0.007*SL	0.45 + 0.007*SL	0.45 + 0.006*SL
	t_R	0.22	0.20 + 0.007*SL	0.20 + 0.007*SL	0.20 + 0.006*SL
	t_F	0.14	0.11 + 0.013*SL	0.12 + 0.011*SL	0.12 + 0.011*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 5, *Group3 : 5 < SL

STDL80 PHICD Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.75	0.74 + 0.007*SL	0.74 + 0.007*SL	0.75 + 0.006*SL
	t_{PHL}	0.39	0.37 + 0.007*SL	0.37 + 0.007*SL	0.37 + 0.006*SL
	t_R	0.24	0.22 + 0.008*SL	0.23 + 0.007*SL	0.22 + 0.008*SL
	t_F	0.14	0.12 + 0.011*SL	0.13 + 0.010*SL	0.12 + 0.011*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 5, *Group3 : 5 < SL

STDL80 PHICU Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.62	0.61 + 0.007*SL	0.61 + 0.006*SL	0.61 + 0.006*SL
	t_{PHL}	0.55	0.53 + 0.007*SL	0.54 + 0.007*SL	0.54 + 0.006*SL
	t_R	0.21	0.19 + 0.007*SL	0.19 + 0.007*SL	0.19 + 0.007*SL
	t_F	0.14	0.12 + 0.010*SL	0.12 + 0.011*SL	0.12 + 0.011*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 5, *Group3 : 5 < SL

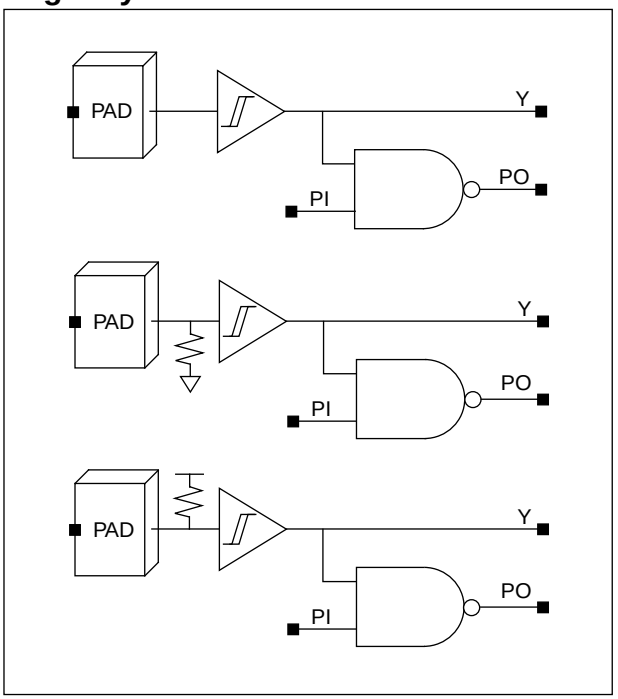
PvIS/PvISD/PvISU

CMOS Schmitt Trigger Level Input Buffers

Cell Availability

3.3V Normal	5V Tolerant
PIS/PISD/PISU	PHIS/PHISD/PHISU

Logic Symbol



Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Input Load (SL)

	PIS/PISD/PISU	PHIS/PHISD/PHISU
PI	3.0	3.0

I/O Slot

PvIS/PvISD/PvISU	1.0

STDL80 PIS Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.49	0.48 + 0.004*SL	0.48 + 0.004*SL	0.48 + 0.004*SL
	t_{PHL}	0.84	0.83 + 0.006*SL	0.83 + 0.005*SL	0.83 + 0.005*SL
	t_R	0.20	0.19 + 0.006*SL	0.19 + 0.004*SL	0.18 + 0.005*SL
	t_F	0.27	0.26 + 0.005*SL	0.26 + 0.005*SL	0.26 + 0.006*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 5, *Group3 : 5 < SL

STDL80 PISD Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.50	0.49 + 0.004*SL	0.49 + 0.004*SL	0.49 + 0.004*SL
	t_{PHL}	0.86	0.85 + 0.005*SL	0.85 + 0.005*SL	0.85 + 0.005*SL
	t_R	0.20	0.19 + 0.006*SL	0.19 + 0.004*SL	0.19 + 0.005*SL
	t_F	0.27	0.26 + 0.005*SL	0.26 + 0.005*SL	0.26 + 0.006*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 5, *Group3 : 5 < SL

STDL80 PISU Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.49	0.48 + 0.004*SL	0.48 + 0.004*SL	0.48 + 0.004*SL
	t_{PHL}	0.86	0.85 + 0.005*SL	0.85 + 0.005*SL	0.85 + 0.005*SL
	t_R	0.20	0.19 + 0.006*SL	0.19 + 0.004*SL	0.18 + 0.005*SL
	t_F	0.27	0.26 + 0.005*SL	0.26 + 0.005*SL	0.26 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 5, *Group3 : 5 < SL

STDL80 PHIS Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.39	1.38 + 0.005*SL	1.38 + 0.005*SL	1.38 + 0.004*SL
	t_{PHL}	1.18	1.17 + 0.006*SL	1.17 + 0.005*SL	1.17 + 0.005*SL
	t_R	0.30	0.29 + 0.004*SL	0.29 + 0.004*SL	0.29 + 0.004*SL
	t_F	0.27	0.27 + 0.004*SL	0.26 + 0.006*SL	0.26 + 0.006*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 5, *Group3 : 5 < SL

STDL80 PHISD Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.62	1.61 + 0.005*SL	1.61 + 0.005*SL	1.61 + 0.004*SL
	t_{PHL}	1.12	1.11 + 0.005*SL	1.11 + 0.005*SL	1.11 + 0.005*SL
	t_R	0.32	0.31 + 0.004*SL	0.31 + 0.004*SL	0.31 + 0.004*SL
	t_F	0.28	0.26 + 0.007*SL	0.27 + 0.005*SL	0.27 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 5, *Group3 : 5 < SL

STDL80 PHISU Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.28	1.28 + 0.005*SL	1.28 + 0.004*SL	1.28 + 0.004*SL
	t_{PHL}	1.33	1.32 + 0.005*SL	1.32 + 0.005*SL	1.32 + 0.005*SL
	t_R	0.28	0.28 + 0.004*SL	0.27 + 0.004*SL	0.28 + 0.004*SL
	t_F	0.28	0.27 + 0.005*SL	0.27 + 0.006*SL	0.27 + 0.005*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 5, *Group3 : 5 < SL

Cell List

Cell Name	Function Description
POB(1/2/4/8/12/16/20/24)	3.3V Normal Output Buffers
POB(4/8/12/16/20/24)SM	3.3V Normal Output Buffers with Medium Slew-Rate
POD(1/2/4/8/12/16/20/24)	3.3V Open Drain Output Buffers
POD(4/8/12/16/20/24)SM	3.3V Open Drain Output Buffers with Medium Slew-Rate
POT(1/2/4/8/12/16/20/24)	3.3V Tri-State Output Buffers
POT(4/8/12/16/20/24)SM	3.3V Tri-State Output Buffers with Medium Slew-Rate
PHOD(1/2/4/6)	5V Tolerant Open Drain Output Buffers
PHOT(1/2/4/6)	5V Tolerant Tri-State Output Buffers

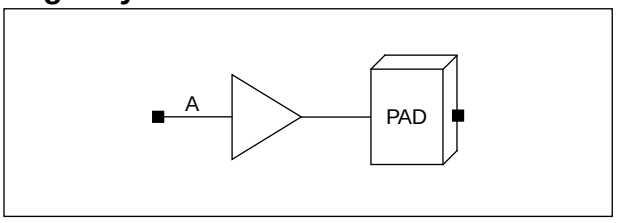
PvOByz

Normal Output Buffers

Cell Availability

3.3V Normal	5V Tolerant
POB(1/2/4/8/12/16/20/24) POB(4/8/12/16/20/24)SM	–

Logic Symbol



Input Load (SL)

	A
POB(1/2/20/24)	10.8
POB(4/8/12)	7.6
POB16	9.2
POB(4/8/12/16/20/214)SM	22.3

Truth Table

A	PAD
0	0
1	1

I/O Slot

PvOByz	1.0

STDL80 POB1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	13.44	0.50 + 0.259*CL	0.50 + 0.259*CL	0.50 + 0.259*CL
	t_{PHL}	10.97	0.49 + 0.210*CL	0.49 + 0.210*CL	0.49 + 0.210*CL
	t_R	29.97	0.86 + 0.582*CL	0.86 + 0.582*CL	0.86 + 0.582*CL
	t_F	23.77	0.63 + 0.463*CL	0.64 + 0.463*CL	0.63 + 0.463*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POB2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	6.84	0.37 + 0.129*CL	0.37 + 0.129*CL	0.37 + 0.129*CL
	t_{PHL}	5.60	0.36 + 0.105*CL	0.36 + 0.105*CL	0.36 + 0.105*CL
	t_R	15.00	0.44 + 0.291*CL	0.44 + 0.291*CL	0.44 + 0.291*CL
	t_F	11.90	0.33 + 0.231*CL	0.33 + 0.231*CL	0.33 + 0.231*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POB4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.54	0.30 + 0.065*CL	0.31 + 0.065*CL	0.30 + 0.065*CL
	t_{PHL}	2.96	0.34 + 0.052*CL	0.34 + 0.052*CL	0.34 + 0.052*CL
	t_R	7.52	0.24 + 0.146*CL	0.24 + 0.145*CL	0.24 + 0.146*CL
	t_F	5.97	0.18 + 0.116*CL	0.18 + 0.116*CL	0.18 + 0.116*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POB8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.21	0.36 + 0.037*CL	0.36 + 0.037*CL	0.36 + 0.037*CL
	t_{PHL}	1.89	0.40 + 0.030*CL	0.39 + 0.030*CL	0.39 + 0.030*CL
	t_R	4.32	0.16 + 0.083*CL	0.17 + 0.083*CL	0.16 + 0.083*CL
	t_F	3.44	0.14 + 0.066*CL	0.13 + 0.066*CL	0.13 + 0.066*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POB12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.73	0.44 + 0.026*CL	0.44 + 0.026*CL	0.43 + 0.026*CL
	t_{PHL}	1.52	0.49 + 0.021*CL	0.48 + 0.021*CL	0.48 + 0.021*CL
	t_R	3.06	0.15 + 0.058*CL	0.15 + 0.058*CL	0.14 + 0.058*CL
	t_F	2.45	0.18 + 0.046*CL	0.15 + 0.046*CL	0.14 + 0.046*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POB16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.49	0.57 + 0.018*CL	0.56 + 0.018*CL	0.56 + 0.018*CL
	t_{PHL}	1.29	0.54 + 0.015*CL	0.54 + 0.015*CL	0.54 + 0.015*CL
	t_R	2.24	0.18 + 0.041*CL	0.17 + 0.041*CL	0.16 + 0.041*CL
	t_F	1.80	0.18 + 0.032*CL	0.17 + 0.033*CL	0.16 + 0.033*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POB20 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.43	0.67 + 0.015*CL	0.67 + 0.015*CL	0.67 + 0.015*CL
	t_{PHL}	1.21	0.58 + 0.013*CL	0.59 + 0.012*CL	0.60 + 0.012*CL
	t_R	1.89	0.22 + 0.034*CL	0.20 + 0.034*CL	0.19 + 0.034*CL
	t_F	1.54	0.22 + 0.026*CL	0.20 + 0.027*CL	0.20 + 0.027*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POB24 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.39	0.75 + 0.013*CL	0.75 + 0.013*CL	0.75 + 0.013*CL
	t_{PHL}	1.18	0.63 + 0.011*CL	0.65 + 0.011*CL	0.66 + 0.011*CL
	t_R	1.67	0.26 + 0.028*CL	0.24 + 0.028*CL	0.23 + 0.029*CL
	t_F	1.37	0.25 + 0.022*CL	0.24 + 0.023*CL	0.24 + 0.023*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POB4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.70	0.46 + 0.065*CL	0.46 + 0.065*CL	0.46 + 0.065*CL
	t_{PHL}	3.16	0.54 + 0.052*CL	0.54 + 0.052*CL	0.54 + 0.052*CL
	t_R	7.53	0.26 + 0.145*CL	0.25 + 0.146*CL	0.25 + 0.146*CL
	t_F	5.99	0.22 + 0.115*CL	0.21 + 0.116*CL	0.20 + 0.116*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POB8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.49	0.63 + 0.037*CL	0.64 + 0.037*CL	0.64 + 0.037*CL
	t_{PHL}	2.29	0.79 + 0.030*CL	0.79 + 0.030*CL	0.79 + 0.030*CL
	t_R	4.38	0.25 + 0.083*CL	0.24 + 0.083*CL	0.22 + 0.083*CL
	t_F	3.57	0.33 + 0.065*CL	0.31 + 0.065*CL	0.28 + 0.065*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POB12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.00	0.70 + 0.026*CL	0.70 + 0.026*CL	0.71 + 0.026*CL
	t_{PHL}	1.93	0.84 + 0.022*CL	0.87 + 0.021*CL	0.88 + 0.021*CL
	t_R	3.16	0.31 + 0.057*CL	0.29 + 0.057*CL	0.27 + 0.058*CL
	t_F	2.67	0.45 + 0.044*CL	0.43 + 0.045*CL	0.40 + 0.045*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POB16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.76	0.80 + 0.019*CL	0.82 + 0.019*CL	0.84 + 0.019*CL
	t_{PHL}	1.75	0.90 + 0.017*CL	0.96 + 0.016*CL	0.99 + 0.016*CL
	t_R	2.43	0.43 + 0.040*CL	0.41 + 0.040*CL	0.39 + 0.040*CL
	t_F	2.18	0.62 + 0.031*CL	0.61 + 0.031*CL	0.60 + 0.031*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POB20SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.66	0.84 + 0.016*CL	0.88 + 0.016*CL	0.89 + 0.016*CL
	t_{PHL}	1.66	0.90 + 0.015*CL	0.97 + 0.014*CL	1.01 + 0.014*CL
	t_R	2.13	0.50 + 0.033*CL	0.49 + 0.033*CL	0.47 + 0.033*CL
	t_F	1.99	0.70 + 0.026*CL	0.71 + 0.026*CL	0.71 + 0.026*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POB24SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

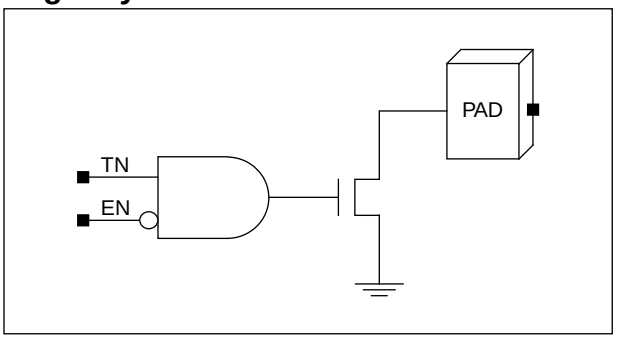
Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.60	0.86 + 0.015*CL	0.91 + 0.014*CL	0.94 + 0.014*CL
	t_{PHL}	1.60	0.88 + 0.014*CL	0.97 + 0.013*CL	1.01 + 0.013*CL
	t_R	1.94	0.56 + 0.028*CL	0.56 + 0.028*CL	0.55 + 0.028*CL
	t_F	1.87	0.74 + 0.023*CL	0.78 + 0.022*CL	0.79 + 0.022*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Cell Availability

3.3V Normal	5V Tolerant
POD(1/2/4/8/12/16/20/24) POD(4/8/12/16/20/24)SM	PHOD(1/2/4/6)

Logic Symbol



NOTES:

1. 3.3V normal open-drain output buffers, POD(1/2/4/8/12/16/20/24), cannot tolerate external pull-ups to more than 3.6V. And 5V tolerant open-drain output buffers, PHOD(1/2/4/6), cannot tolerate external pull-ups more than 5.5V.
2. Fail-safe open-drain output buffers with external pull-ups to more than 3.6V (in case of 3.3V normal) / 5.5V (in case of 5V tolerant) can drive signals to that voltage range.
   However, if you want to use fail-safe open-drains, please contact to SEC ASIC first.

Truth Table

TN	EN	PAD
1	0	0
0	x	Hi-Z
x	1	Hi-Z

Input Load (SL)

	TN	EN
POD(1/2/4/8/12/16/20/24)	3.0	3.0
POD(4/8/12/16/20/24)SM	3.0	3.0
PHOD(1/6)	3.0	5.2
PHOD(2/4)	3.0	5.0

I/O Slot

PvODyz	1.0

STDL80 POD1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	11.19	0.71 + 0.210*CL	0.71 + 0.209*CL	0.71 + 0.210*CL
	t_F	23.77	0.63 + 0.463*CL	0.64 + 0.463*CL	0.63 + 0.463*CL
	t_{PLZ}	0.47	0.47 + 0.000*CL	0.47 + 0.000*CL	0.47 + 0.000*CL
EN to PAD	t_{PHL}	11.33	0.85 + 0.210*CL	0.85 + 0.210*CL	0.86 + 0.209*CL
	t_F	23.77	0.63 + 0.463*CL	0.64 + 0.463*CL	0.63 + 0.463*CL
	t_{PLZ}	0.41	0.41 + 0.000*CL	0.41 + 0.000*CL	0.41 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POD2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	5.81	0.57 + 0.105*CL	0.57 + 0.105*CL	0.58 + 0.105*CL
	t_F	11.90	0.33 + 0.231*CL	0.33 + 0.231*CL	0.33 + 0.231*CL
	t_{PLZ}	0.49	0.49 + 0.000*CL	0.49 + 0.000*CL	0.49 + 0.000*CL
EN to PAD	t_{PHL}	5.96	0.72 + 0.105*CL	0.71 + 0.105*CL	0.72 + 0.105*CL
	t_F	11.90	0.33 + 0.231*CL	0.33 + 0.231*CL	0.33 + 0.231*CL
	t_{PLZ}	0.44	0.44 + 0.000*CL	0.44 + 0.000*CL	0.44 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POD4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.16	0.54 + 0.052*CL	0.54 + 0.052*CL	0.54 + 0.052*CL
	t_F	5.97	0.18 + 0.116*CL	0.18 + 0.116*CL	0.18 + 0.116*CL
	t_{PLZ}	0.54	0.54 + 0.000*CL	0.54 + 0.000*CL	0.54 + 0.000*CL
EN to PAD	t_{PHL}	3.31	0.69 + 0.052*CL	0.69 + 0.052*CL	0.69 + 0.052*CL
	t_F	5.97	0.18 + 0.116*CL	0.18 + 0.116*CL	0.18 + 0.116*CL
	t_{PLZ}	0.48	0.48 + 0.000*CL	0.48 + 0.000*CL	0.48 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POD8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.08	0.58 + 0.030*CL	0.59 + 0.030*CL	0.58 + 0.030*CL
	t_F	3.44	0.14 + 0.066*CL	0.13 + 0.066*CL	0.13 + 0.066*CL
	t_{PLZ}	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL
EN to PAD	t_{PHL}	2.23	0.73 + 0.030*CL	0.73 + 0.030*CL	0.73 + 0.030*CL
	t_F	3.43	0.13 + 0.066*CL	0.13 + 0.066*CL	0.13 + 0.066*CL
	t_{PLZ}	0.55	0.55 + 0.000*CL	0.55 + 0.000*CL	0.55 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POD12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.69	0.64 + 0.021*CL	0.64 + 0.021*CL	0.65 + 0.021*CL
	t_F	2.44	0.14 + 0.046*CL	0.13 + 0.046*CL	0.13 + 0.046*CL
	t_{PLZ}	0.67	0.67 + 0.000*CL	0.67 + 0.000*CL	0.67 + 0.000*CL
EN to PAD	t_{PHL}	1.84	0.79 + 0.021*CL	0.79 + 0.021*CL	0.79 + 0.021*CL
	t_F	2.44	0.15 + 0.046*CL	0.13 + 0.046*CL	0.13 + 0.046*CL
	t_{PLZ}	0.61	0.61 + 0.000*CL	0.61 + 0.000*CL	0.61 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POD16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.48	0.73 + 0.015*CL	0.73 + 0.015*CL	0.73 + 0.015*CL
	t_F	1.81	0.19 + 0.032*CL	0.18 + 0.033*CL	0.17 + 0.033*CL
	t_{PLZ}	0.75	0.75 + 0.000*CL	0.75 + 0.000*CL	0.75 + 0.000*CL
EN to PAD	t_{PHL}	1.63	0.87 + 0.015*CL	0.88 + 0.015*CL	0.87 + 0.015*CL
	t_F	1.81	0.19 + 0.032*CL	0.18 + 0.033*CL	0.17 + 0.033*CL
	t_{PLZ}	0.70	0.70 + 0.000*CL	0.70 + 0.000*CL	0.69 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POD20 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.41	0.78 + 0.013*CL	0.79 + 0.012*CL	0.80 + 0.012*CL
	t_F	1.55	0.23 + 0.026*CL	0.21 + 0.027*CL	0.21 + 0.027*CL
	t_{PLZ}	0.81	0.81 + 0.000*CL	0.81 + 0.000*CL	0.81 + 0.000*CL
EN to PAD	t_{PHL}	1.56	0.93 + 0.013*CL	0.94 + 0.013*CL	0.94 + 0.012*CL
	t_F	1.55	0.23 + 0.026*CL	0.21 + 0.027*CL	0.21 + 0.027*CL
	t_{PLZ}	0.76	0.76 + 0.000*CL	0.76 + 0.000*CL	0.76 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POD24 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.38	0.83 + 0.011*CL	0.85 + 0.011*CL	0.86 + 0.011*CL
	t_F	1.38	0.27 + 0.022*CL	0.26 + 0.022*CL	0.25 + 0.022*CL
	t_{PLZ}	0.88	0.88 + 0.000*CL	0.88 + 0.000*CL	0.88 + 0.000*CL
EN to PAD	t_{PHL}	1.53	0.97 + 0.011*CL	1.00 + 0.011*CL	1.00 + 0.011*CL
	t_F	1.38	0.27 + 0.022*CL	0.26 + 0.022*CL	0.25 + 0.022*CL
	t_{PLZ}	0.82	0.82 + 0.000*CL	0.82 + 0.000*CL	0.82 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POD4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.47	0.85 + 0.052*CL	0.85 + 0.052*CL	0.85 + 0.052*CL
	t_F	6.00	0.23 + 0.115*CL	0.21 + 0.116*CL	0.21 + 0.116*CL
	t_{PLZ}	0.51	0.51 + 0.000*CL	0.51 + 0.000*CL	0.51 + 0.000*CL
EN to PAD	t_{PHL}	3.61	0.99 + 0.052*CL	0.99 + 0.052*CL	0.99 + 0.052*CL
	t_F	6.00	0.23 + 0.115*CL	0.21 + 0.116*CL	0.21 + 0.116*CL
	t_{PLZ}	0.46	0.46 + 0.000*CL	0.46 + 0.000*CL	0.46 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POD8SM Switching Characteristics

[Delays for typical process, 25℃, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.61	1.10 + 0.030*CL	1.11 + 0.030*CL	1.11 + 0.030*CL
	t_F	3.58	0.35 + 0.065*CL	0.31 + 0.065*CL	0.30 + 0.065*CL
	t_{PLZ}	0.51	0.51 + 0.000*CL	0.51 + 0.000*CL	0.51 + 0.000*CL
EN to PAD	t_{PHL}	2.75	1.25 + 0.030*CL	1.26 + 0.030*CL	1.26 + 0.030*CL
	t_F	3.58	0.35 + 0.065*CL	0.31 + 0.065*CL	0.30 + 0.065*CL
	t_{PLZ}	0.46	0.46 + 0.000*CL	0.46 + 0.000*CL	0.46 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POD12SM Switching Characteristics

[Delays for typical process, 25℃, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.24	1.15 + 0.022*CL	1.18 + 0.021*CL	1.20 + 0.021*CL
	t_F	2.69	0.49 + 0.044*CL	0.46 + 0.045*CL	0.43 + 0.045*CL
	t_{PLZ}	0.54	0.54 + 0.000*CL	0.54 + 0.000*CL	0.54 + 0.000*CL
EN to PAD	t_{PHL}	2.39	1.30 + 0.022*CL	1.33 + 0.021*CL	1.34 + 0.021*CL
	t_F	2.69	0.49 + 0.044*CL	0.45 + 0.045*CL	0.43 + 0.045*CL
	t_{PLZ}	0.49	0.49 + 0.000*CL	0.49 + 0.000*CL	0.49 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POD16SM Switching Characteristics

[Delays for typical process, 25℃, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	2.07	1.21 + 0.017*CL	1.28 + 0.016*CL	1.31 + 0.016*CL
	t_F	2.21	0.68 + 0.031*CL	0.65 + 0.031*CL	0.64 + 0.031*CL
	t_{PLZ}	0.57	0.57 + 0.000*CL	0.57 + 0.000*CL	0.57 + 0.000*CL
EN to PAD	t_{PHL}	2.22	1.36 + 0.017*CL	1.42 + 0.016*CL	1.45 + 0.016*CL
	t_F	2.21	0.67 + 0.031*CL	0.65 + 0.031*CL	0.64 + 0.031*CL
	t_{PLZ}	0.51	0.51 + 0.000*CL	0.51 + 0.000*CL	0.51 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POD20SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.98	1.20 + 0.016*CL	1.29 + 0.014*CL	1.32 + 0.014*CL
	t_F	2.03	0.77 + 0.025*CL	0.77 + 0.025*CL	0.76 + 0.025*CL
	t_{PLZ}	0.59	0.59 + 0.000*CL	0.59 + 0.000*CL	0.59 + 0.000*CL
EN to PAD	t_{PHL}	2.12	1.34 + 0.016*CL	1.43 + 0.014*CL	1.47 + 0.014*CL
	t_F	2.03	0.77 + 0.025*CL	0.77 + 0.025*CL	0.76 + 0.025*CL
	t_{PLZ}	0.53	0.53 + 0.000*CL	0.53 + 0.000*CL	0.53 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POD24SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	1.91	1.17 + 0.015*CL	1.27 + 0.013*CL	1.32 + 0.013*CL
	t_F	1.92	0.82 + 0.022*CL	0.85 + 0.022*CL	0.86 + 0.022*CL
	t_{PLZ}	0.61	0.61 + 0.000*CL	0.61 + 0.000*CL	0.61 + 0.000*CL
EN to PAD	t_{PHL}	2.05	1.32 + 0.015*CL	1.42 + 0.013*CL	1.46 + 0.013*CL
	t_F	1.92	0.82 + 0.022*CL	0.84 + 0.022*CL	0.86 + 0.022*CL
	t_{PLZ}	0.56	0.56 + 0.000*CL	0.56 + 0.000*CL	0.56 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 PHOD1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	17.44	0.88 + 0.331*CL	0.88 + 0.331*CL	0.89 + 0.331*CL
	t_F	31.75	1.11 + 0.613*CL	1.11 + 0.613*CL	1.11 + 0.613*CL
	t_{PLZ}	0.49	0.49 + 0.000*CL	0.49 + 0.000*CL	0.49 + 0.000*CL
EN to PAD	t_{PHL}	17.59	1.02 + 0.331*CL	1.03 + 0.331*CL	1.03 + 0.331*CL
	t_F	31.76	1.12 + 0.613*CL	1.12 + 0.613*CL	1.12 + 0.613*CL
	t_{PLZ}	0.44	0.44 + 0.000*CL	0.44 + 0.000*CL	0.44 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 PHOD2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	11.72	0.72 + 0.220*CL	0.72 + 0.220*CL	0.72 + 0.220*CL
	t_F	21.76	0.74 + 0.420*CL	0.74 + 0.420*CL	0.73 + 0.420*CL
	t_{PLZ}	0.49	0.49 + 0.000*CL	0.49 + 0.000*CL	0.49 + 0.000*CL
EN to PAD	t_{PHL}	11.86	0.86 + 0.220*CL	0.87 + 0.220*CL	0.86 + 0.220*CL
	t_F	21.76	0.75 + 0.420*CL	0.74 + 0.420*CL	0.75 + 0.420*CL
	t_{PLZ}	0.44	0.44 + 0.000*CL	0.44 + 0.000*CL	0.44 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 PHOD4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	5.34	0.61 + 0.095*CL	0.61 + 0.095*CL	0.62 + 0.095*CL
	t_F	9.03	0.28 + 0.175*CL	0.28 + 0.175*CL	0.28 + 0.175*CL
	t_{PLZ}	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL
EN to PAD	t_{PHL}	5.49	0.76 + 0.095*CL	0.76 + 0.095*CL	0.76 + 0.095*CL
	t_F	9.04	0.28 + 0.175*CL	0.28 + 0.175*CL	0.29 + 0.175*CL
	t_{PLZ}	0.55	0.55 + 0.000*CL	0.55 + 0.000*CL	0.55 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 PHOD6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TN to PAD	t_{PHL}	3.93	0.62 + 0.066*CL	0.62 + 0.066*CL	0.62 + 0.066*CL
	t_F	6.31	0.18 + 0.123*CL	0.18 + 0.123*CL	0.18 + 0.123*CL
	t_{PLZ}	0.67	0.67 + 0.000*CL	0.67 + 0.000*CL	0.67 + 0.000*CL
EN to PAD	t_{PHL}	4.08	0.77 + 0.066*CL	0.77 + 0.066*CL	0.77 + 0.066*CL
	t_F	6.31	0.18 + 0.123*CL	0.19 + 0.123*CL	0.18 + 0.123*CL
	t_{PLZ}	0.61	0.61 + 0.000*CL	0.61 + 0.000*CL	0.61 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

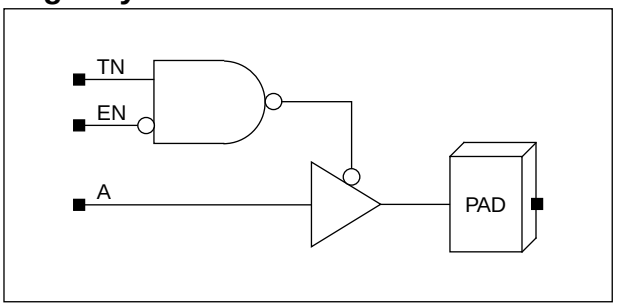
PvOTyz

Tri-State Output Buffers

Cell Availability

3.3V Normal	5V Tolerant
POT(1/2/4/8/12/16/20/24) POT(4/8/12/16/20/24)SM	PHOT(1/2/4/6)

Logic Symbol



Truth Table

TN	EN	A	PAD
1	0	0	0
1	0	1	1
x	1	x	Hi-Z
0	x	x	Hi-Z

I/O Slot

PvOTyz	1.0

Input Load (SL)

	TN	EN	A
POT(1/2/4/8/12/16/20/24)	3.0	3.0	4.6
POT(4/8/12/16/20/24)SM	3.0	3.0	4.6
PHOD(1/2/4/6)	3.3	5.7	4.6

STDL80 POT1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	13.73	0.78 + 0.259*CL	0.78 + 0.259*CL	0.78 + 0.259*CL
	t_{PHL}	11.24	0.76 + 0.210*CL	0.76 + 0.210*CL	0.76 + 0.210*CL
	t_R	29.97	0.86 + 0.582*CL	0.86 + 0.582*CL	0.86 + 0.582*CL
	t_F	23.77	0.63 + 0.463*CL	0.64 + 0.463*CL	0.63 + 0.463*CL
TN to PAD	t_{PLH}	13.74	0.90 + 0.257*CL	1.44 + 0.250*CL	2.43 + 0.238*CL
	t_{PHL}	11.29	0.82 + 0.210*CL	0.82 + 0.209*CL	0.82 + 0.210*CL
	t_R	29.97	0.86 + 0.582*CL	0.86 + 0.582*CL	0.86 + 0.582*CL
	t_F	23.77	0.63 + 0.463*CL	0.64 + 0.463*CL	0.63 + 0.463*CL
	t_{PLZ}	0.63	0.63 + 0.000*CL	0.63 + 0.000*CL	0.63 + 0.000*CL
	t_{PHZ}	0.57	0.57 + 0.000*CL	0.57 + 0.000*CL	0.57 + 0.000*CL
EN to PAD	t_{PLH}	13.88	1.05 + 0.257*CL	1.59 + 0.249*CL	2.60 + 0.238*CL
	t_{PHL}	11.44	0.96 + 0.210*CL	0.96 + 0.209*CL	0.96 + 0.210*CL
	t_R	29.97	0.86 + 0.582*CL	0.86 + 0.582*CL	0.86 + 0.582*CL
	t_F	23.77	0.63 + 0.463*CL	0.64 + 0.463*CL	0.63 + 0.463*CL
	t_{PLZ}	0.58	0.58 + 0.000*CL	0.58 + 0.000*CL	0.58 + 0.000*CL
	t_{PHZ}	0.52	0.52 + 0.000*CL	0.52 + 0.000*CL	0.52 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POT2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	7.14	0.66 + 0.129*CL	0.67 + 0.129*CL	0.66 + 0.129*CL
	t_{PHL}	5.86	0.63 + 0.105*CL	0.63 + 0.105*CL	0.62 + 0.105*CL
	t_R	15.00	0.44 + 0.291*CL	0.44 + 0.291*CL	0.44 + 0.291*CL
	t_F	11.90	0.33 + 0.231*CL	0.33 + 0.231*CL	0.33 + 0.231*CL
TN to PAD	t_{PLH}	7.14	0.67 + 0.129*CL	0.66 + 0.130*CL	0.67 + 0.129*CL
	t_{PHL}	5.92	0.68 + 0.105*CL	0.69 + 0.105*CL	0.68 + 0.105*CL
	t_R	15.00	0.44 + 0.291*CL	0.44 + 0.291*CL	0.44 + 0.291*CL
	t_F	11.90	0.33 + 0.231*CL	0.33 + 0.231*CL	0.33 + 0.231*CL
	t_{PLZ}	0.68	0.68 + 0.000*CL	0.68 + 0.000*CL	0.68 + 0.000*CL
	t_{PHZ}	0.60	0.60 + 0.000*CL	0.60 + 0.000*CL	0.60 + 0.000*CL
EN to PAD	t_{PLH}	7.28	0.81 + 0.129*CL	0.81 + 0.129*CL	0.81 + 0.129*CL
	t_{PHL}	6.07	0.83 + 0.105*CL	0.82 + 0.105*CL	0.83 + 0.105*CL
	t_R	15.00	0.44 + 0.291*CL	0.44 + 0.291*CL	0.44 + 0.291*CL
	t_F	11.90	0.33 + 0.231*CL	0.33 + 0.231*CL	0.33 + 0.231*CL
	t_{PLZ}	0.63	0.63 + 0.000*CL	0.63 + 0.000*CL	0.63 + 0.000*CL
	t_{PHZ}	0.55	0.55 + 0.000*CL	0.55 + 0.000*CL	0.55 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POT4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.81	0.57 + 0.065*CL	0.58 + 0.065*CL	0.57 + 0.065*CL
	t_{PHL}	3.22	0.61 + 0.052*CL	0.60 + 0.052*CL	0.60 + 0.052*CL
	t_R	7.52	0.24 + 0.146*CL	0.24 + 0.145*CL	0.24 + 0.146*CL
	t_F	5.97	0.18 + 0.116*CL	0.18 + 0.116*CL	0.18 + 0.116*CL
TN to PAD	t_{PLH}	3.81	0.57 + 0.065*CL	0.58 + 0.065*CL	0.57 + 0.065*CL
	t_{PHL}	3.27	0.66 + 0.052*CL	0.65 + 0.052*CL	0.65 + 0.052*CL
	t_R	7.52	0.24 + 0.146*CL	0.24 + 0.145*CL	0.24 + 0.146*CL
	t_F	5.97	0.18 + 0.116*CL	0.18 + 0.116*CL	0.18 + 0.116*CL
	t_{PLZ}	0.77	0.77 + 0.000*CL	0.77 + 0.000*CL	0.77 + 0.000*CL
	t_{PHZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
EN to PAD	t_{PLH}	3.95	0.72 + 0.065*CL	0.72 + 0.065*CL	0.72 + 0.065*CL
	t_{PHL}	3.42	0.80 + 0.052*CL	0.80 + 0.052*CL	0.80 + 0.052*CL
	t_R	7.52	0.24 + 0.146*CL	0.24 + 0.145*CL	0.24 + 0.146*CL
	t_F	5.97	0.18 + 0.116*CL	0.18 + 0.116*CL	0.18 + 0.116*CL
	t_{PLZ}	0.72	0.72 + 0.000*CL	0.72 + 0.000*CL	0.72 + 0.000*CL
	t_{PHZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POT8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.48	0.63 + 0.037*CL	0.63 + 0.037*CL	0.63 + 0.037*CL
	t_{PHL}	2.15	0.67 + 0.030*CL	0.66 + 0.030*CL	0.66 + 0.030*CL
	t_R	4.32	0.16 + 0.083*CL	0.17 + 0.083*CL	0.16 + 0.083*CL
	t_F	3.44	0.14 + 0.066*CL	0.13 + 0.066*CL	0.13 + 0.066*CL
TN to PAD	t_{PLH}	2.48	0.63 + 0.037*CL	0.63 + 0.037*CL	0.63 + 0.037*CL
	t_{PHL}	2.19	0.70 + 0.030*CL	0.69 + 0.030*CL	0.70 + 0.030*CL
	t_R	4.32	0.16 + 0.083*CL	0.17 + 0.083*CL	0.16 + 0.083*CL
	t_F	3.43	0.13 + 0.066*CL	0.13 + 0.066*CL	0.13 + 0.066*CL
	t_{PLZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL
EN to PAD	t_{PLH}	2.62	0.77 + 0.037*CL	0.77 + 0.037*CL	0.77 + 0.037*CL
	t_{PHL}	2.34	0.84 + 0.030*CL	0.84 + 0.030*CL	0.84 + 0.030*CL
	t_R	4.32	0.16 + 0.083*CL	0.17 + 0.083*CL	0.16 + 0.083*CL
	t_F	3.43	0.13 + 0.066*CL	0.13 + 0.066*CL	0.13 + 0.066*CL
	t_{PLZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL
	t_{PHZ}	1.13	1.13 + 0.000*CL	1.13 + 0.000*CL	1.13 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POT12 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.00	0.70 + 0.026*CL	0.70 + 0.026*CL	0.70 + 0.026*CL
	t_{PHL}	1.79	0.76 + 0.021*CL	0.75 + 0.021*CL	0.74 + 0.021*CL
	t_R	3.06	0.15 + 0.058*CL	0.15 + 0.058*CL	0.14 + 0.058*CL
	t_F	2.46	0.18 + 0.045*CL	0.15 + 0.046*CL	0.14 + 0.046*CL
TN to PAD	t_{PLH}	2.00	0.70 + 0.026*CL	0.70 + 0.026*CL	0.70 + 0.026*CL
	t_{PHL}	1.81	0.76 + 0.021*CL	0.76 + 0.021*CL	0.76 + 0.021*CL
	t_R	3.06	0.15 + 0.058*CL	0.15 + 0.058*CL	0.14 + 0.058*CL
	t_F	2.44	0.14 + 0.046*CL	0.13 + 0.046*CL	0.13 + 0.046*CL
	t_{PLZ}	1.03	1.03 + 0.000*CL	1.03 + 0.000*CL	1.03 + 0.000*CL
	t_{PHZ}	1.46	1.46 + 0.000*CL	1.46 + 0.000*CL	1.46 + 0.000*CL
EN to PAD	t_{PLH}	2.14	0.84 + 0.026*CL	0.84 + 0.026*CL	0.84 + 0.026*CL
	t_{PHL}	1.95	0.90 + 0.021*CL	0.90 + 0.021*CL	0.90 + 0.021*CL
	t_R	3.06	0.15 + 0.058*CL	0.15 + 0.058*CL	0.14 + 0.058*CL
	t_F	2.44	0.14 + 0.046*CL	0.13 + 0.046*CL	0.13 + 0.046*CL
	t_{PLZ}	0.98	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL
	t_{PHZ}	1.41	1.41 + 0.000*CL	1.41 + 0.000*CL	1.41 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POT16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.77	0.84 + 0.019*CL	0.85 + 0.018*CL	0.85 + 0.018*CL
	t_{PHL}	1.55	0.81 + 0.015*CL	0.81 + 0.015*CL	0.81 + 0.015*CL
	t_R	2.24	0.18 + 0.041*CL	0.17 + 0.041*CL	0.16 + 0.041*CL
	t_F	1.80	0.19 + 0.032*CL	0.17 + 0.033*CL	0.16 + 0.033*CL
TN to PAD	t_{PLH}	1.76	0.84 + 0.019*CL	0.83 + 0.019*CL	0.84 + 0.019*CL
	t_{PHL}	1.60	0.84 + 0.015*CL	0.85 + 0.015*CL	0.85 + 0.015*CL
	t_R	2.24	0.19 + 0.041*CL	0.17 + 0.041*CL	0.16 + 0.041*CL
	t_F	1.80	0.18 + 0.032*CL	0.17 + 0.033*CL	0.16 + 0.033*CL
	t_{PLZ}	1.20	1.20 + 0.000*CL	1.20 + 0.000*CL	1.20 + 0.000*CL
	t_{PHZ}	1.18	1.18 + 0.000*CL	1.18 + 0.000*CL	1.18 + 0.000*CL
EN to PAD	t_{PLH}	1.91	0.98 + 0.019*CL	0.99 + 0.018*CL	0.98 + 0.019*CL
	t_{PHL}	1.74	0.99 + 0.015*CL	0.99 + 0.015*CL	0.99 + 0.015*CL
	t_R	2.24	0.19 + 0.041*CL	0.17 + 0.041*CL	0.16 + 0.041*CL
	t_F	1.80	0.18 + 0.032*CL	0.18 + 0.033*CL	0.16 + 0.033*CL
	t_{PLZ}	1.15	1.15 + 0.000*CL	1.15 + 0.000*CL	1.15 + 0.000*CL
	t_{PHZ}	1.13	1.13 + 0.000*CL	1.13 + 0.000*CL	1.13 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POT20 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.72	0.96 + 0.015*CL	0.95 + 0.015*CL	0.96 + 0.015*CL
	t_{PHL}	1.48	0.85 + 0.013*CL	0.86 + 0.012*CL	0.86 + 0.012*CL
	t_R	1.89	0.22 + 0.034*CL	0.21 + 0.034*CL	0.20 + 0.034*CL
	t_F	1.54	0.22 + 0.026*CL	0.21 + 0.027*CL	0.20 + 0.027*CL
TN to PAD	t_{PLH}	1.71	0.94 + 0.015*CL	0.95 + 0.015*CL	0.95 + 0.015*CL
	t_{PHL}	1.53	0.90 + 0.013*CL	0.91 + 0.012*CL	0.91 + 0.012*CL
	t_R	1.90	0.23 + 0.033*CL	0.21 + 0.034*CL	0.20 + 0.034*CL
	t_F	1.54	0.22 + 0.026*CL	0.21 + 0.027*CL	0.20 + 0.027*CL
	t_{PLZ}	1.33	1.33 + 0.000*CL	1.33 + 0.000*CL	1.33 + 0.000*CL
	t_{PHZ}	1.07	1.07 + 0.000*CL	1.06 + 0.000*CL	1.07 + 0.000*CL
EN to PAD	t_{PLH}	1.86	1.09 + 0.015*CL	1.09 + 0.015*CL	1.09 + 0.015*CL
	t_{PHL}	1.67	1.04 + 0.013*CL	1.05 + 0.012*CL	1.06 + 0.012*CL
	t_R	1.90	0.23 + 0.033*CL	0.21 + 0.034*CL	0.20 + 0.034*CL
	t_F	1.54	0.22 + 0.026*CL	0.21 + 0.027*CL	0.20 + 0.027*CL
	t_{PLZ}	1.28	1.28 + 0.000*CL	1.28 + 0.000*CL	1.28 + 0.000*CL
	t_{PHZ}	1.01	1.01 + 0.000*CL	1.01 + 0.000*CL	1.01 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POT24 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.69	1.03 + 0.013*CL	1.05 + 0.013*CL	1.04 + 0.013*CL
	t_{PHL}	1.45	0.90 + 0.011*CL	0.92 + 0.011*CL	0.93 + 0.011*CL
	t_R	1.67	0.26 + 0.028*CL	0.24 + 0.028*CL	0.23 + 0.029*CL
	t_F	1.37	0.25 + 0.022*CL	0.25 + 0.022*CL	0.24 + 0.023*CL
TN to PAD	t_{PLH}	1.67	1.01 + 0.013*CL	1.02 + 0.013*CL	1.03 + 0.013*CL
	t_{PHL}	1.50	0.94 + 0.011*CL	0.96 + 0.011*CL	0.97 + 0.011*CL
	t_R	1.68	0.27 + 0.028*CL	0.26 + 0.028*CL	0.24 + 0.028*CL
	t_F	1.37	0.26 + 0.022*CL	0.25 + 0.022*CL	0.24 + 0.022*CL
	t_{PLZ}	1.46	1.46 + 0.000*CL	1.46 + 0.000*CL	1.46 + 0.000*CL
	t_{PHZ}	1.16	1.16 + 0.000*CL	1.16 + 0.000*CL	1.15 + 0.000*CL
EN to PAD	t_{PLH}	1.82	1.15 + 0.013*CL	1.17 + 0.013*CL	1.17 + 0.013*CL
	t_{PHL}	1.64	1.09 + 0.011*CL	1.11 + 0.011*CL	1.12 + 0.011*CL
	t_R	1.68	0.27 + 0.028*CL	0.25 + 0.028*CL	0.24 + 0.028*CL
	t_F	1.37	0.26 + 0.022*CL	0.25 + 0.022*CL	0.24 + 0.022*CL
	t_{PLZ}	1.40	1.40 + 0.000*CL	1.40 + 0.000*CL	1.40 + 0.000*CL
	t_{PHZ}	1.10	1.10 + 0.000*CL	1.10 + 0.000*CL	1.10 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POT4SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.05	0.81 + 0.065*CL	0.81 + 0.065*CL	0.81 + 0.065*CL
	t_{PHL}	3.50	0.88 + 0.052*CL	0.89 + 0.052*CL	0.88 + 0.052*CL
	t_R	7.53	0.25 + 0.146*CL	0.26 + 0.145*CL	0.25 + 0.146*CL
	t_F	6.00	0.23 + 0.115*CL	0.22 + 0.115*CL	0.20 + 0.116*CL
TN to PAD	t_{PLH}	4.04	0.81 + 0.065*CL	0.81 + 0.065*CL	0.80 + 0.065*CL
	t_{PHL}	3.56	0.94 + 0.052*CL	0.94 + 0.052*CL	0.94 + 0.052*CL
	t_R	7.53	0.25 + 0.146*CL	0.26 + 0.145*CL	0.25 + 0.146*CL
	t_F	6.00	0.23 + 0.115*CL	0.22 + 0.115*CL	0.20 + 0.116*CL
	t_{PLZ}	0.74	0.74 + 0.000*CL	0.75 + 0.000*CL	0.75 + 0.000*CL
	t_{PHZ}	0.65	0.65 + 0.000*CL	0.65 + 0.000*CL	0.65 + 0.000*CL
EN to PAD	t_{PLH}	4.19	0.95 + 0.065*CL	0.95 + 0.065*CL	0.95 + 0.065*CL
	t_{PHL}	3.70	1.08 + 0.052*CL	1.08 + 0.052*CL	1.08 + 0.052*CL
	t_R	7.53	0.25 + 0.146*CL	0.26 + 0.145*CL	0.25 + 0.146*CL
	t_F	6.00	0.23 + 0.115*CL	0.22 + 0.115*CL	0.20 + 0.116*CL
	t_{PLZ}	0.69	0.69 + 0.000*CL	0.69 + 0.000*CL	0.69 + 0.000*CL
	t_{PHZ}	0.59	0.59 + 0.000*CL	0.59 + 0.000*CL	0.59 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POT8SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.86	1.01 + 0.037*CL	1.01 + 0.037*CL	1.01 + 0.037*CL
	t_{PHL}	2.62	1.11 + 0.030*CL	1.12 + 0.030*CL	1.13 + 0.030*CL
	t_R	4.38	0.26 + 0.083*CL	0.24 + 0.083*CL	0.23 + 0.083*CL
	t_F	3.57	0.34 + 0.065*CL	0.30 + 0.065*CL	0.29 + 0.065*CL
TN to PAD	t_{PLH}	2.86	1.00 + 0.037*CL	1.00 + 0.037*CL	1.01 + 0.037*CL
	t_{PHL}	2.67	1.17 + 0.030*CL	1.18 + 0.030*CL	1.18 + 0.030*CL
	t_R	4.38	0.26 + 0.083*CL	0.24 + 0.083*CL	0.23 + 0.083*CL
	t_F	3.57	0.34 + 0.065*CL	0.31 + 0.065*CL	0.29 + 0.065*CL
	t_{PLZ}	0.69	0.69 + 0.000*CL	0.69 + 0.000*CL	0.69 + 0.000*CL
	t_{PHZ}	0.63	0.63 + 0.000*CL	0.63 + 0.000*CL	0.63 + 0.000*CL
EN to PAD	t_{PLH}	3.00	1.15 + 0.037*CL	1.14 + 0.037*CL	1.15 + 0.037*CL
	t_{PHL}	2.82	1.31 + 0.030*CL	1.32 + 0.030*CL	1.33 + 0.030*CL
	t_R	4.38	0.26 + 0.083*CL	0.24 + 0.083*CL	0.23 + 0.083*CL
	t_F	3.57	0.34 + 0.065*CL	0.31 + 0.065*CL	0.29 + 0.065*CL
	t_{PLZ}	0.64	0.64 + 0.000*CL	0.64 + 0.000*CL	0.64 + 0.000*CL
	t_{PHZ}	0.58	0.58 + 0.000*CL	0.58 + 0.000*CL	0.58 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POT12SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.38	1.07 + 0.026*CL	1.08 + 0.026*CL	1.08 + 0.026*CL
	t_{PHL}	2.26	1.17 + 0.022*CL	1.20 + 0.021*CL	1.21 + 0.021*CL
	t_R	3.17	0.32 + 0.057*CL	0.30 + 0.057*CL	0.28 + 0.058*CL
	t_F	2.68	0.46 + 0.044*CL	0.42 + 0.045*CL	0.41 + 0.045*CL
TN to PAD	t_{PLH}	2.37	1.07 + 0.026*CL	1.07 + 0.026*CL	1.08 + 0.026*CL
	t_{PHL}	2.31	1.22 + 0.022*CL	1.26 + 0.021*CL	1.26 + 0.021*CL
	t_R	3.17	0.32 + 0.057*CL	0.30 + 0.057*CL	0.28 + 0.058*CL
	t_F	2.68	0.46 + 0.044*CL	0.43 + 0.045*CL	0.42 + 0.045*CL
	t_{PLZ}	0.74	0.74 + 0.000*CL	0.74 + 0.000*CL	0.74 + 0.000*CL
	t_{PHZ}	0.66	0.66 + 0.000*CL	0.66 + 0.000*CL	0.66 + 0.000*CL
EN to PAD	t_{PLH}	2.52	1.21 + 0.026*CL	1.22 + 0.026*CL	1.22 + 0.026*CL
	t_{PHL}	2.45	1.37 + 0.022*CL	1.39 + 0.021*CL	1.41 + 0.021*CL
	t_R	3.17	0.32 + 0.057*CL	0.30 + 0.057*CL	0.28 + 0.058*CL
	t_F	2.68	0.46 + 0.044*CL	0.43 + 0.045*CL	0.42 + 0.045*CL
	t_{PLZ}	0.69	0.69 + 0.000*CL	0.69 + 0.000*CL	0.69 + 0.000*CL
	t_{PHZ}	0.61	0.61 + 0.000*CL	0.61 + 0.000*CL	0.61 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POT16SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.11	1.16 + 0.019*CL	1.18 + 0.019*CL	1.20 + 0.019*CL
	t_{PHL}	2.11	1.25 + 0.017*CL	1.31 + 0.016*CL	1.34 + 0.016*CL
	t_R	2.44	0.45 + 0.040*CL	0.42 + 0.040*CL	0.40 + 0.040*CL
	t_F	2.19	0.63 + 0.031*CL	0.62 + 0.031*CL	0.61 + 0.031*CL
TN to PAD	t_{PLH}	2.10	1.14 + 0.019*CL	1.17 + 0.019*CL	1.18 + 0.019*CL
	t_{PHL}	2.15	1.30 + 0.017*CL	1.37 + 0.016*CL	1.39 + 0.016*CL
	t_R	2.44	0.45 + 0.040*CL	0.42 + 0.040*CL	0.40 + 0.040*CL
	t_F	2.20	0.65 + 0.031*CL	0.64 + 0.031*CL	0.63 + 0.031*CL
	t_{PLZ}	0.84	0.83 + 0.000*CL	0.84 + 0.000*CL	0.84 + 0.000*CL
	t_{PHZ}	0.74	0.74 + 0.000*CL	0.74 + 0.000*CL	0.74 + 0.000*CL
EN to PAD	t_{PLH}	2.25	1.29 + 0.019*CL	1.32 + 0.019*CL	1.33 + 0.019*CL
	t_{PHL}	2.30	1.44 + 0.017*CL	1.51 + 0.016*CL	1.54 + 0.016*CL
	t_R	2.44	0.45 + 0.040*CL	0.42 + 0.040*CL	0.40 + 0.040*CL
	t_F	2.20	0.65 + 0.031*CL	0.64 + 0.031*CL	0.63 + 0.031*CL
	t_{PLZ}	0.78	0.78 + 0.000*CL	0.78 + 0.000*CL	0.78 + 0.000*CL
	t_{PHZ}	0.68	0.68 + 0.000*CL	0.68 + 0.000*CL	0.68 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POT20SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	2.01	1.19 + 0.016*CL	1.23 + 0.016*CL	1.24 + 0.016*CL
	t_{PHL}	2.01	1.25 + 0.015*CL	1.32 + 0.014*CL	1.36 + 0.014*CL
	t_R	2.14	0.53 + 0.032*CL	0.50 + 0.033*CL	0.49 + 0.033*CL
	t_F	2.00	0.71 + 0.026*CL	0.72 + 0.026*CL	0.73 + 0.026*CL
TN to PAD	t_{PLH}	2.00	1.17 + 0.017*CL	1.21 + 0.016*CL	1.23 + 0.016*CL
	t_{PHL}	2.06	1.28 + 0.016*CL	1.37 + 0.014*CL	1.41 + 0.014*CL
	t_R	2.15	0.54 + 0.032*CL	0.51 + 0.033*CL	0.50 + 0.033*CL
	t_F	2.02	0.74 + 0.025*CL	0.75 + 0.025*CL	0.75 + 0.025*CL
	t_{PLZ}	0.88	0.88 + 0.000*CL	0.88 + 0.000*CL	0.87 + 0.000*CL
	t_{PHZ}	0.79	0.79 + 0.000*CL	0.79 + 0.000*CL	0.79 + 0.000*CL
EN to PAD	t_{PLH}	2.14	1.32 + 0.017*CL	1.36 + 0.016*CL	1.37 + 0.016*CL
	t_{PHL}	2.20	1.43 + 0.016*CL	1.52 + 0.014*CL	1.55 + 0.014*CL
	t_R	2.15	0.54 + 0.032*CL	0.51 + 0.033*CL	0.49 + 0.033*CL
	t_F	2.02	0.74 + 0.025*CL	0.75 + 0.025*CL	0.75 + 0.025*CL
	t_{PLZ}	0.83	0.83 + 0.000*CL	0.83 + 0.000*CL	0.83 + 0.000*CL
	t_{PHZ}	0.73	0.73 + 0.000*CL	0.73 + 0.000*CL	0.73 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 POT24SM Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	1.95	1.21 + 0.015*CL	1.26 + 0.014*CL	1.29 + 0.014*CL
	t_{PHL}	1.95	1.23 + 0.014*CL	1.32 + 0.013*CL	1.37 + 0.013*CL
	t_R	1.96	0.58 + 0.027*CL	0.58 + 0.028*CL	0.57 + 0.028*CL
	t_F	1.88	0.75 + 0.023*CL	0.79 + 0.022*CL	0.81 + 0.022*CL
TN to PAD	t_{PLH}	1.93	1.18 + 0.015*CL	1.25 + 0.014*CL	1.27 + 0.014*CL
	t_{PHL}	1.98	1.25 + 0.015*CL	1.35 + 0.013*CL	1.40 + 0.013*CL
	t_R	1.97	0.61 + 0.027*CL	0.59 + 0.027*CL	0.58 + 0.028*CL
	t_F	1.91	0.80 + 0.022*CL	0.83 + 0.022*CL	0.84 + 0.022*CL
	t_{PLZ}	0.93	0.93 + 0.000*CL	0.93 + 0.000*CL	0.93 + 0.000*CL
	t_{PHZ}	0.83	0.83 + 0.000*CL	0.83 + 0.000*CL	0.83 + 0.000*CL
EN to PAD	t_{PLH}	2.08	1.33 + 0.015*CL	1.39 + 0.014*CL	1.42 + 0.014*CL
	t_{PHL}	2.13	1.39 + 0.015*CL	1.49 + 0.013*CL	1.54 + 0.013*CL
	t_R	1.97	0.61 + 0.027*CL	0.59 + 0.027*CL	0.58 + 0.028*CL
	t_F	1.91	0.80 + 0.022*CL	0.83 + 0.022*CL	0.84 + 0.022*CL
	t_{PLZ}	0.87	0.87 + 0.000*CL	0.86 + 0.000*CL	0.87 + 0.000*CL
	t_{PHZ}	0.78	0.78 + 0.000*CL	0.78 + 0.000*CL	0.78 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 PHOT1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	17.35	1.25 + 0.322*CL	1.24 + 0.322*CL	1.25 + 0.322*CL
	t_{PHL}	17.49	0.94 + 0.331*CL	0.94 + 0.331*CL	0.94 + 0.331*CL
	t_R	35.24	1.17 + 0.681*CL	1.17 + 0.681*CL	1.18 + 0.681*CL
	t_F	31.74	1.10 + 0.613*CL	1.09 + 0.613*CL	1.09 + 0.613*CL
TN to PAD	t_{PLH}	17.34	1.70 + 0.313*CL	3.85 + 0.284*CL	7.68 + 0.239*CL
	t_{PHL}	17.55	1.00 + 0.331*CL	1.00 + 0.331*CL	1.00 + 0.331*CL
	t_R	35.24	1.17 + 0.681*CL	1.17 + 0.681*CL	1.18 + 0.681*CL
	t_F	31.74	1.10 + 0.613*CL	1.09 + 0.613*CL	1.09 + 0.613*CL
	t_{PLZ}	0.68	0.68 + 0.000*CL	0.67 + 0.000*CL	0.67 + 0.000*CL
	t_{PHZ}	53.82	42.59 + 0.225*CL	42.91 + 0.220*CL	43.10 + 0.218*CL
EN to PAD	t_{PLH}	17.49	1.85 + 0.313*CL	4.03 + 0.284*CL	7.90 + 0.238*CL
	t_{PHL}	17.69	1.14 + 0.331*CL	1.15 + 0.331*CL	1.14 + 0.331*CL
	t_R	35.24	1.17 + 0.681*CL	1.17 + 0.681*CL	1.18 + 0.681*CL
	t_F	31.74	1.10 + 0.613*CL	1.09 + 0.613*CL	1.09 + 0.613*CL
	t_{PLZ}	0.63	0.63 + 0.000*CL	0.63 + 0.000*CL	0.62 + 0.000*CL
	t_{PHZ}	53.97	42.74 + 0.225*CL	43.05 + 0.220*CL	43.24 + 0.218*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 PHOT2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	8.99	0.94 + 0.161*CL	0.93 + 0.161*CL	0.94 + 0.161*CL
	t_{PHL}	11.78	0.79 + 0.220*CL	0.79 + 0.220*CL	0.79 + 0.220*CL
	t_R	17.64	0.61 + 0.341*CL	0.60 + 0.341*CL	0.61 + 0.341*CL
	t_F	21.75	0.73 + 0.420*CL	0.73 + 0.420*CL	0.73 + 0.420*CL
TN to PAD	t_{PLH}	8.99	0.95 + 0.161*CL	1.06 + 0.159*CL	1.35 + 0.156*CL
	t_{PHL}	11.83	0.84 + 0.220*CL	0.84 + 0.220*CL	0.84 + 0.220*CL
	t_R	17.64	0.61 + 0.341*CL	0.60 + 0.341*CL	0.61 + 0.341*CL
	t_F	21.75	0.73 + 0.420*CL	0.73 + 0.420*CL	0.73 + 0.420*CL
	t_{PLZ}	0.68	0.68 + 0.000*CL	0.68 + 0.000*CL	0.68 + 0.000*CL
	t_{PHZ}	50.38	42.42 + 0.159*CL	42.69 + 0.156*CL	42.85 + 0.154*CL
EN to PAD	t_{PLH}	9.14	1.10 + 0.161*CL	1.21 + 0.159*CL	1.50 + 0.156*CL
	t_{PHL}	11.98	0.99 + 0.220*CL	0.99 + 0.220*CL	0.98 + 0.220*CL
	t_R	17.64	0.61 + 0.341*CL	0.60 + 0.341*CL	0.61 + 0.341*CL
	t_F	21.75	0.72 + 0.420*CL	0.73 + 0.420*CL	0.73 + 0.420*CL
	t_{PLZ}	0.63	0.63 + 0.000*CL	0.63 + 0.000*CL	0.63 + 0.000*CL
	t_{PHZ}	50.52	42.57 + 0.159*CL	42.83 + 0.156*CL	43.00 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 PHOT4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	4.88	0.86 + 0.081*CL	0.85 + 0.081*CL	0.86 + 0.080*CL
	t_{PHL}	5.41	0.68 + 0.095*CL	0.69 + 0.095*CL	0.68 + 0.095*CL
	t_R	8.85	0.33 + 0.170*CL	0.34 + 0.170*CL	0.34 + 0.170*CL
	t_F	9.04	0.28 + 0.175*CL	0.28 + 0.175*CL	0.29 + 0.175*CL
TN to PAD	t_{PLH}	4.88	0.85 + 0.081*CL	0.86 + 0.080*CL	0.86 + 0.081*CL
	t_{PHL}	5.46	0.73 + 0.095*CL	0.73 + 0.095*CL	0.73 + 0.095*CL
	t_R	8.85	0.33 + 0.170*CL	0.34 + 0.170*CL	0.34 + 0.170*CL
	t_F	9.04	0.28 + 0.175*CL	0.28 + 0.175*CL	0.28 + 0.175*CL
	t_{PLZ}	0.90	0.90 + 0.000*CL	0.90 + 0.000*CL	0.90 + 0.000*CL
	t_{PHZ}	46.13	42.17 + 0.079*CL	42.35 + 0.077*CL	42.44 + 0.076*CL
EN to PAD	t_{PLH}	5.03	1.00 + 0.081*CL	1.00 + 0.081*CL	1.00 + 0.081*CL
	t_{PHL}	5.61	0.88 + 0.095*CL	0.88 + 0.095*CL	0.89 + 0.095*CL
	t_R	8.85	0.33 + 0.170*CL	0.34 + 0.170*CL	0.34 + 0.170*CL
	t_F	9.04	0.28 + 0.175*CL	0.28 + 0.175*CL	0.28 + 0.175*CL
	t_{PLZ}	0.85	0.85 + 0.000*CL	0.85 + 0.000*CL	0.85 + 0.000*CL
	t_{PHZ}	46.27	42.32 + 0.079*CL	42.49 + 0.077*CL	42.59 + 0.076*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

STDL80 PHOT6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to PAD	t_{PLH}	3.56	0.87 + 0.054*CL	0.87 + 0.054*CL	0.87 + 0.054*CL
	t_{PHL}	4.00	0.69 + 0.066*CL	0.69 + 0.066*CL	0.70 + 0.066*CL
	t_R	5.93	0.26 + 0.113*CL	0.25 + 0.114*CL	0.26 + 0.114*CL
	t_F	6.31	0.19 + 0.123*CL	0.18 + 0.123*CL	0.19 + 0.123*CL
TN to PAD	t_{PLH}	3.56	0.87 + 0.054*CL	0.87 + 0.054*CL	0.87 + 0.054*CL
	t_{PHL}	4.06	0.75 + 0.066*CL	0.75 + 0.066*CL	0.74 + 0.066*CL
	t_R	5.94	0.26 + 0.113*CL	0.25 + 0.114*CL	0.26 + 0.114*CL
	t_F	6.31	0.18 + 0.123*CL	0.19 + 0.123*CL	0.18 + 0.123*CL
	t_{PLZ}	1.03	1.03 + 0.000*CL	1.03 + 0.000*CL	1.03 + 0.000*CL
	t_{PHZ}	45.34	42.31 + 0.061*CL	42.47 + 0.059*CL	42.56 + 0.057*CL
EN to PAD	t_{PLH}	3.70	1.02 + 0.054*CL	1.02 + 0.054*CL	1.02 + 0.054*CL
	t_{PHL}	4.20	0.89 + 0.066*CL	0.89 + 0.066*CL	0.89 + 0.066*CL
	t_R	5.94	0.26 + 0.113*CL	0.25 + 0.114*CL	0.26 + 0.114*CL
	t_F	6.31	0.18 + 0.123*CL	0.19 + 0.123*CL	0.18 + 0.123*CL
	t_{PLZ}	0.98	0.98 + 0.000*CL	0.98 + 0.000*CL	0.98 + 0.000*CL
	t_{PHZ}	45.49	42.46 + 0.061*CL	42.61 + 0.059*CL	42.70 + 0.058*CL

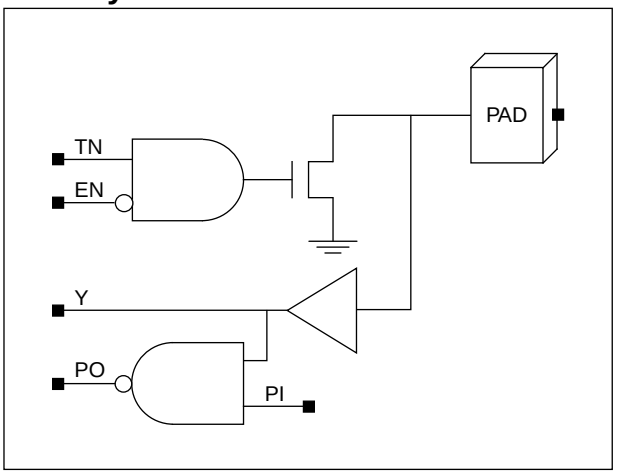
*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

BI-DIRECTIONAL BUFFERS

Cell List

Cell Name	Function Description
PBaDyz	3.3V Open-Drain Bi-Directional Buffers
PBaUDyz	3.3V Open-Drain Bi-Directional Buffers with Pull-Up
PBaTyz	3.3V Tri-State Bi-Directional Buffers
PBaDTyz	3.3V Tri-State Bi-Directional Buffers with Pull-Down
PBaUTyz	3.3V Tri-State Bi-Directional Buffers with Pull-Up
PHBaDyz	5V Tolerant Open-Drain Bi-Directional Buffers
PHBaUDyz	5V Tolerant Open-Drain Bi-Directional Buffers with Pull-Up
PHBaTyz	5V Tolerant Tri-State Bi-Directional Buffers
PHBaDTyz	5V Tolerant Tri-State Bi-Directional Buffers with Pull-Down
PHBaUTyz	5V Tolerant Tri-State Bi-Directional Buffers with Pull-Up

PvBaDyz



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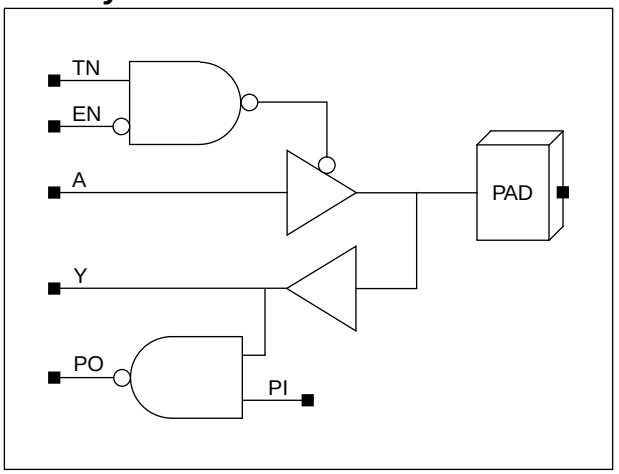

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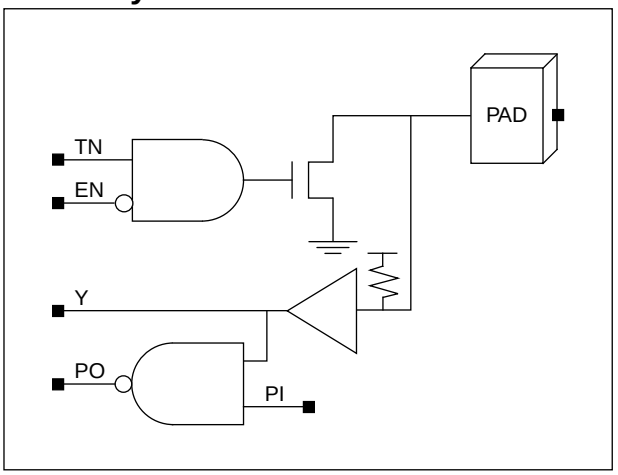

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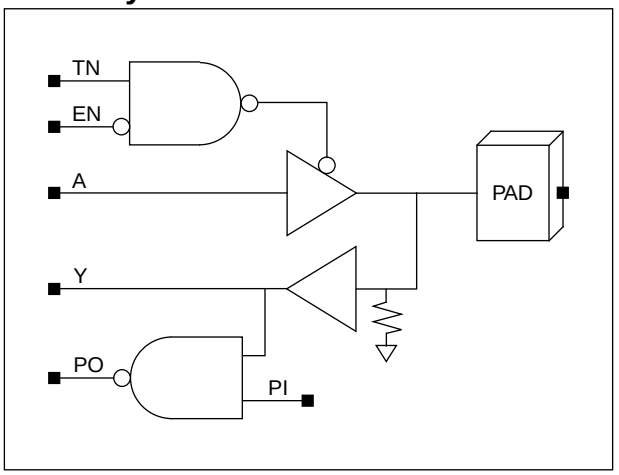

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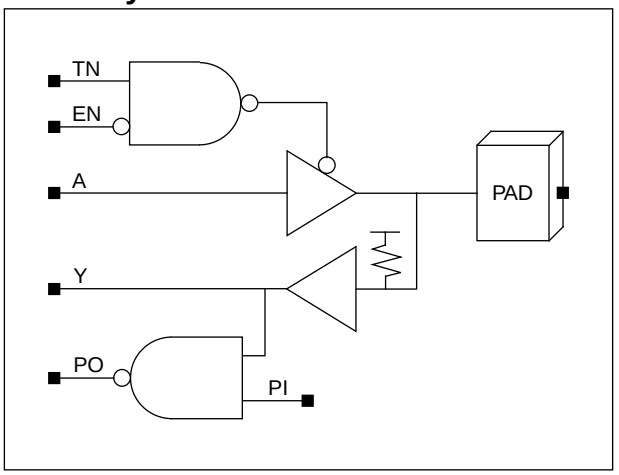


INPUT CLOCK DRIVERS

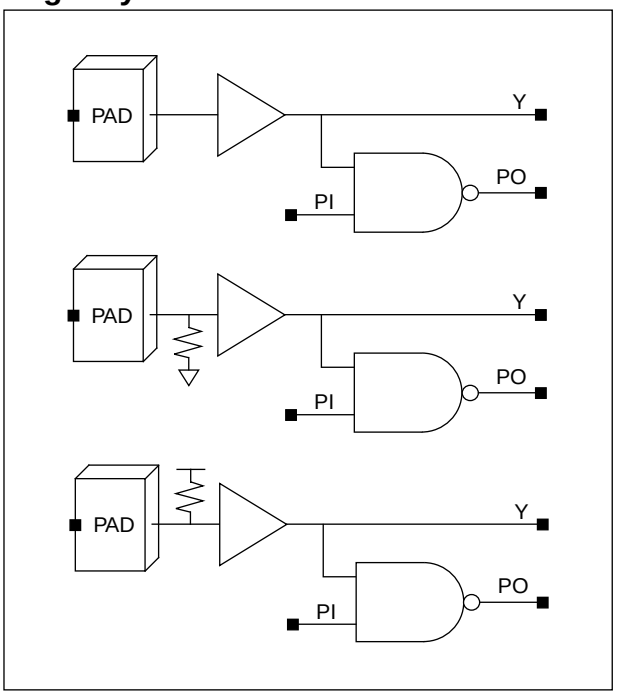
Cell List

Cell Name	Function Description
PSCKDC(2/4/6/8)	3.3V CMOS Level Input Clock Drivers
PSCKDCD(2/4/6/8)	3.3V CMOS Level Input Clock Drivers with Pull-Down
PSCKDCU(2/4/6/8)	3.3V CMOS Level Input Clock Drivers with Pull-Up
PSCKDS(2/4/6/8)	3.3V CMOS Schmitt Trigger Level Input Clock Drivers
PSCKDSD(2/4/6/8)	3.3V CMOS Schmitt Trigger Level Input Clock Drivers with Pull-Down
PSCKDSU(2/4/6/8)	3.3V CMOS Schmitt Trigger Level Input Clock Drivers with Pull-Up
PHSCKDC(2/4/6/8)	5V Tolerant CMOS Level Input Clock Drivers
PHSCKDCD(2/4/6/8)	5V Tolerant CMOS Level Input Clock Drivers with Pull-Down
PHSCKDCU(2/4/6/8)	5V Tolerant CMOS Level Input Clock Drivers with Pull-Up
PHSCKDS(2/4/6/8)	5V Tolerant CMOS Schmitt Trigger Level Input Clock Drivers
PHSCKDSD(2/4/6/8)	5V Tolerant CMOS Schmitt Trigger Level Input Clock Drivers with Pull-Down
PHSCKDSU(2/4/6/8)	5V Tolerant CMOS Schmitt Trigger Level Input Clock Drivers with Pull-Up

Cell Availability

3.3V Normal	5V Tolerant
PSCKDC(2/4/6/8) PSCKDCD(2/4/6/8) PSCKDCU(2/4/6/8)	PHSCKDC(2/4/6/8) PHSCKDCD(2/4/6/8) PHSCKDCU(2/4/6/8)

Logic Symbol



Input Load (SL)

	PI
PSCKDC(2/4/6/8)	3.0
PSCKDCD(2/4/6/8)	3.0
PSCKDCU(2/4/6/8)	3.0
PHSCKDC(2/4/6/8)	3.0
PHSCKDCD(2/4/6/8)	3.0
PHSCKDCU(2/4/6/8)	3.0

I/O Slot

PvSCKDCy/PvSCKDCDy/PvSCKDCUy	1.0

STDL80 PSCKDC2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 103	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.58	0.29 + 0.003*SL	0.29 + 0.003*SL	0.29 + 0.003*SL
	t_{PHL}	0.55	0.25 + 0.003*SL	0.26 + 0.003*SL	0.26 + 0.003*SL
	t_R	0.73	0.10 + 0.006*SL	0.09 + 0.006*SL	0.09 + 0.006*SL
	t_F	0.66	0.09 + 0.005*SL	0.08 + 0.006*SL	0.08 + 0.006*SL

*Group1 : SL < 69, *Group2 : 69 ≦SL≦ 103, *Group3 : 103 < SL

STDL80 PSCKDC4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 202	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.64	0.35 + 0.001*SL	0.36 + 0.001*SL	0.36 + 0.001*SL
	t_{PHL}	0.60	0.30 + 0.001*SL	0.30 + 0.001*SL	0.31 + 0.001*SL
	t_R	0.73	0.12 + 0.003*SL	0.12 + 0.003*SL	0.11 + 0.003*SL
	t_F	0.65	0.10 + 0.003*SL	0.09 + 0.003*SL	0.09 + 0.003*SL

*Group1 : SL < 135, *Group2 : 135 ≦SL≦ 202, *Group3 : 202 < SL

STDL80 PSCKDC6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 307	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.65	0.36 + 0.001*SL	0.36 + 0.001*SL	0.36 + 0.001*SL
	t_{PHL}	0.64	0.34 + 0.001*SL	0.35 + 0.001*SL	0.35 + 0.001*SL
	t_R	0.73	0.11 + 0.002*SL	0.10 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.66	0.10 + 0.002*SL	0.09 + 0.002*SL	0.08 + 0.002*SL

*Group1 : SL < 204, *Group2 : 204 ≦SL≦ 307, *Group3 : 307 < SL

STDL80 PSCKDC8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 405	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.68	0.39 + 0.001*SL	0.40 + 0.001*SL	0.40 + 0.001*SL
	t_{PHL}	0.67	0.37 + 0.001*SL	0.37 + 0.001*SL	0.38 + 0.001*SL
	t_R	0.73	0.13 + 0.001*SL	0.11 + 0.002*SL	0.11 + 0.002*SL
	t_F	0.66	0.11 + 0.001*SL	0.10 + 0.001*SL	0.09 + 0.001*SL

*Group1 : SL < 270, *Group2 : 270 ≦SL≦ 405, *Group3 : 405 < SL

STDL80 PSCKDCD2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 103	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.59	0.30 + 0.003*SL	0.31 + 0.003*SL	0.30 + 0.003*SL
	t_{PHL}	0.56	0.26 + 0.003*SL	0.26 + 0.003*SL	0.26 + 0.003*SL
	t_R	0.73	0.10 + 0.006*SL	0.10 + 0.006*SL	0.09 + 0.006*SL
	t_F	0.66	0.09 + 0.005*SL	0.08 + 0.006*SL	0.08 + 0.006*SL

*Group1 : SL < 69, *Group2 : 69 ≦SL≦ 103, *Group3 : 103 < SL

STDL80 PSCKDCD4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 202	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.65	0.37 + 0.001*SL	0.37 + 0.001*SL	0.37 + 0.001*SL
	t_{PHL}	0.60	0.31 + 0.001*SL	0.31 + 0.001*SL	0.31 + 0.001*SL
	t_R	0.73	0.12 + 0.003*SL	0.12 + 0.003*SL	0.11 + 0.003*SL
	t_F	0.65	0.10 + 0.003*SL	0.10 + 0.003*SL	0.08 + 0.003*SL

*Group1 : SL < 135, *Group2 : 135 ≦SL≦ 202, *Group3 : 202 < SL

STDL80 PSCKDCD6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 307	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.66	0.37 + 0.001*SL	0.37 + 0.001*SL	0.38 + 0.001*SL
	t_{PHL}	0.65	0.35 + 0.001*SL	0.35 + 0.001*SL	0.35 + 0.001*SL
	t_R	0.73	0.11 + 0.002*SL	0.10 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.66	0.10 + 0.002*SL	0.09 + 0.002*SL	0.08 + 0.002*SL

*Group1 : SL < 204, *Group2 : 204 ≦SL≦ 307, *Group3 : 307 < SL

STDL80 PSCKDCD8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 405	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.69	0.40 + 0.001*SL	0.41 + 0.001*SL	0.41 + 0.001*SL
	t_{PHL}	0.67	0.37 + 0.001*SL	0.38 + 0.001*SL	0.38 + 0.001*SL
	t_R	0.73	0.13 + 0.001*SL	0.11 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.66	0.11 + 0.001*SL	0.10 + 0.001*SL	0.10 + 0.001*SL

*Group1 : SL < 270, *Group2 : 270 ≦SL≦ 405, *Group3 : 405 < SL

STDL80 PSCKDCU2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 103	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.58	0.29 + 0.003*SL	0.29 + 0.003*SL	0.29 + 0.003*SL
	t_{PHL}	0.56	0.26 + 0.003*SL	0.26 + 0.003*SL	0.27 + 0.003*SL
	t_R	0.73	0.10 + 0.006*SL	0.10 + 0.006*SL	0.09 + 0.006*SL
	t_F	0.66	0.09 + 0.005*SL	0.08 + 0.006*SL	0.07 + 0.006*SL

*Group1 : SL < 69, *Group2 : 69 ≦ SL ≦ 103, *Group3 : 103 < SL

STDL80 PSCKDCU4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 202	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.64	0.35 + 0.001*SL	0.36 + 0.001*SL	0.36 + 0.001*SL
	t_{PHL}	0.60	0.31 + 0.001*SL	0.31 + 0.001*SL	0.32 + 0.001*SL
	t_R	0.73	0.12 + 0.003*SL	0.12 + 0.003*SL	0.11 + 0.003*SL
	t_F	0.65	0.10 + 0.003*SL	0.09 + 0.003*SL	0.09 + 0.003*SL

*Group1 : SL < 135, *Group2 : 135 ≦ SL ≦ 202, *Group3 : 202 < SL

STDL80 PSCKDCU6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 307	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.65	0.36 + 0.001*SL	0.36 + 0.001*SL	0.37 + 0.001*SL
	t_{PHL}	0.65	0.35 + 0.001*SL	0.35 + 0.001*SL	0.35 + 0.001*SL
	t_R	0.73	0.11 + 0.002*SL	0.10 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.66	0.10 + 0.002*SL	0.09 + 0.002*SL	0.08 + 0.002*SL

*Group1 : SL < 204, *Group2 : 204 ≦ SL ≦ 307, *Group3 : 307 < SL

STDL80 PSCKDCU8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 405	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.68	0.39 + 0.001*SL	0.40 + 0.001*SL	0.40 + 0.001*SL
	t_{PHL}	0.67	0.37 + 0.001*SL	0.38 + 0.001*SL	0.38 + 0.001*SL
	t_R	0.73	0.12 + 0.001*SL	0.12 + 0.002*SL	0.11 + 0.002*SL
	t_F	0.66	0.11 + 0.001*SL	0.10 + 0.001*SL	0.09 + 0.001*SL

*Group1 : SL < 270, *Group2 : 270 ≦ SL ≦ 405, *Group3 : 405 < SL

STDL80 PHSCKDC2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 103	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.05	0.72 + 0.003*SL	0.73 + 0.003*SL	0.74 + 0.003*SL
	t_{PHL}	0.76	0.46 + 0.003*SL	0.46 + 0.003*SL	0.46 + 0.003*SL
	t_R	0.82	0.20 + 0.006*SL	0.19 + 0.006*SL	0.17 + 0.006*SL
	t_F	0.67	0.10 + 0.005*SL	0.09 + 0.006*SL	0.09 + 0.006*SL

*Group1 : SL < 69, *Group2 : 69 ≦SL≦ 103, *Group3 : 103 < SL

STDL80 PHSCKDC4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 202	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.17	0.85 + 0.002*SL	0.85 + 0.002*SL	0.86 + 0.001*SL
	t_{PHL}	0.81	0.51 + 0.001*SL	0.51 + 0.001*SL	0.52 + 0.001*SL
	t_R	0.83	0.25 + 0.003*SL	0.23 + 0.003*SL	0.22 + 0.003*SL
	t_F	0.66	0.11 + 0.003*SL	0.10 + 0.003*SL	0.10 + 0.003*SL

*Group1 : SL < 135, *Group2 : 135 ≦SL≦ 202, *Group3 : 202 < SL

STDL80 PHSCKDC6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 307	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.29	0.97 + 0.001*SL	0.98 + 0.001*SL	0.98 + 0.001*SL
	t_{PHL}	0.93	0.63 + 0.001*SL	0.64 + 0.001*SL	0.64 + 0.001*SL
	t_R	0.85	0.25 + 0.002*SL	0.23 + 0.002*SL	0.22 + 0.002*SL
	t_F	0.67	0.12 + 0.002*SL	0.11 + 0.002*SL	0.10 + 0.002*SL

*Group1 : SL < 204, *Group2 : 204 ≦SL≦ 307, *Group3 : 307 < SL

STDL80 PHSCKDC8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 405	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.36	1.03 + 0.001*SL	1.04 + 0.001*SL	1.05 + 0.001*SL
	t_{PHL}	0.96	0.66 + 0.001*SL	0.67 + 0.001*SL	0.67 + 0.001*SL
	t_R	0.86	0.28 + 0.001*SL	0.26 + 0.001*SL	0.25 + 0.002*SL
	t_F	0.67	0.13 + 0.001*SL	0.12 + 0.001*SL	0.11 + 0.001*SL

*Group1 : SL < 270, *Group2 : 270 ≦SL≦ 405, *Group3 : 405 < SL

STDL80 PHSCKDCD2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 103	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.16	0.83 + 0.003*SL	0.84 + 0.003*SL	0.84 + 0.003*SL
	t_{PHL}	0.68	0.38 + 0.003*SL	0.39 + 0.003*SL	0.39 + 0.003*SL
	t_R	0.84	0.22 + 0.006*SL	0.20 + 0.006*SL	0.19 + 0.006*SL
	t_F	0.67	0.11 + 0.005*SL	0.09 + 0.006*SL	0.09 + 0.006*SL

*Group1 : SL < 69, *Group2 : 69 ≦ SL ≦ 103, *Group3 : 103 < SL

STDL80 PHSCKDCD4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 202	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.29	0.97 + 0.002*SL	0.98 + 0.002*SL	0.98 + 0.002*SL
	t_{PHL}	0.73	0.44 + 0.001*SL	0.44 + 0.001*SL	0.44 + 0.001*SL
	t_R	0.87	0.28 + 0.003*SL	0.26 + 0.003*SL	0.24 + 0.003*SL
	t_F	0.66	0.12 + 0.003*SL	0.11 + 0.003*SL	0.10 + 0.003*SL

*Group1 : SL < 135, *Group2 : 135 ≦ SL ≦ 202, *Group3 : 202 < SL

STDL80 PHSCKDCD6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 307	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.41	1.08 + 0.001*SL	1.09 + 0.001*SL	1.10 + 0.001*SL
	t_{PHL}	0.82	0.52 + 0.001*SL	0.52 + 0.001*SL	0.53 + 0.001*SL
	t_R	0.88	0.28 + 0.002*SL	0.26 + 0.002*SL	0.25 + 0.002*SL
	t_F	0.67	0.12 + 0.002*SL	0.12 + 0.002*SL	0.10 + 0.002*SL

*Group1 : SL < 204, *Group2 : 204 ≦ SL ≦ 307, *Group3 : 307 < SL

STDL80 PHSCKDCD8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 405	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.48	1.15 + 0.001*SL	1.17 + 0.001*SL	1.17 + 0.001*SL
	t_{PHL}	0.85	0.55 + 0.001*SL	0.56 + 0.001*SL	0.56 + 0.001*SL
	t_R	0.89	0.31 + 0.001*SL	0.29 + 0.001*SL	0.27 + 0.002*SL
	t_F	0.67	0.13 + 0.001*SL	0.13 + 0.001*SL	0.11 + 0.001*SL

*Group1 : SL < 270, *Group2 : 270 ≦ SL ≦ 405, *Group3 : 405 < SL

STDL80 PHSCKDCU2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 103	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.01	0.69 + 0.003*SL	0.69 + 0.003*SL	0.70 + 0.003*SL
	t_{PHL}	0.85	0.54 + 0.003*SL	0.55 + 0.003*SL	0.55 + 0.003*SL
	t_R	0.80	0.19 + 0.006*SL	0.18 + 0.006*SL	0.17 + 0.006*SL
	t_F	0.67	0.10 + 0.005*SL	0.09 + 0.006*SL	0.09 + 0.006*SL

*Group1 : SL < 69, *Group2 : 69 ≦SL≦ 103, *Group3 : 103 < SL

STDL80 PHSCKDCU4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 202	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.12	0.80 + 0.002*SL	0.81 + 0.002*SL	0.82 + 0.001*SL
	t_{PHL}	0.90	0.60 + 0.001*SL	0.61 + 0.001*SL	0.61 + 0.001*SL
	t_R	0.82	0.23 + 0.003*SL	0.22 + 0.003*SL	0.21 + 0.003*SL
	t_F	0.66	0.12 + 0.003*SL	0.11 + 0.003*SL	0.10 + 0.003*SL

*Group1 : SL < 135, *Group2 : 135 ≦SL≦ 202, *Group3 : 202 < SL

STDL80 PHSCKDCU6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 307	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.24	0.91 + 0.001*SL	0.92 + 0.001*SL	0.93 + 0.001*SL
	t_{PHL}	1.05	0.75 + 0.001*SL	0.75 + 0.001*SL	0.76 + 0.001*SL
	t_R	0.83	0.24 + 0.002*SL	0.22 + 0.002*SL	0.21 + 0.002*SL
	t_F	0.67	0.13 + 0.002*SL	0.12 + 0.002*SL	0.11 + 0.002*SL

*Group1 : SL < 204, *Group2 : 204 ≦SL≦ 307, *Group3 : 307 < SL

STDL80 PHSCKDCU8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 405	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.30	0.97 + 0.001*SL	0.99 + 0.001*SL	0.99 + 0.001*SL
	t_{PHL}	1.08	0.78 + 0.001*SL	0.79 + 0.001*SL	0.79 + 0.001*SL
	t_R	0.84	0.26 + 0.001*SL	0.25 + 0.001*SL	0.23 + 0.002*SL
	t_F	0.67	0.14 + 0.001*SL	0.13 + 0.001*SL	0.12 + 0.001*SL

*Group1 : SL < 270, *Group2 : 270 ≦SL≦ 405, *Group3 : 405 < SL

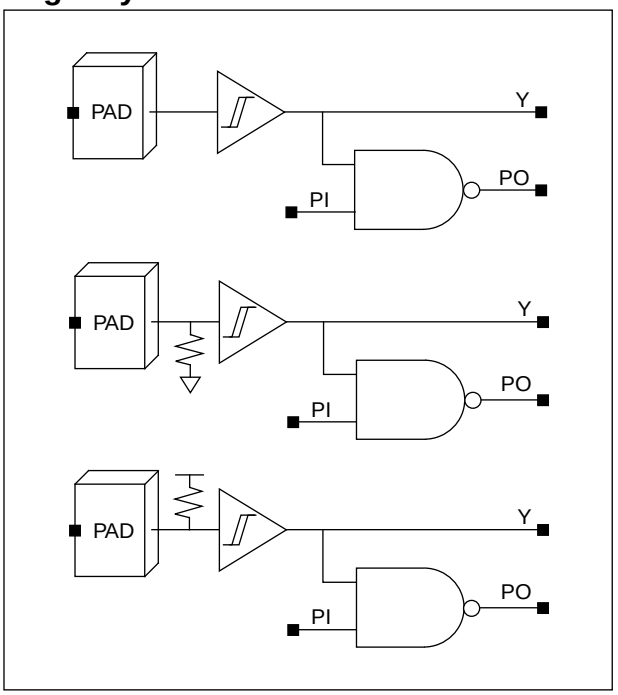
PvSCKDSy/PvSCKDSDy/PvSCKDSUy

CMOS Schmitt Trigger Level Input Clock Drivers

Cell Availability

3.3V Normal	5V Tolerant
PSCKDS(2/4/6/8) PSCKDSD(2/4/6/8) PSCKDSU(2/4/6/8)	PHSCKDS(2/4/6/8) PHSCKDSD(2/4/6/8) PHSCKDSU(2/4/6/8)

Logic Symbol



Input Load (SL)

	PI
PSCKDS(2/4/6/8)	3.0
PSCKDSD(2/4/6/8)	3.0
PSCKDSU(2/4/6/8)	3.0
PHSCKDS(2/4/6/8)	3.0
PHSCKDSD(2/4/6/8)	3.0
PHSCKDSU(2/4/6/8)	3.0

I/O Slot

PvSCKDSy/PvSCKDSDy/PvSCKDSUy	1.0

STDL80 PSCKDS2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 103	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.81	0.49 + 0.003*SL	0.51 + 0.003*SL	0.51 + 0.003*SL
	t_{PHL}	1.14	0.79 + 0.003*SL	0.81 + 0.003*SL	0.82 + 0.003*SL
	t_R	0.79	0.17 + 0.006*SL	0.17 + 0.006*SL	0.17 + 0.006*SL
	t_F	0.78	0.24 + 0.005*SL	0.24 + 0.005*SL	0.23 + 0.005*SL

*Group1 : SL < 69, *Group2 : 69 ≦ SL ≦ 103, *Group3 : 103 < SL

STDL80 PSCKDS4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 202	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.96	0.63 + 0.002*SL	0.65 + 0.002*SL	0.66 + 0.001*SL
	t_{PHL}	1.44	1.07 + 0.002*SL	1.09 + 0.002*SL	1.11 + 0.002*SL
	t_R	0.83	0.24 + 0.003*SL	0.23 + 0.003*SL	0.23 + 0.003*SL
	t_F	0.88	0.36 + 0.003*SL	0.35 + 0.003*SL	0.35 + 0.003*SL

*Group1 : SL < 135, *Group2 : 135 ≦ SL ≦ 202, *Group3 : 202 < SL

STDL80 PSCKDS6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 307	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.94	0.62 + 0.001*SL	0.63 + 0.001*SL	0.64 + 0.001*SL
	t_{PHL}	1.37	1.01 + 0.001*SL	1.03 + 0.001*SL	1.05 + 0.001*SL
	t_R	0.80	0.20 + 0.002*SL	0.20 + 0.002*SL	0.19 + 0.002*SL
	t_F	0.83	0.28 + 0.002*SL	0.28 + 0.002*SL	0.28 + 0.002*SL

*Group1 : SL < 204, *Group2 : 204 ≦ SL ≦ 307, *Group3 : 307 < SL

STDL80 PSCKDS8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 405	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.02	0.69 + 0.001*SL	0.70 + 0.001*SL	0.72 + 0.001*SL
	t_{PHL}	1.52	1.15 + 0.001*SL	1.18 + 0.001*SL	1.19 + 0.001*SL
	t_R	0.83	0.23 + 0.001*SL	0.23 + 0.001*SL	0.22 + 0.001*SL
	t_F	0.87	0.35 + 0.001*SL	0.34 + 0.001*SL	0.34 + 0.001*SL

*Group1 : SL < 270, *Group2 : 270 ≦ SL ≦ 405, *Group3 : 405 < SL

STDL80 PSCKDSD2 Switching Characteristics

[Delays for typical process, 25℃, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 103	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.83	0.51 + 0.003*SL	0.52 + 0.003*SL	0.53 + 0.003*SL
	t_{PHL}	1.16	0.81 + 0.003*SL	0.83 + 0.003*SL	0.84 + 0.003*SL
	t_R	0.79	0.18 + 0.006*SL	0.17 + 0.006*SL	0.17 + 0.006*SL
	t_F	0.78	0.24 + 0.005*SL	0.24 + 0.005*SL	0.23 + 0.005*SL

*Group1 : SL < 69, *Group2 : 69 ≦ SL ≦ 103, *Group3 : 103 < SL

STDL80 PSCKDSD4 Switching Characteristics

[Delays for typical process, 25℃, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 202	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.98	0.65 + 0.002*SL	0.66 + 0.002*SL	0.68 + 0.001*SL
	t_{PHL}	1.46	1.09 + 0.002*SL	1.11 + 0.002*SL	1.13 + 0.002*SL
	t_R	0.83	0.24 + 0.003*SL	0.24 + 0.003*SL	0.23 + 0.003*SL
	t_F	0.88	0.36 + 0.003*SL	0.35 + 0.003*SL	0.35 + 0.003*SL

*Group1 : SL < 135, *Group2 : 135 ≦ SL ≦ 202, *Group3 : 202 < SL

STDL80 PSCKDSD6 Switching Characteristics

[Delays for typical process, 25℃, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 307	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.96	0.64 + 0.001*SL	0.65 + 0.001*SL	0.66 + 0.001*SL
	t_{PHL}	1.39	1.02 + 0.001*SL	1.05 + 0.001*SL	1.06 + 0.001*SL
	t_R	0.81	0.20 + 0.002*SL	0.19 + 0.002*SL	0.19 + 0.002*SL
	t_F	0.82	0.29 + 0.002*SL	0.28 + 0.002*SL	0.28 + 0.002*SL

*Group1 : SL < 204, *Group2 : 204 ≦ SL ≦ 307, *Group3 : 307 < SL

STDL80 PSCKDSD8 Switching Characteristics

[Delays for typical process, 25℃, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 405	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.04	0.71 + 0.001*SL	0.72 + 0.001*SL	0.73 + 0.001*SL
	t_{PHL}	1.54	1.17 + 0.001*SL	1.19 + 0.001*SL	1.21 + 0.001*SL
	t_R	0.83	0.23 + 0.001*SL	0.23 + 0.001*SL	0.23 + 0.001*SL
	t_F	0.87	0.35 + 0.001*SL	0.34 + 0.001*SL	0.34 + 0.001*SL

*Group1 : SL < 270, *Group2 : 270 ≦ SL ≦ 405, *Group3 : 405 < SL

STDL80 PSCKDSU2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 103	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.81	0.49 + 0.003*SL	0.51 + 0.003*SL	0.52 + 0.003*SL
	t_{PHL}	1.16	0.81 + 0.003*SL	0.83 + 0.003*SL	0.84 + 0.003*SL
	t_R	0.79	0.18 + 0.006*SL	0.17 + 0.006*SL	0.16 + 0.006*SL
	t_F	0.78	0.24 + 0.005*SL	0.24 + 0.005*SL	0.23 + 0.005*SL

*Group1 : SL < 69, *Group2 : 69 ≦ SL ≦ 103, *Group3 : 103 < SL

STDL80 PSCKDSU4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 202	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.96	0.63 + 0.002*SL	0.65 + 0.002*SL	0.66 + 0.001*SL
	t_{PHL}	1.46	1.09 + 0.002*SL	1.12 + 0.002*SL	1.14 + 0.002*SL
	t_R	0.83	0.24 + 0.003*SL	0.23 + 0.003*SL	0.23 + 0.003*SL
	t_F	0.88	0.36 + 0.003*SL	0.35 + 0.003*SL	0.35 + 0.003*SL

*Group1 : SL < 135, *Group2 : 135 ≦ SL ≦ 202, *Group3 : 202 < SL

STDL80 PSCKDSU6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 307	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	0.94	0.62 + 0.001*SL	0.63 + 0.001*SL	0.64 + 0.001*SL
	t_{PHL}	1.39	1.03 + 0.001*SL	1.05 + 0.001*SL	1.07 + 0.001*SL
	t_R	0.80	0.20 + 0.002*SL	0.20 + 0.002*SL	0.19 + 0.002*SL
	t_F	0.83	0.29 + 0.002*SL	0.29 + 0.002*SL	0.28 + 0.002*SL

*Group1 : SL < 204, *Group2 : 204 ≦ SL ≦ 307, *Group3 : 307 < SL

STDL80 PSCKDSU8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 405	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.02	0.69 + 0.001*SL	0.70 + 0.001*SL	0.71 + 0.001*SL
	t_{PHL}	1.55	1.18 + 0.001*SL	1.20 + 0.001*SL	1.22 + 0.001*SL
	t_R	0.83	0.23 + 0.001*SL	0.23 + 0.001*SL	0.22 + 0.001*SL
	t_F	0.88	0.36 + 0.001*SL	0.35 + 0.001*SL	0.35 + 0.001*SL

*Group1 : SL < 270, *Group2 : 270 ≦ SL ≦ 405, *Group3 : 405 < SL

STDL80 PHSCKDS2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 103	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.70	1.37 + 0.003*SL	1.39 + 0.003*SL	1.40 + 0.003*SL
	t_{PHL}	1.47	1.12 + 0.003*SL	1.14 + 0.003*SL	1.16 + 0.003*SL
	t_R	0.84	0.25 + 0.006*SL	0.25 + 0.006*SL	0.23 + 0.006*SL
	t_F	0.79	0.24 + 0.005*SL	0.24 + 0.005*SL	0.23 + 0.005*SL

*Group1 : SL < 69, *Group2 : 69 ≦SL≦ 103, *Group3 : 103 < SL

STDL80 PHSCKDS4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 202	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	2.04	1.70 + 0.002*SL	1.72 + 0.002*SL	1.73 + 0.002*SL
	t_{PHL}	1.78	1.41 + 0.002*SL	1.44 + 0.002*SL	1.46 + 0.002*SL
	t_R	0.93	0.36 + 0.003*SL	0.35 + 0.003*SL	0.35 + 0.003*SL
	t_F	0.89	0.36 + 0.003*SL	0.36 + 0.003*SL	0.36 + 0.003*SL

*Group1 : SL < 135, *Group2 : 135 ≦SL≦ 202, *Group3 : 202 < SL

STDL80 PHSCKDS6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 307	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	2.15	1.81 + 0.001*SL	1.83 + 0.001*SL	1.84 + 0.001*SL
	t_{PHL}	1.91	1.55 + 0.001*SL	1.57 + 0.001*SL	1.59 + 0.001*SL
	t_R	0.89	0.32 + 0.002*SL	0.31 + 0.002*SL	0.30 + 0.002*SL
	t_F	0.83	0.30 + 0.002*SL	0.30 + 0.002*SL	0.29 + 0.002*SL

*Group1 : SL < 204, *Group2 : 204 ≦SL≦ 307, *Group3 : 307 < SL

STDL80 PHSCKDS8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 405	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	2.32	1.98 + 0.001*SL	2.00 + 0.001*SL	2.02 + 0.001*SL
	t_{PHL}	2.07	1.70 + 0.001*SL	1.73 + 0.001*SL	1.75 + 0.001*SL
	t_R	0.93	0.38 + 0.001*SL	0.37 + 0.001*SL	0.35 + 0.001*SL
	t_F	0.89	0.36 + 0.001*SL	0.36 + 0.001*SL	0.36 + 0.001*SL

*Group1 : SL < 270, *Group2 : 270 ≦SL≦ 405, *Group3 : 405 < SL

STDL80 PHSCKDSD2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 103	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.92	1.60 + 0.003*SL	1.61 + 0.003*SL	1.63 + 0.003*SL
	t_{PHL}	1.41	1.06 + 0.003*SL	1.08 + 0.003*SL	1.10 + 0.003*SL
	t_R	0.85	0.27 + 0.006*SL	0.26 + 0.006*SL	0.25 + 0.006*SL
	t_F	0.79	0.24 + 0.005*SL	0.24 + 0.005*SL	0.24 + 0.005*SL

*Group1 : SL < 69, *Group2 : 69 ≦ SL ≦ 103, *Group3 : 103 < SL

STDL80 PHSCKDSD4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 202	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	2.32	1.98 + 0.002*SL	2.00 + 0.002*SL	2.01 + 0.002*SL
	t_{PHL}	1.72	1.35 + 0.002*SL	1.37 + 0.002*SL	1.39 + 0.002*SL
	t_R	0.95	0.40 + 0.003*SL	0.38 + 0.003*SL	0.37 + 0.003*SL
	t_F	0.88	0.36 + 0.003*SL	0.36 + 0.003*SL	0.35 + 0.003*SL

*Group1 : SL < 135, *Group2 : 135 ≦ SL ≦ 202, *Group3 : 202 < SL

STDL80 PHSCKDSD6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 307	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	2.37	2.03 + 0.001*SL	2.05 + 0.001*SL	2.06 + 0.001*SL
	t_{PHL}	1.77	1.41 + 0.001*SL	1.43 + 0.001*SL	1.45 + 0.001*SL
	t_R	0.90	0.34 + 0.002*SL	0.32 + 0.002*SL	0.32 + 0.002*SL
	t_F	0.84	0.30 + 0.002*SL	0.29 + 0.002*SL	0.29 + 0.002*SL

*Group1 : SL < 204, *Group2 : 204 ≦ SL ≦ 307, *Group3 : 307 < SL

STDL80 PHSCKDSD8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 405	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	2.56	2.22 + 0.001*SL	2.25 + 0.001*SL	2.26 + 0.001*SL
	t_{PHL}	1.93	1.56 + 0.001*SL	1.59 + 0.001*SL	1.61 + 0.001*SL
	t_R	0.95	0.41 + 0.001*SL	0.39 + 0.001*SL	0.38 + 0.001*SL
	t_F	0.89	0.37 + 0.001*SL	0.36 + 0.001*SL	0.35 + 0.001*SL

*Group1 : SL < 270, *Group2 : 270 ≦ SL ≦ 405, *Group3 : 405 < SL

STDL80 PHSCKDSU2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 103	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.60	1.27 + 0.003*SL	1.29 + 0.003*SL	1.30 + 0.003*SL
	t_{PHL}	1.62	1.27 + 0.003*SL	1.29 + 0.003*SL	1.31 + 0.003*SL
	t_R	0.84	0.24 + 0.006*SL	0.23 + 0.006*SL	0.23 + 0.006*SL
	t_F	0.79	0.24 + 0.005*SL	0.24 + 0.005*SL	0.24 + 0.005*SL

*Group1 : SL < 69, *Group2 : 69 ≦ SL ≦ 103, *Group3 : 103 < SL

STDL80 PHSCKDSU4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 202	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	1.91	1.57 + 0.002*SL	1.60 + 0.002*SL	1.60 + 0.002*SL
	t_{PHL}	1.95	1.58 + 0.002*SL	1.60 + 0.002*SL	1.62 + 0.002*SL
	t_R	0.91	0.35 + 0.003*SL	0.34 + 0.003*SL	0.33 + 0.003*SL
	t_F	0.89	0.37 + 0.003*SL	0.36 + 0.003*SL	0.36 + 0.003*SL

*Group1 : SL < 135, *Group2 : 135 ≦ SL ≦ 202, *Group3 : 202 < SL

STDL80 PHSCKDSU6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 307	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	2.02	1.69 + 0.001*SL	1.71 + 0.001*SL	1.72 + 0.001*SL
	t_{PHL}	2.12	1.75 + 0.001*SL	1.77 + 0.001*SL	1.79 + 0.001*SL
	t_R	0.88	0.30 + 0.002*SL	0.30 + 0.002*SL	0.28 + 0.002*SL
	t_F	0.84	0.30 + 0.002*SL	0.30 + 0.002*SL	0.29 + 0.002*SL

*Group1 : SL < 204, *Group2 : 204 ≦ SL ≦ 307, *Group3 : 307 < SL

STDL80 PHSCKDSU8 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 405	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PAD to Y	t_{PLH}	2.18	1.85 + 0.001*SL	1.87 + 0.001*SL	1.88 + 0.001*SL
	t_{PHL}	2.29	1.91 + 0.001*SL	1.94 + 0.001*SL	1.96 + 0.001*SL
	t_R	0.92	0.37 + 0.001*SL	0.35 + 0.001*SL	0.34 + 0.001*SL
	t_F	0.89	0.37 + 0.001*SL	0.36 + 0.001*SL	0.36 + 0.001*SL

*Group1 : SL < 270, *Group2 : 270 ≦ SL ≦ 405, *Group3 : 405 < SL

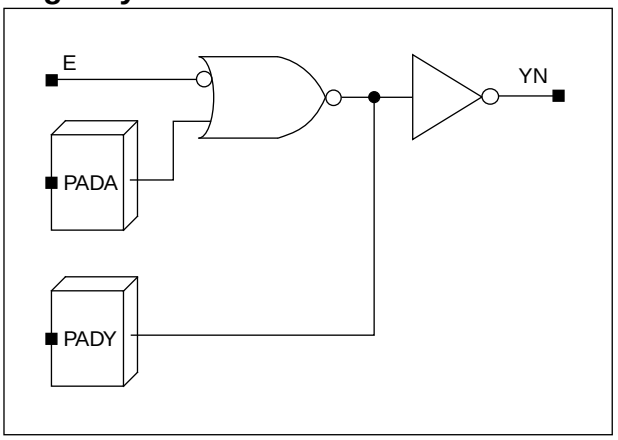
Cell List

Cell Name	Function Description
PSOSCK1	Oscillator Cell with Enable (~ 100KHz)
PSOSCK2	Oscillator Cell with Enable (100K ~ 1MHz)
PSOSCK16	Oscillator Cell with Enable and Resistor (~ 100KHz)
PSOSCK26	Oscillator Cell with Enable and Resistor (100K ~ 1MHz)
PSOSCM1	Oscillator Cell with Enable (1M ~ 10MHz)
PSOSCM2	Oscillator Cell with Enable (10M ~ 30MHz)
PSOSCM3	Oscillator Cell with Enable (30M ~ 60MHz)
PSOSCM4	Oscillator Cell with Enable (60M ~ 80MHz)
PSOSCM5	Oscillator Cell with Enable (80M ~ 100MHz)
PSOSCM6	Oscillator Cell with Enable (50M ~ 100MHz)
PSOSCM16	Oscillator Cell with Enable and Resistor (1M ~ 10MHz)
PSOSCM26	Oscillator Cell with Enable and Resistor (10M ~ 30MHz)
PSOSCM36	Oscillator Cell with Enable and Resistor (30M ~ 60MHz)
PSOSCM46	Oscillator Cell with Enable and Resistor (60M ~ 80MHz)
PSOSCM56	Oscillator Cell with Enable and Resistor (80M ~ 100MHz)
PSOSCM66	Oscillator Cell with Enable and Resistor (50M ~ 100MHz)

PSOSCK(1/2)

Oscillator Cell with Enable

Logic Symbol



Truth Table

PADA	E	PADY	YN
0	0	0	1
0	1	1	0
1	0	0	1
1	1	0	1

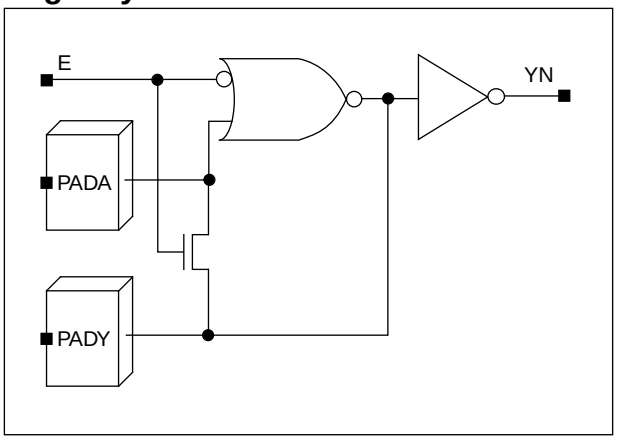
Cell Data

Input Load (SL)	I/O Slots
PSOSCK1/2	*PSOSCK1/2*
E	
2.6	2.0

PSOSCK(16/26)

Oscillator Cell with Enable and Resistor

Logic Symbol



Truth Table

PADA	E	PADY	YN
0	0	0	1
0	1	1	0
1	0	0	1
1	1	0	1

Cell Data

Input Load (SL)	I/O Slots
PSOSCK(16/26)	*PSOSCK(16/26)*
E	
2.6	2.0

STDL80 PSOSCK1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	259.38	0.46 + 5.178*CL	0.49 + 5.178*CL	0.44 + 5.179*CL
	t_{PHL}	349.70	0.50 + 6.984*CL	0.50 + 6.984*CL	0.50 + 6.984*CL
	t_R	582.75	0.55 + 11.644*CL	0.62 + 11.643*CL	0.77 + 11.641*CL
	t_F	772.14	0.82 + 15.426*CL	0.55 + 15.430*CL	0.83 + 15.427*CL

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to PADY	t_{PLH}	259.45	0.53 + 5.178*CL	0.48 + 5.179*CL	0.57 + 5.178*CL
	t_{PHL}	349.81	0.61 + 6.984*CL	0.61 + 6.984*CL	0.61 + 6.984*CL
	t_R	582.75	0.59 + 11.643*CL	0.54 + 11.644*CL	0.70 + 11.642*CL
	t_F	772.14	0.82 + 15.426*CL	0.55 + 15.430*CL	0.83 + 15.427*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.60	0.60 + 0.188*SL	0.61 + 0.187*SL	0.60 + 0.187*SL
	t_{PHL}	0.53	0.53 + 0.137*SL	0.54 + 0.136*SL	0.54 + 0.136*SL
	t_R	0.26	0.26 + 0.086*SL	0.25 + 0.090*SL	0.24 + 0.091*SL
	t_F	0.18	0.18 + 0.072*SL	0.17 + 0.075*SL	0.17 + 0.075*SL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to YN	t_{PLH}	0.72	0.72 + 0.188*SL	0.72 + 0.187*SL	0.72 + 0.187*SL
	t_{PHL}	0.60	0.60 + 0.137*SL	0.61 + 0.136*SL	0.61 + 0.136*SL
	t_R	0.25	0.25 + 0.088*SL	0.25 + 0.090*SL	0.24 + 0.091*SL
	t_F	0.18	0.18 + 0.073*SL	0.17 + 0.075*SL	0.17 + 0.075*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCK2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	26.32	0.43 + 0.518*CL	0.42 + 0.518*CL	0.43 + 0.518*CL
	t_{PHL}	35.38	0.46 + 0.698*CL	0.46 + 0.698*CL	0.46 + 0.698*CL
	t_R	58.61	0.39 + 1.164*CL	0.40 + 1.164*CL	0.37 + 1.165*CL
	t_F	77.67	0.54 + 1.543*CL	0.51 + 1.543*CL	0.54 + 1.543*CL

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to PADY	t_{PLH}	26.40	0.50 + 0.518*CL	0.50 + 0.518*CL	0.51 + 0.518*CL
	t_{PHL}	35.48	0.56 + 0.698*CL	0.56 + 0.698*CL	0.56 + 0.698*CL
	t_R	58.61	0.39 + 1.164*CL	0.40 + 1.164*CL	0.37 + 1.165*CL
	t_F	77.67	0.52 + 1.543*CL	0.59 + 1.542*CL	0.53 + 1.543*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.54	0.54 + 0.023*SL	0.54 + 0.022*SL	0.55 + 0.021*SL
	t_{PHL}	0.46	0.46 + 0.015*SL	0.46 + 0.015*SL	0.47 + 0.014*SL
	t_R	0.20	0.20 + 0.009*SL	0.20 + 0.010*SL	0.19 + 0.011*SL
	t_F	0.14	0.14 + 0.008*SL	0.14 + 0.008*SL	0.13 + 0.008*SL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to YN	t_{PLH}	0.66	0.66 + 0.021*SL	0.66 + 0.021*SL	0.66 + 0.021*SL
	t_{PHL}	0.54	0.54 + 0.016*SL	0.54 + 0.015*SL	0.54 + 0.014*SL
	t_R	0.18	0.18 + 0.010*SL	0.18 + 0.010*SL	0.18 + 0.011*SL
	t_F	0.13	0.13 + 0.008*SL	0.13 + 0.008*SL	0.13 + 0.008*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCK16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	259.38	0.46 + 5.178*CL	0.49 + 5.178*CL	0.44 + 5.179*CL
	t_{PHL}	349.70	0.50 + 6.984*CL	0.50 + 6.984*CL	0.50 + 6.984*CL
	t_R	582.75	0.55 + 11.644*CL	0.62 + 11.643*CL	0.77 + 11.641*CL
	t_F	772.14	0.82 + 15.426*CL	0.55 + 15.430*CL	0.83 + 15.427*CL

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to PADY	t_{PLH}	259.45	0.53 + 5.178*CL	0.48 + 5.179*CL	0.57 + 5.178*CL
	t_{PHL}	349.81	0.61 + 6.984*CL	0.61 + 6.984*CL	0.61 + 6.984*CL
	t_R	582.75	0.59 + 11.643*CL	0.54 + 11.644*CL	0.70 + 11.642*CL
	t_F	772.14	0.82 + 15.426*CL	0.55 + 15.430*CL	0.83 + 15.427*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.60	0.60 + 0.188*SL	0.61 + 0.187*SL	0.60 + 0.187*SL
	t_{PHL}	0.53	0.53 + 0.137*SL	0.54 + 0.136*SL	0.54 + 0.136*SL
	t_R	0.26	0.26 + 0.086*SL	0.25 + 0.090*SL	0.24 + 0.091*SL
	t_F	0.18	0.18 + 0.072*SL	0.17 + 0.075*SL	0.17 + 0.075*SL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to YN	t_{PLH}	0.72	0.72 + 0.188*SL	0.72 + 0.187*SL	0.72 + 0.187*SL
	t_{PHL}	0.60	0.60 + 0.137*SL	0.61 + 0.136*SL	0.61 + 0.136*SL
	t_R	0.25	0.25 + 0.088*SL	0.25 + 0.090*SL	0.24 + 0.091*SL
	t_F	0.18	0.18 + 0.073*SL	0.17 + 0.075*SL	0.17 + 0.075*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCK26 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R, t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	26.32	0.43 + 0.518*CL	0.42 + 0.518*CL	0.43 + 0.518*CL
	t_{PHL}	35.38	0.46 + 0.698*CL	0.46 + 0.698*CL	0.46 + 0.698*CL
	t_R	58.61	0.39 + 1.164*CL	0.40 + 1.164*CL	0.37 + 1.165*CL
	t_F	77.67	0.54 + 1.543*CL	0.51 + 1.543*CL	0.54 + 1.543*CL

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to PADY	t_{PLH}	26.40	0.50 + 0.518*CL	0.50 + 0.518*CL	0.51 + 0.518*CL
	t_{PHL}	35.48	0.56 + 0.698*CL	0.56 + 0.698*CL	0.56 + 0.698*CL
	t_R	58.61	0.39 + 1.164*CL	0.40 + 1.164*CL	0.37 + 1.165*CL
	t_F	77.67	0.52 + 1.543*CL	0.59 + 1.542*CL	0.53 + 1.543*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.54	0.54 + 0.023*SL	0.54 + 0.022*SL	0.55 + 0.021*SL
	t_{PHL}	0.46	0.46 + 0.015*SL	0.46 + 0.015*SL	0.47 + 0.014*SL
	t_R	0.20	0.20 + 0.009*SL	0.20 + 0.010*SL	0.19 + 0.011*SL
	t_F	0.14	0.14 + 0.008*SL	0.14 + 0.008*SL	0.13 + 0.008*SL

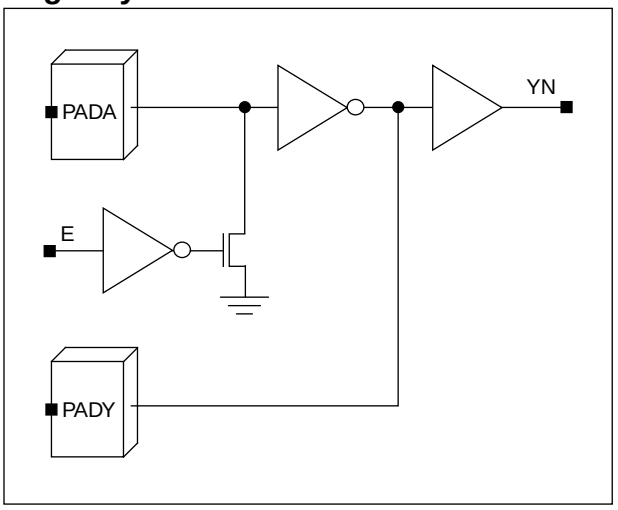
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
E to YN	t_{PLH}	0.66	0.66 + 0.021*SL	0.66 + 0.021*SL	0.66 + 0.021*SL
	t_{PHL}	0.54	0.54 + 0.016*SL	0.54 + 0.015*SL	0.54 + 0.014*SL
	t_R	0.18	0.18 + 0.010*SL	0.18 + 0.010*SL	0.18 + 0.011*SL
	t_F	0.13	0.13 + 0.008*SL	0.13 + 0.008*SL	0.13 + 0.008*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

PSOSCM(1/2/3/4/5/6)

Oscillator Cell with Enable

Logic Symbol



Truth Table

SEC Tester Standard

PADA	E	PADY	YN
0	0	1	1
0	1	1	1
1	0	x	x
1	1	0	0

Real Application

PADA	E	PADY	YN
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

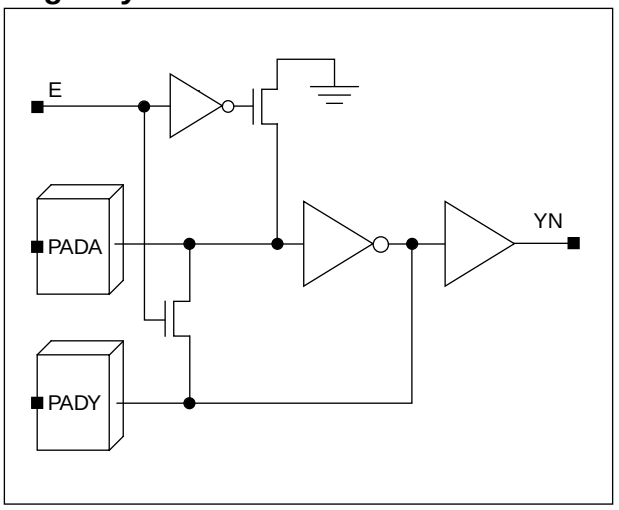
Cell Data

Input Load (SL)	I/O Slots
PSOSCM(1/2/3/4/5/6)	*PSOSCM(1/2/3/4/5/6)*
E	
2.6	2.0

PSOSCM(16/26/36/46/56/66)

Oscillator Cell with Enable and Resistor

Logic Symbol



Truth Table

SEC Tester Standard

PADA	E	PADY	YN
0	0	1	1
0	1	1	1
1	0	x	x
1	1	0	0

Real Application

PADA	E	PADY	YN
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

Cell Data

Input Load (SL)	I/O Slots
PSOSCM (16/26/36/46/56/66)	*PSOSCM (16/26/36/46/56/66)*
E	
2.6	2.0

STDL80 PSOSCM1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.24 + 0.004*SL	0.24 + 0.004*SL
	t_R	0.10	0.10 + 0.001*SL	0.09 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCM2 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.24 + 0.004*SL	0.24 + 0.004*SL
	t_R	0.10	0.10 + 0.001*SL	0.09 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCM3 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	1.41	0.12 + 0.026*CL	0.12 + 0.026*CL	0.12 + 0.026*CL
	t_{PHL}	1.87	0.12 + 0.035*CL	0.12 + 0.035*CL	0.12 + 0.035*CL
	t_R	3.00	0.10 + 0.058*CL	0.09 + 0.058*CL	0.09 + 0.058*CL
	t_F	3.96	0.11 + 0.077*CL	0.11 + 0.077*CL	0.10 + 0.077*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.19	0.19 + 0.003*SL	0.19 + 0.003*SL	0.20 + 0.002*SL
	t_{PHL}	0.21	0.21 + 0.002*SL	0.21 + 0.003*SL	0.21 + 0.003*SL
	t_R	0.10	0.10 + 0.003*SL	0.10 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.08	0.08 + 0.004*SL	0.09 + 0.001*SL	0.08 + 0.003*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCM4 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.76	0.12 + 0.013*CL	0.12 + 0.013*CL	0.12 + 0.013*CL
	t_{PHL}	0.99	0.12 + 0.017*CL	0.11 + 0.017*CL	0.12 + 0.017*CL
	t_R	1.54	0.10 + 0.029*CL	0.09 + 0.029*CL	0.09 + 0.029*CL
	t_F	2.02	0.10 + 0.038*CL	0.10 + 0.038*CL	0.10 + 0.038*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.002*SL	0.23 + 0.002*SL	0.23 + 0.002*SL
	t_R	0.11	0.11 + 0.000*SL	0.11 + 0.001*SL	0.10 + 0.001*SL
	t_F	0.09	0.09 + 0.001*SL	0.09 + 0.001*SL	0.09 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCM5 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.55	0.11 + 0.009*CL	0.11 + 0.009*CL	0.12 + 0.009*CL
	t_{PHL}	0.70	0.12 + 0.012*CL	0.12 + 0.012*CL	0.11 + 0.012*CL
	t_R	1.06	0.10 + 0.019*CL	0.09 + 0.019*CL	0.09 + 0.019*CL
	t_F	1.38	0.10 + 0.025*CL	0.10 + 0.026*CL	0.09 + 0.026*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.001*SL	0.23 + 0.001*SL	0.23 + 0.001*SL
	t_R	0.11	0.11 + 0.001*SL	0.11 + 0.000*SL	0.10 + 0.001*SL
	t_F	0.10	0.10 + 0.001*SL	0.10 + 0.000*SL	0.09 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCM6 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.44	0.11 + 0.007*CL	0.11 + 0.007*CL	0.12 + 0.006*CL
	t_{PHL}	0.55	0.11 + 0.009*CL	0.12 + 0.009*CL	0.11 + 0.009*CL
	t_R	0.82	0.11 + 0.014*CL	0.11 + 0.014*CL	0.09 + 0.014*CL
	t_F	1.06	0.11 + 0.019*CL	0.10 + 0.019*CL	0.10 + 0.019*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.25	0.25 + 0.001*SL	0.25 + 0.001*SL	0.25 + 0.001*SL
	t_{PHL}	0.26	0.26 + 0.002*SL	0.26 + 0.001*SL	0.26 + 0.001*SL
	t_R	0.11	0.11 + 0.001*SL	0.11 + 0.001*SL	0.11 + 0.001*SL
	t_F	0.11	0.11 + 0.001*SL	0.11 + 0.001*SL	0.10 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCM16 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.24 + 0.004*SL	0.24 + 0.004*SL
	t_R	0.10	0.10 + 0.001*SL	0.09 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCM26 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	2.72	0.13 + 0.052*CL	0.13 + 0.052*CL	0.13 + 0.052*CL
	t_{PHL}	3.62	0.13 + 0.070*CL	0.14 + 0.070*CL	0.13 + 0.070*CL
	t_R	5.93	0.11 + 0.116*CL	0.11 + 0.116*CL	0.10 + 0.116*CL
	t_F	7.85	0.13 + 0.154*CL	0.13 + 0.154*CL	0.13 + 0.154*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.004*SL	0.22 + 0.003*SL	0.22 + 0.003*SL
	t_{PHL}	0.24	0.24 + 0.005*SL	0.24 + 0.004*SL	0.24 + 0.004*SL
	t_R	0.10	0.10 + 0.001*SL	0.09 + 0.002*SL	0.09 + 0.002*SL
	t_F	0.08	0.08 + 0.003*SL	0.08 + 0.003*SL	0.08 + 0.002*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCM36 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	1.41	0.12 + 0.026*CL	0.12 + 0.026*CL	0.12 + 0.026*CL
	t_{PHL}	1.87	0.12 + 0.035*CL	0.12 + 0.035*CL	0.12 + 0.035*CL
	t_R	3.00	0.10 + 0.058*CL	0.09 + 0.058*CL	0.09 + 0.058*CL
	t_F	3.96	0.11 + 0.077*CL	0.11 + 0.077*CL	0.10 + 0.077*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.19	0.19 + 0.003*SL	0.19 + 0.003*SL	0.20 + 0.002*SL
	t_{PHL}	0.21	0.21 + 0.002*SL	0.21 + 0.003*SL	0.21 + 0.003*SL
	t_R	0.10	0.10 + 0.003*SL	0.10 + 0.002*SL	0.10 + 0.002*SL
	t_F	0.08	0.08 + 0.004*SL	0.09 + 0.001*SL	0.08 + 0.003*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCM46 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.76	0.12 + 0.013*CL	0.12 + 0.013*CL	0.12 + 0.013*CL
	t_{PHL}	0.99	0.12 + 0.017*CL	0.11 + 0.017*CL	0.12 + 0.017*CL
	t_R	1.54	0.10 + 0.029*CL	0.09 + 0.029*CL	0.09 + 0.029*CL
	t_F	2.02	0.10 + 0.038*CL	0.10 + 0.038*CL	0.10 + 0.038*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.002*SL	0.23 + 0.002*SL	0.23 + 0.002*SL
	t_R	0.11	0.11 + 0.000*SL	0.11 + 0.001*SL	0.10 + 0.001*SL
	t_F	0.09	0.09 + 0.001*SL	0.09 + 0.001*SL	0.09 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCM56 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.55	0.11 + 0.009*CL	0.11 + 0.009*CL	0.12 + 0.009*CL
	t_{PHL}	0.70	0.12 + 0.012*CL	0.12 + 0.012*CL	0.11 + 0.012*CL
	t_R	1.06	0.10 + 0.019*CL	0.09 + 0.019*CL	0.09 + 0.019*CL
	t_F	1.38	0.10 + 0.025*CL	0.10 + 0.026*CL	0.09 + 0.026*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.22	0.22 + 0.001*SL	0.22 + 0.001*SL	0.22 + 0.001*SL
	t_{PHL}	0.23	0.23 + 0.001*SL	0.23 + 0.001*SL	0.23 + 0.001*SL
	t_R	0.11	0.11 + 0.001*SL	0.11 + 0.000*SL	0.10 + 0.001*SL
	t_F	0.10	0.10 + 0.001*SL	0.10 + 0.000*SL	0.09 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

STDL80 PSOSCM66 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to PADY	t_{PLH}	0.44	0.11 + 0.007*CL	0.11 + 0.007*CL	0.12 + 0.006*CL
	t_{PHL}	0.55	0.11 + 0.009*CL	0.12 + 0.009*CL	0.11 + 0.009*CL
	t_R	0.82	0.11 + 0.014*CL	0.11 + 0.014*CL	0.09 + 0.014*CL
	t_F	1.06	0.11 + 0.019*CL	0.10 + 0.019*CL	0.10 + 0.019*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
PADA to YN	t_{PLH}	0.25	0.25 + 0.001*SL	0.25 + 0.001*SL	0.25 + 0.001*SL
	t_{PHL}	0.26	0.26 + 0.002*SL	0.26 + 0.001*SL	0.26 + 0.001*SL
	t_R	0.11	0.11 + 0.001*SL	0.11 + 0.001*SL	0.11 + 0.001*SL
	t_F	0.11	0.11 + 0.001*SL	0.11 + 0.001*SL	0.10 + 0.001*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

PCI BUFFERS

Overview

PCI buffers are designed for PCI local bus application which is an industry-standard, high-performance 32- or 64-bit bus architecture.

SEC ASIC supports 5V and 3.3V signalling environment PCI bi-directional buffers. But in STDL80, only 3.3V signaling environment bi-directional buffers are suppported. One is a normal type, and the other is a 5V tolerant type. The tolerant type of PCI buffer is larger than the normal type, and requires 5V power supply.

Features

– High performance
– Low cost
– Easy use
– Longevity: both 5V and 3.3V signalling environments specified.

Cell List

Cell Name	Function Description
PSPCIA3	3.3V PCI Buffer
PHSPCIA	5V Tolerant PCI Buffer

Electrical Characteristics

SEC ASIC guarantees PCI buffers' electrical characteristics under all conditions (V_{CC} = 3.6V, Temp. = 0°C ~ V_{CC} = 3.0V, Temp. = 125°C).

3.3V DC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply Voltage		3.0	3.6	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CC}$	
V_{IH}	Input High Voltage		$0.5V_{CC}$	V_{CC}[1] + 0.5	
V_{OL}	Output Low Voltage	I_{OUT} = 1500µA		$0.1V_{CC}$	
V_{OH}	Output High Voltage	I_{OUT} = –500µA	$0.9V_{CC}$		
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{CC}$		±10 (±60)[2]	µA
C_{IN}	Input Pin Capacitance			10	pF

3.3V AC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
$I_{OH (AC)}$	Switching Current High	$V_{OUT} = 0.3V_{CC}$	$–12V_{CC}$		mA
		$V_{OUT} = 0.7V_{CC}$		$–32V_{CC}$	
$I_{OL (AC)}$	Switching Current Low	$V_{OUT} = 0.6V_{CC}$	$16V_{CC}$		
		$V_{OUT} = 0.18V_{CC}$	$26.7V_{OUT}$	$38V_{CC}$	
I_{CL}	Low Clamp Current[3]	$–3 < V_{IN} \leq –1$	$–25 + (V_{IN} + 1) / 0.015$		
I_{CH}	High Clamp Current[3]	$V_{CC} + 4 > V_{IN} \geq V_{CC} + 1$	$25 + (V_{IN} – V_{CC} – 1) / 0.015$		
$Slew_R$	Output Rise Slew Rate	$0.2V_{CC}$ to $0.6V_{CC}$	1	4	V/ns
$Slew_F$	Output Fall Slew Rate	$0.6V_{CC}$ to $0.2V_{CC}$	1	4	

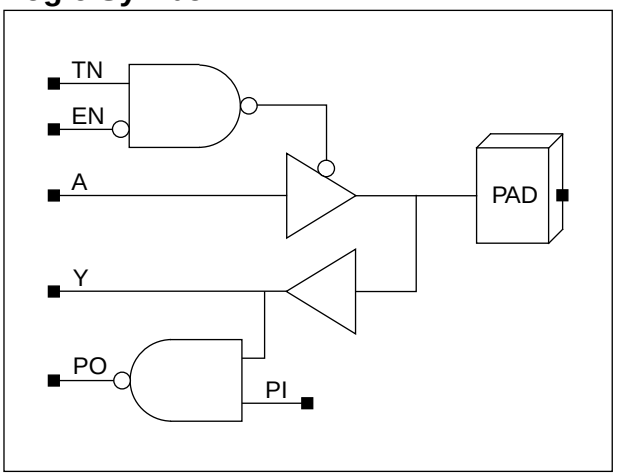
NOTES:

1. In case of a tolerant PCI buffer, V_{CC} = 5V (Bulk Bias).
2. Input current in the tolerant PCI is larger than that in the normal type PCI. However, in the conditions of V_{IN} < 1.4V, V_{IN} > 2.7V, input current is about 0.
3. In case of a tolerant PCI buffer, the Clamp Current is measured at V_{BULK} = 3.3V.

PSPCIA3/PHSPCIA

PCI Buffer

Logic Symbol



Input Load (SL)

	TN	EN	A	PI
PSPCIA3/PHSPCIA	1.0	1.6	3.6	1.0

Truth Table

Input Truth Table

PAD	PI	Y	PO
1	1	1	0
0	x	0	1
1	0	1	1

Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

I/O Slot

PSPCIA3/PHSPCIA	1.0

CARDBUS I/O BUFFERS

Overview

CardBus I/O buffers have 3.3V operation, 32-bit bus width and 33MHz of transmission speed. The latest version of the PC card standard adds information to improve compatibility with the standard by requiring a Card Information Structure (CIS) on every PC card.

The standard has also been enhanced to support the following optional features:

– Low-Voltage Only Operation (3.3V)
– Hardware Direct Memory Access (DMA)
– Multiple-Function Cards
– Industry Standard Power Management Interface (APM)
– High Throughput 32-Bit Bus Mastering Interface (CardBus)

SEC ASIC supports nine different CardBus I/O buffers. CardBus I/O buffers have only 3.3V electrical specifications. Regardless of the I/O voltage, S3V5V pin controls the same input level and output driving current.

For minimizing power consumption, CardBus I/O buffers have a nand type input with a control pin. Therefore, the input buffers operate as active-high input buffers. However, if the control pin is in low state, the output Y is low and not tri-state.

General Description

The CardBus I/O buffer is controlled by S3V5V signal that is logically low in a 5V operation and logically high in a 3.3V operation.

CSTSCHG Buffer Specification

The CSTSCHG pin can be used by the CardBus PC card to remotely power up the system. The design of the CardBus PC card's output buffer and the system's input buffer must ensure no electrical damage results.

– An output buffer for CSTSCHG pin never exceed 1mA.
– An input buffer for CSTSCHG pin is able to withstand sustained forward bias current of 1mA.

CCLK Specification

The electrical characteristics of CCLK follows 3.3V signalling of PCI Local bus specification Revision 2.1. Refer to the PCI buffer electrical characteristics.

CARDBUS I/O BUFFERS

Cell Names & Function Descriptions

Cell Name	Function Description
PITCBU	Universal TTL CardBus Input Buffer with Pull-Up
POTCBU	Tri-State CardBus Output Buffer
POTCCKCBU	Tri-State CardBus Output Clock Driver
POTCVSCBU	Tri-State Output Card Voltage Sense
PODCCKCBU	Open Drain CardBus Output Clock Driver
PBTTCBU	Tri-State CardBus Bi-Directional Buffer with Pull-Up
PBTCCKCBU	CardBus Bi-Directional Clock Driver with Pull-Up
PBTCVSCBU	Tri-State Bi-Directional Card Voltage Sense with Pull-Up
PBDCCKCBU	Open Drain CardBus Bi-Directional Clock Driver with Pull-Up

Electrical Characteristics (Normal CardBus interface type buffers)

3.3V DC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply Voltage		3.0	3.6	V
V_{IH}	Input High Voltage		$0.475V_{CC}$	V_{CC} + 0.5	
V_{IL}	Input Low Voltage		–0.5	$0.325V_{CC}$	
V_{OH}	Output High Voltage	I_{OUT} = –150µA	$0.9V_{CC}$		
V_{OL}	Output Low Voltage	I_{OUT} = 700µA		$0.1V_{CC}$	
I_{CC}[1]	Supply Current			1	A
I_{IL}[2]	Input Leakage Current	$0 < V_{IN} < V_{CC}$		±10	µA

NOTES:

1. This is determined solely by the maximum current capacity of the V_{CC} pins on the connector.
2. Input leakage currents include High-Z output leakage for all bi-directional buffers with High-Z outputs. CCD1#, CCD2#, CVS1 and CVS2 do not have to meet leakage requirements.

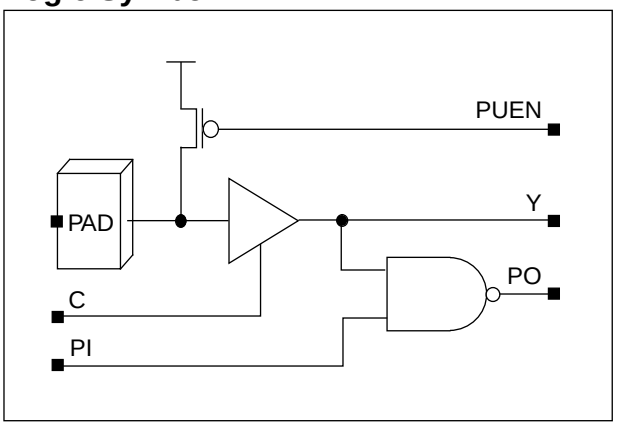
3.3V AC Specifications

Symbol	Parameter	Condition	Min	Max	Unit
t_{RCB}[1]	Output Rise Time	$0.2V_{CC} – 0.6V_{CC}$	0.25	1.0	V/ns
t_{FCB}[1]	Output Fall Time	$0.6V_{CC} – 0.2V_{CC}$	0.25	1.0	
I_{CL}	Low Clamp Current	$–3 < V_{IN} < –1$	$–25 + (V_{IN} + 1) / 0.015$		mA
I_{CH}	High Clamp Current	$V_{CC} + 4 > V_{IN} > V_{CC} + 1$	$25 + (V_{IN} – V_{CC} – 1) / 0.015$		

NOTE:

1. This does not apply to **CCLK**. Minimum and maximum rates are measured with the minimum capacitive load a driver will see (7pF). The values ensure the fastest edge rate will not switch rail-to-rail faster than 3.6ns.

Logic Symbol



Truth Table

PAD	C	PI	Y	PO
1	1	1	1	0
0	1	x	0	1
1	1	0	1	1
x	0	x	0	1

* PUEN (Pull-up control pin) is low enable.

Input Load (SL)

	C	PI
PITCBU	4.0	1.6

I/O Slot

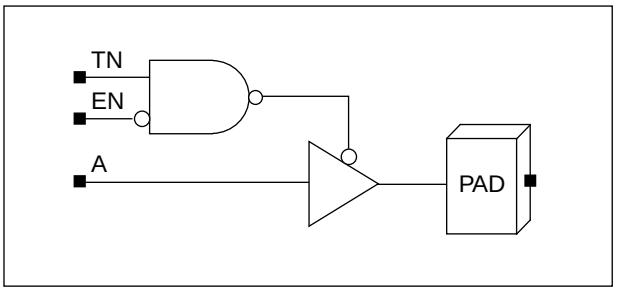
PITCBU	1.0

POTCBU/POTCCKCBU/POTCVSCBU

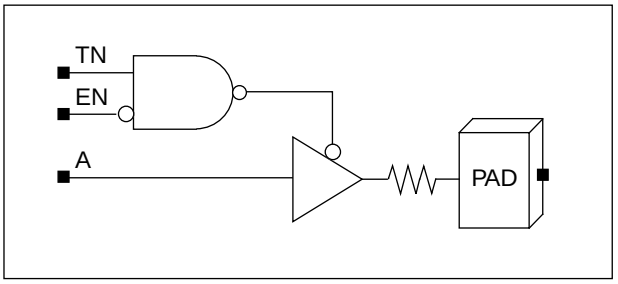
Tri-State CardBus Output Buffers

Logic Symbol

POTCBU/POTCCKCBU



POTCVSCBU



Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

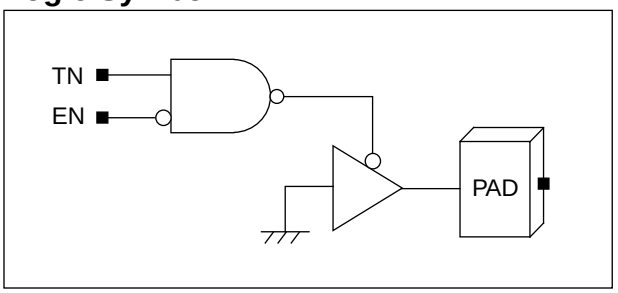
Input Load (SL)

	A	EN	TN
POTCBU/ POTCCKCBU/ POTCVSCBU	2.3	1.2	1.2

I/O Slot

POTCBU/ POTCCKCBU/ POTCVSCBU	1.0

Logic Symbol



Truth Table

EN	TN	PAD
0	1	0
1	x	Hi-Z
x	0	Hi-Z

Input Load (SL)

	EN	TN
PODCCKCBU	1.2	1.2

I/O Slot

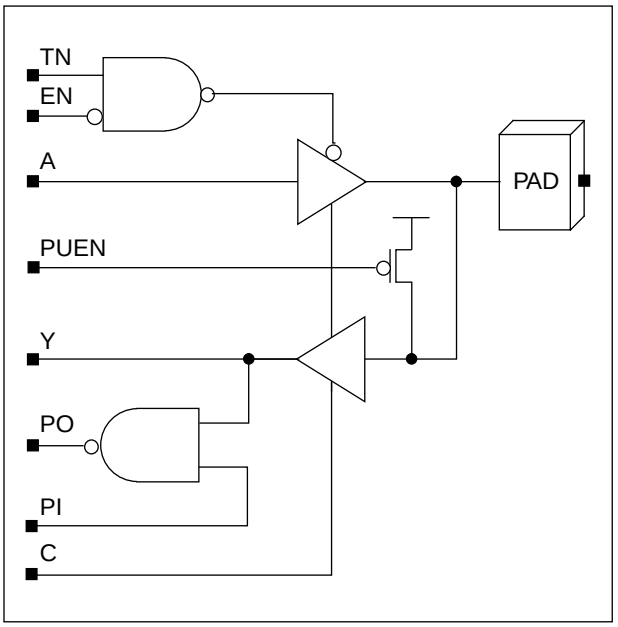
PODCCKCBU	1.0

PBTTCBU/PBTCCKCBU/PBTCVSCBU

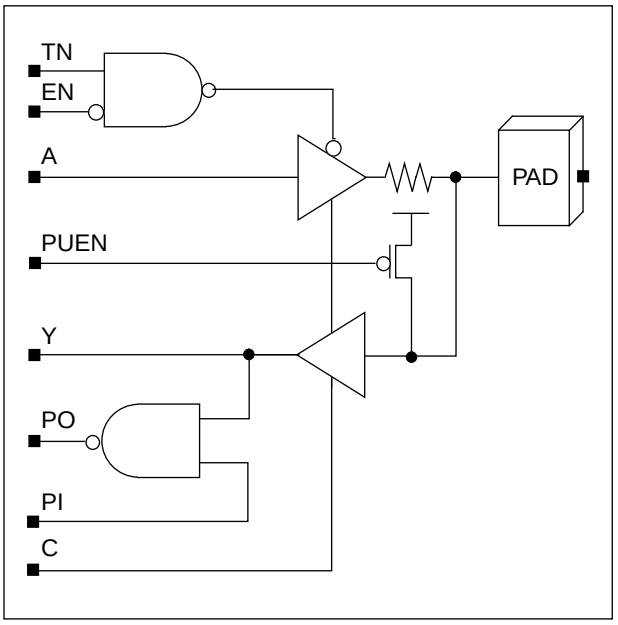
CardBus Bi-Directional Buffers with Pull-Up

Logic Symbol

PBTTCBU/PBTCCKCBU



PBTCVSCBU



Truth Table

Input Truth Table

PAD	C	PI	Y	PO
1	1	1	1	0
0	1	x	0	1
1	1	0	1	1
x	0	x	0	1

Output Truth Table

A	EN	TN	PAD
0	0	1	0
1	0	1	1
x	1	x	Hi-Z
x	x	0	Hi-Z

* PUEN (Pull-up control pin) is low enable.

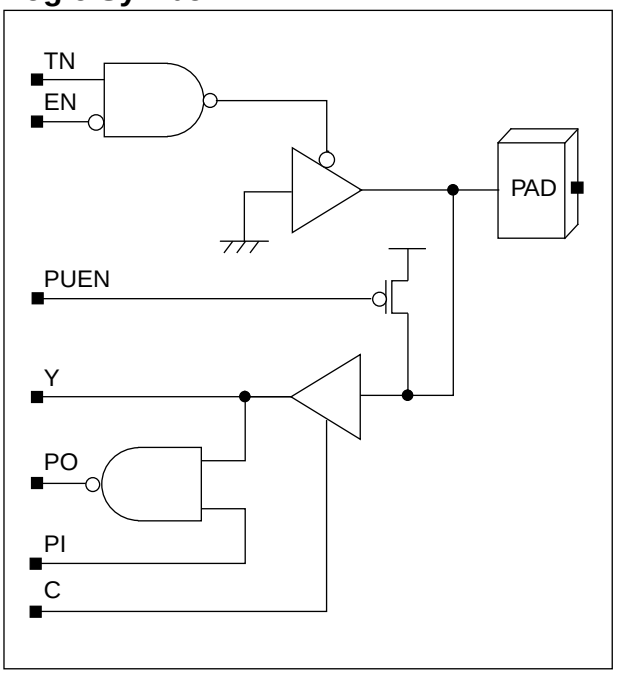
Input Load (SL)

	A	EN	TN	PUEN	C	PI
PBTTCBU/ PBTCCKCBU/ PBTCVSCBU	2.3	1.2	1.2	0.5	4.0	1.6

I/O Slot

PBTTCBU/ PBTCCKCBU/ PBTCVSCBU	1.0

Logic Symbol



Truth Table

Input Truth Table

PAD	C	PI	Y	PO
1	1	1	1	0
0	1	x	0	1
1	1	0	1	1
x	0	x	0	1

Output Truth Table

EN	TN	PAD
0	1	0
1	x	Hi-Z
x	0	Hi-Z

* PUEN (Pull-up control pin) is low enable.

Input Load (SL)

	EN	TN	PUEN	C	PI
PBDCCKCBU	1.2	1.2	0.5	4.0	1.6

I/O Slot

PBDCCKCBU	1.0

USB (Universal Serial Bus) I/O Buffers

Overview

USB I/O buffer consists of a differential input receiver, a differential output driver, two single-ended drivers and two pads. The differential input receiver has 0.8V ~ 2.5V common mode input voltage range and both of the two single-ended receivers have 0.8V and 2.0V as their low and high input threshold voltages, V_{IL}, V_{IH}.

For low power consumption in a stand-by mode, the stand-by (STBYS) pins of two kinds of receivers should be in high state. The differential output drivers has LOw speed Slew Rate (LOSR) pin to select the operation speed and has ENL to achieve bi-directional half duplex operation.

Electrical Specifications

DC Electrical Characteristics

Parameter	Symbol	Condition (Notes 1, 2)	Min	Max	Unit
Supply Current					
High Power Function	I_{CCHPF}			500	mA
Low Power Function	I_{CCLPF}			100	
Unconfig. Function / Hub	I_{CCINIT}			100	
Suspended Device	I_{CCS}			500	µA
Leakage Current					
Hi-Z State Data Line Leakage	I_{LO}	0V < VIN < 3.3V	–10	10	µA
Input Levels					
Differential Input Sensitivity	V_{DI}		0.2		V
Differential Common Mode Range	V_{CM}	Includes V_{DI} range	0.8	2.5	
Single Ended Receiver Threshold	V_{SE}		0.8	2.0	
Output Levels					
Static Output Low	V_{OL}	RL of 1.5KΩ to 3.6V		0.3	V
Static Output High	V_{OH}	RL of 15KΩ to GND	2.8	3.6	

Full Speed Source Electrical Characteristics

Parameter	Symbol	Condition (Notes 1, 2, 3)	Min	Max	Unit
Driver Characteristics					
Transition Time		Notes 5, 6 and Figure 1			ns
Rise Time	T_R	CL = 50pF	4.0	20.0	
Fall Time	T_F	CL = 50pF	4.0	20.0	
Rise/Fall Time Matching	T_{REM}	(T_R/T_F)	90	110	%
Output Signal Crossover Voltage	V_{CRS}		1.3	2.0	V

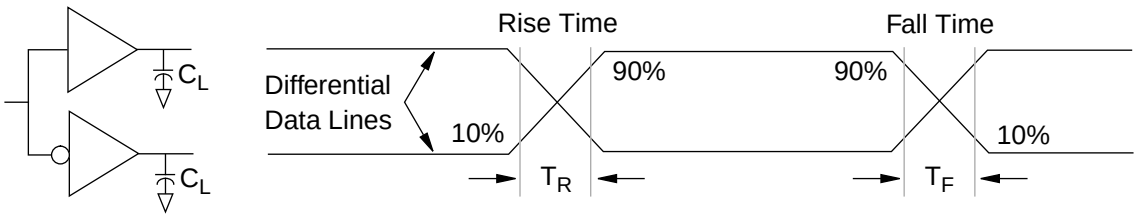
Low Speed Source Electrical Characteristics

Parameter	Symbol	Condition (Notes 1, 2, 4)	Min	Max	Unit
Driver Characteristics					
Transition Time		Notes 5, 6 and Figure 1			ns
Rise Time	T_R	CL = 50pF	75		
		CL = 350pF		300	
Fall Time	T_F	CL = 50pF	75		
		CL = 350pF		300	
Rise/Fall Time Matching	T_{REM}	(T_R/T_F)	80	120	%
Output Signal Crossover Voltage	V_{CRS}		1.3	2.0	V

NOTES:

1. All voltages are measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load (CL) to ground of 50pF, unless otherwise specified.
3. Full speed timings have a 1.5KΩ pull-up to 2.8V on the D+ data line.
4. Low speed timings have a 1.5KΩ pull-up to 2.8V on the D– data line.
5. Measured from 10% to 90% of the data signal.
6. The rising and falling edges should be smoothly transitioning (monotonic).

FIGURE 1: Data Signal Rise and Fall Time

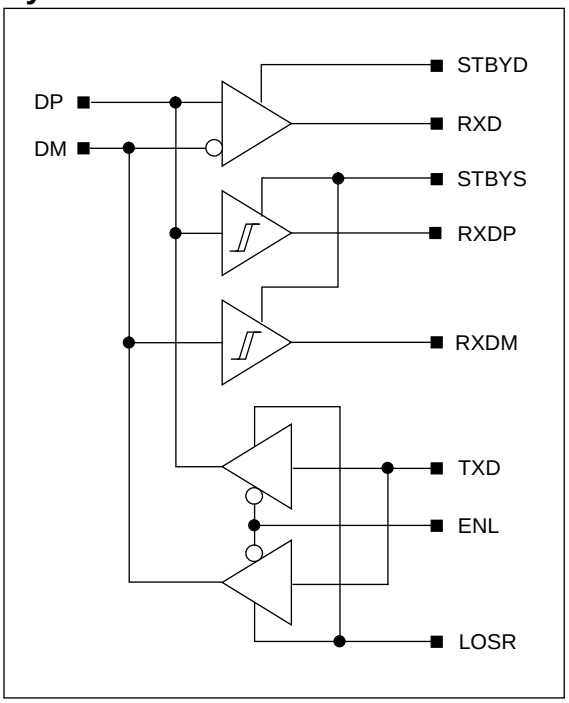


Full Speed: 4 to 20ns at C_L = 50pF Low Speed: 75ns at C_L = 50pF, 300ns at C_L = 350pF

PBUSB/PBUSB1

Universal Serial Bus Buffer

Symbol



Pin Connection

Input	Output	Bi-Direction
STBYD	RXD	DP
STBYS	RXDP	DM
TXD	RXDM	
ENL		
LOSR		

Input Load (SL)

	PBUSB/PBUSB1
STBYD	2.8
STBYS	6.3
TXD	5.6
ENL	41.6
LOSR	31.4

Cell Structure

PBUSB = PICDR + PISER + POTFLS (+ NDT3)

PBUSB1 = PICDR + PISER + POTFLS1 (+ NDT3)

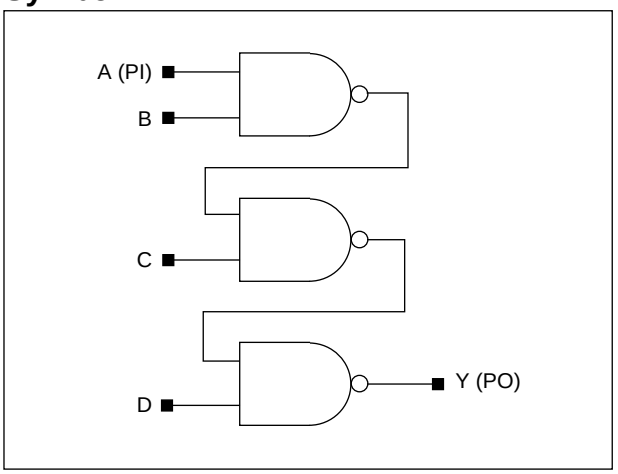
NDT3	Input Nand Tree (Soft-Macro Internal Cell)
PICDR	Differential Receiver
PISER	Single-Ended Receiver
POTFLS	Tri-State Output Buffer with Low Speed
POTFLS1	Tri-State Output Buffer with Full Speed

There only exists PBUSB not PBUSB1 in the physical DB. The division of cell name (PBUSB/PBUSB1) is caused to notify that one of their component cells, POTFLS/POTFLS1 has different AC timing values each other.

NDT3

Input Nand Tree (Soft-Macro Internal Cell)

Symbol



Pin Connection

Input	Output
A (PI) B C D	Y (PO)

Input Load (SL)

	NDT3
A (PI), B, C, D	1.0

NDT3 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.40ns] **(SL : Standard Load)**

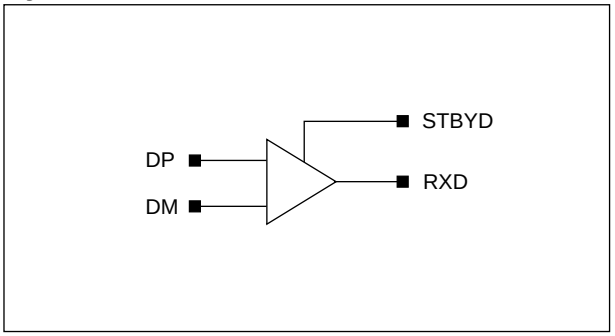
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
A to Y	t_{PLH}	0.32	0.32 + 0.029*SL	0.33 + 0.027*SL	0.33 + 0.027*SL
	t_{PHL}	0.28	0.28 + 0.036*SL	0.28 + 0.036*SL	0.28 + 0.036*SL
	t_R	0.14	0.14 + 0.053*SL	0.13 + 0.057*SL	0.11 + 0.060*SL
	t_F	0.11	0.11 + 0.074*SL	0.11 + 0.075*SL	0.09 + 0.077*SL
B to Y	t_{PLH}	0.30	0.30 + 0.029*SL	0.31 + 0.027*SL	0.31 + 0.027*SL
	t_{PHL}	0.30	0.30 + 0.036*SL	0.30 + 0.036*SL	0.30 + 0.036*SL
	t_R	0.14	0.14 + 0.054*SL	0.13 + 0.057*SL	0.11 + 0.060*SL
	t_F	0.12	0.12 + 0.071*SL	0.11 + 0.075*SL	0.09 + 0.077*SL
C to Y	t_{PLH}	0.20	0.20 + 0.030*SL	0.21 + 0.027*SL	0.21 + 0.027*SL
	t_{PHL}	0.18	0.18 + 0.036*SL	0.19 + 0.036*SL	0.19 + 0.036*SL
	t_R	0.14	0.14 + 0.056*SL	0.14 + 0.057*SL	0.11 + 0.060*SL
	t_F	0.12	0.12 + 0.073*SL	0.11 + 0.075*SL	0.09 + 0.077*SL
D to Y	t_{PLH}	0.09	0.09 + 0.033*SL	0.11 + 0.027*SL	0.11 + 0.027*SL
	t_{PHL}	0.09	0.09 + 0.041*SL	0.10 + 0.035*SL	0.10 + 0.036*SL
	t_R	0.19	0.19 + 0.044*SL	0.16 + 0.054*SL	0.10 + 0.059*SL
	t_F	0.19	0.19 + 0.062*SL	0.16 + 0.072*SL	0.11 + 0.077*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

PICDR

Differential Receiver

Symbol



Pin Connection

Input	Output
STBYD DP DM	RXD

Input Load (SL)

	PICDR
STBYD	2.8

PICDR Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.80ns] **(SL : Standard Load)**

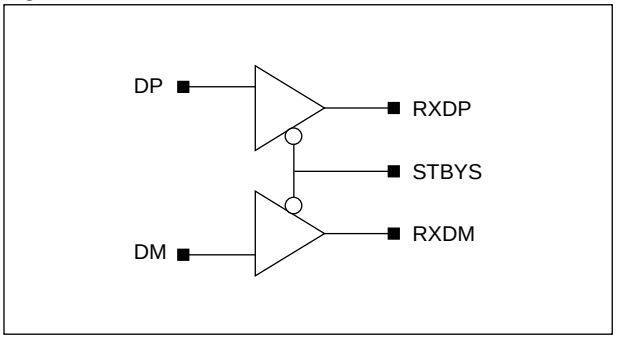
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
DP to RXD	t_{PLH}	0.95	0.95 + 0.011*SL	0.95 + 0.011*SL	0.95 + 0.010*SL
	t_{PHL}	0.45	0.45 + 0.007*SL	0.45 + 0.006*SL	0.46 + 0.005*SL
	t_R	0.11	0.11 + 0.024*SL	0.12 + 0.021*SL	0.11 + 0.022*SL
	t_F	0.08	0.08 + 0.011*SL	0.08 + 0.010*SL	0.08 + 0.010*SL
DM to RXD	t_{PLH}	0.35	0.35 + 0.012*SL	0.36 + 0.010*SL	0.36 + 0.010*SL
	t_{PHL}	0.53	0.53 + 0.007*SL	0.53 + 0.007*SL	0.54 + 0.005*SL
	t_R	0.10	0.10 + 0.021*SL	0.09 + 0.023*SL	0.10 + 0.022*SL
	t_F	0.10	0.10 + 0.008*SL	0.09 + 0.010*SL	0.09 + 0.010*SL
STBYD to RXD	t_{PLH}	1.01	1.01 + 0.012*SL	1.02 + 0.010*SL	1.02 + 0.010*SL
	t_{PHL}	0.27	0.27 + 0.008*SL	0.28 + 0.006*SL	0.29 + 0.005*SL
	t_R	0.11	0.11 + 0.020*SL	0.11 + 0.021*SL	0.10 + 0.023*SL
	t_F	0.08	0.08 + 0.012*SL	0.08 + 0.010*SL	0.08 + 0.010*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

PISER

Single-Ended Receiver

Symbol



Pin Connection

Input	Output
STBYS DP DM	RXDP RXDM

Input Load (SL)

	PISER
STBYS	6.3

PISER Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.80ns] **(SL : Standard Load)**

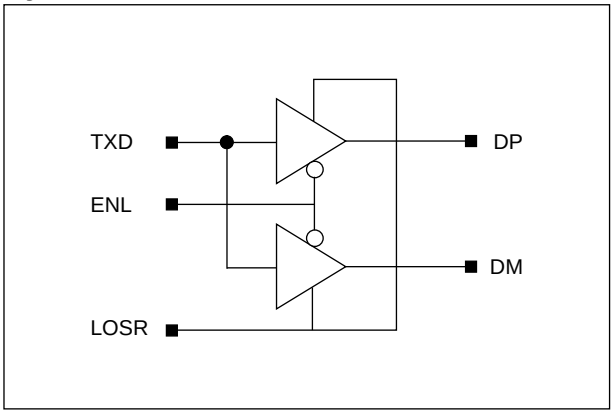
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
DP to RXDP	t_{PLH}	0.36	0.36 + 0.012*SL	0.36 + 0.011*SL	0.37 + 0.010*SL
	t_{PHL}	0.70	0.70 + 0.013*SL	0.70 + 0.010*SL	0.74 + 0.007*SL
	t_R	0.11	0.11 + 0.024*SL	0.12 + 0.021*SL	0.11 + 0.022*SL
	t_F	0.15	0.15 + 0.014*SL	0.16 + 0.011*SL	0.17 + 0.010*SL
STBYS to RXDP	t_{PLH}	0.13	0.13 + 0.012*SL	0.13 + 0.011*SL	0.14 + 0.010*SL
	t_R	0.13	0.13 + 0.021*SL	0.13 + 0.021*SL	0.12 + 0.022*SL
DM to RXDM	t_{PLH}	0.36	0.36 + 0.012*SL	0.36 + 0.011*SL	0.37 + 0.010*SL
	t_{PHL}	0.70	0.70 + 0.013*SL	0.70 + 0.010*SL	0.74 + 0.007*SL
	t_R	0.11	0.11 + 0.024*SL	0.12 + 0.021*SL	0.11 + 0.022*SL
	t_F	0.15	0.15 + 0.014*SL	0.16 + 0.011*SL	0.17 + 0.010*SL
STBYS to RXDM	t_{PLH}	0.13	0.13 + 0.012*SL	0.13 + 0.011*SL	0.14 + 0.010*SL
	t_R	0.13	0.13 + 0.021*SL	0.13 + 0.021*SL	0.12 + 0.022*SL

*Group1 : SL < 3, *Group2 : 3 ≤ SL ≤ 10, *Group3 : 10 < SL

POTFLS/POTFLS1

Tri-State Output Buffer with Low/Full Speed

Symbol



Pin Connection

Input	Output
TXD	DP
ENL	DM
LOSR	

Input Load (SL)

	POTFLS/POTFLS1
TXD	5.6
ENL	41.6
LOSR	31.4

PLOTFLS has AC characteristics for low speed, and PLOTFLS1 for full speed. Their AC timing data are as follows.

POTFLS Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.80ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TXD to DP	t_{PLH}	107.48	88.60 + 0.378*CL	91.57 + 0.338*CL	93.02 + 0.321*CL
	t_{PHL}	115.71	96.31 + 0.388*CL	99.61 + 0.344*CL	101.42 + 0.323*CL
	t_R	92.18	73.88 + 0.366*CL	76.21 + 0.335*CL	77.54 + 0.319*CL
	t_F	109.71	94.01 + 0.314*CL	95.53 + 0.294*CL	96.47 + 0.283*CL
ENL to DP	t_{PLH}	105.12	85.70 + 0.388*CL	88.40 + 0.352*CL	90.58 + 0.327*CL
	t_{PHL}	138.99	119.08 + 0.398*CL	123.77 + 0.336*CL	124.79 + 0.324*CL
	t_R	83.63	65.41 + 0.364*CL	67.41 + 0.338*CL	68.76 + 0.322*CL
	t_F	122.05	105.91 + 0.323*CL	115.39 + 0.196*CL	118.49 + 0.160*CL
	t_{PLZ}	0.54	0.54 + 0.000*CL	0.54 + 0.000*CL	0.54 + 0.000*CL
	t_{PHZ}	0.89	0.89 + 0.000*CL	0.89 + 0.000*CL	0.89 + 0.000*CL
TXD to DM	t_{PLH}	107.48	88.60 + 0.378*CL	91.57 + 0.338*CL	93.02 + 0.321*CL
	t_{PHL}	115.71	96.31 + 0.388*CL	99.61 + 0.344*CL	101.42 + 0.323*CL
	t_R	92.18	73.88 + 0.366*CL	76.21 + 0.335*CL	77.54 + 0.319*CL
	t_F	109.71	94.01 + 0.314*CL	95.53 + 0.294*CL	96.47 + 0.283*CL
ENL to DM	t_{PLH}	105.12	85.70 + 0.388*CL	88.40 + 0.352*CL	90.58 + 0.327*CL
	t_{PHL}	138.99	119.08 + 0.398*CL	123.77 + 0.336*CL	124.79 + 0.324*CL
	t_R	83.63	65.41 + 0.364*CL	67.41 + 0.338*CL	68.76 + 0.322*CL
	t_F	122.05	105.91 + 0.323*CL	115.39 + 0.196*CL	118.49 + 0.160*CL
	t_{PLZ}	0.54	0.54 + 0.000*CL	0.54 + 0.000*CL	0.54 + 0.000*CL
	t_{PHZ}	0.89	0.89 + 0.000*CL	0.89 + 0.000*CL	0.89 + 0.000*CL

*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POTFLS1 Switching Characteristics

[Delays for typical process, 25°C, 3.3V, when t_R , t_F = 0.80ns] **(CL : Capacitive Load [pF])**

Path	Parameter	Delay [ns] CL = 50.0pF	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TXD to DP	t_{PLH}	5.82	0.60 + 0.104*CL	0.60 + 0.104*CL	0.60 + 0.104*CL
	t_{PHL}	4.89	0.95 + 0.079*CL	0.95 + 0.079*CL	0.95 + 0.079*CL
	t_R	11.83	0.09 + 0.235*CL	0.09 + 0.235*CL	0.09 + 0.235*CL
	t_F	8.81	0.11 + 0.174*CL	0.11 + 0.174*CL	0.10 + 0.174*CL
ENL to DP	t_{PLH}	5.92	0.70 + 0.104*CL	0.70 + 0.104*CL	0.70 + 0.104*CL
	t_{PHL}	4.87	0.93 + 0.079*CL	1.00 + 0.078*CL	0.91 + 0.079*CL
	t_R	11.83	0.09 + 0.235*CL	0.09 + 0.235*CL	0.09 + 0.235*CL
	t_F	8.99	-0.01 + 0.180*CL	3.35 + 0.135*CL	-1.85 + 0.196*CL
	t_{PLZ}	0.55	0.55 + 0.000*CL	0.55 + 0.000*CL	0.55 + 0.000*CL
	t_{PHZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL
TXD to DM	t_{PLH}	5.82	0.60 + 0.104*CL	0.60 + 0.104*CL	0.60 + 0.104*CL
	t_{PHL}	4.89	0.95 + 0.079*CL	0.95 + 0.079*CL	0.95 + 0.079*CL
	t_R	11.83	0.09 + 0.235*CL	0.09 + 0.235*CL	0.09 + 0.235*CL
	t_F	8.81	0.11 + 0.174*CL	0.11 + 0.174*CL	0.10 + 0.174*CL
ENL to DM	t_{PLH}	5.92	0.70 + 0.104*CL	0.70 + 0.104*CL	0.70 + 0.104*CL
	t_{PHL}	4.87	0.93 + 0.079*CL	1.00 + 0.078*CL	0.91 + 0.079*CL
	t_R	11.83	0.09 + 0.235*CL	0.09 + 0.235*CL	0.09 + 0.235*CL
	t_F	8.99	-0.01 + 0.180*CL	3.35 + 0.135*CL	-1.85 + 0.196*CL
	t_{PLZ}	0.55	0.55 + 0.000*CL	0.55 + 0.000*CL	0.55 + 0.000*CL
	t_{PHZ}	0.91	0.91 + 0.000*CL	0.91 + 0.000*CL	0.91 + 0.000*CL

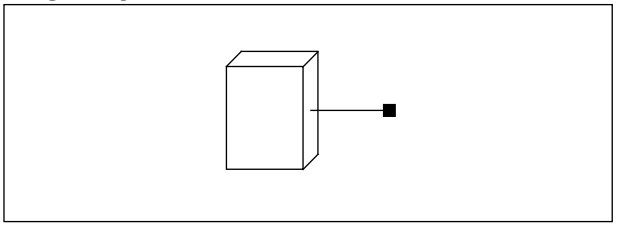
*Group1 : CL < 75, *Group2 : 75 ≦ CL ≦ 85, *Group3 : 85 < CL

POWER PADS

Cell Names & Function Descriptions

Cell Name	Function Description
VDD Power Pads	
VDD3I	3.3V Normal Internal VDD
VDD3P	3.3V Normal Pre-Driver VDD
VDD3O	3.3V Normal Output-Driver VDD
VDD3IP	3.3V Normal Internal and Pre-Driver VDD
VDD3OI	3.3V Normal Output-Driver and Internal VDD
VDD3OP	3.3V Normal Output-Driver and Pre-Driver VDD
VDD3T	3.3V Normal Total VDD
VDD5O	5V Normal Output-Driver VDD
VSS Power Pads	
VSS3I	3.3V Normal Internal VSS
VSS3P	3.3V Normal Pre-Driver VSS
VSS3O	3.3V Normal Output-Driver VSS
VSS3IP	3.3V Normal Internal and Pre-Driver VSS
VSS3OI	3.3V Normal Output-Driver and Internal VSS
VSS3OP	3.3V Normal Output-Driver and Pre-Driver VSS
VSS3T	3.3V Normal Total VSS
VSS5O	5V Normal Output-Driver VSS

Logic Symbol



Memory Compilers 5

Contents

OVERVIEW

This chapter contains information for memory compilers available in STDL80 cell library. These are complete compilers that consist of various generators to satisfy the requirements of the circuit at hand. Each of the final building block, the physical layout, will be implemented as a stand-alone, densely packed, pitch-matched array. Using this complex layout generator and adopting state-of-the-art logic and circuit design technique, these memory cells can realize extreme density and performance. In each layout generator, we added an option which makes the aspect ratio of the physical layout selectable so that the ASIC designers can choose the aspect ratio according to the convenience of the chip level layout.

In the STDL80 cell library, there are 4 groups of memory compilers — ROMs; Static RAMs; Register File; FIFO.

Generators

Each memory compiler is a set of various, parameterized generators. The generators are:

- Layout Generator
  : generates an array of custom, pitch-matched leaf cells.
- Schematic Generator & Netlister
  : extracts a netlist which can be used for both LVS check and functional verification.
- Function & Timing Model Generators
  : for gate level simulation, dynamic/static timing analysis and synthesis
- Symbol Generator
  : for schematic capture
- Critical Path Generator & ETC
  : there are many special purpose generators such as critical path generator used for both circuit design and AC timing characterization.

Advanced Design Technique

All of 0.5μm CMOS standard cell memory compilers adopt very advanced design technique to obtain extremely high performance in terms of both speed and power consumption. Below are major techniques.

For reducing power consumption

- Minimized bit-line precharge/discharge voltage swing
- Zero static current consuming sense amplifier
- Automatic power down after an access

For optimizing and minimizing the read access time

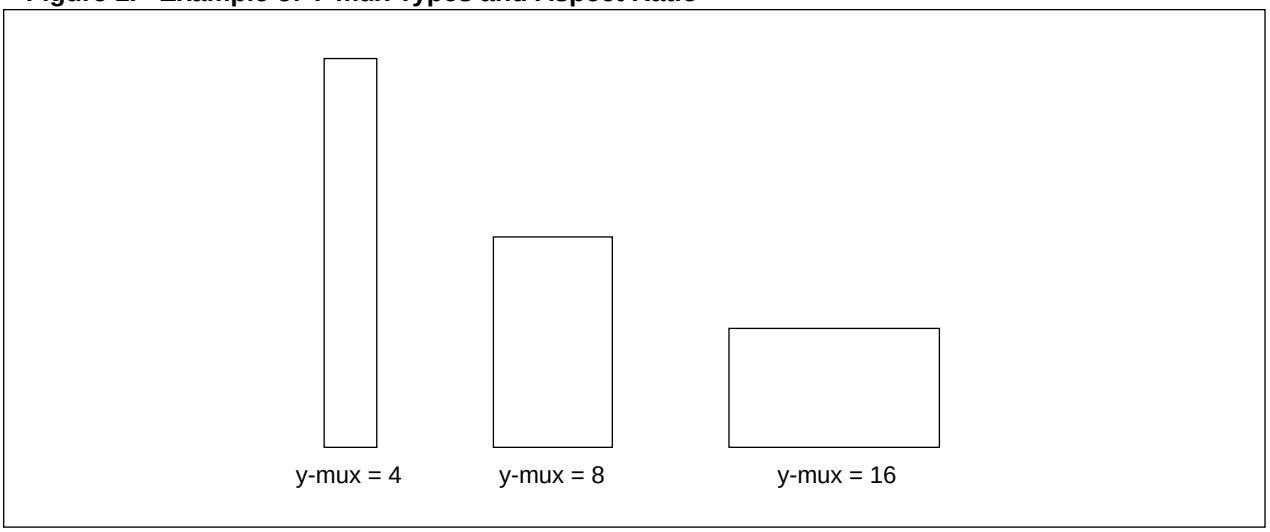
- Size sensitive self-timer delay
- Extremely simple tri-state output circuit

Flexible Aspect Ratio

The size of a memory cell is defined by its number of words (WORDS) and number of bits per word (BPW). But, this size is only a logical size. The physical size of a memory is defined by the number of rows (ROWS) and the number of columns (COLS) of its bit cell array. Usually, we can't make the bit cell array with WORDS and BPW because the range of WORDS is much larger than the range of BPW. If we make the bit cell array with WORDS and BPW, most of memory layouts will have too tall and too thin aspect ratio. Therefore, column decoder and y-mux circuit are included in most of memory cells to adjust the aspect ratio.

In 0.5μm CMOS standard cell memory compilers, the y-mux type selecting option was added to give the customers freedom selecting aspect ratio of the memory layout. Many of the characteristics of a memory cell are depend on its y-mux type. So, when you change the y-mux type from one to the other to change the aspect ratio, you have to know that it will change many major characteristics, such as access time, area and power consumption, of the memory.

< Figure 1. Example of Y-mux Types and Aspect Ratio >



Dual Banks

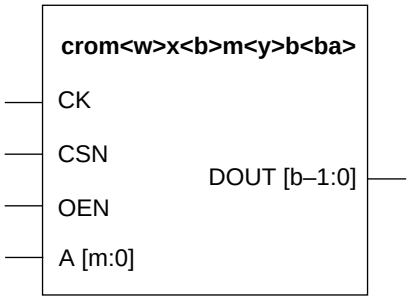
In some of 0.5μm CMOS standard cell memory compilers is a generator option which defines the number of bit array banks. This dual bank scheme doubles the maximum capacity of the memory compilers.

MEMORY COMPILERS SELECTION GUIDE

Memory Group	Cell Name	Function Description
ROM	CROM Gen	Contact Programmable Synchronous ROM Generator
	DROM Gen	Diffusion Programmable Synchronous ROM Generator
Static RAM	SPSRAM Gen	Single-Port Synchronous RAM Generator – Reads and writes at the same edge of clock
	SPSRAMA Gen	Single-Port Synchronous RAM Generator – Alternative – Reads and writes at different edges of clock
	SPARAM Gen	Single-Port Asynchronous RAM Generator – Fully asynchronous read, WEN synchronized write
	DPSRAM Gen	Dual-Port Synchronous RAM Generator – Reads and writes at the same edge of clock
	DPARAM* Gen	Dual-Port Asynchronous RAM Generator – Fully asynchronous read, WEN synchronized write
	DPSRAMA Gen	Dual-Port Synchronous RAM Generator – Alternative – Reads and writes at different edges of clock
Register File	IRIW*	1 Read Port, 1 Write Port Synchronous Register File
FIFO	FIFO*	Synchronous FIFO

* Under-Developed

Logic Symbol



NOTES:

1. Words (w) is the number of words in CROM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Static differential operation
- Stand-by (power down) mode available
- Tri-state output
- Low noise output circuit
- Programmable with contact layer
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 128K bits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

CROM Gen is a contact programmable synchronous ROM. When CK rises, DOUT [ ] presents data programmed in the location addressed by A [ ]. CSN is used to enable/disable the clock. OEN is used to enable/disable the data output driver.

Generators and Cell Configurations

CROM Gen. generates layout, netlist, symbol and functional & timing model of CROM. The layout of CROM is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of CROM, you can give certain values to following four generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	32	64	128	256
		Max	1024	2048	4096	8192
		Step	8	16	32	64
Bpw (b)	ba = 1	Min	1	1	1	1
		Max	64	32	16	8
		Step	1	1	1	1
	ba = 2	Min	2	2	2	2
		Max	128	64	32	16
		Step	1	1	1	1

CROM Gen

Contact Programmable Synchronous ROM Generator

Pin Descriptions

Name	I/O	Description
CK	I	“Clock” serves as the input clock to the memory block. When CK is low the memory is in a precharge state. Upon the rising edge, an access cycle begins.
CSN	I	“Chip Select Negative” acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read access occur. CSN may not change during CK is high.
OEN	I	“Output Enable Negative” controls the output drivers from driven to tri-state condition. OEN may not change during CK is high.
A [ ]	I	“Address” selects the location to be accessed. A [ ] may not change during CK is high.
DOUT [ ]	O	During a read access, data word programmed will be presented to the “Data Out” ports. DOUT [ ] is tri-statable. When CK is high, CSN is low and OEN is low, only then, DOUT [ ] drives a certain value. Otherwise, DOUT [ ] keeps Hi-Z state.

Pin Capacitance

(Unit = SL)

	CK	CSN	OEN	A	DOUT			
					Ymux 4	Ymux 8	Ymux 16	Ymux 32
1-bank	5.8	1.8	2.2	1.7	4.0	8.7	18.0	37.0
2-bank	11.5	3.7	4.4	1.7	4.0	8.7	18.0	37.0

Application Notes

1) Putting Busholders on DOUT [ ]

As you will see in the timing diagrams, DOUT [ ] is valid only when CK is high. If you want DOUT [ ] to be stable regardless of CK state, you should put STDL80 Busholder cells on the DOUT [ ] bus externally.

2) Customizing Aspect Ratio

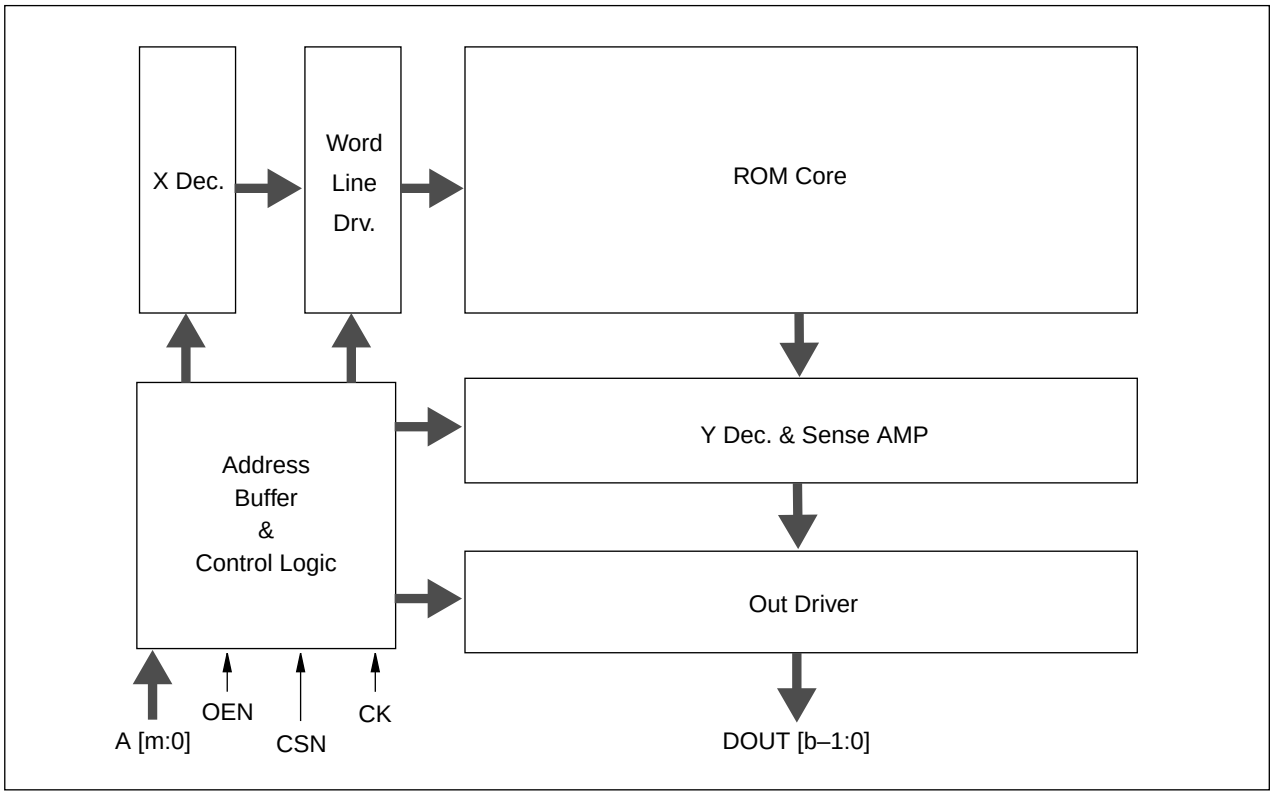
Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 4 selections of Ymux for the same Words and the same Bpw CROM. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of CROM, In general, larger Ymux CROM has faster speed and bigger area than smaller Ymux CROM.

3) Selecting Number of Banks

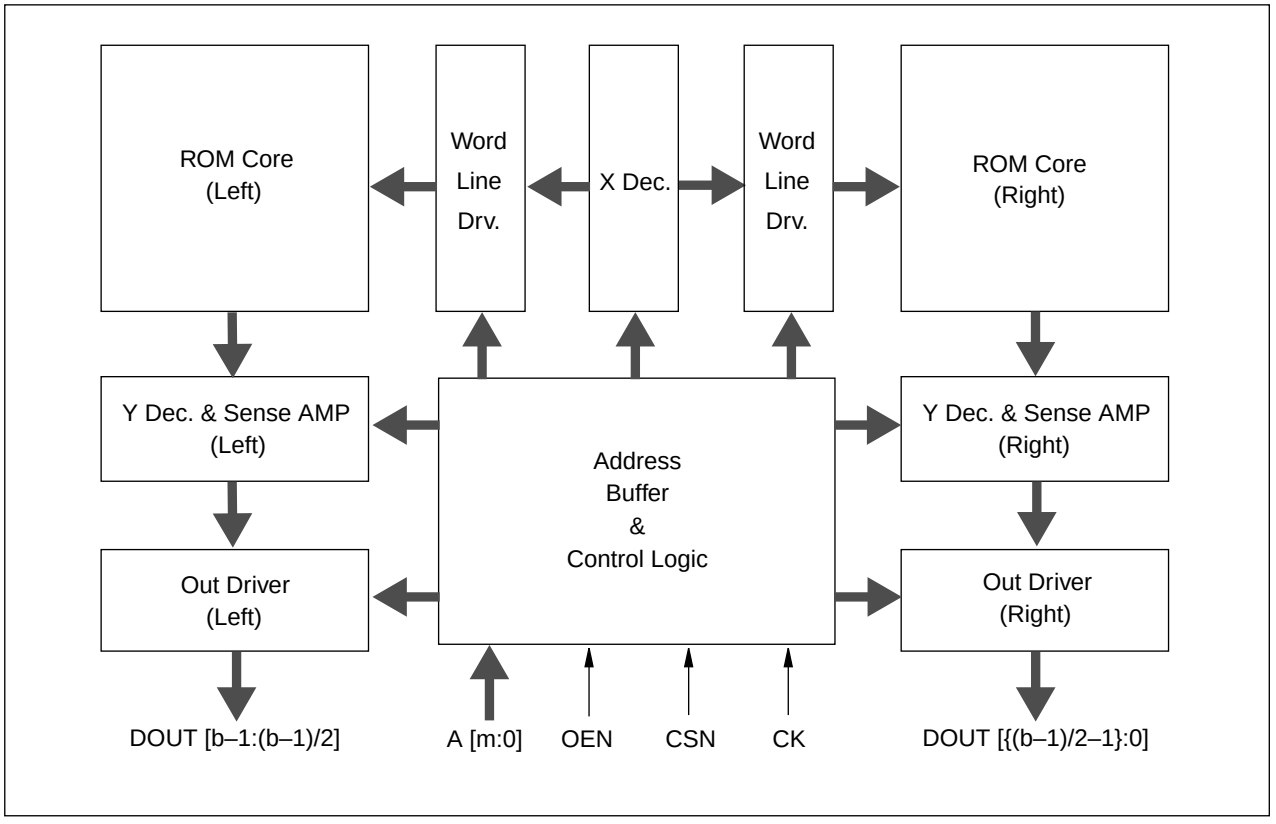
To enlarge the capacity of CROM, we added one more option to choose number of banks. If you want to use larger CROM than 64K bit CROM, you can select dual bank (ba = 2). You can also select dual bank for smaller one than 64K bit CROM. Dual bank CROM is a little bigger and a little faster than single bank one. (Please refer to the characteristic tables.)

Block Diagrams

< 1-bank >



< 2-bank >



CROM Gen

Contact Programmable Synchronous ROM Generator

Characteristic Reference Table

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{O}C, Output load = 10SL, Unit = ns)							
minckl	Minimum Clock Pulse Width Low	2.80	2.80	3.20	3.20	4.20	4.20
minckh	Minimum Clock Pulse Width High	5.20	5.20	6.50	6.50	8.90	8.90
t_{as}	Address Setup Time	0.30	0.30	0.50	0.50	1.00	1.00
t_{ah}	Address Hold Time	0.30	0.30	1.40	1.40	1.80	1.80
t_{cs}	CSN Setup Time	0.40	0.40	0.40	0.40	0.40	0.40
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{os}	OEN Setup Time	0	0	0	0	0	0
t_{oh}	OEN Hold Time	1.90	1.80	2.00	1.90	2.10	2.00
t_{acc}	Access Time	3.20	3.20	3.60	3.60	4.40	4.40
t_{da}	Deaccess Time	2.00	2.00	2.00	2.00	2.00	2.00
SIZE (μm)							
Width		466	595	757	886	1329	1458
Height		443	443	638	638	1028	1028
POWER (μW/MHz)							
power_ck (normal mode: CSN Low)			653		1426		3767
power_csn (stand-by mode: CSN High)			20		32		54

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
Y: Ymux Type
S: Input Slope (Unit: ns)
VDD: Operating Voltage (Unit: V)
B: Bits per Word
BA: Number of Banks (1 or 2)
SL: Number of Fanouts (Unit: Standard Load)
F: Operating Frequency (Unit: MHz)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 4
minckh	(4.2863e – 03 * W + 1.6025e – 01 * S + 1.2091e – 01 * 0.02 * SL + 3.1188) * 1.1
minckl	(1.8303e – 03 * W + 2.4102e – 01 * S – 7.6923e – 03 * 0.02 * SL + 2.0153)
tacc	(1.5275e – 03 * W + 1.7051e – 01 * S + 3.4519e – 01 * 0.02 * SL + 2.4596)
	Y = 8
minckh	(2.1200e – 03 * W + 1.2948e – 01 * S + 1.2560e – 01 * 0.02 * SL + 3.1802) * 1.1
minckl	(9.1519e – 04 * W + 2.4102e – 01 * S – 7.6923e – 03 * 0.02 * SL + 2.0153)
tacc	(7.6375e – 04 * W + 1.7051e – 01 * S + 3.4519e – 01 * 0.02 * SL + 2.4596)
	Y = 16
minckh	(1.0472e – 03 * W + 1.6410e – 01 * S + 1.5997e – 01 * 0.02 * SL + 3.1662) * 1.1
minckl	(4.5759e – 04 * W + 2.4102e – 01 * S – 7.6923e – 03 * 0.02 * SL + 2.0153)
tacc	(3.8187e – 04 * W + 1.7051e – 01 * S + 3.4519e – 01 * 0.02 * SL + 2.4596)
	Y = 32
minckh	(5.0309e – 04 * W + 1.2435e – 01 * S + 2.4771e – 01 * 0.02 * SL + 3.2136) * 1.1
minckl	(2.2879e – 04 * W + 2.4102e – 01 * S – 7.6923e – 03 * 0.02 * SL + 2.0153)
tacc	(1.9093e – 04 * W + 1.7051e – 01 * S + 3.4519e – 01 * 0.02 * SL + 2.4596)

2) Power Characteristics [Unit: μW]

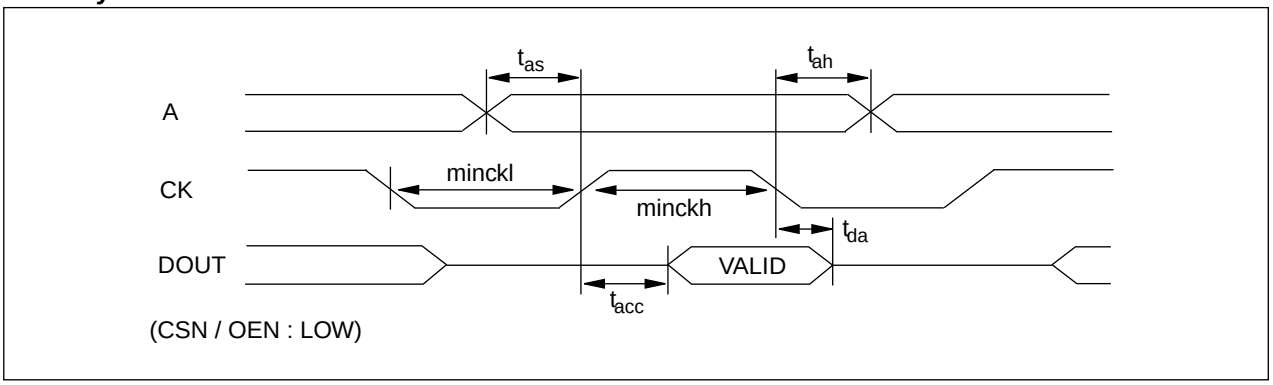
Power Type	Power Equation
	Y = 4
power_ck	(4.7057e – 02 * W + 1.7340 * B + 7.1595 + 3.2654e – 03 * W * B) * VDD^2 * F
power_csn	(–1.4914e – 05 * W + 6.7259e – 02 * B + 8.2631e – 01 + 1.1615e – 06 * W * B) * VDD^2 * F
	Y = 8
power_ck	(2.3345e – 02 * W + 2.9248 * B + 6.8769 + 3.2650e – 03 * W * B) * VDD^2 * F
power_csn	(–7.4573e – 06 * W + 1.3451e – 01 * B + 8.2631e – 01 + 1.1615e – 06 * W * B) * VDD^2 * F
	Y = 16
power_ck	(1.1254e – 02 * W + 5.2769 * B + 7.1131 + 3.1936e – 03 * W * B) * VDD^2 * F
power_csn	(–3.7287e – 06 * W + 2.6903e – 01 * B + 8.2631e – 01 + 1.1615e – 06 * W * B) * VDD^2 * F
	Y = 32
power_ck	(6.1194e – 03 * W + 1.0430e + 01 * B + 6.8749 + 2.9601e – 03 * W * B) * VDD^2 * F
power_csn	(–1.8643e – 06 * W + 5.3807e – 01 * B + 8.2631e – 01 + 1.1615e – 06 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

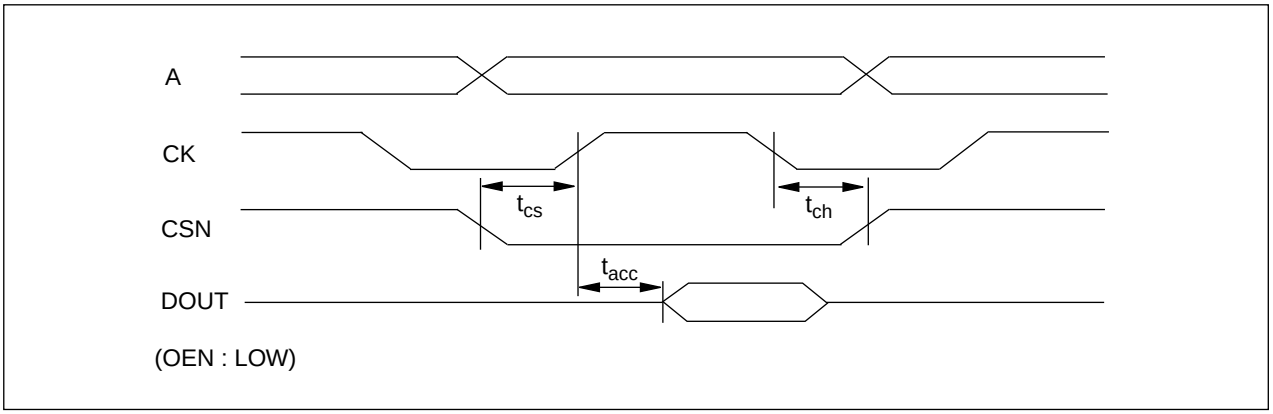
Width = 8.75 * (log2(W / Y)) + 129.65 * BA + 4.4 * (B * Y) + 1.4 [μm]
Height = 247.15 + 3.05 * W / Y [μm]

Timing Diagrams

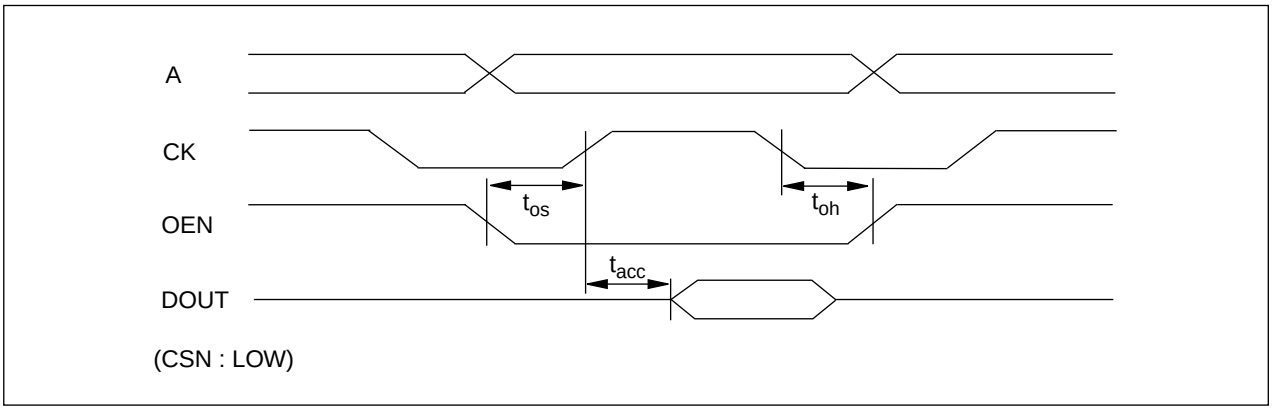
Read Cycle



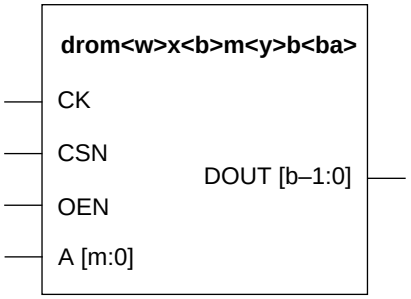
CSN Control



OEN Control



Logic Symbol



NOTES:

1. Words (w) is the number of words in a DROM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Stand-by (power down) mode available
- Latched output
- Unconditionally controlled tri-state output
- Low noise output circuit
- Programmable with diffusion layer
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 512K bits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

DROM is a diffusion programmable synchronous ROM. When CK rises, DOUT [ ] presents data programmed in the location addressed by A [ ]. CSN is used to enable/disable the clock. OEN is used to enable/disable the data output driver.

Generators and Cell Configurations

DROM Gen. generates layout, netlist, symbol and functional & timing model of DROM. The layout of DROM is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of DROM, you can give certain values to following four generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	16	32	64
		Max	4096	8192	16384
		Step	16	32	64
Bpw (b)	ba = 1	Min	2	2	2
		Max	64	32	16
		Step	1	1	1
	ba = 2	Min	4	4	4
		Max	128	64	32
		Step	1	1	1

DROM Gen

Diffusion Programmable Synchronous ROM Generator

Pin Descriptions

Name	I/O	Description
CK	I	“Clock” serves as the input clock to the memory block. When CK is low the memory is in a precharge state. Upon the rising edge, an access cycle begins.
CSN	I	“Chip Select Negative” acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read access occur. CSN may not change during CK is high.
OEN	I	“Output Enable Negative” unconditionally controls the output drivers from driven to tri-state condition.
A [ ]	I	“Address” selects the location to be accessed. A [ ] may not change during CK is high.
DOUT [ ]	O	During a read access, data word programmed will be presented to the “Data Out” ports. DOUT [ ] is latched during a full cycle. When CSN is low and OEN is low, only then, DOUT [ ] drives a certain value. Otherwise, DOUT [ ] keeps Hi-Z state.

Pin Capacitance

(Unit = SL)

	CK	CSN	OEN	A	DOUT
1-bank	2.1	0.6	1.1	2.3	44.0
2-bank	4.2	1.2	2.2	2.3	44.0

Application Notes

1) Customizing Aspect Ratio

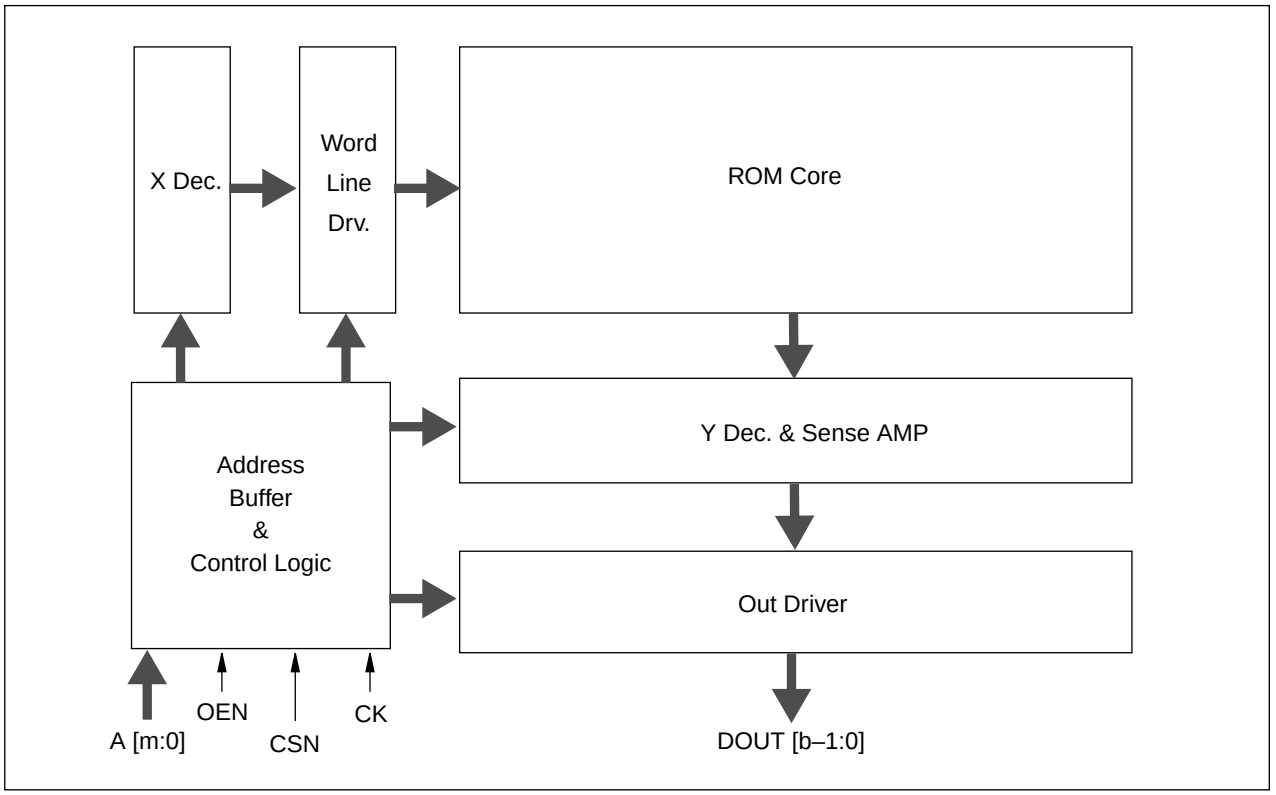
Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 3 selections of Ymux for the same Words and the same Bpw DROM. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of DROM, In general, larger Ymux DROM has faster speed and bigger area than smaller Ymux DROM.

2) Selecting Number of Banks

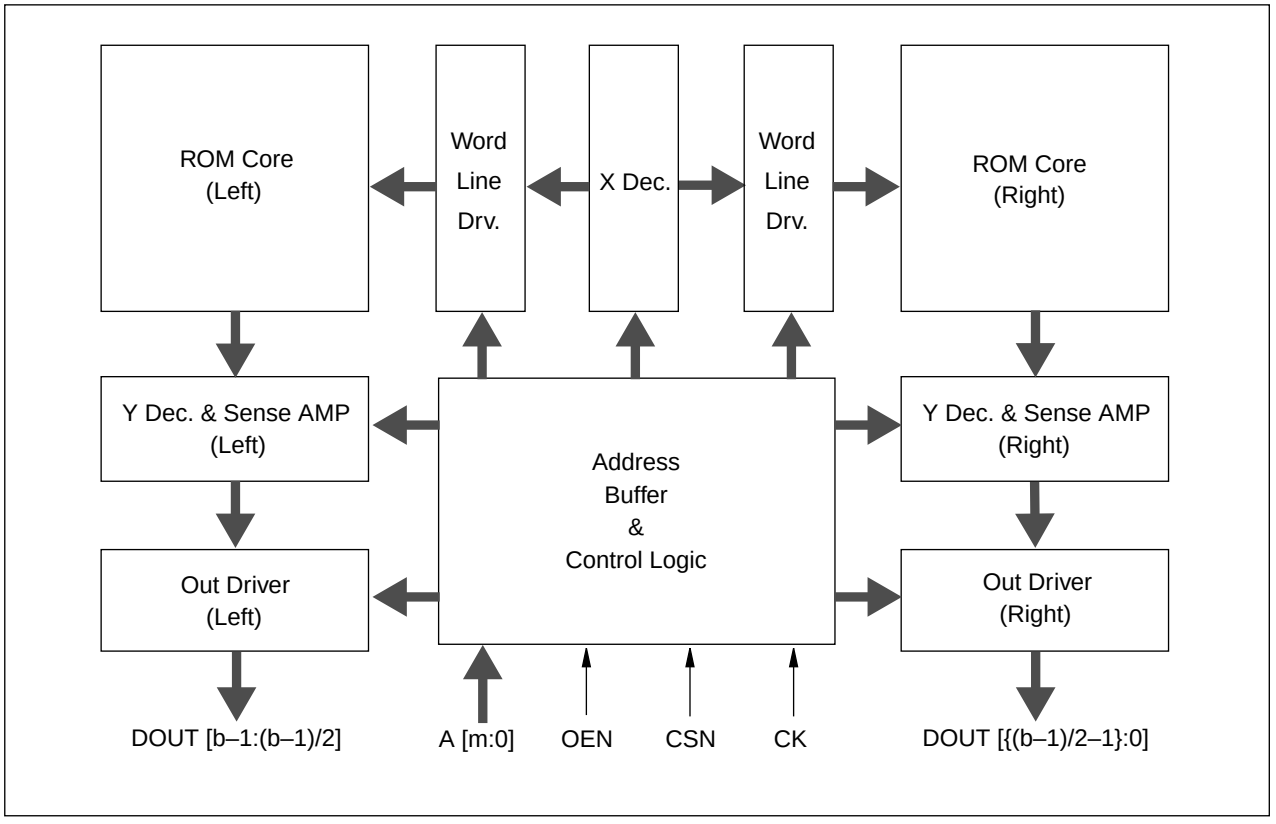
To enlarge the capacity of DROM, we added one more option to choose number of banks. If you want to use larger DROM than 256K bit DROM, you can select dual bank (ba = 2). You can also select dual bank for smaller one than 256K bit DROM. Dual bank DROM is a little bigger and a little faster than single bank one. (Please refer to the characteristic tables.)

Block Diagrams

< 1-bank >



< 2-bank >



DROM Gen

Diffusion Programmable Synchronous ROM Generator

Characteristic Reference Table

Symbol	Description	256x16m8		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{O}C, Output load = 10SL, Unit = ns)							
minckl	Minimum Clock Pulse Width Low	1.80	1.70	1.80	1.70	2.10	1.80
minckh	Minimum Clock Pulse Width High	4.70	4.50	5.40	5.20	6.90	6.50
t_{as}	Address Setup Time	0.28	0.28	0.31	0.31	0.32	0.32
t_{ah}	Address Hold Time	0	0	0	0	0	0
t_{cs}	CSN Setup Time	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{acc}	Access Time	5.60	5.40	6.20	6.00	7.50	7.10
t_{da}	Deaccess Time	4.10	4.00	4.80	4.60	6.0	5.60
t_{zd}	Hi-Z to Valid Data	1.90	1.90	1.90	1.90	1.90	1.90
t_{dz}	Valid Data to Hi-Z	1.60	1.50	1.60	1.50	1.70	1.60
mincyc	Minimum Clock Cycle Time	6.10	5.80	8.00	7.80	11.30	10.80
SIZE (μm)							
Width		556	720	576	740	917	1081
Height		305	305	526	526	823	823
POWER (μW/MHz)							
power_ck (normal mode: CSN Low)			390		749		2027
power_csn (stand-by mode: CSN High)			9.8		9.8		16

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
Y: Ymux Type
S: Input Slope (Unit: ns)
VDD: Operating Voltage (Unit: V)
B: Bits per Word
BA: Number of Banks (1 or 2)
SL: Number of Fanouts (Unit: Standard Load)
F: Operating Frequency (Unit: MHz)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 8
mincyc	(2.5468e – 03 * W + 3.1940e – 02 * B / BA + 1.0384e – 01 * S + 4.7966)
minckh	(8.4451e – 04 * W + 2.3114e – 02 * B / BA + 7.1153e – 02 * S + 4.0270)
minckl	(1.3917e – 02 * B / BA + 2.8361e – 01 * S + 1.2142 + 1.5719e – 03 * B / BA * S)
tacc	(8.4234e – 04 * W + 2.3033e – 02 * B / BA + 1.0288e – 01 * S + 5.8079e – 01 * 0.02 * SL + 4.7546)
	Y = 16
mincyc	(1.2326e – 03 * W + 6.7538e – 02 * B / BA + 2.7115e – 01 * S +4.8548)
minckh	(4.2208e – 04 * W + 4.6630e – 02 * B / BA + 8.6538e – 02 * S + 4.3200)
minckl	(2.7834e – 02 * B / BA + 2.8361e – 01 * S + 1.2142 + 3.1438e – 03 * B / BA * S)
tacc	(4.2117e – 04 * W + 4.6066e – 02 * B / BA + 1.0288e – 01 * S + 5.8079e – 01 * 0.02 * SL + 4.7546)
	Y = 32
mincyc	(5.8723e – 04 * W + 1.4387e – 01 * B / BA + 1.8942e – 01 * S + 5.4184)
minckh	(2.1195e – 04 * W + 9.2951e – 02 * B / BA + 9.7115e – 02 * S + 4.9479)
minckl	(5.5668e – 02 * B / BA + 2.8361e – 01 * S + 1.2142 + 6.2876e – 03 * B / BA * S)
tacc	(2.1058e – 04 * W + 9.2132e – 02 * B / BA + 1.0288e – 01 * S + 5.8079e – 01 * 0.02 * SL + 4.7546)

2) Power Characteristics [Unit: μW]

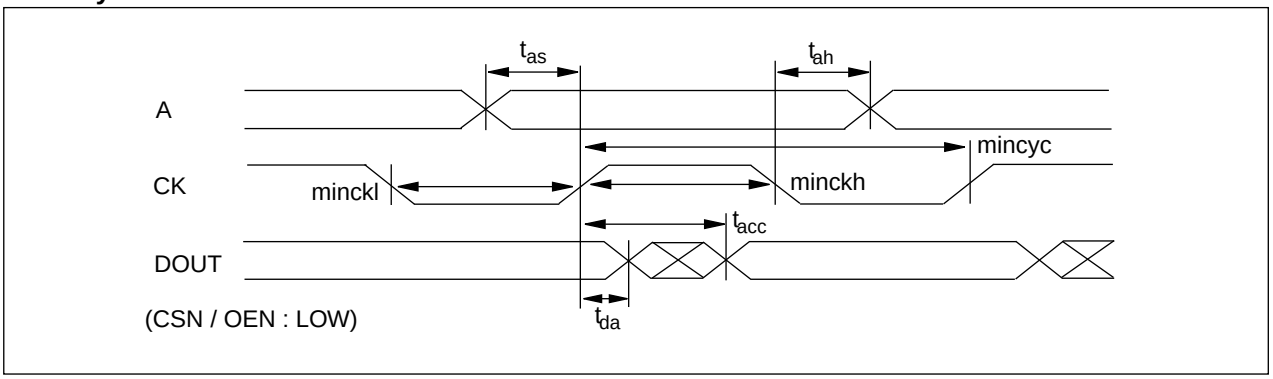
Power Type	Power Equation
	Y = 8
power_ck	(1.7976e – 02 * W + 1.2560 * B + 5.7252 + 1.4992e – 03 * W * B) * VDD^2 * F
power_csn	(–1.8602e – 05 * W + 3.0168e – 02 * B + 4.1766e – 01 + 1.9173e – 06 * W * B) * VDD^2 * F
	Y = 16
power_ck	(8.6750e – 03 * W + 2.0183 * B + 5.6958 + 1.7184e – 03 * W * B) * VDD^2 * F
power_csn	(–9.3013e – 06 * W + 6.0336e – 02 * B + 4.1766e – 01 + 1.9173e – 06 * W * B) * VDD^2 * F
	Y = 32
power_ck	(4.1580e – 03 * W + 4.1059 * B + 6.0523 + 1.8497e – 03 * W * B) * VDD^2 * F
power_csn	(–4.6506e – 06 * W + 1.2067e – 01 * B + 4.1766e – 01 + 1.9173e – 06 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

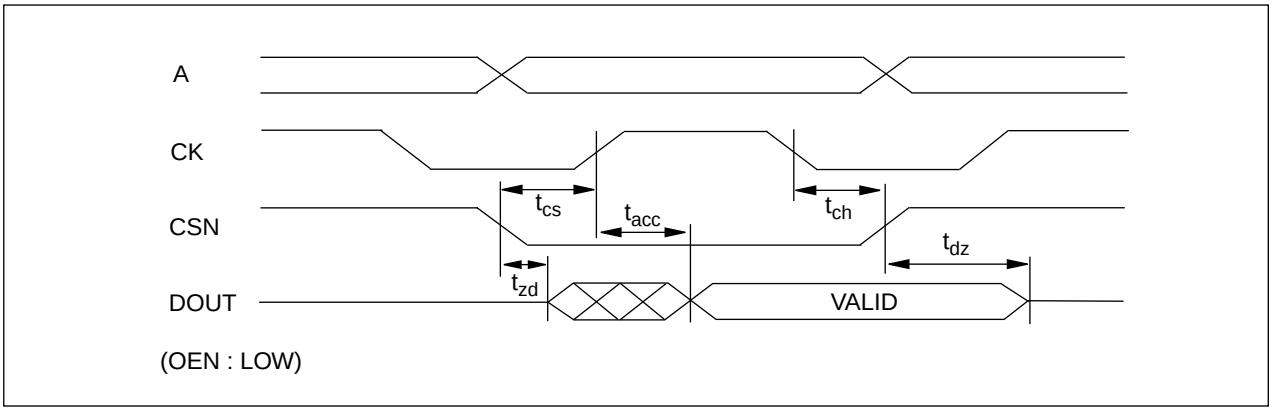
Width = 10.2 * ($\lceil \log_2 (W / Y) \rceil$) + 164.8 * BA + 2.5843(B * Y) + 8.2 [μm]
Height = 225.1 + 2.30 * W / Y + M [μm]
M = 6.05 (if Y = 8), M = 8.45 (if Y = 16), M = 10.85 (if Y = 32)

Timing Diagrams

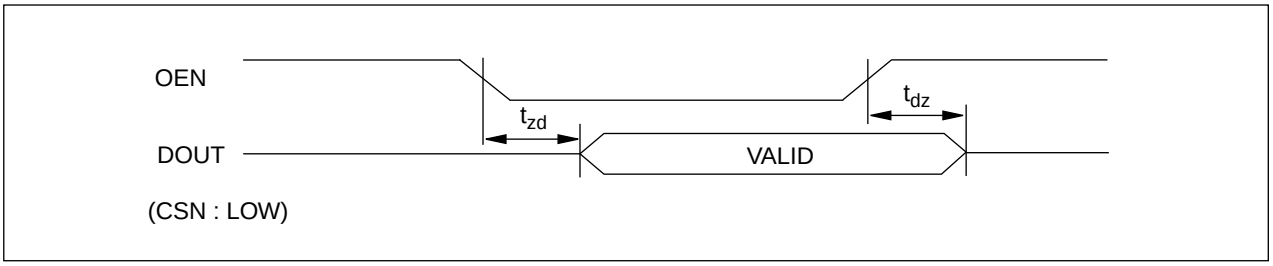
Read Cycle



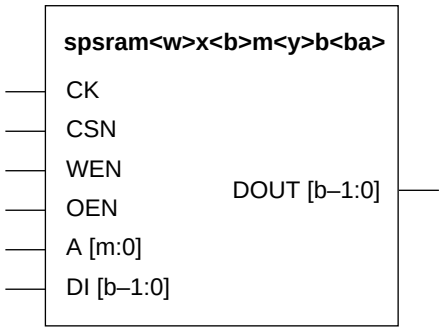
CSN Control



OEN Control



Logic Symbol



NOTES:

1. Words (w) is the number of words in SPSRAM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Write completed at rising edge of clock
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 128K bits capacity
- Up to 8K number of words
- Up to 256 number of bits per word

Function Description

SPSRAM is a single-port synchronous static RAM. When CK rises, if WEN is high, DOUT [ ] presents data stored in the location addressed by A [ ], otherwise the value of DI [ ] is written into the location addressed by A [ ]. CSN is used to enable/disable the clock. OEN is used to enable/disable the data output driver.

Generators and Cell Configurations

SPSRAM Gen. generates layout, netlist, symbol and functional & timing model of SPSRAM. The layout of SPSRAM is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of SPSRAM, you can give certain values to following four generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	4	8	16	32	64
		Max	512	1024	2048	4096	8192
		Step	2	4	8	16	32
Bpw (b)	ba = 1	Min	1	1	1	1	1
		Max	128	64	32	16	8
		Step	1	1	1	1	1
	ba = 2	Min	2	2	2	2	2
		Max	256	128	64	32	16
		Step	1	1	1	1	1

SPSRAM Gen

Single-Port Synchronous RAM Generator

Pin Descriptions

Name	I/O	Input Cap.	Description
CK	I		“Clock” serves as the input clock to the memory block. When CK is low, the memory is in a precharge state. Upon the rising edge, an access begins.
CSN	I		“Chip Select Negative” acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read or write access occur. CSN may not change during CK is high.
WEN	I		“Write Enable Negative” selects the type of memory access. Read is the high state, and write is the low state.
OEN	I		“Output Enable Negative” controls the output drivers from driven to tri-state condition. OEN may not change during CK is high.
A [ ]	I		“Address” selects the location to be accessed. A [ ] may not change during CK is high.
DI [ ]	I		When CK rises while WEN is low, the “Data In” word value is written to the accessed location.
DOUT [ ]	O		During a read access, data word stored will be presented to the “Data Out” ports. DOUT [ ] is tri-statable. When CK is high, CSN is low and OEN is low, only then, DOUT [ ] drives a certain value. Otherwise, DOUT [ ] keeps Hi-Z state. During a write access, data word written will be presented at the “Data Out” ports if output driver is enabled.

Pin Capacitance

(Unit = SL)

	CK	CSN	WEN	OEN	A	DI	DOUT				
							Ymux 2	Ymux 4	Ymux 8	Ymux 16	Ymux 32
1-bank	3.5	1.0	0.5	1.6	1.2	2.1	3.1	3.3	7.7	15.0	31.0
2-bank	7.0	2.1	1.0	3.1	1.2	2.1	3.1	3.3	7.7	15.0	31.0

Application Notes

1) Putting Busholders on DOUT [ ]

As you will see in the timing diagrams, DOUT [ ] is valid only when CK is high. If you want DOUT [ ] to be stable regardless of CK state, you should put STDL80 Busholder cells on the DOUT [ ] bus externally.

2) Customizing Aspect Ratio

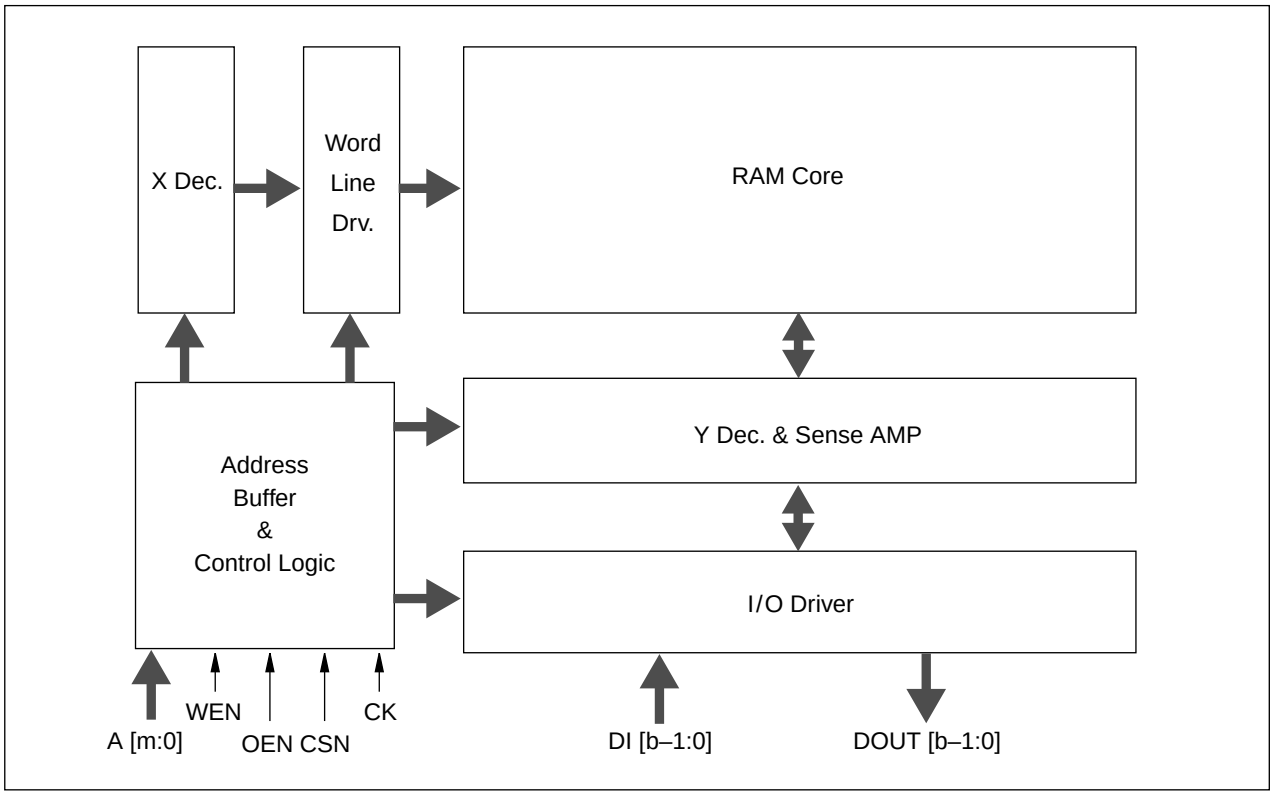
Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 5 selections of Ymux for the same Words and the same Bpw SPSRAM. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of SPSRAM, In general, larger Ymux SPSRAM has faster speed and bigger area than smaller Ymux SPSRAM.

3) Selecting Number of Banks

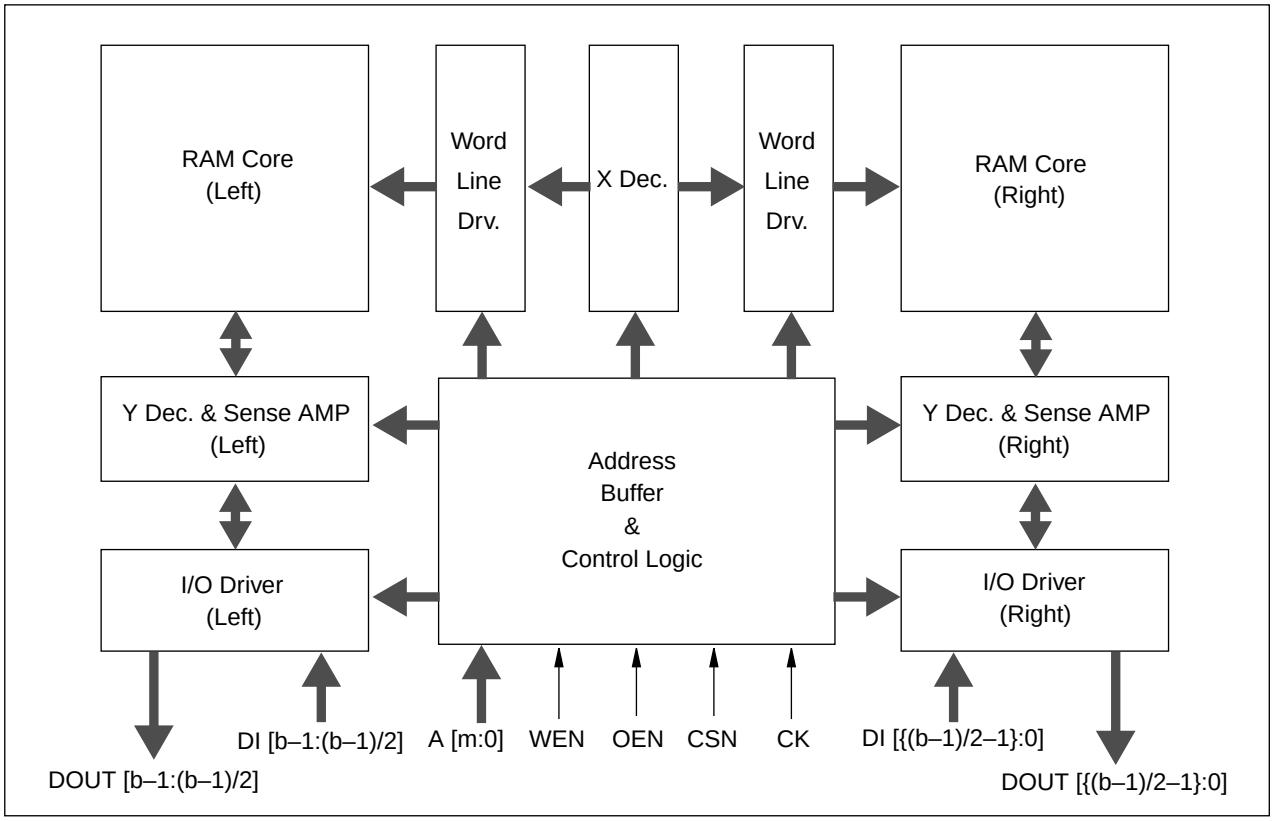
To enlarge the capacity of SPSRAM, we added one more option to choose number of banks. If you want to use larger SPSRAM than 64K bit SPSRAM, you can select dual bank (ba = 2). You can also select dual bank for smaller one than 64K bit SPSRAM. Dual bank SPSRAM is a little bigger and a little faster than single bank one. (Please refer to the characteristic tables.)

Block Diagrams

< 1-bank >



< 2-bank >



Characteristic Reference Table

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{O}C, Output load = 10SL, Unit = ns)							
minckl	Minimum Clock Pulse Width Low	2.10	2.00	2.50	2.40	3.30	3.10
minckh	Minimum Clock Pulse Width High	5.90	5.90	6.30	6.20	6.90	6.70
t_{as}	Address Setup Time	0.30	0.30	0.50	0.50	0.70	0.70
t_{ah}	Address Hold Time	0.30	0.30	0.40	0.40	0.40	0.40
t_{cs}	CSN Setup Time	0.40	0.40	0.40	0.40	0.40	0.40
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{ds}	Data Input Setup Time	0	0	0	0	0	0
t_{dh}	Data Input Hold Time	3.00	2.80	3.70	3.40	5.10	4.70
t_{os}	OEN Setup Time	0	0	0	0	0	0
t_{oh}	OEN Hold Time	1.70	1.70	1.90	1.80	2.20	2.00
t_{ws}	WEN Setup Time	0	0	0	0	0	0
t_{wh}	WEN Hold Time	0	0	0	0	0	0
t_{acc}	Access Time	3.20	3.10	3.70	3.50	4.90	4.50
t_{da}	Deaccess Time	2.30	2.20	2.50	2.30	2.70	2.30
mincyc	Minimum Clock Cycle Time	8.20	8. 0	9.40	9.00	11.80	11.00
SIZE (μm)							
Width		622	703	1131	1212	2142	2222
Height		902	902	1501	1501	2697	2697
POWER (μW/MHz)							
power_ck (normal mode: CSN Low)			593		1165		2403
power_csn (stand-by mode: CSN High)			54		96		155

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
B: Bits per Word
Y: Ymux Type
BA: Number of Banks (1 or 2)
S: Input Slope (Unit: ns)
SL: Number of Fanouts (Unit: Standard Load)
VDD: Operating Voltage (Unit: V)
F: Operating Frequency (Unit: MHz)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
cycle_time	(5.8213e – 03 * W + 1.1171e – 02 * B / BA + 9.6628e – 01 * 0.02 * SL + 3.7318) * 1.08
minckh	(1.9096e – 03 * W + 2.4791e – 03 * B / BA + 1.2200 * 0.02 * SL + 2.1295)
minckl	(2.1603e – 03 * W + 3.5437e – 03 * B / BA + 1.7035 + 2.8208e – 07 * W * B / BA)
tacc	(2.8038e – 03 * W + 5.8650e – 03 * B / BA + 1.7115e – 01 * S + 4.9717e – 01 * 0.02 * SL + 2.3023)
	Y = 4
cycle_time	(2.9106e – 03 * W + 2.2342e – 02 * B / BA + 9.6628e – 01 * 0.02 * SL + 3.7318) * 1.08
minckh	(9.5482e – 04 * W + 4.9583e – 03 * B / BA + 1.2200 * 0.02 * SL + 2.1295)
minckl	(1.0801e – 03 * W + 7.0874e – 03 * B / BA + 1.7035 + 2.8207e – 07 * W * B / BA)
tacc	(1.4019e – 03 * W + 1.1730e – 02 * B / BA + 1.7115e – 01 * S + 4.9717e – 01 * 0.02 * SL + 2.3023)
	Y = 8
cycle_time	(1.4553e – 03 * W + 4.4684e – 02 * B / BA + 9.6628e – 01 * 0.02 * SL + 3.7318) * 1.08
minckh	(4.7741e – 04 * W + 9.9166e – 03 * B / BA + 1.2200 * 0.02 * SL + 2.1295)
minckl	(5.4009e – 04 * W + 1.4174e – 02 * B / BA + 1.7035 + 2.8208e – 07 * W * B / BA)
tacc	(7.0097e – 04 * W + 2.3460e – 02 * B / BA + 1.7115e – 01 * S + 4.9717e – 01 * 0.02 * SL + 2.3023)
	Y = 16
cycle_time	(7.2766e – 04 * W + 8.9369e – 02 * B / BA + 9.6628e – 01 * 0.02 * SL + 3.7318) * 1.08
minckh	(2.3870e – 04 * W + 1.9833e – 02 * B / BA + 1.2200 * 0.02 * SL + 2.1295)
minckl	(2.7004e – 04 * W + 2.8349e – 02 * B / BA + 1.7035 + 2.8208e – 07 * W * B / BA)
tacc	(3.5048e – 04 * W + 4.6920e – 02 * B / BA + 1.7115e – 01 * S + 4.9717e – 01 * 0.02 * SL + 2.3023)
	Y = 32
cycle_time	(3.6383e – 04 * W + 1.7873e – 01 * B / BA + 9.6628e – 01 * 0.02 * SL + 3.7318) * 1.08
minckh	(1.1935e – 04 * W + 3.9666e – 02 * B / BA + 1.2200 * 0.02 * SL + 2.1295)
minckl	(1.3502e – 04 * W + 5.6699e – 02 * B / BA + 1.7035 + 2.8205e – 07 * W * B / BA)
tacc	(1.7524e – 04 * W + 9.3840e – 02 * B / BA + 1.7115e – 01 * S + 4.9717e – 01 * 0.02 * SL + 2.3023)

2) Power Characteristics [Unit: μW]

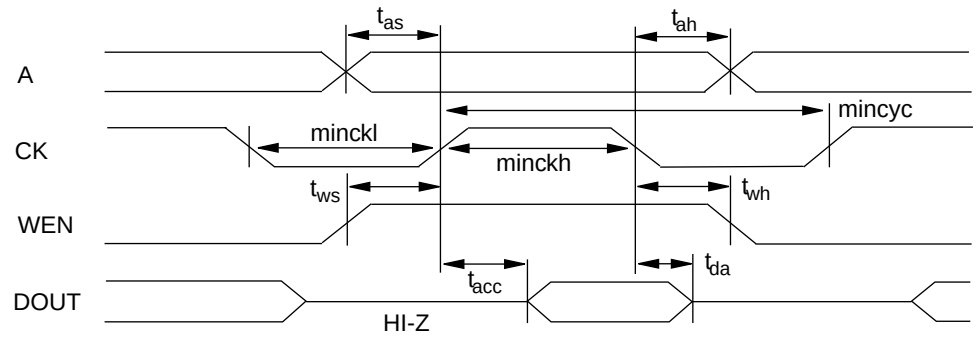
Power Type	Power Equation
	Y = 2
power_ck	(1.7046e – 01 * W + 8.7926e – 01 * B + 1.2869 + 7.9009e – 04 * W * B) * VDD^2 * F
power_csn	(4.6346e – 03 * W + 1.3484e – 01 * B + 5.8215e – 01 – 9.0563e – 05 * W * B) * VDD^2 * F
	Y = 4
power_ck	(8.5232e – 02 * W + 1.7585 * B + 1.2869 + 7.9009e – 04 * W * B) * VDD^2 * F
power_csn	(2.3173e – 03 * W + 2.6969e – 01 * B + 5.8215e – 01 – 9.0563e – 05 * W * B) * VDD^2 * F
	Y = 8
power_ck	(4.1803e – 02 * W + 3.3360 * B + 3.3968e – 01 + 6.4193e – 04 * W * B) * VDD^2 * F
power_csn	(1.1586e – 03 * W + 5.3939e – 01 * B + 5.8215e – 01 – 9.0563e – 05 * W * B) * VDD^2 * F
	Y = 16
power_ck	(1.8749e – 02 * W + 5.2054 * B + 3.5471 + 8.7095e – 04 * W * B) * VDD^2 * F
power_csn	(5.7933e – 04 * W + 1.0787 * B + 5.8215e – 01 – 9.0563e – 05 * W * B) * VDD^2 * F
	Y = 32
power_ck	(9.0824e – 03 * W + 9.4829 * B + 4.6843 + 7.9026e – 04 * W * B) * VDD^2 * F
power_csn	(2.8966e – 04 * W + 2.1575 * B + 5.8215e – 01 – 9.0563e – 05 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 6 * ($\lceil \log_2 (W / Y) \rceil$) + 76.3 * BA + 4.4(B * Y / 4 + BA) + 6.75 * B * Y + 2.25 [μm]
Height = 297.5 + 9.35 * W / Y + M [μm]
M = 5.75 (if Y = 2, 4, 8, 16), M = 8.15 (if Y = 32)

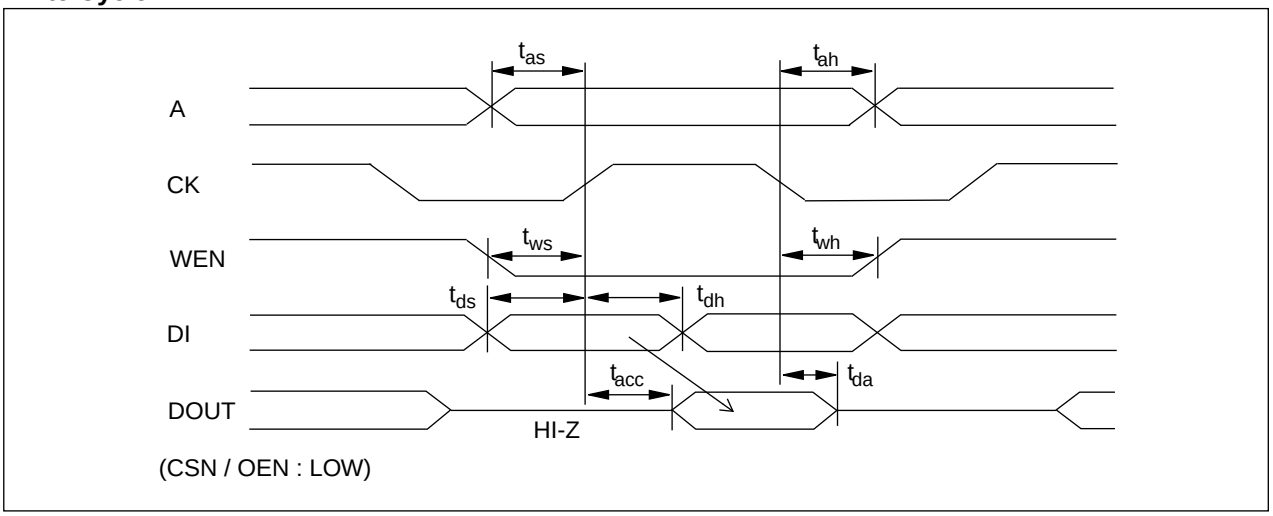
Timing Diagrams

Read Cycle

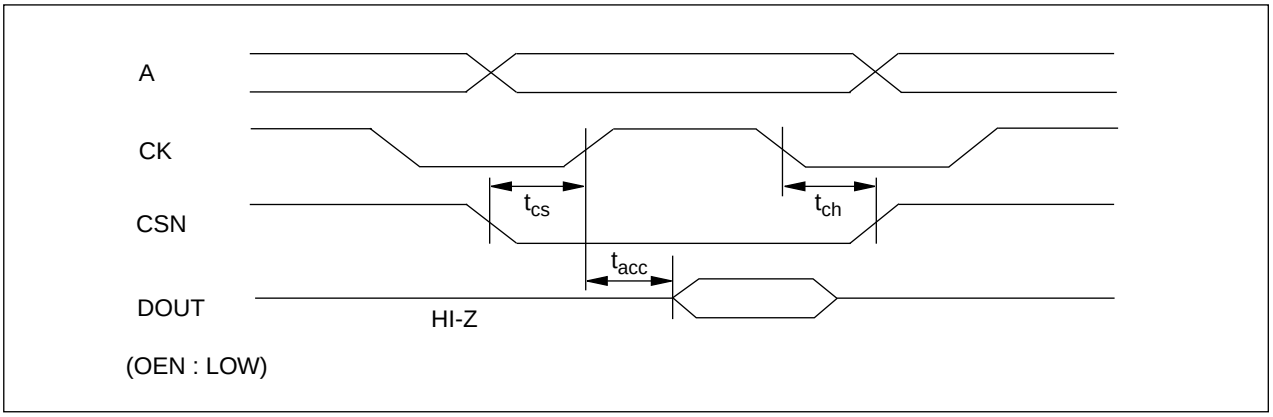


(CSN / OEN : LOW)

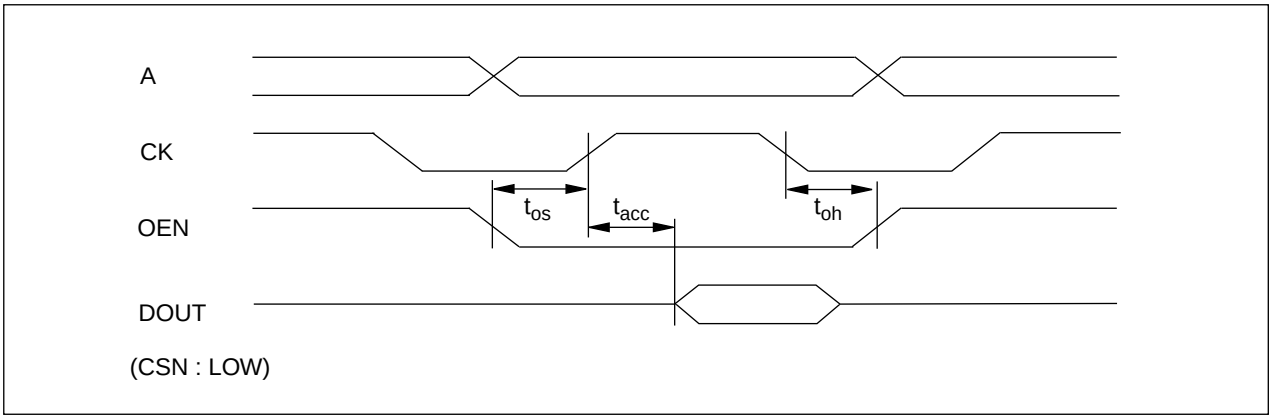
Write Cycle



CSN Control



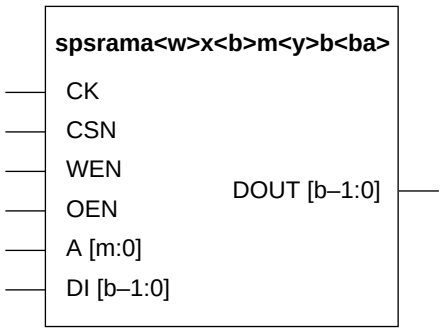
OEN Control



SPSRAMA Gen

Single-Port Synchronous RAM Generator – Alternative

Logic Symbol



NOTES:

1. Words (w) is the number of words in SPSRAMA.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Write completed at falling edge of clock
- Possible read modified write cycle
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Possible bi-directional operation
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 128K bits capacity
- Up to 8K number of words
- Up to 256 number of bits per word

Function Description

SPSRAMA is a single-port synchronous static RAM. When WEN is high and CK rises, DOUT [ ] presents data stored in the location addressed by A [ ]. When WEN is low and CK falls, or when CK is high and WEN rises, the value of DI [ ] is written into the location addressed by A [ ]. CSN is used to enable/disable the clock. OEN is used to enable/disable the data output driver.
SPSRAMA is an alternative of SPSRAM. The major difference of these two RAMs is the timing of read and write. SPSRAMA reads and writes at different edge of the clock since SPSRAM reads and writes at the same edge of the clock.

Generators and Cell Configurations

SPSRAMA Gen. generates layout, netlist, symbol and functional & timing model of SPSRAMA. The layout of SPSRAMA is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of SPSRAMA, you can give certain values to following four generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	4	8	16	32	64
		Max	512	1024	2048	4096	8192
		Step	2	4	8	16	32
Bpw (b)	ba = 1	Min	1	1	1	1	1
		Max	128	64	32	16	8
		Step	1	1	1	1	1
	ba = 2	Min	2	2	2	2	2
		Max	256	128	64	32	16
		Step	1	1	1	1	1

Pin Descriptions

Name	I/O	Description
CK	I	“Clock” serves as the input clock to the memory block. When CK is low, the memory is in a precharge state. Upon the rising edge, a read cycle begins. Upon the falling edge, a write cycle ends.
CSN	I	“Chip Select Negative” acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read or write access occur. CSN may not change during CK is high.
WEN	I	“Write Enable Negative” selects the type of memory access. Read is the high state, and write is the low state. When WEN rises while CK is high, a write cycle ends.
OEN	I	“Output Enable Negative” controls the output drivers from driven to tri-state condition. OEN may not change during CK is high.
A [ ]	I	“Address” selects the location to be accessed. A [ ] may not change during CK is high.
DI [ ]	I	When CK falls while WEN is low, or when WEN rises while CK is high, the “Data In” word value is written to the accessed location.
DOUT [ ]	O	During a read access, data word stored will be presented to the “Data Out” ports. DOUT [ ] is tri-statable. When CK is high, CSN is low and OEN is low, only then, DOUT [ ] drives a certain value. Otherwise, DOUT [ ] keeps Hi-Z state. During a write access, the value of DOUT [ ] is unpredictable.

Pin Capacitance

(Unit = SL)

	CK	CSN	WEN	OEN	A	DI	DOUT				
							Ymux 2	Ymux 4	Ymux 8	Ymux 16	Ymux 32
1-bank	3.5	1.0	0.5	1.6	1.2	2.1	3.1	3.3	7.7	15.0	31.0
2-bank	7.0	2.1	1.0	3.1	1.2	2.1	3.1	3.3	7.7	15.0	31.0

Application Notes

1) Putting Busholders on DOUT [ ]

As you will see in the timing diagrams, DOUT [ ] is valid only when CK is high. If you want DOUT [ ] to be stable regardless of CK state, you should put STDL80 Busholder cells on the DOUT [ ] bus externally.

2) Customizing Aspect Ratio

Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 5 selections of Ymux for the same Words and the same Bpw SPSRAMA. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of SPSRAM, In general, larger Ymux SPSRAMA has faster speed and bigger area than smaller Ymux SPSRAMA.

3) Selecting Number of Banks

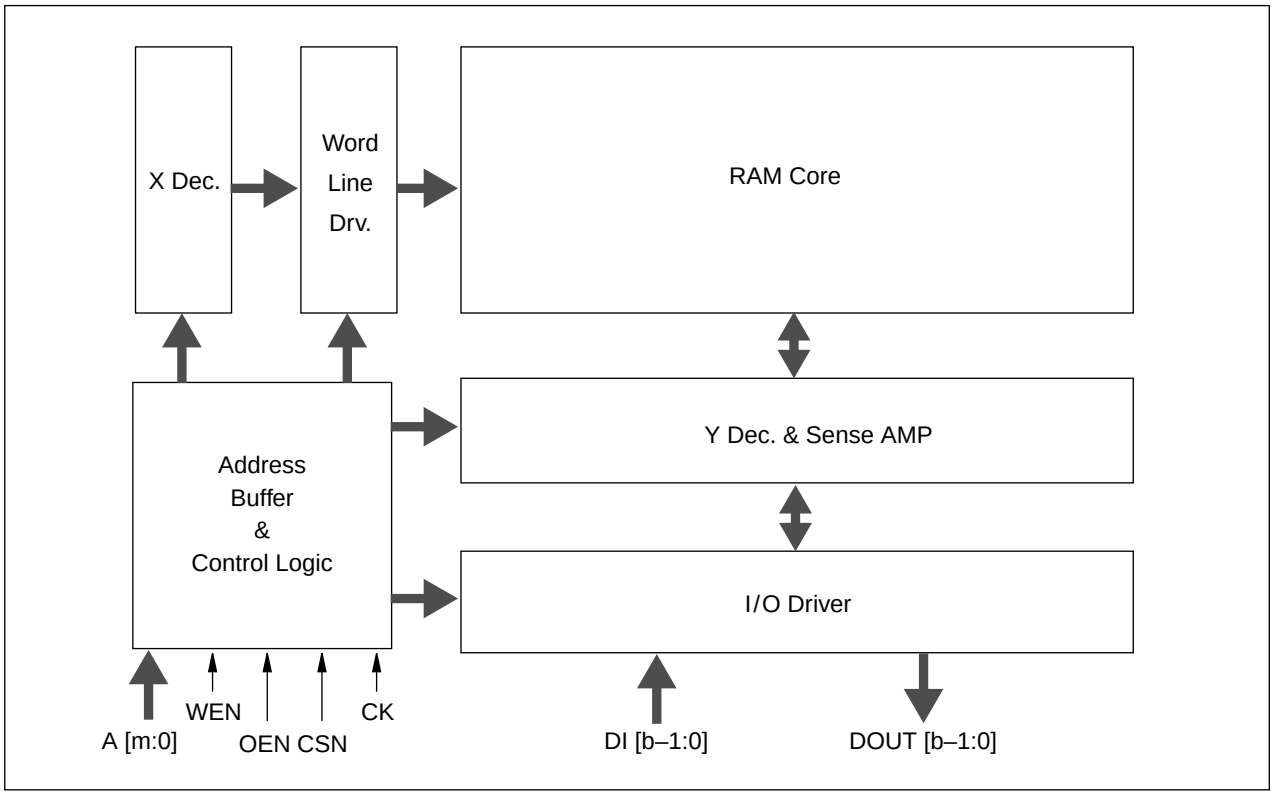
To enlarge the capacity of SPSRAMA, we added one more option to choose number of banks. If you want to use larger SPSRAMA than 64K bit SPSRAMA, you can select dual bank (ba = 2). You can also select dual bank for smaller one than 64K bit SPSRAMA. Dual bank SPSRAMA is a little bigger and a little faster than single bank one. (Please refer to the characteristic tables.)

4) Using Bi-Directional Data Port

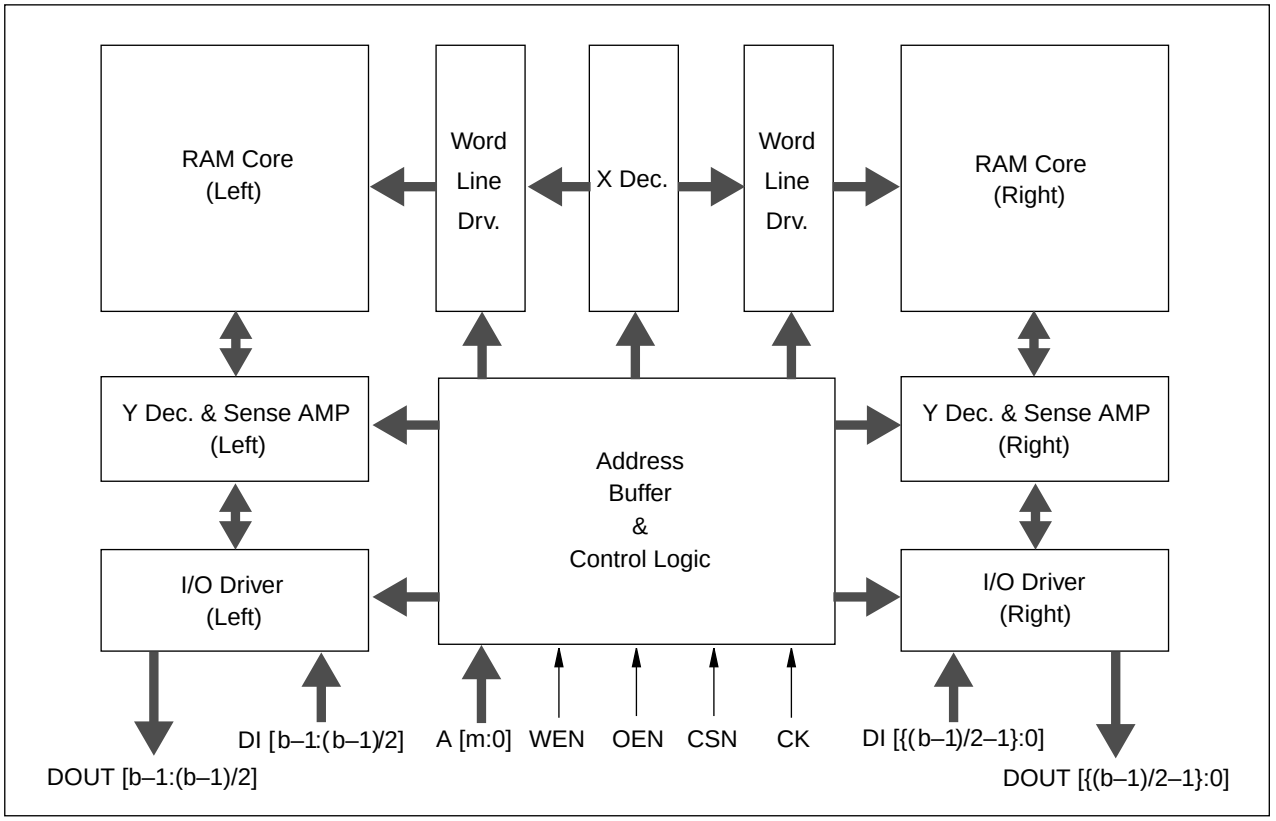
Because having the same phase, DI [ ] and DOUT [ ] of SPSRAMA can be tied directly. With tying them up together and controlling WEN and OEN properly, you can use them as bi-directional data ports.

Block Diagrams

< 1-bank >



< 2-bank >



Characteristic Reference Table

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{O}C, Output load = 10SL, Unit = ns)							
t_{rp}	Minimum Read Pulse Width	6.55	6.47	7.10	6.90	8.20	7.90
t_{pc}	Minimum Pre-Charge Period	2.73	2.52	3.90	3.40	6.20	5.30
t_{wp}	Minimum Write Pulse Width	1.20	1.20	1.52	1.55	2.10	2.20
t_{as}	Address Setup Time	0.44	0.44	0.63	0.63	1.03	1.02
t_{ah}	Address Hold Time	0.97	0.92	1.20	1.00	1.64	1.41
t_{cs}	CSN Setup Time	0.51	0.51	0.51	0.51	0.51	0.51
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{ds}	Data Input Setup Time	0.68	0.75	0.91	1.00	1.36	1.61
t_{dh}	Data Input Hold Time	1.74	1.59	2.04	1.75	2.66	2.00
t_{os}	OEN Setup Time	0	0	0	0	0	0
t_{oh}	OEN Hold Time	1.36	1.33	1.50	1.40	1.78	1.66
t_{wh}	WEN Hold Time	0.74	0.72	0.79	0.74	0.88	0.79
t_{acc}	Access Time	4.50	0.43	5.10	0.48	6.20	5.80
t_{da}	Deaccess Time	2.10	1.90	2.30	2.00	2.60	2.10
SIZE (µm)							
Width		622	703	1131	1212	2142	2222
Height		902	902	1501	1501	2697	2697
POWER (µW/MHz)							
power_ck (normal mode: CSN Low)		717		1816		5318	
power_csn (stand-by mode: CSN High)		48		93		197	

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
B: Bits per Word
Y: Ymux Type
BA: Number of Banks (1 or 2)
S: Input Slope (Unit: ns)
SL: Number of Fanouts (Unit: Standard Load)
VDD: Operating Voltage (Unit: V)
F: Operating Frequency (Unit: MHz)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
tpc	5.79e – 03 * W + 1.31e – 02 * B / BA + 3.48e – 01 * S + 1.1579
trp	3.14e – 03 * W + 4.71e – 03 * B / BA – 3.02e – 01 * S + 1.4025 * 0.02 * SL + 2.3669
tacc	2.82e – 03 * W + 6.89e – 03 * B / BA + 5.39e – 01 * 0.02 * SL + 2.3079
	Y = 4
tpc	2.89e – 03 * W + 2.63e – 02 * B / BA + 3.48e – 01 * S + 1.1579
trp	1.57e – 03 * W + 9.42e – 03 * B / BA – 3.02e – 01 * S + 1.4025 * 0.02 * SL + 2.3669
tacc	1.41e – 03 * W + 1.37e – 02 * B / BA + 5.39e – 01 * 0.02 * SL + 2.3079
	Y = 8
tpc	1.44e – 03 * W + 5.26e – 02 * B / BA + 3.48e – 01 * S + 1.1579
trp	7.85e – 04 * W + 1.88e – 02 * B / BA – 3.02e – 01 * S + 1.4025 * 0.02 * SL + 2.3669
tacc	7.06e – 04 * W + 2.75e – 02 * B / BA + 5.39e – 01 * 0.02 * SL + 2.3079
	Y = 16
tpc	7.23e – 04 * W + 1.05e – 01 * B / BA + 3.48e – 01 * S + 1.1579
trp	3.92e – 04 * W + 3.76e – 02 * B / BA – 3.02e – 01 * S + 1.4025 * 0.02 * SL + 2.3669
tacc	3.53e – 04 * W + 5.51e – 02 * B / BA + 5.39e – 01 * 0.02 * SL + 2.3079
	Y = 32
tpc	3.61e – 04 * W + 2.10e – 01 * B / BA + 3.48e – 01 * S + 1.1579
trp	1.96e – 04 * W + 7.53e – 02 * B / BA – 3.02e – 01 * S + 1.4025 * 0.02 * SL + 2.3669
tacc	1.76e – 04 * W + 1.10e – 01 * B / BA + 5.39e – 01 * 0.02 * SL + 2.3079

2) Power Characteristics [Unit: μW]

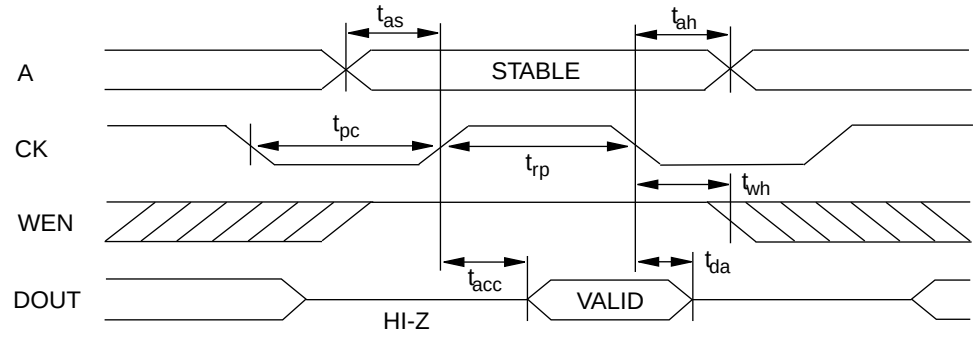
Power Type	Power Equation
	Y = 2
power_ck	(1.6311e – 01 * W + 6.2978e – 01 * B + 4.9380 + 4.8722e – 03 * W * B) * VDD^2 * F
power_csn	(3.7429e – 03 * W + 9.8542e – 02 * B + 5.8775e – 01 + 4.6534e – 05 * W * B) * VDD^2 * F
	Y = 4
power_ck	(8.1556e – 02 * W + 1.2595 * B + 4.9380 + 4.8722e – 03 * W * B) * VDD^2 * F
power_csn	(1.8714e – 03 * W + 1.9708e – 01 * B + 5.8775e – 01 + 4.6534e – 05 * W * B) * VDD^2 * F
	Y = 8
power_ck	(4.0778e – 02 * W + 2.5191 * B + 4.9380 + 4.8722e – 03 * W * B) * VDD^2 * F
power_csn	(9.3573e – 04 * W + 3.9417e – 01 * B + 5.8775e – 01 + 4.6534e – 05 * W * B) * VDD^2 * F
	Y = 16
power_ck	(2.0389e – 02 * W + 5.0382 * B + 4.9380 + 4.8722e – 03 * W * B) * VDD^2 * F
power_csn	(4.6786e – 04 * W + 7.8834e – 01 * B + 5.8775e – 01 + 4.6534e – 05 * W * B) * VDD^2 * F
	Y = 32
power_ck	(1.0194e – 02 * W + 1.0076e + 01 * B + 4.9380 + 4.8722e – 03 * W * B) * VDD^2 * F
power_csn	(2.3393e – 04 * W + 1.5766 * B + 5.8775e – 01 + 4.6534e – 05 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 6 * ($\lceil \log_2 (W / Y) \rceil$) + 76.3 * BA + 4.4 (B * Y / 4 + BA) + 6.75 * B * Y + 2.25 [μm]
Height = 297.5 + 9.35 * W / Y + M [μm]
M = 5.75 (if Y = 2, 4, 8, 16), M = 8.15 (if Y = 32)

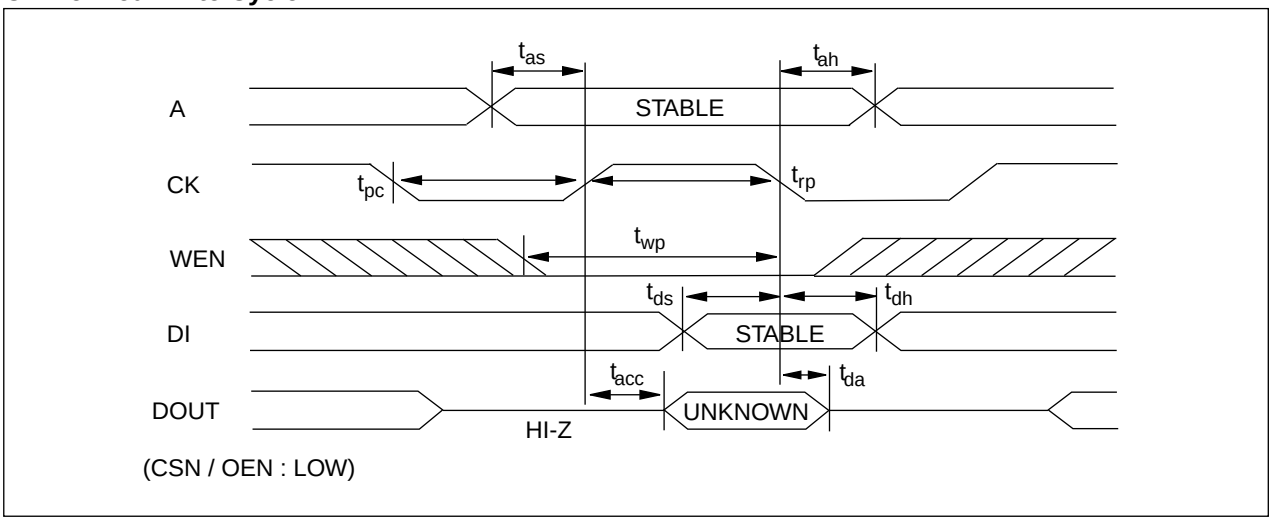
Timing Diagrams

Read Cycle

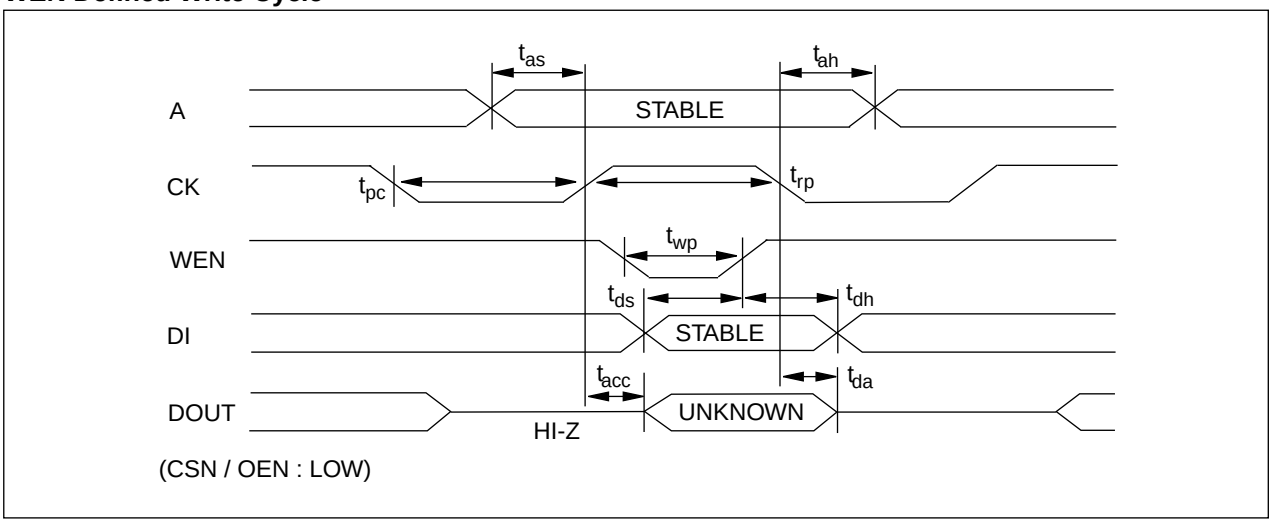


(CSN / OEN : LOW, DI :DON'T CARE)

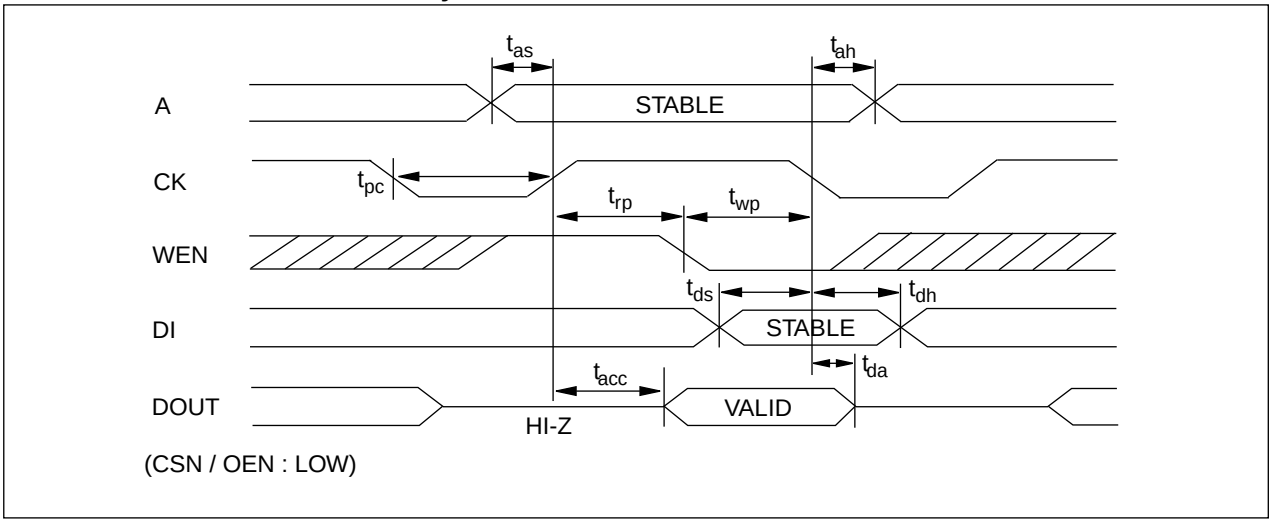
CK Defined Write Cycle



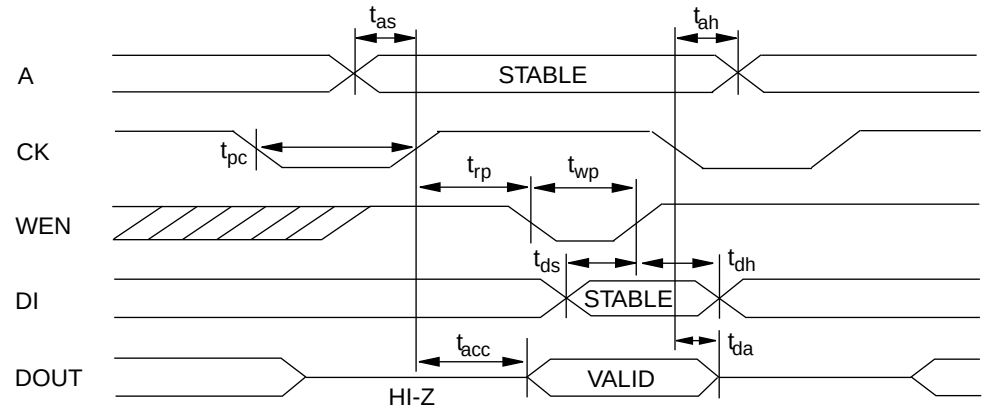
WEN Defined Write Cycle



CK Defined Read-Modified-Write Cycle

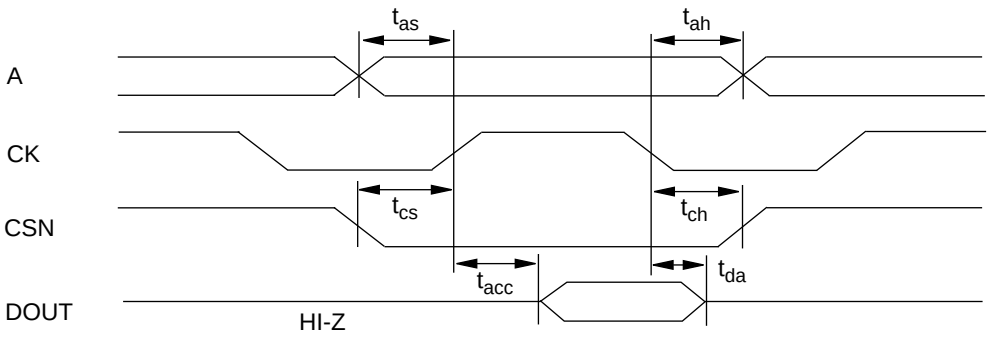


WEN Defined Read-Modified-Write Cycle



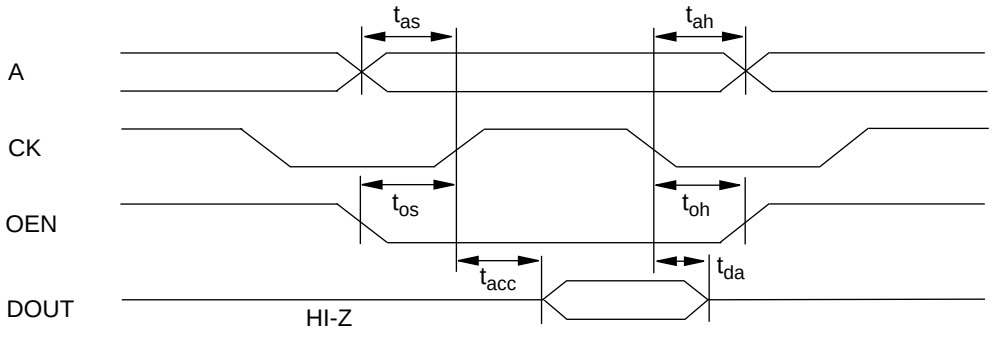
(CSN / OEN : LOW)

CSN Control



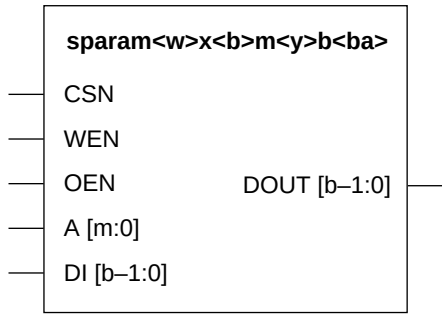
(OEN : LOW, WEN / DI : DON'T CARE)

OEN Control



(CSN : LOW, WEN / DI : DON'T CARE)

Logic Symbol



NOTES:

1. Words (w) is the number of words in SPARAM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Asynchronous operation
- Address transition detectors
- Write enable transition detector
- Chip select transition detector
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 128K bits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

A SPARAM is a single port asynchronous static RAM. When WEN is high, just after the address(A[]) transition, DOUT[ ] presents the data stored in the location addressed by A[]. Upon WEN rising edge, the value of DI[] is written into the location addressed by A[ ]. CSN is used to enable/disable the accesses. OEN is used to enable/disable the data output driver.

Generators and Cell Configurations

SPARAM generates layout, netlist, symbol and functional & timing model of a SPARAM. The layout of SPARAM is an automatically generated array of custom, pitch-matched leaf cells. There are four generator parameters to resolve the configuration of a SPARAM.

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	16	32	64	128
		Max	1024	2048	4096	8192
		Step	8	16	32	64
Bpw (b)	ba = 1	Min	1	1	1	1
		Max	64	32	16	8
		Step	1	1	1	1
	ba = 2	Min	2	2	2	2
		Max	128	64	32	16
		Step	1	1	1	1

SPARAM Gen

Single-Port Asynchronous RAM Generator

Pin Descriptions

Name	I/O	Description
CSN	I	"Chip Select Negative" acts as the memory enable signal for selecting one of multiple memory blocks. When CSN is high, DOUT[ ] goes to Hi-Z state, the memory goes to stand-by (power down) mode and no access to the memory can occur. Conversely, if CSN is low only then may a read or write access occur. When CSN falls, a read access is initiated. CSN should be stable when WEN is low.
WEN	I	"Write Enable Negative" selects the type of memory access. When WEN is high, the SPARAM is in read mode. Otherwise, it is in write mode. Upon the rising edge of WEN, a write access completed and a read access initiated. When WEN is low, A[ ] and CSN should be stable.
OEN	I	"Output Enable Negative" unconditionally enables or disables the output drivers.
A [ ]	I	"Address" selects the location to be accessed. When A[ ] changes, the transition is detected and the internal clock pulse will be generated. A[ ] should be stable when WEN is low.
DI [ ]	I	When WEN rises, the "Data In" word value is written to the location addressed.
DOUT [ ]	O	During a read access, the data word stored will be presented to the "Data OUT" ports. DOUT[ ] is tri-statable. When CSN is low and OEN is low, only then, DOUT[ ] drives a certain value. Otherwise, DOUT[ ] keeps Hi-Z state. During a write access, the data on DOUT is unpredictable.

Pin Capacitance

(Unit = SL)

	CSN	WEN	OEN	A	DI	DOUT			
						Ymux 4	Ymux 8	Ymux 16	Ymux 32
1-bank	9.7	4.2	0.7	4.2	1.9	5.5	11.7	24.1	49.0
2-bank	19.3	8.4	1.3	4.2	1.9	5.5	11.7	24.1	49.0

Application Notes

1) Fitting the Layout Shape(Aspect Ratio)

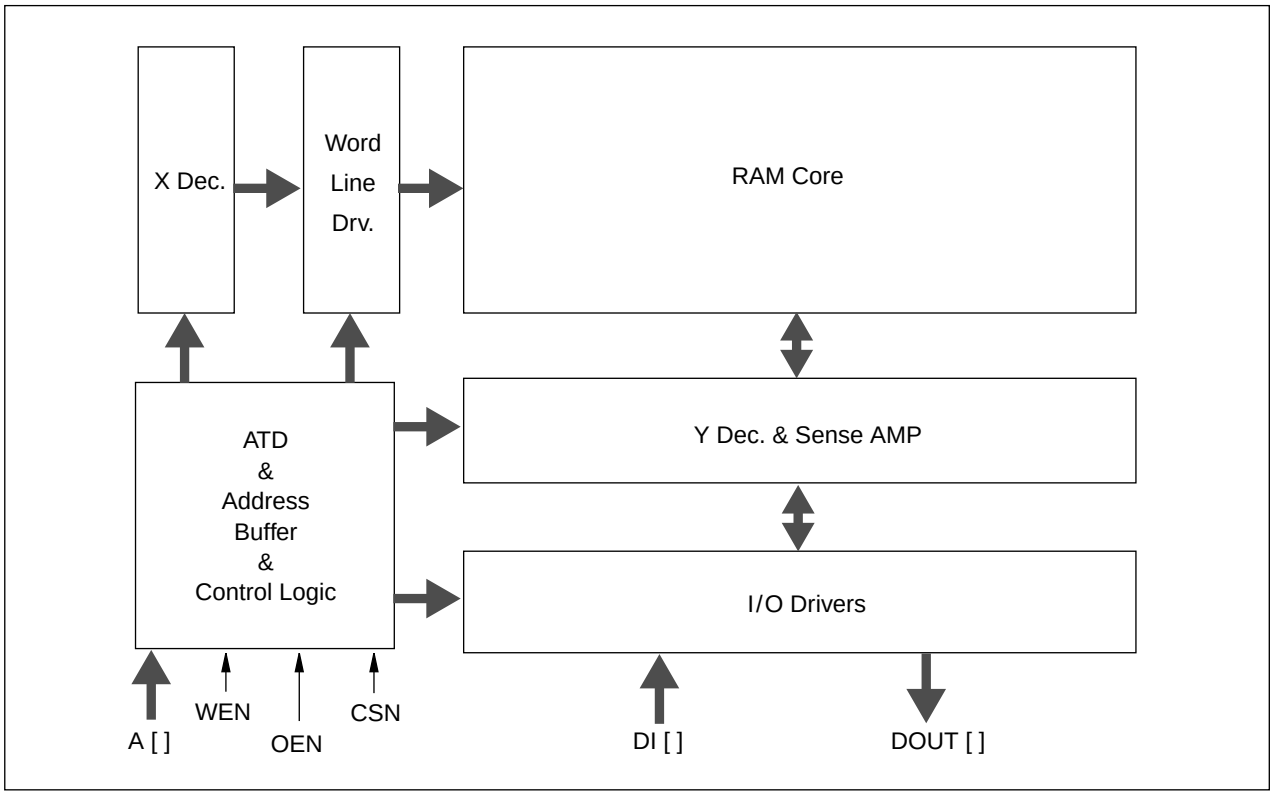
Layout Shape can be fitted by choosing one of 4 Ymux parameters in the above configuration table in accordance with your chip level layout design preference. Larger one makes the layout shape flat and short. Smaller one makes it thin and tall. In general, flat and short SPARAM is faster than thin and tall one.

2) Selecting Number of Banks

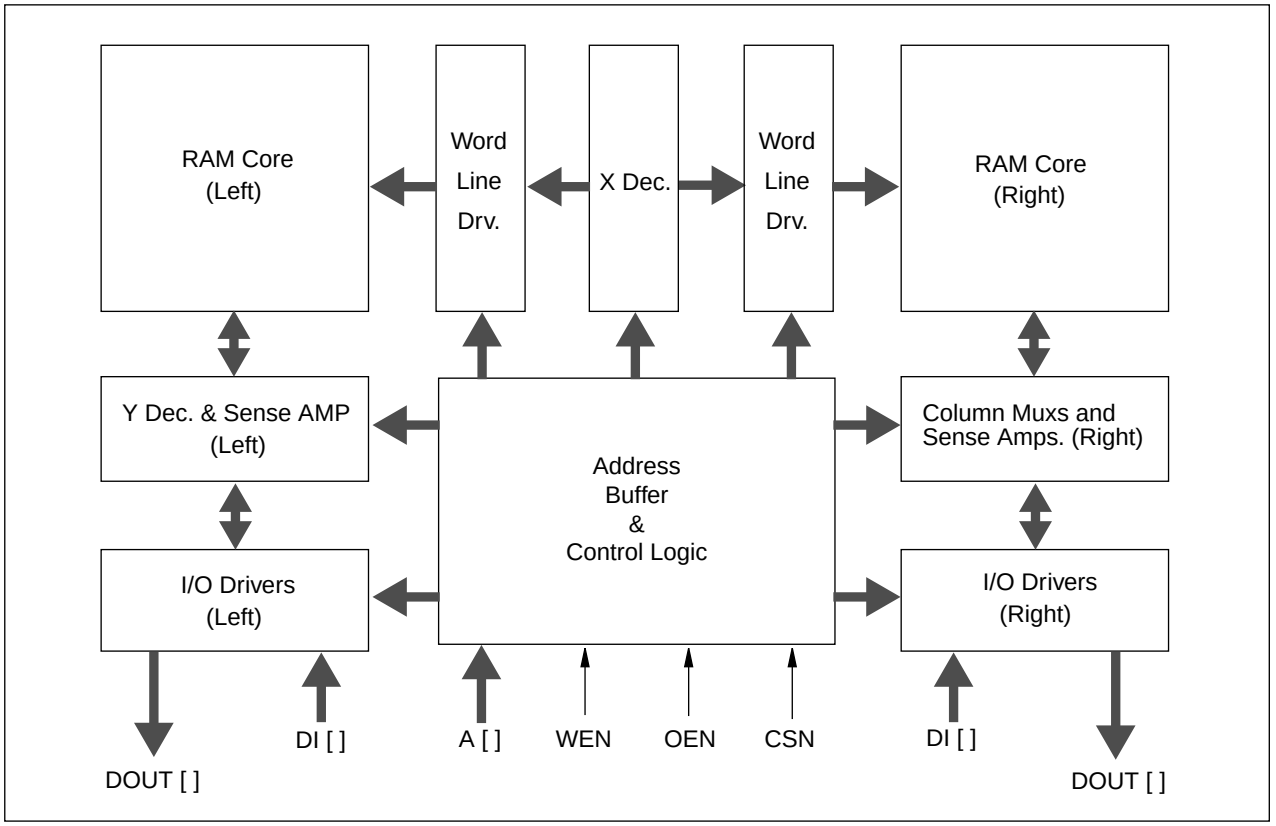
The maximum capacity of SPARAM (ba=1) reaches to 64K. It can be doubled by setting the bank parameter (ba) 2 and the bpw double. In that case, note that the words can't be doubled. By the way, the bank parameter ba=2 can be applied to the configuration smaller than 64K. Please refer to the configuration table above. SPARAM (ba=2) is a little bigger than SPARAM (ba=1) for the same capacity.

Block Diagrams (1 Bank)

< 1-bank >



< 2-bank >



Characteristic Reference Table

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING (Typical process, 3.3V, 25 ^{o}C, Output load = 10SL, Input slop = 0.2ns, Unit = ns)							
t_{acc}	Access Time	6.1	6.1	6.3	6.3	6.8	6.8
t_{da}	Deaccess Time	0.7	0.7	0.7	0.7	0.7	0.7
t_{dz}	Active to Hi-Z	1.4	1.4	1.4	1.4	1.4	1.4
t_{zd}	Hi-Z to Active	1.7	1.7	1.7	1.7	1.7	1.7
t_{as}	Address Setup Time	0.1	0.1	0.1	0.1	0.1	0.1
t_{ah}	Address Hold Time	1.1	1.0	1.2	1.1	1.4	1.1
t_{ds}	Input Data Setup Time	0.6	0.7	0.7	0.9	0.8	1.1
t_{dh}	Input Data Hold Time	0.8	0.7	1.0	0.8	1.4	1.0
t_{wen}	Minimum WEN Pulse Width Low	3.0	3.0	3.1	3.1	3.3	3.3
t_{cs}	CSN Setup Time	0.1	0.1	0.1	0.1	0.1	0.1
t_{ch}	CSN Hold Time	1.4	1.4	1.4	1.4	1.6	1.6
SIZE (μm)							
Width		723	891	1206	1374	2172	2340
Height		972	972	1577	1577	2786	2786
POWER (μW/MHz)							
power_add (normal mode: CSN Low)			1418		2776		6370
power_csn (stand-by mode: CSN High)			228		435		827

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
Y: Ymux Type
S: Input Slope (Unit: ns)
VDD: Operating Voltage (Unit: V)
B: Bits per Word
BA: Number of Banks (1 or 2)
SL: Number of Fanouts (Unit: Standard Load)
F: Operating Frequency (Unit: MHz)

Condition: Typical process, 3.3V, 25 ^{o}C

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 4
tacc	(9.19e-04*W+6.28e-02*S+1.34e-01*SL*0.020+5.77)
twen	(4.05e-04*W+2.26e-01*S+2.77-3.03e-05*W*S)
	Y = 8
tacc	(4.59e-04*W+6.28e-02*S+1.34e-01*SL*0.020+5.77)
twen	(2.02e-04*W+2.26e-01*S+2.77-1.51e-05*W*S)
	Y = 16
tacc	(2.29e-04*W+6.28e-02*S+1.34e-01*SL*0.020+5.77)
twen	(1.01e-04*W+2.26e-01*S+2.77-7.57e-06*W*S)
	Y = 32
tacc	(1.14e-04*W+6.28e-02*S+1.34e-01*SL*0.020+5.77)
twen	(5.07e-05*W+2.26e-01*S+2.77-3.78e-06*W*S)

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 4
power_add	(3.0602e-02*W+3.8308*B+4.0483e+01 +5.0528e-03*W*B)*VDD^2*F
power_csn	(1.6749e-02*W+9.3084e-01*B+2.4629 -4.7554e-05*W*B)*VDD^2*F
	Y = 8
power_add	(9.9226e-03*W+6.2904*B+4.0384e+01 +6.3934e-03*W*B)*VDD^2*F
power_csn	(8.3748e-03*W+1.8616*B+2.4629 -4.7554e-05*W*B)*VDD^2*F
	Y = 16
power_add	(6.0183e-03*W+1.3309e+01*B+4.3131e+01 +4.6519e-03*W*B)*VDD^2*F
power_csn	(4.1874e-03*W+3.7233*B+2.4629 -4.7554e-05*W*B)*VDD^2*F
	Y = 32
power_add	(2.0329e-03*W+2.6417e+01*B+4.6469e+01 +4.7973e-03*W*B)*VDD^2*F
power_csn	(2.0937e-03*W+7.4467*B+2.4629 -4.7554e-05*W*B)*VDD^2*F

NOTES:

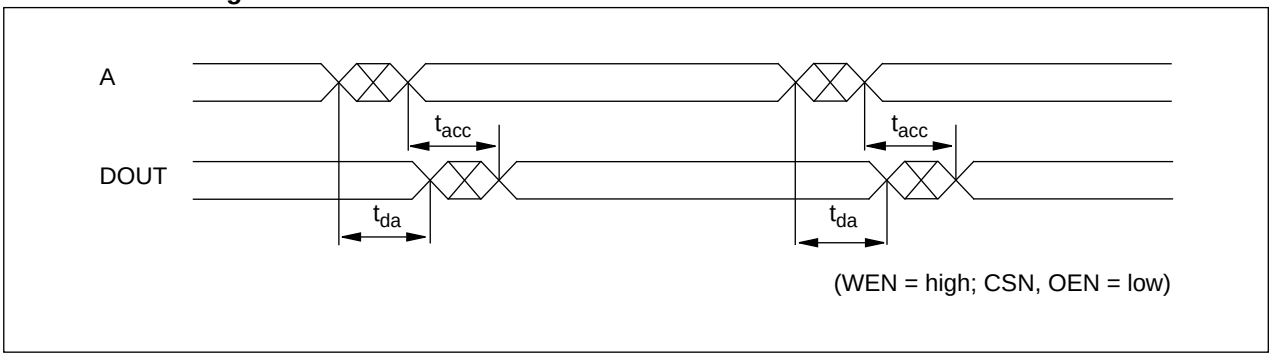
1. power_add : This is a normal mode power of memory. When CSN is low.
2. power_csn : This is a standby mode power of memory. When CSN is high.

3) Size Equation [Unit: μm]

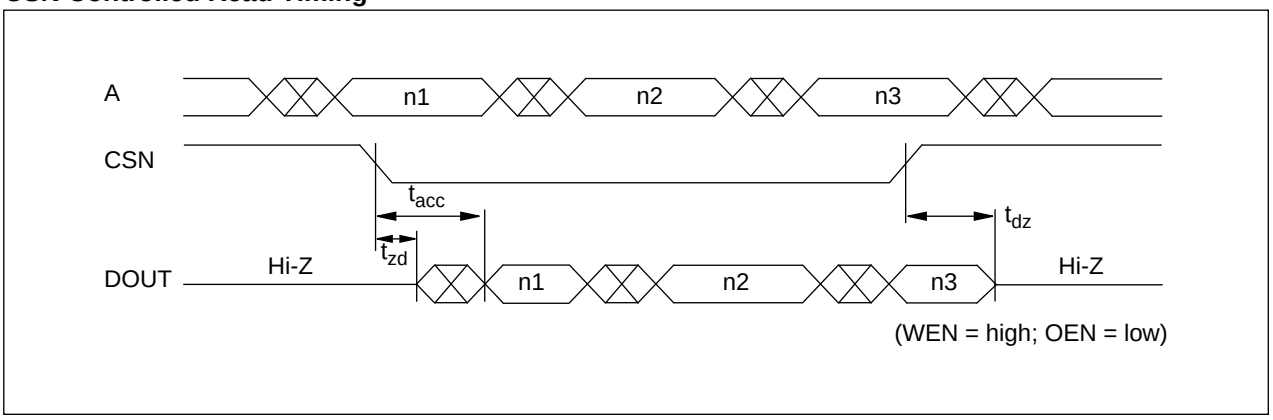
Width = 12*(log2(W/Y))+170*BA+7.55*(B*Y)-5
Height = 366.7+9.45*W/Y

Timing Diagrams

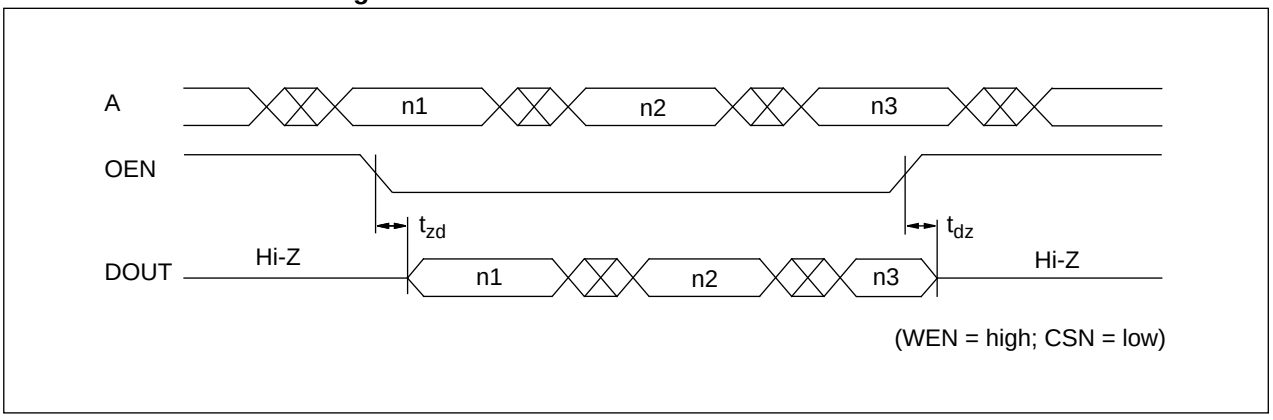
Basic Read Timing



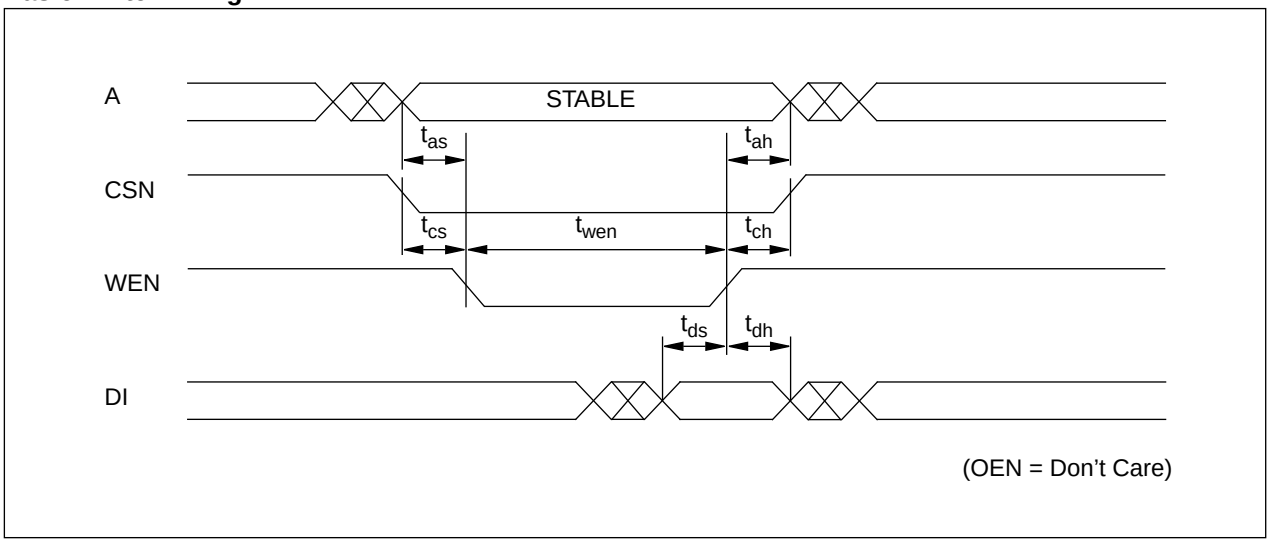
CSN Controlled Read Timing



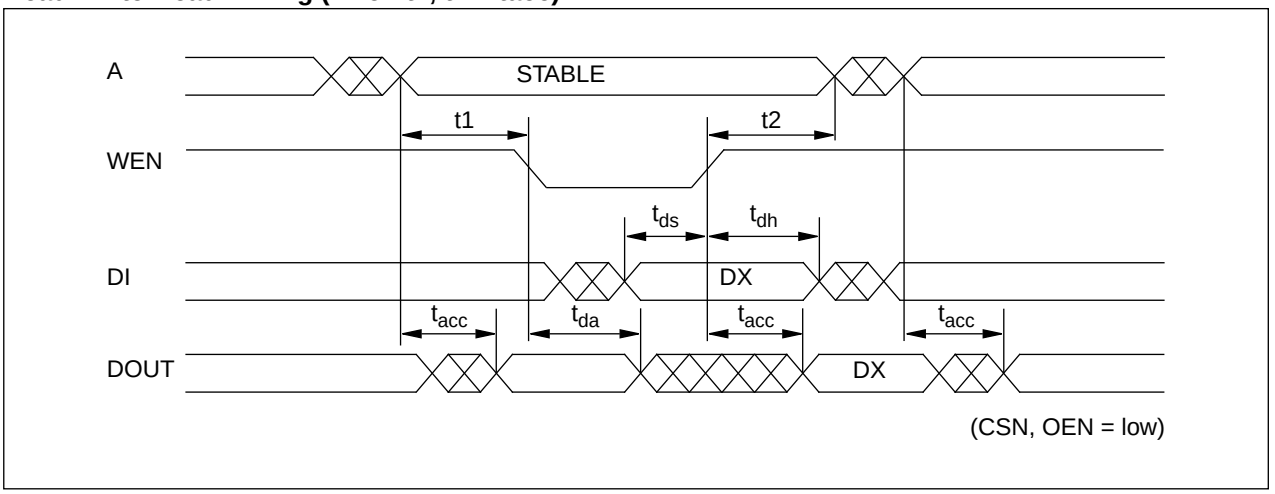
OEN Controlled Read Timing



Basic Write Timing



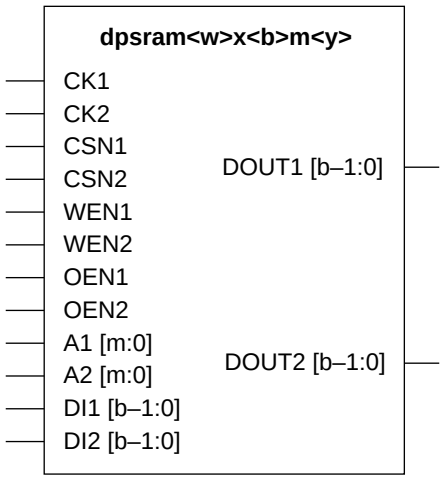
Read-Write-Read Timing (when t1, t2 > tacc)



DPSRAM Gen

Dual-Port Synchronous RAM Generator

Logic Symbol



NOTES:

1. Words (w) is the number of words in DPSRAM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Write completed at rising edge of clock
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Flexible aspect ratio
- Up to 64K bits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

DPSRAM is a dual-port synchronous static RAM. When CK1 rises, if WEN1 is high, DOUT1 [ ] presents data stored in the location addressed by A1 [ ], otherwise the value of DI1 [ ] is written into the location addressed by A1 [ ]. CSN1 is used to enable/disable CK1. OEN1 is used to enable/disable tri-state drivers of DOUT1 [ ]. The functionality of port2 is the same to port1. The port1 and port2 function independently each other.

Generators and Cell Configurations

DPSRAM Gen. generates layout, netlist, symbol and functional & timing model of DPSRAM. The layout of DPSRAM is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of DPSRAM, you can give certain values to following three generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y).

The valid range of these parameters is specified in the following table:

Parameters		YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	Min	4	8	16	32	64
	Max	512	1024	2048	4096	8192
	Step	2	4	8	16	32
Bpw (b)	Min	1	1	1	1	1
	Max	128	64	32	16	8
	Step	1	1	1	1	1

Pin Descriptions

Name	I/O	Description
CK1 CK2	I	“Clock”s serve as input clocks to each port of the memory block. When CK1 (CK2) is low, port1 (port2) is in a precharge state. Upon the rising edge, an access begins.
CSN1 CSN2	I	“Chip Select Negative”s act as each port’s enable signal for selections of multiple blocks on a common clock. When CSN1 (CSN2) is high, port1 (port2) goes to stand-by (power down) mode and no access can occur, conversely, if low only then may a read or write access occur. CSN1 (CSN2) may not change during CK1 (CK2) is high.
WEN1 WEN2	I	“Write Enable Negative”s select the type of memory access. Read is the high state, and write is the low state.
OEN1 OEN2	I	“Output Enable Negative”s control the output drivers from driven to tri-state condition. OEN1 (OEN2) may not change during CK1 (CK2) is high.
A1 [ ] A2 [ ]	I	“Address”es select the location to be accessed. A1 [ ] (A2 [ ]) may not change during CK1 (CK2) is high.
DI1 [ ] DI2 [ ]	I	When CK1 (CK2) rises while WEN1 (WEN2) is low, the “Data In” word value is written to the accessed location.
DOUT1 [ ] DOUT2 [ ]	O	During a read access, data word stored will be presented to the “Data Out” ports. DOUT1 [ ] and DOUT2 [ ] are tri-statable. Only when CK1 (CK2) is high, CSN1 (CSN2) and OEN1 (OEN2) is low, DOUT1 [ ] (DOUT2 [ ]) drives a certain value. Otherwise, DOUT1 [ ] (DOUT2 [ ]) keeps Hi-Z state. During a write access, data word written will be presented at the “Data Out” ports if output driver is enabled.

Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	A	DI	DOUT				
						Ymux 2	Ymux 4	Ymux 8	Ymux 16	Ymux 32
5.8	1.9	0.9	2.3	1.0	2.0	5.4	5.4	12.0	25.0	51.0

Application Notes

1) Putting Busholders on DOUT1 [ ] and DOUT2 [ ]

As you will see in the timing diagrams, DOUT1 [ ] (DOUT2 [ ]) is valid only when CK1 (CK2) is high. If you want DOUT1 [ ] (DOUT2 [ ]) to be stable regardless of CK1 (CK2) state, you should put STDL80 Busholder cells on the DOUT1 [ ] (DOUT2 [ ]) bus externally.

2) Customizing Aspect Ratio

Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 5 selections of Ymux for the same Words and the same Bpw DPSRAM. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of DPSRAM, In general, larger Ymux DPSRAM has faster speed and bigger area than smaller Ymux DPSRAM.

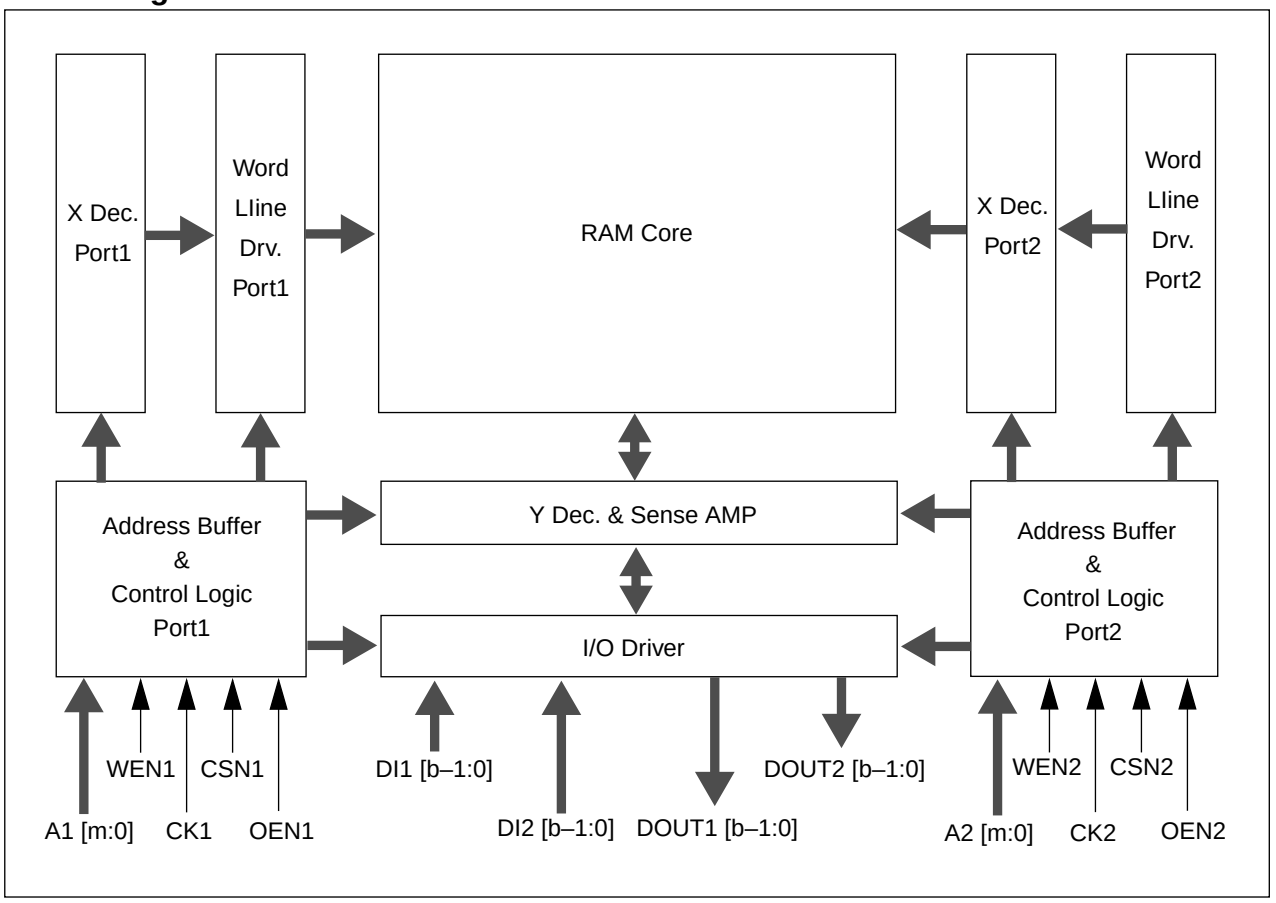
3) Contention Modes

Simultaneous accesses to the same location through both ports cause a contention. DPSRAM has no contention preventing scheme. You have to take care of the contention modes. Please refer to the timing diagrams of contention modes to get more information of contention modes.

DPSRAM Gen

Dual-Port Synchronous RAM Generator

Block Diagram



Characteristic Reference Table

Symbol	Description	256x16m4	1024x16m8	4Kx16m16
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{o}C, Output load = 10SL, Unit = ns)				
minckl	Minimum Clock Pulse Width Low	2.30	2.90	4.10
minckh	Minimum Clock Pulse Width High	4.00	4.60	5.70
t_{cc}	Clock to Clock Setup Time	3.20	4.30	6.40
t_{as}	Address Setup Time	0.31	0.55	0.96
t_{ah}	Address Hold Time	0.43	0.43	0.42
t_{cs}	CSN Setup Time	0.52	0.52	0.52
t_{ch}	CSN Hold Time	0	0	0
t_{ds}	Data Input Setup Time	0	0	0
t_{dh}	Data Input Hold Time	3.30	4.30	5.60
t_{os}	OEN Setup Time	0	0	0
t_{oh}	OEN Hold Time	1.45	1.60	1.83
t_{ws}	WEN Setup Time	0	0	0
t_{wh}	WEN Hold Time	0	0	0
t_{acc}	Access Time	3.40	4.00	5.30
t_{da}	Deaccess Time	1.90	2.00	2.40
mincyc	Minimum Clock Cycle Time	7.00	9.60	14.60
SIZE (μm)				
Width		996	1787	3353
Height		1110	1802	3194
POWER (μW/MHz)				
power_ck (normal mode: CSN Low)		805	1675	4094
power_csn (stand-by mode: CSN High)		118	217	370

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
Y: Ymux Type
S: Input Slope (Unit: ns)
VDD: Operating Voltage (Unit: V)
B: Bits per Word
SL: Number of Fanouts (Unit: Standard Load)
F: Operating Frequency (Unit: MHz)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
mincyc	(1.6027e – 02 * W + 7.7418e – 03 * B + 2.3100e – 01 * 0.02 * SL + 3.4424) * 1.1
minckh	(2.5018e – 03 * W + 4.0217e – 03 * B + 6.0637e – 01 * 0.02 * SL + 1.8118)
minckl	(3.3328e – 03 * W + 5.7062e – 03 * B + 1.6429 + 9.4074e – 07 * W * B)
tacc	(3.0738e – 03 * W + 7.8335e – 03 * B + 1.4519e – 01 * S + 3.0153e – 01 * 0.02 * SL + 2.4784)
	Y = 4
mincyc	(8.0139e – 03 * W + 1.5483e – 02 * B + 2.3100e – 01 * 0.02 * SL + 3.4424) * 1.1
minckh	(1.2509e – 03 * W + 8.0434e – 03 * B + 6.0637e – 01 * 0.02 * SL + 1.8118)
minckl	(1.6664e – 03 * W + 1.1412e – 02 * B + 1.6429 + 9.4073e – 07 * W * B)
tacc	(1.5369e – 03 * W + 1.5667e – 02 * B + 1.4519e – 01 * S + 3.0153e – 01 * 0.02 * SL + 2.4784)
	Y = 8
mincyc	(4.0069e – 03 * W + 3.0967e – 02 * B + 2.3100e – 01 * 0.02 * SL + 3.4424) * 1.1
minckh	(6.1447e – 04 * W + 1.5623e – 02 * B + 6.3323e – 01 * 0.02 * SL + 1.9109)
minckl	(8.3320e – 04 * W + 2.2825e – 02 * B + 1.6429 + 9.4074e – 07 * W * B)
tacc	(7.6846e – 04 * W + 3.1334e – 02 * B + 1.4519e – 01 * S + 3.0153e – 01 * 0.02 * SL + 2.4784)
	Y = 16
mincyc	(2.0034e – 03 * W + 6.1934e – 02 * B + 2.3100e – 01 * 0.02 * SL + 3.4424) * 1.1
minckh	(3.1497e – 04 * W + 3.2373e – 02 * B + 6.2668e – 01 * 0.02 * SL + 2.0565)
minckl	(4.1660e – 04 * W + 4.5650e – 02 * B + 1.6429 + 9.4074e – 07 * W * B)
tacc	(3.8423e – 04 * W + 6.2668e – 02 * B + 1.4519e – 01 * S + 3.0153e – 01 * 0.02 * SL + 2.4784)
	Y = 32
mincyc	(1.0017e – 03 * W + 1.2386e – 01 * B + 2.3100e – 01 * 0.02 * SL + 3.4424) * 1.1
minckh	(1.5092e – 04 * W + 5.2514e – 02 * B + 7.0162e – 01 * 0.02 * SL + 2.4402)
minckl	(2.0830e – 04 * W + 9.1300e – 02 * B + 1.6429 + 9.4073e – 07 * W * B)
tacc	(1.9211e – 04 * W + 1.2533e – 01 * B + 1.4519e – 01 * S + 3.0153e – 01 * 0.02 * SL + 2.4784)

2) Power Characteristics [Unit: μW]

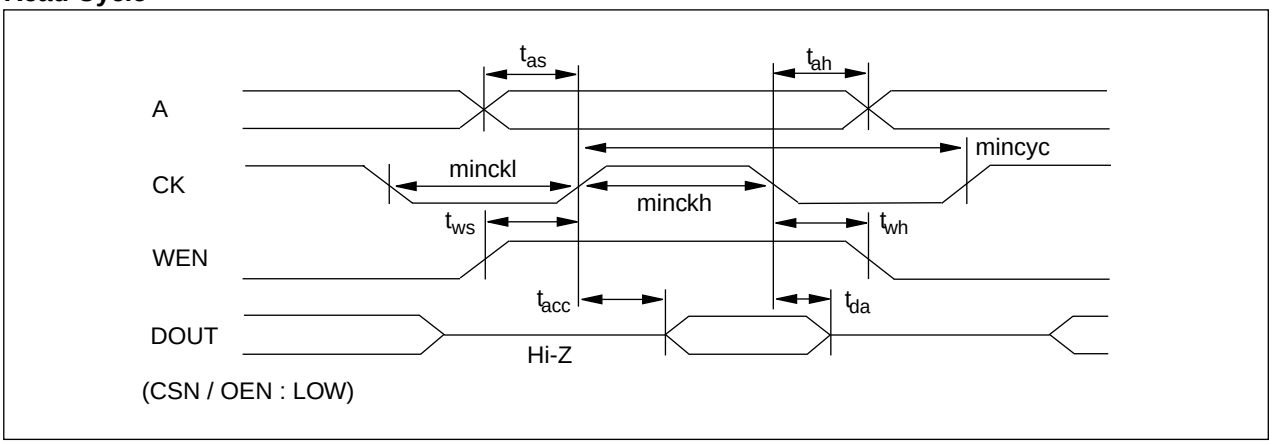
Power Type	Power Equation
	Y = 2
power_ck	(1.9286e – 01 * W + 1.2120 * B + 6.6767 + 1.0122e – 03 * W * B) * VDD^2 * F
power_csn	(1.4833e – 02 * W + 2.7771e – 01 * B + 6.7137e – 01 – 1.3698e – 04 * W * B) * VDD^2 * F
	Y = 4
power_ck	(9.6430e – 02 * W + 2.4241 * B + 6.6767 + 1.0122e – 03 * W * B) * VDD^2 * F
power_csn	(7.4166e – 03 * W + 5.5542e – 01 * B + 6.7137e – 01 – 1.3698e – 04 * W * B) * VDD^2 * F
	Y = 8
power_ck	(4.5015e – 02 * W + 4.0033 * B + 6.9783 + 2.2423e – 03 * W * B) * VDD^2 * F
power_csn	(3.7083e – 03 * W + 1.1108 * B + 6.7137e – 01 – 1.3698e – 04 * W * B) * VDD^2 * F
	Y = 16
power_ck	(2.1634e – 02 * W + 6.4680 * B + 7.4439 + 2.6999e – 03 * W * B) * VDD^2 * F
power_csn	(1.8541e – 03 * W + 2.2216 * B + 6.7137e – 01 – 1.3698e – 04 * W * B) * VDD^2 * F
	Y = 32
power_ck	(1.0383e – 02 * W + 1.0897e + 01 * B + 9.5049 + 2.6458e – 03 * W * B) * VDD^2 * F
power_csn	(9.2708e – 04 * W + 4.4433 * B + 6.7137e – 01 – 1.3698e – 04 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

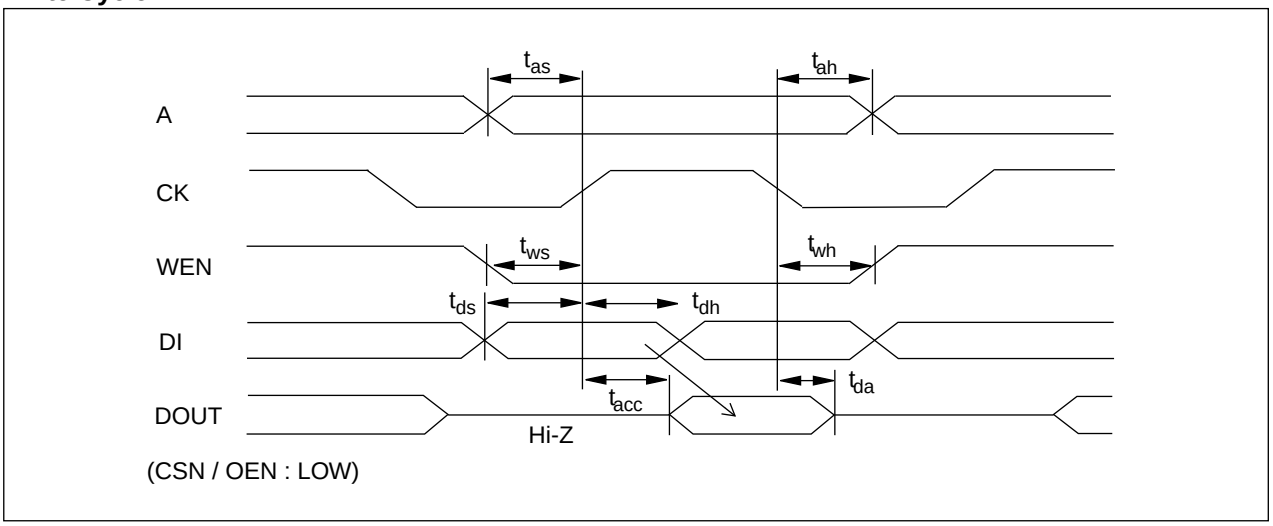
Width = 16.6 * ($\lceil \log_2 (W / Y) \rceil$) + 12.1 * B * Y + 121.7 [μm]
Height = 404.95 + 10.85 * W / Y + M [μm]
M = 8.15 (if Y = 2, 8), M = 10.55 (if Y = 4, 16), M = 12.95 (if Y = 32)

Timing Diagrams

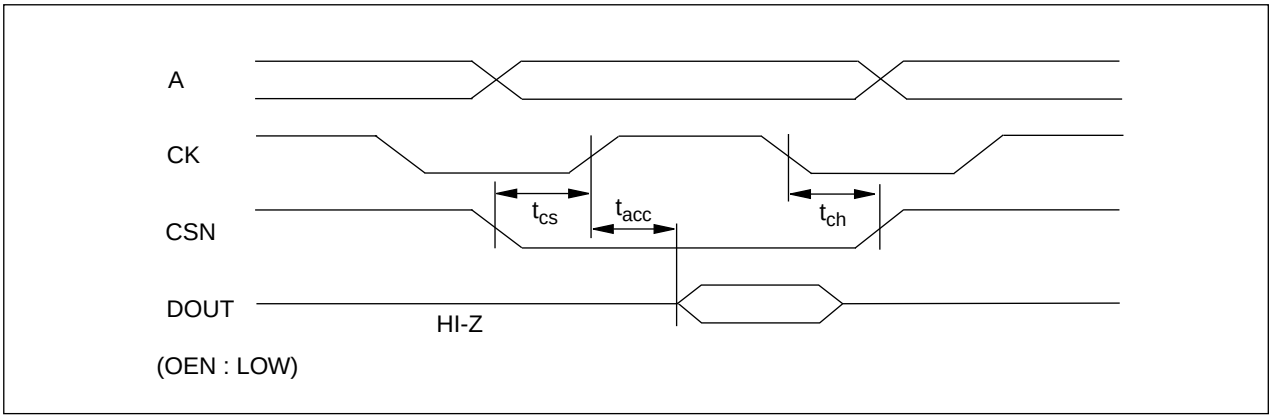
Read Cycle



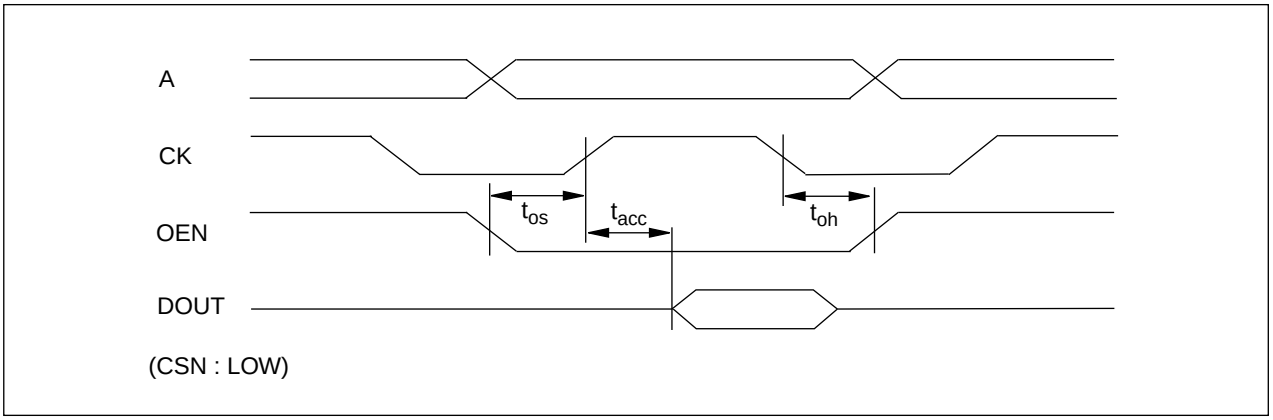
Write Cycle



CSN Control

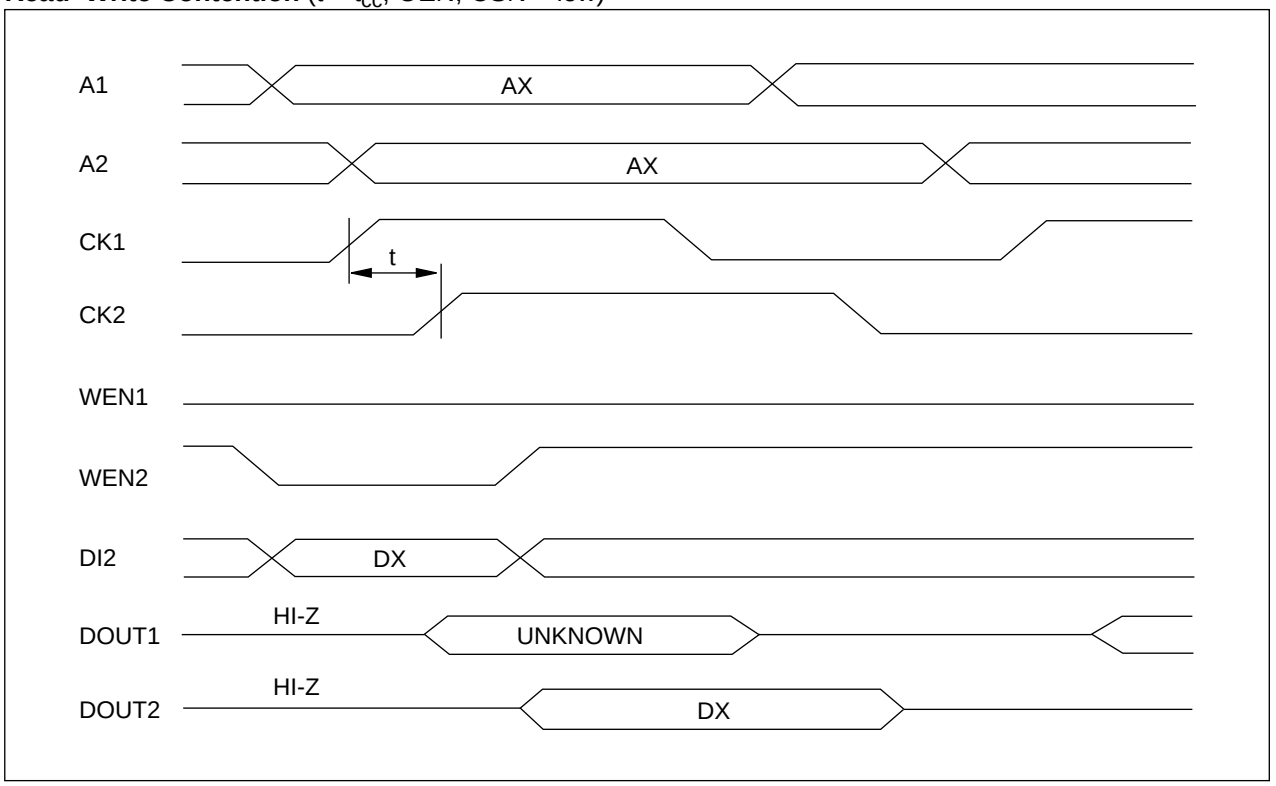


OEN Control

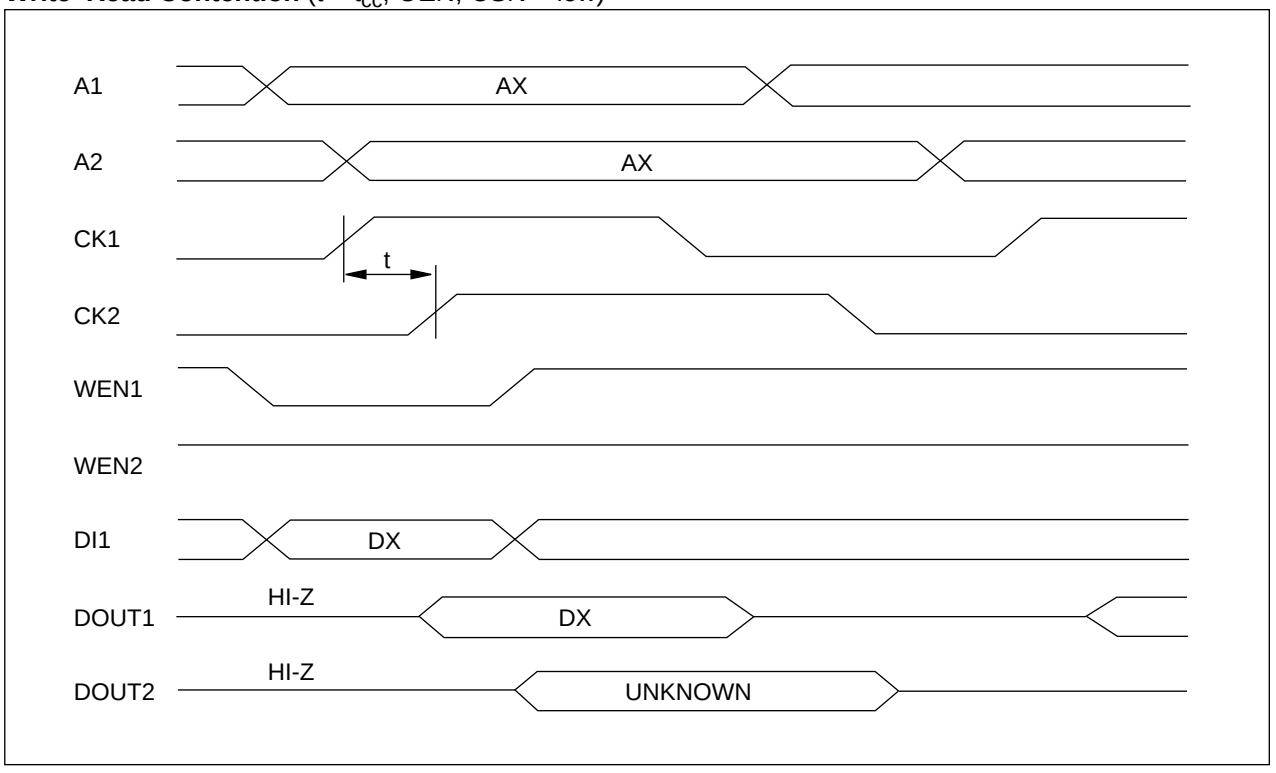


Function Diagrams

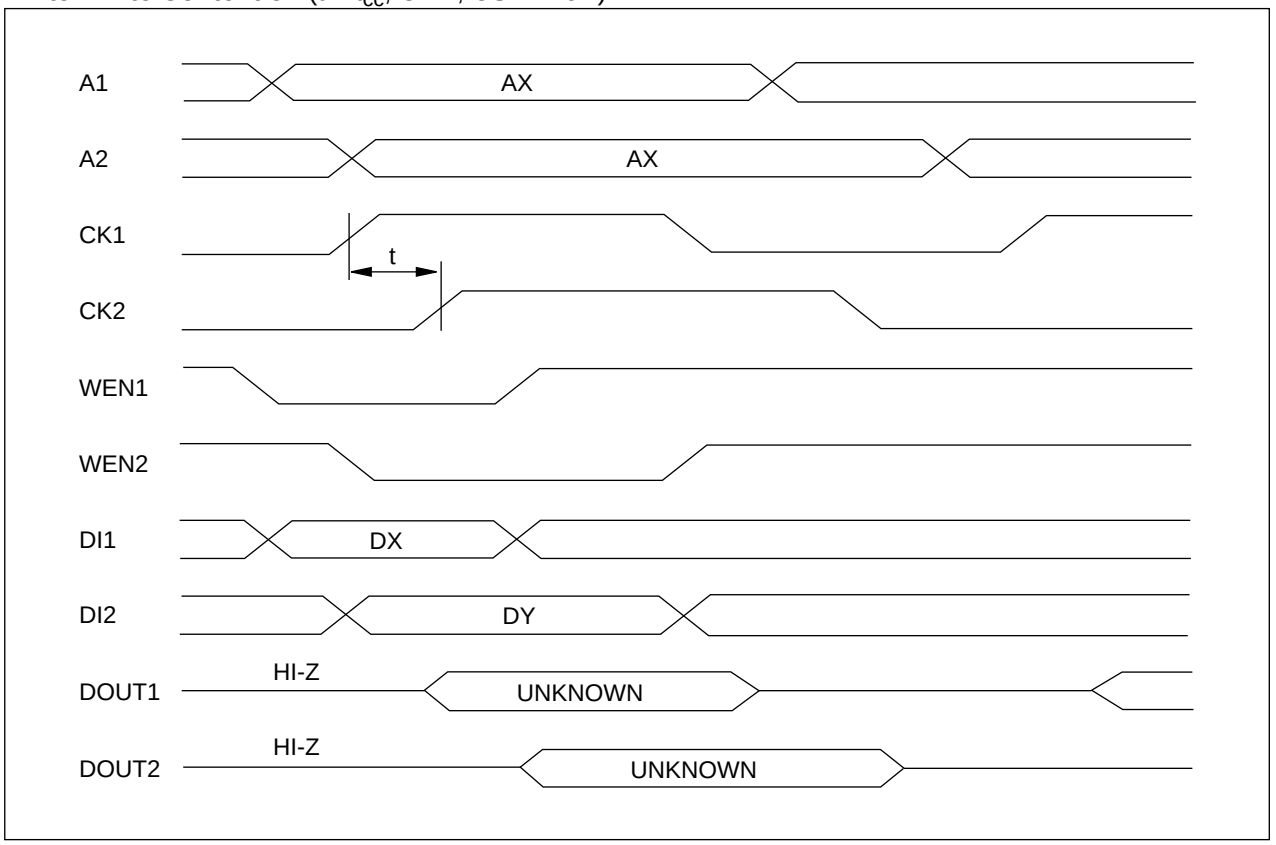
Read–Write Contention ($t < t_{cc}$; OEN, CSN = low)



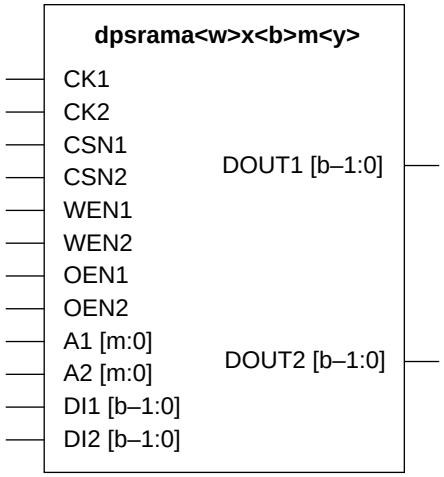
Write–Read Contention ($t < t_{cc}$; OEN, CSN = low)



Write–Write Contention (t < t_{cc}; OEN, CSN = low)



Logic Symbol



NOTES:

1. Words (w) is the number of words in DPSRAMA.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Write completed at falling edge of clock
- Possible read modified write cycle
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Possible bi-directional operation
- Flexible aspect ratio
- Up to 64K bits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

DPSRAMA is a dual-port synchronous static RAM. When WEN1 is high and CK1 rises, DOUT1 [ ] presents data stored in the location addressed by A1 [ ]. When WEN1 is low and CK1 falls, or when CK1 is high and WEN1 rises, the value of DI1 [ ] is written into the location addressed by A1 [ ]. CSN1 is used to enable/disable CK1. OEN1 is used to enable/disable tri-state drivers of DOUT1 [ ]. The functionality of port2 is the same to port1. The port1 and port2 function independently each other.
DPSRAMA is an alternative of DPSRAM. The major difference of these two RAMs is the timing of read and write. DPSRAMA reads and writes at different edge of the clock since DPSRAM reads and writes at the same edge of the clock.

Generators and Cell Configurations

DPSRAMA Gen. generates layout, netlist, symbol and functional & timing model of DPSRAMA. The layout of DPSRAMA is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of DPSRAMA, you can give certain values to following three generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y).

The valid range of these parameters is specified in the following table:

Parameters		YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	Min	4	8	16	32	64
	Max	512	1024	2048	4096	8192
	Step	2	4	8	16	32
Bpw (b)	Min	1	1	1	1	1
	Max	128	64	32	16	8
	Step	1	1	1	1	1

Pin Descriptions

Name	I/O	Description
CK1 CK2	I	“Clock”s serve as input clocks to each port of the memory block. When CK1 (CK2) is low, port1 (port2) is in a precharge state. Upon the rising edge, a read cycle begins. Upon the falling edge, a write cycle ends.
CSN1 CSN2	I	“Chip Select Negative”s act as each port’s enable signal for selections of multiple blocks on a common clock. When CSN1 (CSN2) is high, port1 (port2) goes to stand-by (power down) mode and no access can occur, conversely, if low only then may a read or write access occur. CSN1 (CSN2) may not change during CK1 (CK2) is high.
WEN1 WEN2	I	“Write Enable Negative”s select the type of memory access. Read is the high state, and write is the low state.
OEN1 OEN2	I	“Output Enable Negative”s control the output drivers from driven to tri-state condition. OEN1 (OEN2) may not change during CK1 (CK2) is high.
A1 [ ] A2 [ ]	I	“Address”es select the location to be accessed. A1 [ ] (A2 [ ]) may not change during CK1 (CK2) is high.
DI1 [ ] DI2 [ ]	I	When CK1 (CK2) falls while WEN1 (WEN2) is low, or when WEN1 (WEN2) rises while CK1 (CK2) is high, the “Data In” word value is written to the accessed location.
DOUT1 [ ] DOUT2 [ ]	O	During a read access, data word stored will be presented to the “Data Out” ports. DOUT1 [ ] and DOUT2 [ ] are tri-statable. When CK1 (CK2) is high, CSN1 (CSN2) is low and OEN1 (OEN2) is low, only then, DOUT1 [ ] (DOUT2 [ ]) drives a certain value. Otherwise, DOUT1 [ ] (DOUT2 [ ]) keeps Hi-Z state. During a write access, the value of DOUT1 [ ] (DOUT2 [ ]) is unpredictable.

Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	A	DI	DOUT				
						Ymux 2	Ymux 4	Ymux 8	Ymux 16	Ymux 32
5.8	1.9	0.9	2.3	1.0	2.0	5.4	5.4	12.0	25.0	51.0

Application Notes

1) Putting Busholders on DOUT1 [ ] and DOUT2 [ ]

As you will see in the timing diagrams, DOUT1 [ ] (DOUT2 [ ]) is valid only when CK1 (CK2) is high. If you want DOUT1 [ ] (DOUT2 [ ]) to be stable regardless of CK1 (CK2) state, you should put STDL80 Busholder cells on the DOUT1 [ ] (DOUT2 [ ]) bus externally.

2) Customizing Aspect Ratio

Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 5 selections of Ymux for the same Words and the same Bpw DPSRAMA. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of DPSRAM, In general, larger Ymux DPSRAMA has faster speed and bigger area than smaller Ymux DPSRAMA.

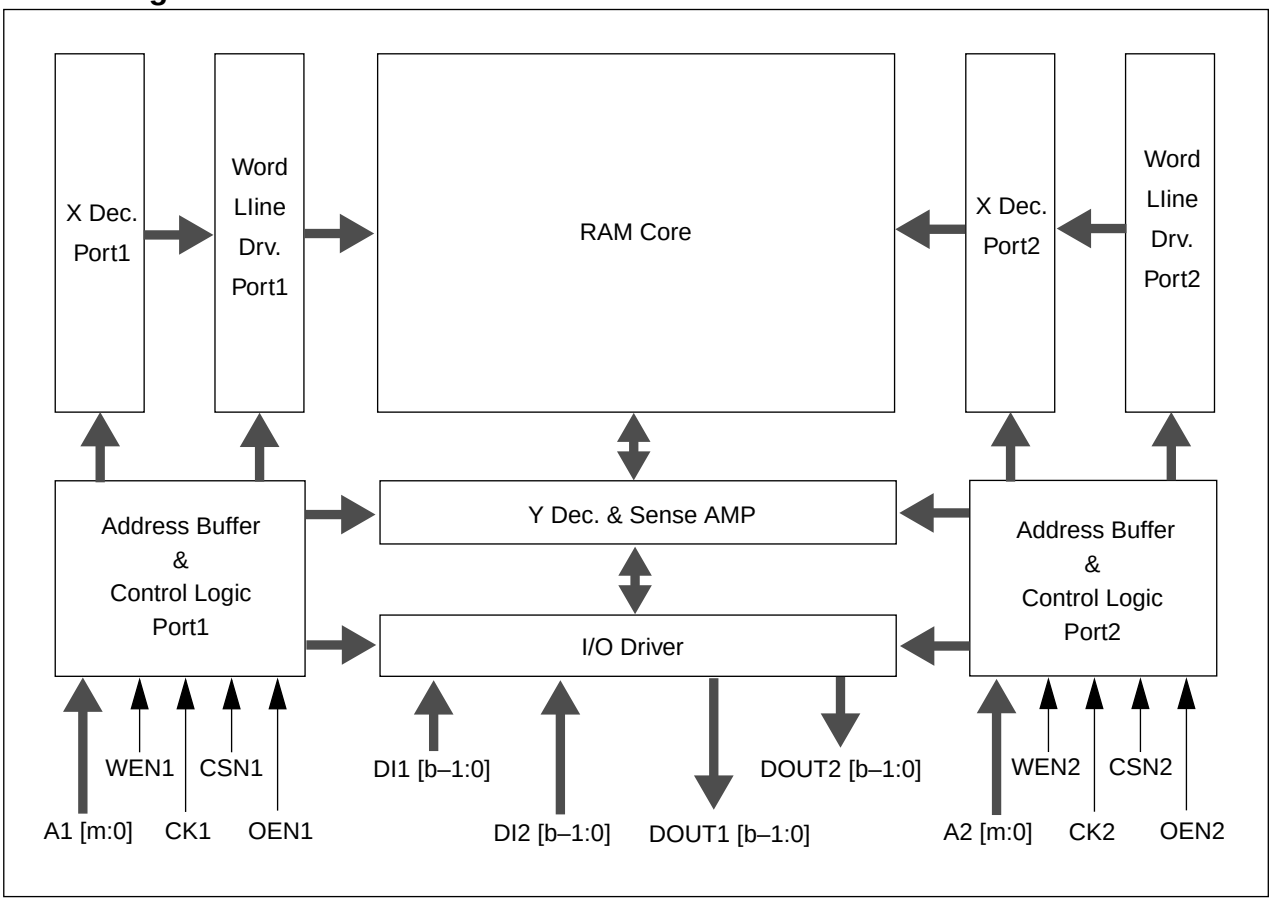
3) Contention Modes

Simultaneous accesses to the same location through both ports cause a contention. DPSRAMA has no contention preventing scheme. You have to take care of the contention modes. Please refer to the timing diagrams of contention modes to get more information of contention modes.

4) Using Bi-Directional Data Port

Because having the same phase, DI1 [ ] (DI2 [ ]) and DOUT1 [ ] (DOUT2 [ ]) of DPSRAMA can be tied directly. With tying them up together and controlling WEN1 (WEN2) and OEN1 (OEN2) properly, you can use them as bi-directional data ports.

Block Diagram



Characteristic Reference Table

Symbol	Description	256x16m4	1024x16m8	4Kx16m16
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{o}C, Output load = 10SL, Unit = ns)				
t_{rp}	Minimum Read Pulse Width	3.75	4.50	5.62
t_{pc}	Minimum Pre-Charge Period	5.12	6.06	12.50
t_{wp}	Minimum Write Pulse Width	1.63	2.35	4.48
t_{rwc}	Read-Write Contention	1.28	1.84	2.97
t_{wrc}	Write-Read Contention	0	0	0
t_{wwc}	Write-Write Contention	1.18	1.98	3.58
t_{as}	Address Setup Time	0.40	0.75	1.45
t_{ah}	Address Hold Time	1.20	2,05	3.75
t_{cs}	CSN Setup Time	0.70	0.70	0.70
t_{ch}	CSN Hold Time	0	0	0
t_{ds}	Data Input Setup Time	1.10	1.64	2.77
t_{dh}	Data Input Hold Time	1.30	1.58	2.21
t_{os}	OEN Setup Time	0	0	0
t_{oh}	OEN Hold Time	1.08	1.18	1.37
t_{wh}	WEN Hold Time	0.27	0.21	0.10
t_{acc}	Access Time	4.00	4.80	6.10
t_{da}	Deaccess Time	1.80	1.90	2.20
SIZE (µm)				
Width		996	1787	3353
Height		1110	1802	3194
POWER (µW/MHz)				
power_ck (normal mode: CSN Low)		1001	2249	6004
power_csn (stand-by mode: CSN High)		116	221	439

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
Y: Ymux Type
S: Input Slope (Unit: ns)
VDD: Operating Voltage (Unit: V)
B: Bits per Word
SL: Number of Fanouts (Unit: Standard Load)
F: Operating Frequency (Unit: MHz)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
tpc	1.59e – 02 * W – 4.37e – 03 * B – 4.90e – 01 * S + 2.2354 + 1.90e – 05 * W * B + 5.20e – 04 * W * S + 1.08e – 02 * B * S
trp	3.21e – 03 * W + 4.70e – 03 * B – 2.05e – 01 * S + 8.19e – 01 * 0.02 * SL + 2.5261
tacc	3.29e – 03 * W + 8.45e – 03 * B + 1.00e – 01 * S + 3.44e – 01 * 0.02 * SL + 2.3147
	Y = 4
tpc	7.99e – 03 * W – 8.74e – 03 * B – 4.90e – 01 * S + 2.2354 + 1.90e – 05 * W * B + 2.60e – 04 * W * S + 2.16e – 02 * B * S
trp	1.60e – 03 * W + 9.41e – 03 * B – 2.05e – 01 * S + 8.19e – 01 * 0.02 * SL + 2.5261
tacc	1.64e – 03 * W + 1.69e – 02 * B + 1.00e – 01 * S + 3.44e – 01 * 0.02 * SL + 2.3147
	Y = 8
tpc	3.99e – 03 * W – 1.74e – 02 * B – 4.90e – 01 * S + 2.2354 + 1.90e – 05 * W * B + 1.30e – 04 * W * S + 4.33e – 02 * B * S
trp	8.03e – 04 * W + 1.88e – 02 * B – 2.05e – 01 * S + 8.19e – 01 * 0.02 * SL + 2.5261
tacc	8.24e – 04 * W + 3.38e – 02 * B + 1.00e – 01 * S + 3.44e – 01 * 0.02 * SL + 2.3147
	Y = 16
tpc	1.99e – 03 * W – 3.49e – 02 * B – 4.90e – 01 * S + 2.2354 + 1.90e – 05 * W * B + 6.50e – 05 * W * S + 8.66e – 02 * B * S
trp	4.01e – 04 * W + 3.76e – 02 * B – 2.05e – 01 * S + 8.19e – 01 * 0.02 * SL + 2.5261
tacc	4.12e – 04 * W + 6.76e – 02 * B + 1.00e – 01 * S + 3.44e – 01 * 0.02 * SL + 2.3147
	Y = 32
tpc	9.99e – 04 * W – 6.99e – 02 * B – 4.90e – 01 * S + 2.2354 + 1.90e – 05 * W * B + 3.25e – 05 * W * S + 1.73e – 01 * B * S
trp	2.00e – 04 * W + 7.53e – 02 * B – 2.05e – 01 * S + 8.19e – 01 * 0.02 * SL + 2.5261
tacc	2.06e – 04 * W + 1.35e – 01 * B + 1.00e – 01 * S + 3.44e – 01 * 0.02 * SL + 2.3147

2) Power Characteristics [Unit: μW]

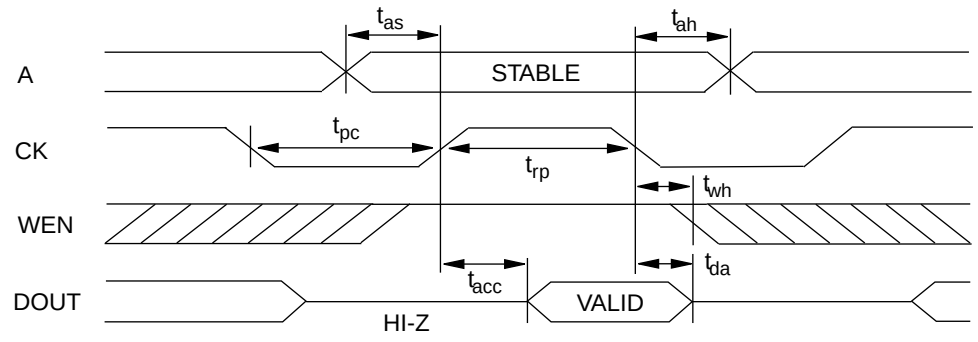
Power Type	Power Equation
	Y = 2
power_ck	(1.5772e – 01 * W + 1.1458 * B + 1.5858e + 01 + 4.7004e – 03 * W * B) * VDD^2 * F
power_csn	(9.2587e – 03 * W + 2.5036e – 01 * B + 1.3734 + 3.4497e – 05 * W * B) * VDD^2 * F
	Y = 4
power_ck	(7.8864e – 02 * W + 2.2916 * B + 1.5858e + 01 + 4.7004e – 03 * W * B) * VDD^2 * F
power_csn	(4.6293e – 03 * W + 5.0073e – 01 * B + 1.3734 + 3.4497e – 05 * W * B) * VDD^2 * F
	Y = 8
power_ck	(3.9432e – 02 * W + 4.5833 * B + 1.5858e + 01 + 4.7004e – 03 * W * B) * VDD^2 * F
power_csn	(2.3146e – 03 * W + 1.0014 * B + 1.3734 + 3.4497e – 05 * W * B) * VDD^2 * F
	Y = 16
power_ck	(1.9716e – 02 * W + 9.1667 * B + 1.5858e + 01 + 4.7004e – 03 * W * B) * VDD^2 * F
power_csn	(1.1573e – 03 * W + 2.0029 * B + 1.3734 + 3.4497e – 05 * W * B) * VDD^2 * F
	Y = 32
power_ck	(9.8581e – 03 * W + 1.8333e + 01 * B + 1.5858e + 01 + 4.7004e – 03 * W * B) * VDD^2 * F
power_csn	(5.7867e – 04 * W + 4.0058 * B + 1.3734 + 3.4497e – 05 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 16.6 * ($\lceil \log_2 (W / Y) \rceil$) + 12.1 * B * Y + 121.7 [μm]
Height = 404.95 + 10.85 * W / Y + M [μm]
M = 8.15 (if Y = 2, 8), M = 10.55 (if Y = 4, 16), M = 12.95 (if Y = 32)

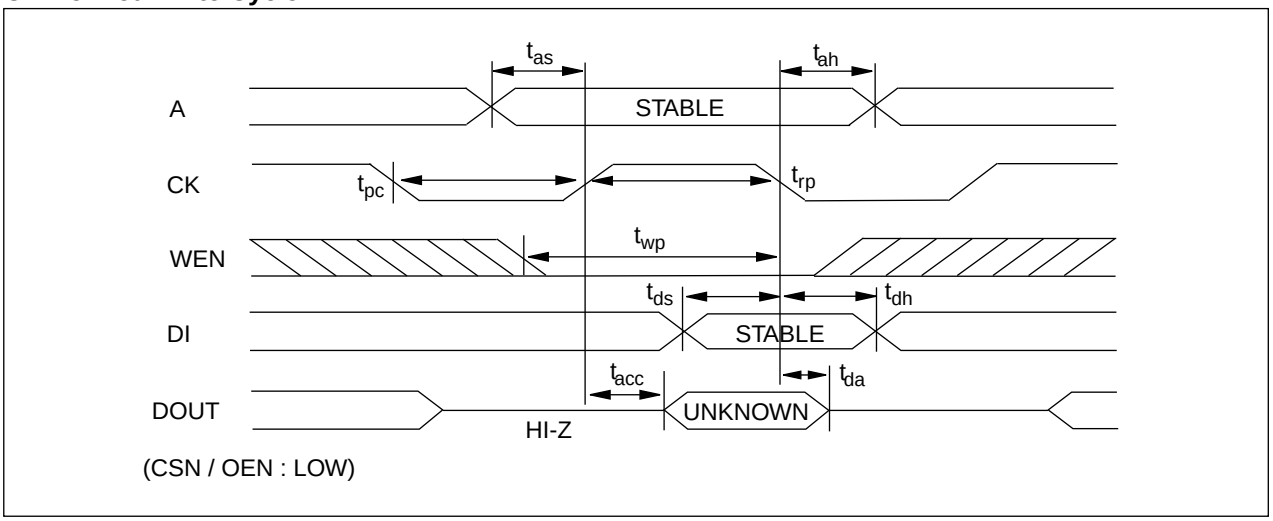
Timing Diagrams

Read Cycle

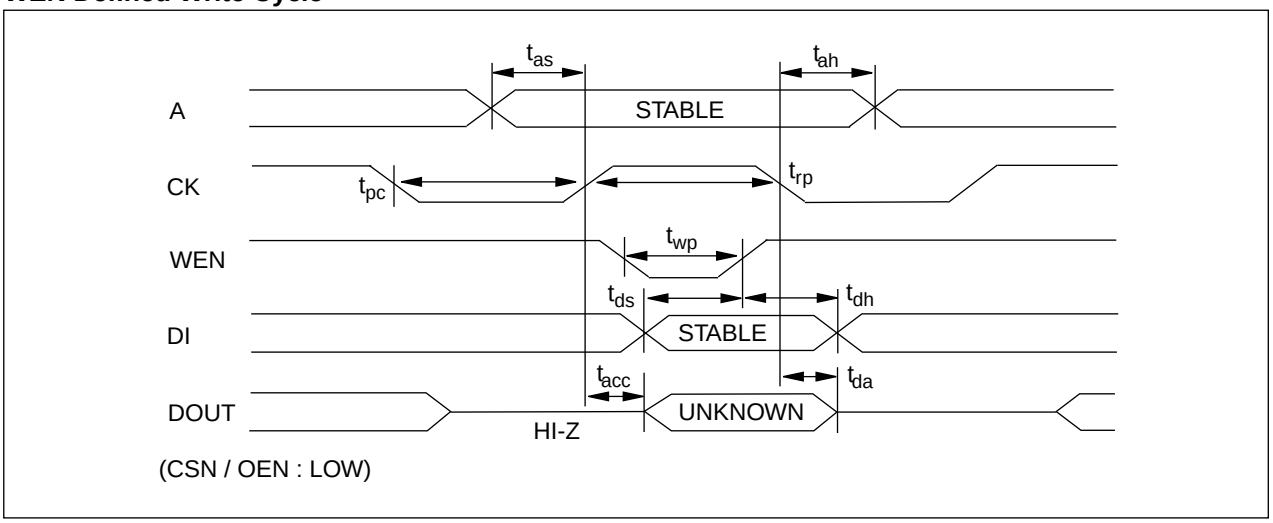


(CSN / OEN : LOW, DI :DON'T CARE)

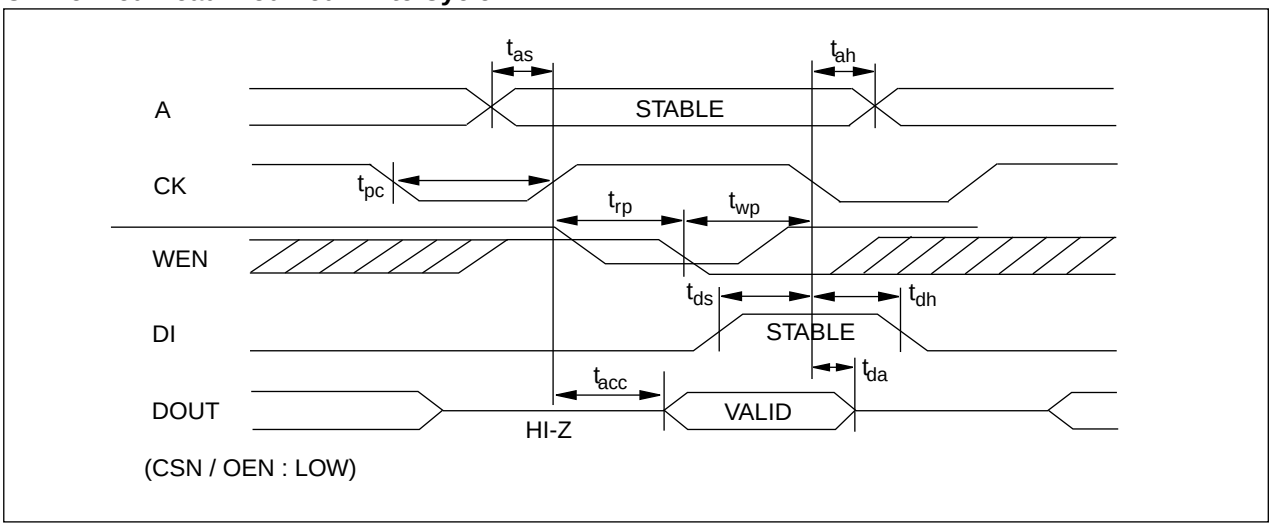
CK Defined Write Cycle



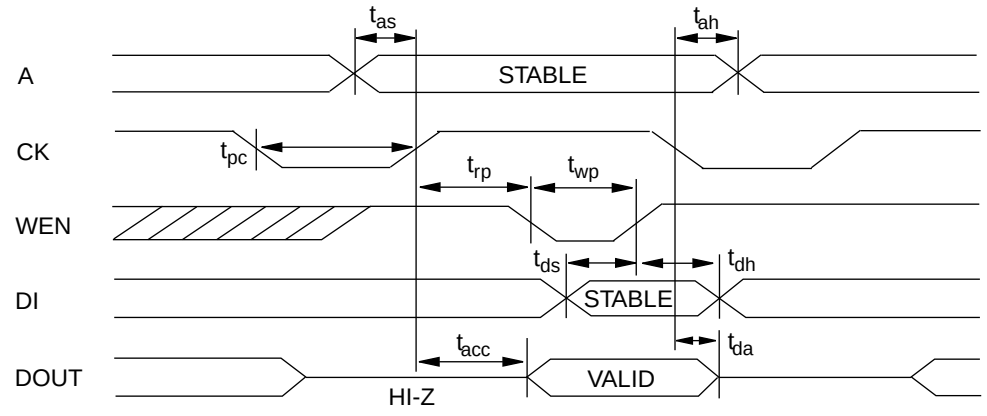
WEN Defined Write Cycle



CK Defined Read-Modified-Write Cycle

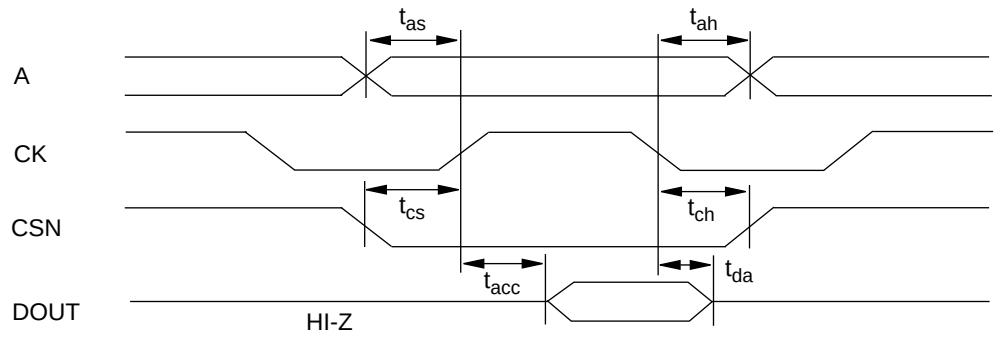


WEN Defined Read-Modified-Write Cycle



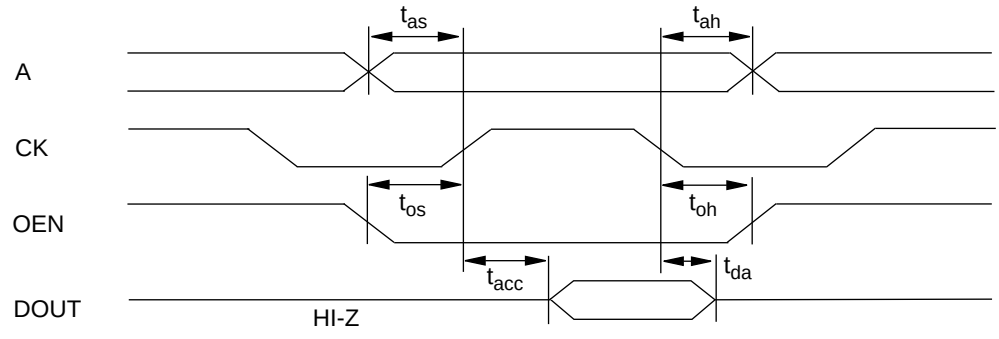
(CSN / OEN : LOW)

CSN Control



(OEN : LOW, WEN / DI : DON'T CARE)

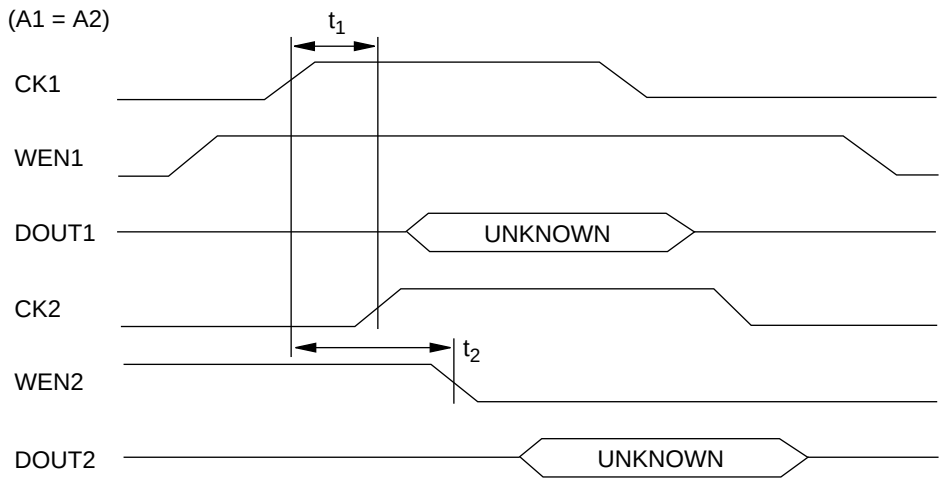
OEN Control



(CSN : LOW, WEN / DI : DON'T CARE)

Function Diagrams

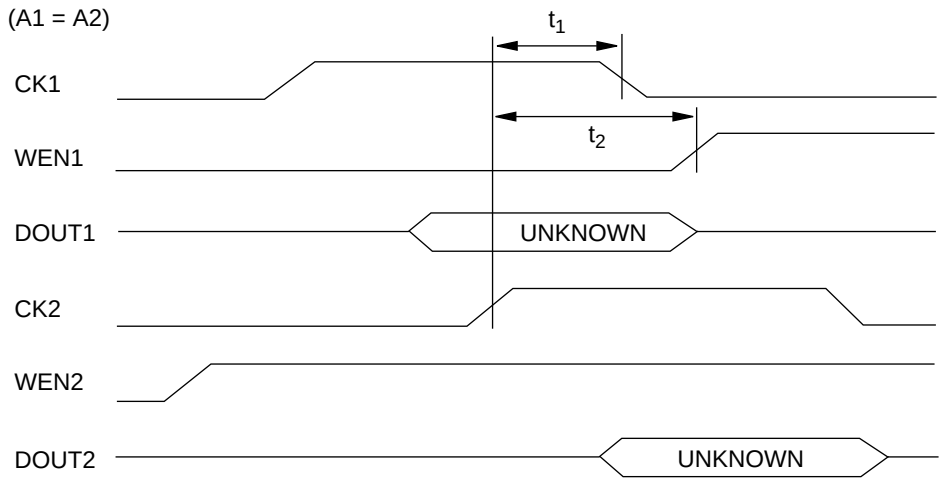
Read–Write Contention (max (t_1, t_2) ≤ t_{rwc})



(CSN1 / CSN2 / OEN1 / OEN2 : LOW, DI1 : DON'T CARE, DI2 : VALID)

* If the greater of t_1 or t_2 is smaller than or equal to t_{rwc}, it is Read-Write Contention.
The read by port1 is invalid, the write by port2 is still valid.

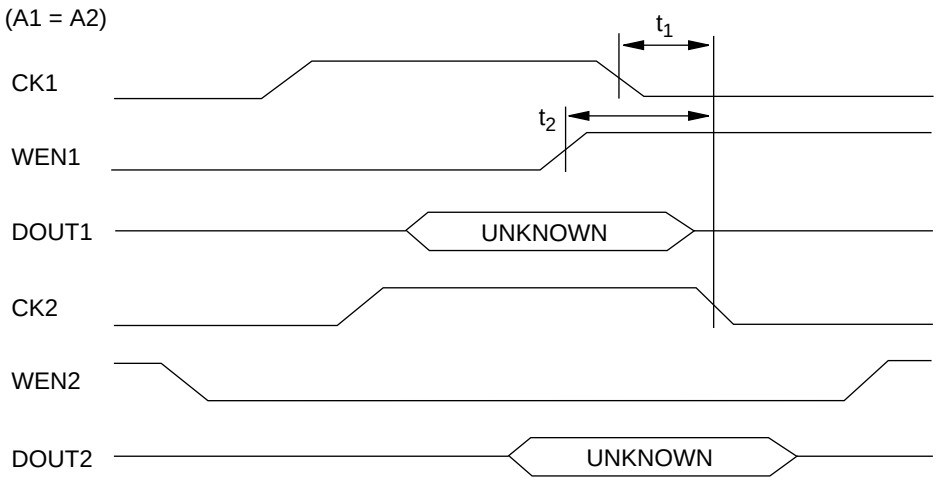
Write–Read Contention (min (t_1, t_2) ≥ t_{wrc})



(CSN1 / CSN2 / OEN1 / OEN2 : LOW, DI1 : VALID, DI2 : DON'T CARE)

* If the smaller of t_1 or t_2 is greater than or equal to t_{wrc}, it is Write-Read Contention.
The read by port2 is invalid, the write by port1 is still valid.

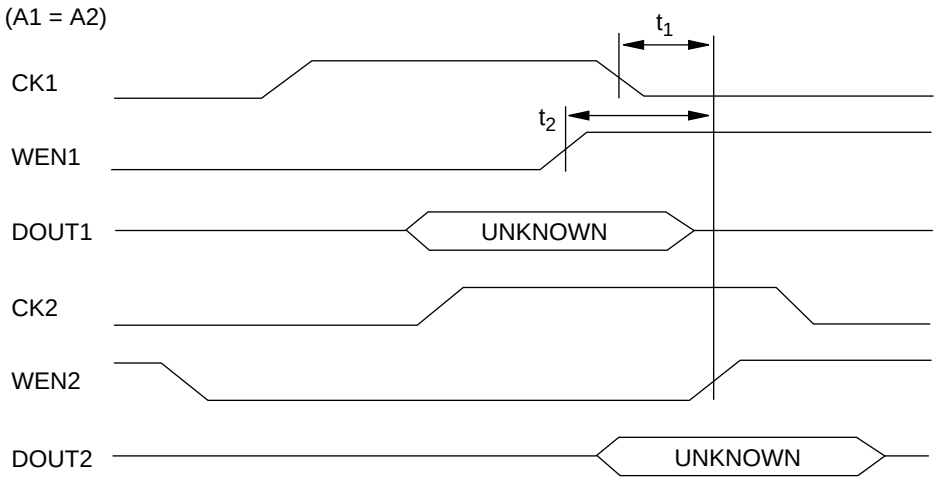
Write–Write Contention (max (t_1, t_2) ≤ t_{wwc} at CK Defined Write Cycle)



(CSN1 / CSN2 / OEN1 / OEN2 : LOW, DI1 / DI2 : VALID)

* If the greater of t_1 or t_2 is smaller than or equal to t_{wwc}, it is Write-Write Contention. Data stored at current address will be unpredictable.

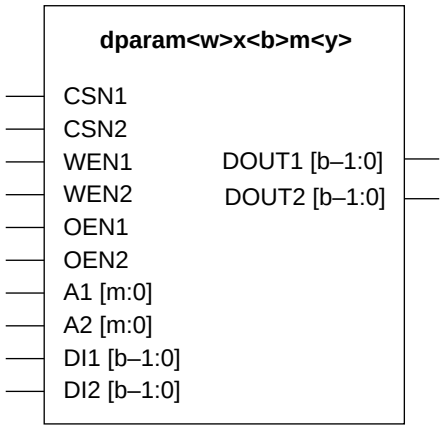
Write–Write Contention (max (t_1, t_2) ≤ t_{wwc} at WEN Defined Write Cycle)



(CSN1 / CSN2 / OEN1 / OEN2 : LOW, DI1 / DI2 : VALID)

* If the greater of t_1 or t_2 is smaller than or equal to t_{wwc}, it is Write-Write Contention. Data stored at current address will be unpredictable.

Logic Symbol



NOTES:

1. Words (w) is the number of words in DPARAM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. $m = \lceil \log_2 w \rceil - 1$

Features

- Asynchronous operation
- Address transition detectors
- Write enable transition detector
- Chip select transition detector
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Flexible aspect ratio
- Up to 64K bits capacity
- Up to 8K number of words
- Up to 64 number of bits per word

Function Description

DPARAM is a dual port asynchronous static RAM. When WEN1 is high, just after the address(A1[ ]) transition, DOUT1[ ] presents the data stored in the location addressed by A1[ ]. Upon WEN1 rising edge, the value of DI1[ ] is written into the location addressed by A1[ ]. CSN1 is used to enable/disable the accesses. OEN1 is used to enable/disable the data output driver. Port2 has the same functionalities as those of port1, and two functionalities are independent of each other.

Generators and Cell Configurations

DPARAM generates layout, netlist, symbol and functional & timing model of DPARAM. The layout of DPARAM is an automatically generated array of custom, pitch-matched leaf cells. There are three generator parameters to resolve the configuration of a DPARAM.

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y).

The valid range of these parameters is specified in the following table:

Parameters		YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	Min	16	32	64	128
	Max	1024	2048	4096	8192
	Step	8	16	32	64
Bpw (b)	Min	1	1	1	1
	Max	64	32	16	8
	Step	1	1	1	1

DPARAM Gen

Dual-Port Asynchronous RAM Generator

Pin Descriptions

Name	I/O	Description
CSN	I	"Chip Select Negative" acts as the memory enable signal for selecting one of multiple memory blocks. When CSN is high, DOUT[] goes to Hi-Z state, the memory goes to stand-by (power down) mode and no access to the memory can occur. Conversely, if CSN is low only then may a read or write access occur. When CSN falls, a read access is initiated. CSN should be table when WEN is low.
WEN1	I	"Write Enable Negative" selects the type of memory access. When WEN is high, the SPARAM is in read mode. Otherwise, it is in write mode. Upon the rising edge of WEN, a write access completed and a read access initiated. When WEN is low, A[] and CSN should be stable.
OEN1	I	"Output Enable Negative" unconditionally enables or disables the output drivers.
A [ ]	I	"Address" selects the location to be accessed. When A[] changes, the transition is detected and the internal clock pulse will be generated. A[] should be stable when WEN is low.
D [ ]	I	When WEN rises, the "Data In" word value is written to the location addressed.
DOUT [ ]	O	During a read access, the data word stored will be presented to the "Data OUT" ports. DOUT[] is tri-statable. When CSN is low and OEN is low, only then, DOUT[] drives a certain value. Otherwise, DOUT[] keeps Hi-Z state. During a write access, the data on DOUT is unpredictable.

Pin Capacitance

(Unit = SL)

CSN	WEN	OEN	A	DI	DOUT			
					Ymux 4	Ymux 8	Ymux 16	Ymux 32
13.80	6.0	1.1	6.0	2.9	7.7	16.9	35.1	71.6

Application Notes

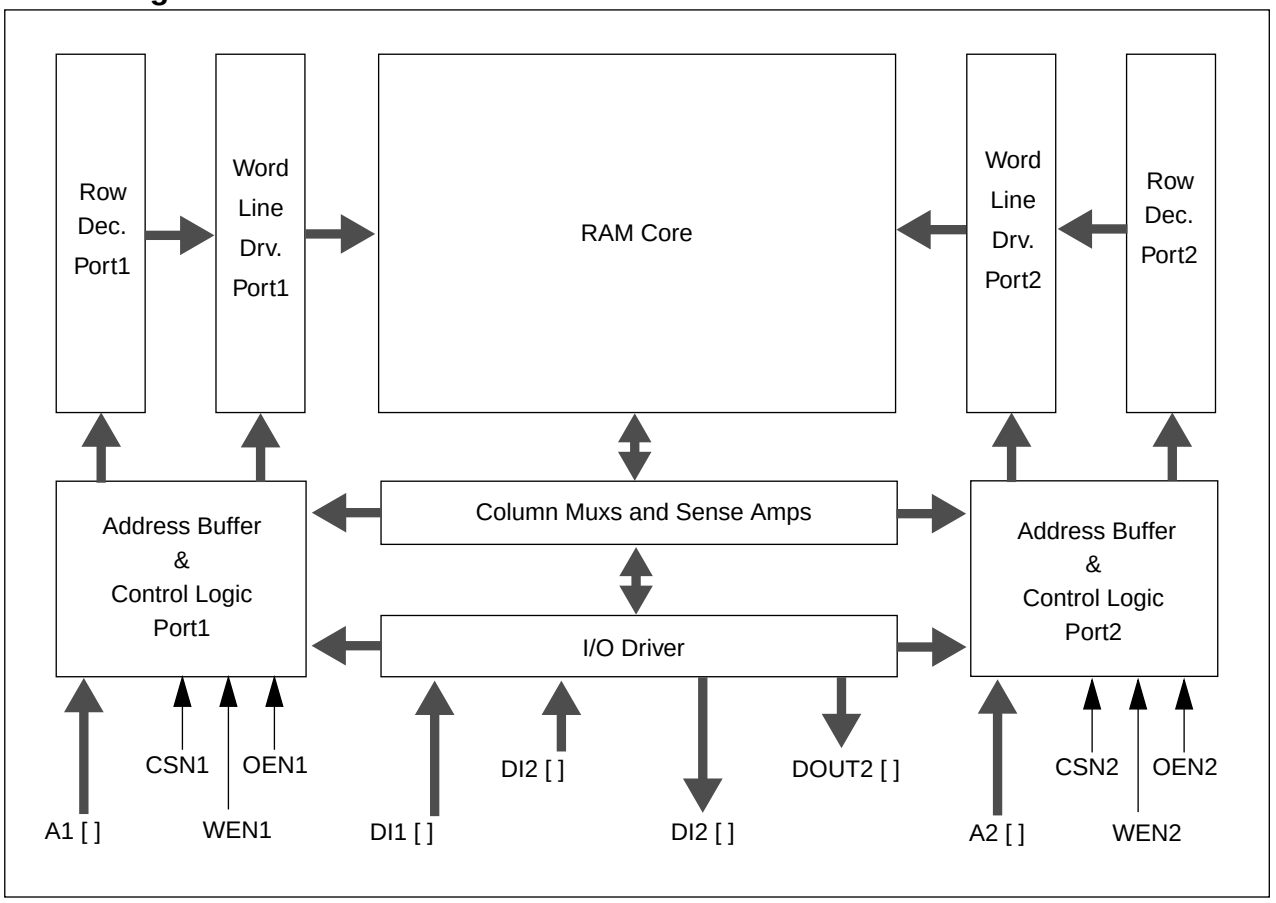
1) Fitting the Layout Shape(Aspect Ratio)

Layout Shape can be fitted by choosing one of 4 Ymux parameters in the above configuration table in accordance with your chip level layout design preference. Larger one makes the layout shape flat and short. Smaller one makes it thin and tall. In general, flat and short DPARAM is faster than thin and tall one.

2) Contention Modes

Simultaneous accesses to the same location through both ports cause a contention. DPARAM has no contention-preventing scheme. User has to take care of the contention modes. Please refer to the timing diagrams of contention modes to get more information of contention modes.

Block Diagram



Characteristic Reference Table

Symbol	Description	256x16m4	1024x16m8	4Kx16m16
TIMING (Typical process, 3.3V, 25 ^{o}C, Output load = 10SL, Input slope = 0.2ns Unit = ns)				
t_{acc}	Access Time	6.7	7.1	8.0
t_{da}	Deaccess Time	5.1	5.2	5.2
t_{dz}	Active to Hi-z	0.9	0.9	0.9
t_{zd}	Hi-z to Active	1.9	1.9	1.9
t_{as}	Address Setup Time	0.1	0.1	0.1
t_{ah}	Address Hold Time	1.2	1.5	2.1
t_{ds}	Input Data Setup Time	1.1	1.3	2.0
t_{dh}	Input Data Hold Time	0.9	1.1	1.6
t_{wen}	Minimum WEN Pulse Width Low	3.5	3.8	4.3
t_{cs}	CSN Setup Time	0.1	0.1	0.1
t_{ch}	CSN Hold Time	1.6	1.6	1.5
t_{rwc}	Read-Write Contention Time	6.7	7.1	8.0
t_{wwc}	Write-Write Contention Time	3.5	3.8	4.3
SIZE (μm)				
Width		1239	2013	3562
Height		1075	1770	3158
POWER (μW/MHz)				
power_add (normal mode: CSN Low)		1564	2485	4541
power_csn (stand-by mode: CSN High)		241	426	802

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words	B: Bits per Word
Y: Ymux Type	BA: Number of Banks (1 or 2)
S: Input Slope (Unit: ns)	SL: Number of Fanouts (Unit: Standard Load)
VDD: Operating Voltage (Unit: V)	F: Operating Frequency (Unit: MHz)

Condition: Typical process, 3.3V, 25 ^{o}C

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 4
tacc	(1.63e-03*W+8.71e-02*S+1.51e-01*SL*0.020+6.17)
twen	(1.23e-03*W+4.76e-01*S+2.99-2.70e-04*W*S)
	Y = 8
tacc	(8.23e-04*W+5.76e-02*S+1.47e-01*SL*0.020+6.21)
twen	(6.15e-04*W+4.76e-01*S+2.99-1.35e-04*W*S)
	Y = 16
tacc	(4.10e-04*W+6.66e-02*S+1.38e-01*SL*0.020+6.28)
twen	(3.07e-04*W+4.76e-01*S+2.99-6.76e-05*W*S)
	Y = 32
tacc	(2.04e-04*W+7.30e-02*S+1.29e-01*SL*0.020+6.38)
twen	(1.53e-04*W+4.76e-01*S+2.99-3.38e-05*W*S)

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 4
power_add	((0.322*W+18.4*B+97.2)/3.3)*VDD^2*F
power_csn	((0.114*W+1.7*B+16.3)/3.3)*VDD^2*F
	Y = 8
power_add	((0.164*W+29.2*B+119)/3.3)*VDD^2*F
power_csn	((0.0572*W+3.41*B+16.3)/3.3)*VDD^2*F
	Y = 16
power_add	((0.068*W+59.9*B+139)/3.3)*VDD^2*F
power_csn	((0.0286*W+6.83*B+16.3)/3.3)*VDD^2*F
	Y = 32
power_add	((0.038*W+120*B+145)/3.3)*VDD^2*F
power_csn	((0.0143*W+13.6*B+16.3)/3.3)*VDD^2*F

NOTES:

1. power_add : This is a normal mode power of memory. When CSN is low.
2. power_csn : This is a standby mode power of memory. When CSN is high.

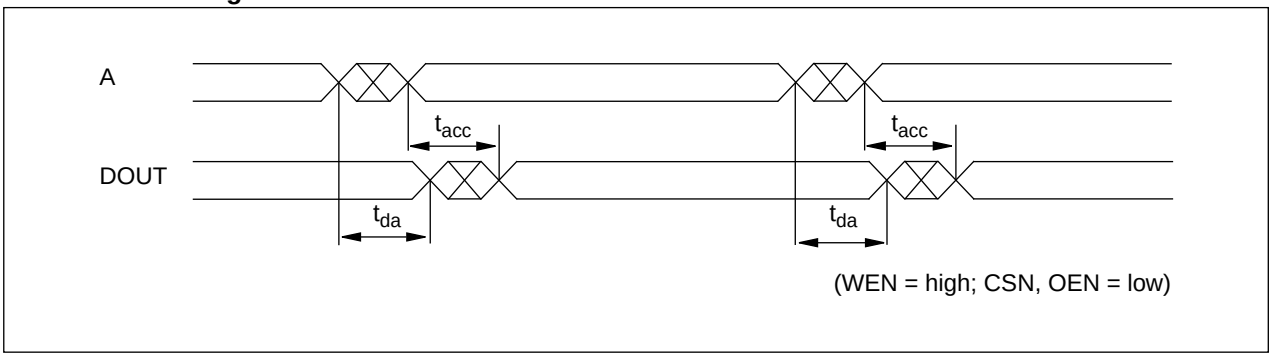
3) Size Equation [Unit: μm]

Width 12.1*B*Y+464.6

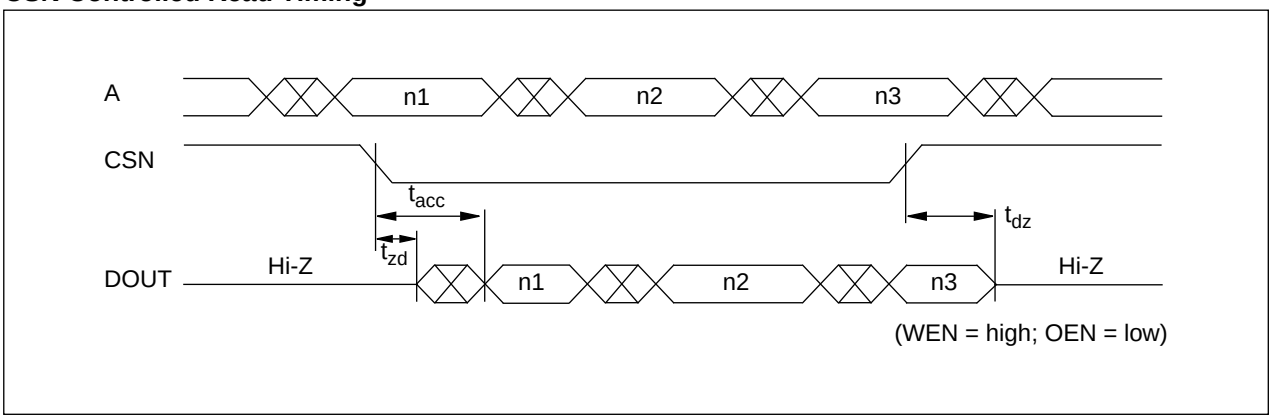
Height 10.85*W/Y+380.75

Timing Diagrams

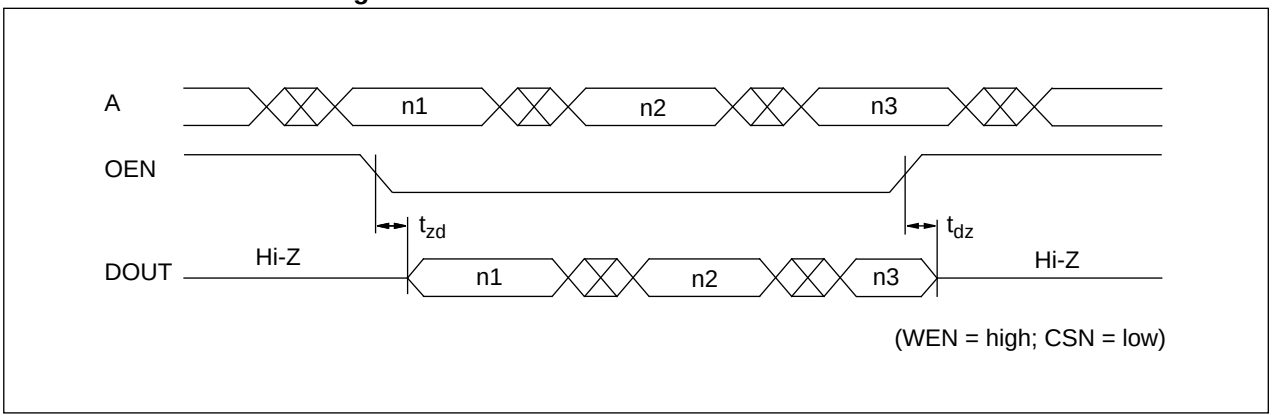
Basic Read Timing



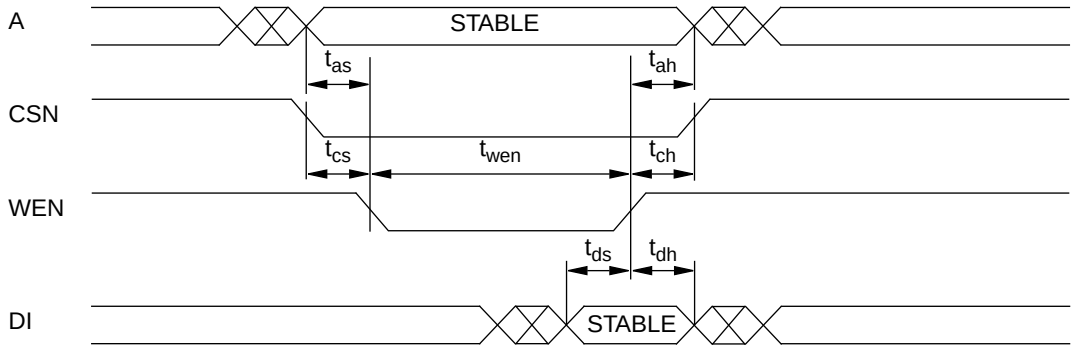
CSN Controlled Read Timing



OEN Controlled Read Timing

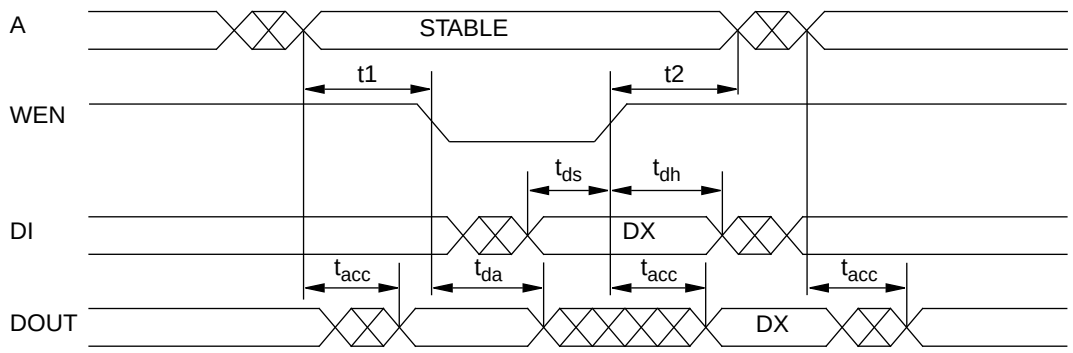


Basic Write Timing



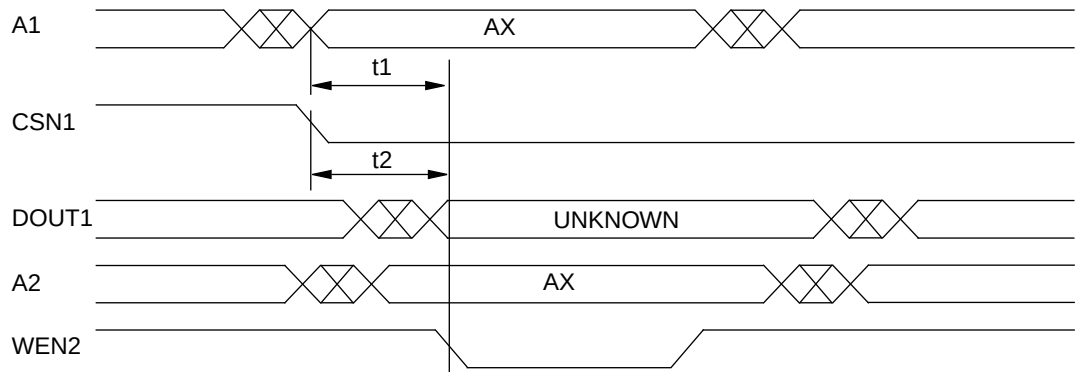
(OEN = Don't Care)

Read-Write-Read Timing (when t1, t2 > tacc)



(CSN, OEN = low)

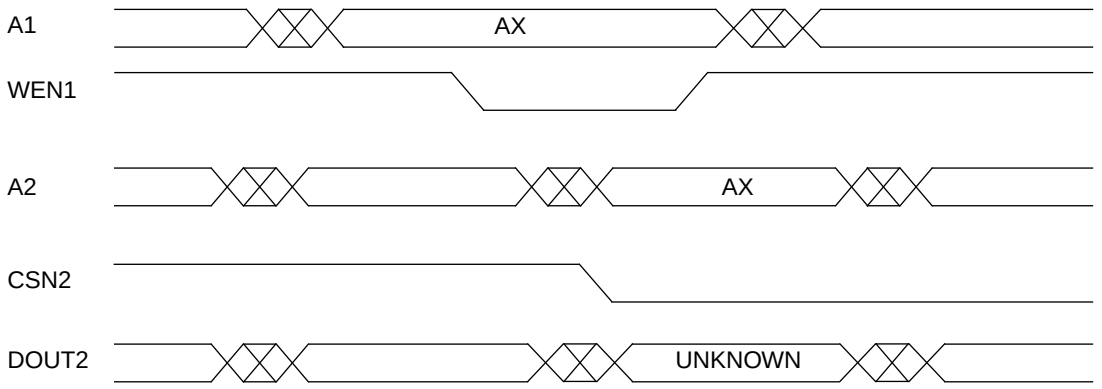
Read-Write Contention (when MIN (t1, t2) <= trwc)



(WEN = high; OEN1,CSN2 = low)

* If the smaller of t1 or t2 is smaller than or equal to Trwc, it is Read-Write Contention.
The read by port1 is invalid, the write by port2 is still valid.

Write-Read Contention



(CSN1, OEN2 = low; WEN2 = high)

* If read access by port2 begins while WEN1 is low and the addresses of both ports are same, it is Write-Read Contention. The read by port2 is invalid, the write by port1 is still valid.

Write-Write Contention (when t1 <= twwc)

(CSN1, CSN2 = low)

* If t1 is smaller than or equal to twwc, it is Write-Write Contention. The data stored at current address will be unpredictable. Regardless of the value of t1, read by port1 after WEN1 rise is invalid. It is a sort of Write-Read Contention.

Datapath Compilers 6

Contents

OVERVIEW

The datapath cell library is a set of high-level logic elements developed by Samsung ASIC. Datapath cells generate application-specific design libraries that can be used with the datapath place and route tool to construct complex datapaths. The blocks which are produced using datapath cells can then be globally routed using the chip level place and route tool like ArcCell.

Datapath compiler automatically places and routes circuits that have an inherently regular structure. Datapath compiler differs from a standard cell place and route tool in that it enables you to map regularity from a logical design into a layout. With datapath, you can create layouts that are as dense as custom layouts. A typical application of datapath is a multi-bit arithmetic logic function.

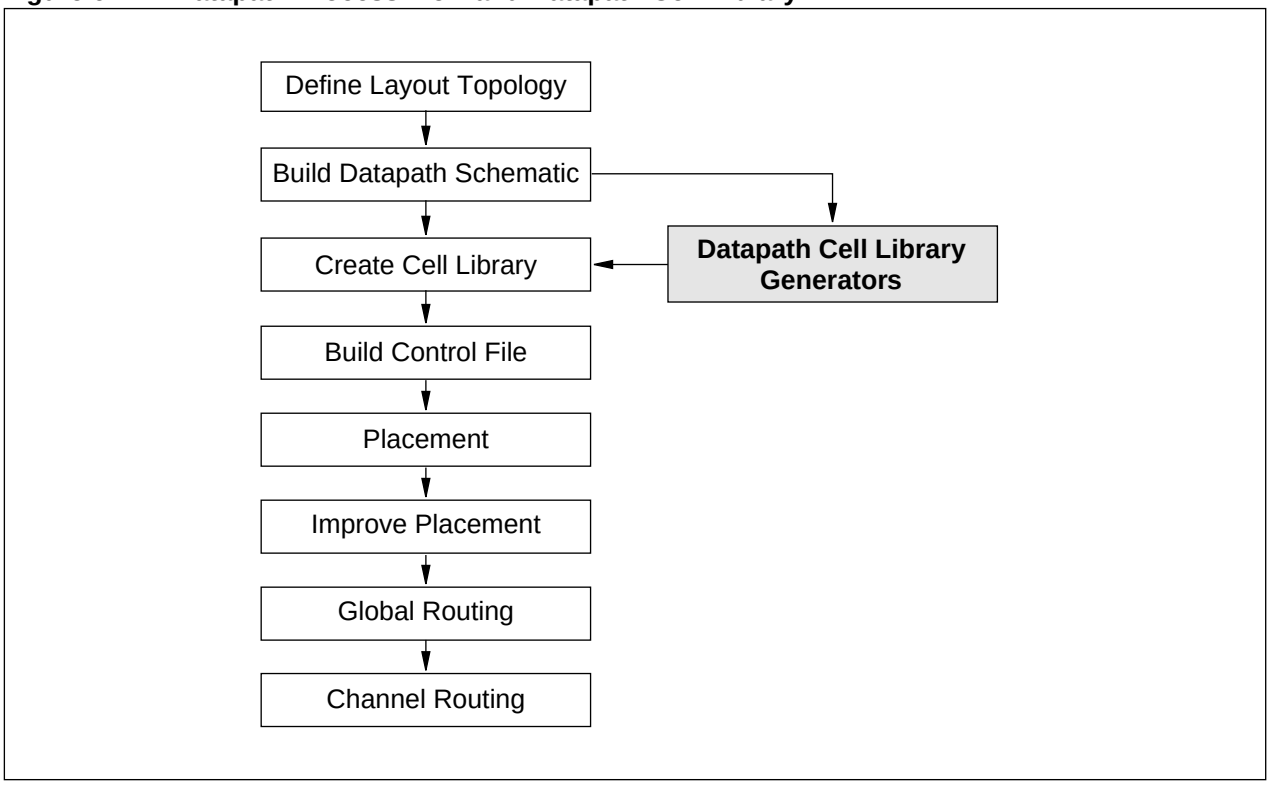
Datapath compiler enables you to:

- Generate schematics automatically according to the user-specific parameters
- Support functional models, test vectors and auto-characterized timing models
- Produce layouts that exhibit modularity and topological regularity
- Control the layout placement and density
- Perform over-the-cell routing and TLM maze routing with channel compaction
- Produce “cap” file and “wire delay” file for back-annotation process.

Datapath Process Flow

The datapath process flow begins the physical design portion of the IC design process. The logic design and circuit analysis have been completed and the next step is to produce a layout for the design. The figure 6-1 illustrates the recommended methodology for using datapath to create a layout for a design and illustrates how the datapath cell library fits into the datapath process flow.

Figure 6-1. Datapath Process Flow and Datapath Cell Library

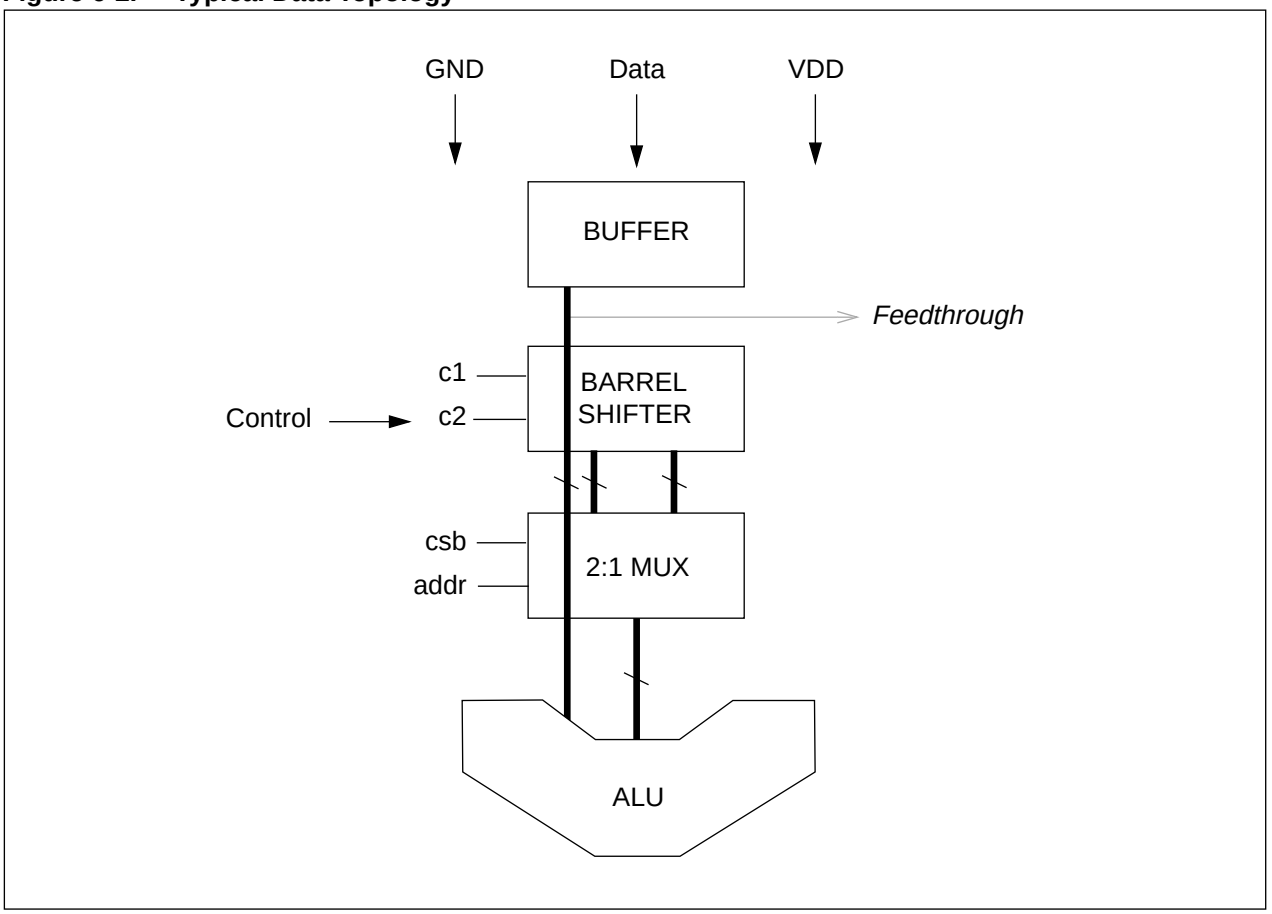


A datapath layout is a two-dimensional array of rows and columns with routing channels between the rows. The orientation of bits and words with respect to rows and columns defines the datapath layout topology.

Feedthrough terminals are the locations on a datapath cell where the datapath router can cross the row without connecting to the cell. Feedthroughs can be built into the cell (that is, the cell contains a vertical wire with a top and bottom terminal that is not connected internal to the cell), or they can be locations where there is sufficient room to route a wire vertically over the cell.

The figure 6-2 illustrates a typical datapath topology.

Figure 6-2. Typical Data Topology



DATAPATH COMPILERS INFORMATION

Macro Cells

Cell Name	Function	Bits	Features
adder	Adder/Subtracter	4 ~ 128	• Ripple/Carry-Bypass Scheme • 2's Complement Overflow Flag
addersat	Saturating Adder	4 ~ 128	• Ripple/Carry-Bypass Scheme • 2's Complement
alu	Arithmetic Logic Unit	4 ~ 128	• 2's Complement Overflow/Carry-Out Flag • 9 Arithmetic, 15 Logical Functions
bs	Barrel Shifter	4 ~ 128	• Transmission Gate Multiplexing Scheme • Bi-Directional Shift or Rotate • Fill Vacant Bits with Data
cmp	Comparator	4 ~ 128	• Less than or Equal Flag & Equal Flag • Greater than or Equal Flag & Equal Flag • Greater than & Equal Flag • Less than & Equal Flag • 2's Complement
csadder	Carry-Select Adder	4 ~ 128	• Double Carry-Select Algorithm • 2's Complement Overflow Flag
dec	Decrementer	4 ~ 128	• Ripple/Carry-Bypass Scheme
enc	Priority Encoder	4 ~ 128	• Detect from LSB/MSB
fmpy	Fast Multiplier	8 ~ 64	• Modified Wallace Tree Architecture • 2's Complement
inc	Incrementer	4 ~ 128	• Ripple/Carry-Bypass Scheme
incdec	Incrementer/Decrementer according to select signal	4 ~ 128	• Ripple/Carry-Bypass Scheme
mpy	Array Multiplier	6 ~ 64	• Supporting Accumulator and Pipes • 2's Complement Multiplication
norm	Normalizer	4 ~ 128	• Outputs Shift Amount and All0 Flag
oned	One Detector	4 ~ 128	• Generating One Flag
parity	Parity Generator	4 ~ 128	• Generating Parity Flag
regf	Register File	8 ~ 128	• Configurable Read (1 ~ 4)/Write (1 ~ 2) • Address Decoders on Either Side of Block
zerod	Zero Detector	4 ~ 128	• Generating Zero Flag

Logic Cells

Cell Name	Function	Bits	Features
ao	AND-OR	4 ~ 128	• Configurable 21 and 22 Types
aoi	AND-OR-INVERT	4 ~ 128	• Configurable 21 and 22 Types
buffer	Buffer/Inverter	4 ~ 128	• Buffers and Inverters
bushldr	Bus Holder	4 ~ 128	• Bus Holder
dff	D Flip-Flop	4 ~ 128	• Negative/Positive Edge Triggered • Scan Logic and Set/Reset Options • Tri-State and Normal Outputs
fadder	Full Adder	4 ~ 128	• Full Adder Array
latch	Transparent Latch	4 ~ 128	• High Input Enable • Scan Logic and Set/Reset Options • Tri-State and Normal Outputs
mux	Multiplexer	4 ~ 128	• Inverting/Non-Inverting • Configurable 2, 3, 4 and 8 Inputs
nand	NAND/AND	4 ~ 128	• Configurable 2, 3 and 4 Inputs
nor	NOR/OR	4 ~ 128	• Configurable 2, 3 and 4 Inputs
oa	OR-AND	4 ~ 128	• Configurable 21 and 22 Types
oai	OR-AND-INVERT	4 ~ 128	• Configurable 21 and 22 Types
tristate	Tri-State Buffer/Inverter	4 ~ 128	• Tri-State Buffers and Inverters
xor	Exclusive OR/NOR	4 ~ 128	• Configurable 2 and 3 Inputs

Features

- Two’s complement or unsigned magnitude operation
- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Simple ripple and sophisticated group bypass scheme
- Two’s complement overflow flag
- *n*-bit (4 to 128) Adder
- Three drive strength options for output

General Description

The Adder/Subtracter builds an *n*-bit wide Adder schematic. The schematic generated is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells.

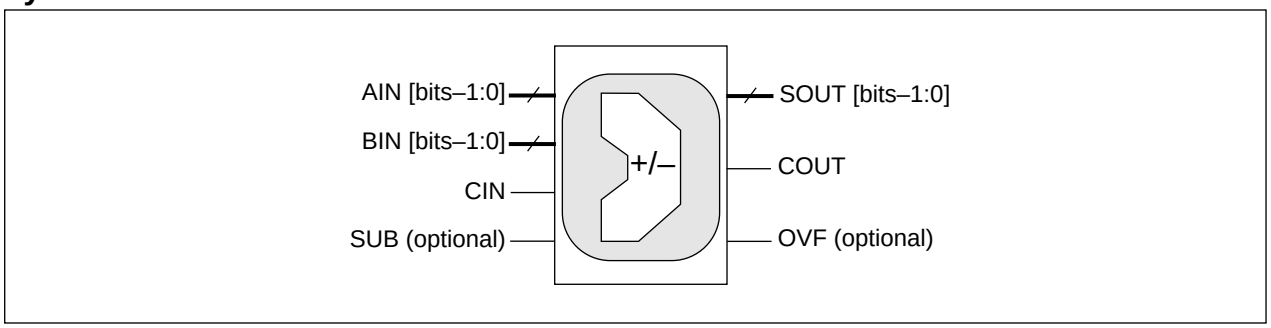
The Adder/Subtracter performs two’s complement addition/subtraction or unsigned magnitude addition. The overflow flag gets set if an overflow occurs while adding two positive or negative numbers. The overflow is ignored while doing unsigned magnitude operations.

Design Description

The Adder/Subtracter performs add/subtract function. An *n*-bit wide operand (AIN), an *n*-bit wide operand (BIN), a 1-bit wide input carry signal (CIN), an *n*-bit wide output bus (SOUT) and 1-bit wide output carry signal (COUT) serve as the I/O signals to the module.

The Adder/Subtracter can be built with two different carry chains allowing speed/area trade-offs. The ripple carry chain is high in density, but low in performance. The carry-bypass chain has a unique grouping of bits which creates a high performance design. This scheme is preferable for the addition of large data words to attain high speed.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
nopass	0: group bypass; 1: ripple adder	0/1
subtract	0: adder; 1: subtracter	0/1
cinlogic	0: CIN ← ~CIN; 1: CIN ← CIN	0/1
overflow	Overflow flag for signed operation	0/1
drv	Drive strength	1/2/4

Adder/Subtracter

Function Table

Type	Function
Adder	If (cinlogic == 1), SOUT = AIN + BIN + CIN, else SOUT = AIN + BIN + ~CIN
Subtracter	If (cinlogic == 1), SOUT = AIN + ~BIN + CIN, else SOUT = AIN + ~BIN + ~CIN
Overflow	(~SOUT [bits–1]) • (AIN [bits–1] • BIN [bits–1]) + (SOUT [bits–1]) • (~AIN [bits–1]) • (~ BIN [bits–1])

Truth Table

Inputs			Outputs	
AIN	BIN	CIN	SOUT	COUT
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Pin Capacitance

Pin Name	Value (pF)
AIN	0.052
BIN	0.042
CIN	0.102

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input
BIN [bits–1:0]		Data input
CIN		Carry-in
SUB		It specifies addition/subtraction (optional when the parameter subtract = 1).
SOUT[bits–1:0]	O	Result of addition/subtraction
COUT		It specifies the carry-out of two given numbers.
OVF		Overflow/underflow of signal addition/subtraction (optional when the parameter overflow = 1).

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: nopass = 0, subtract = 0, cinlogic = 1, overflow = 1, drv =1					
Bit	Area (μm x μm)		Delay (ns)		Current (mA)
	Width	Height	T_{PLH}	T_{PHL}	
8	240.5	104.8	3.338	2.964	0.164
16	451.7	103.4	3.748	3.374	0.311
24	662.9	107.8	3.948	3.574	0.446
32	874.1	108.9	4.188	3.832	0.586

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- High performance Arithmetic Logic Unit
- Two’s complement overflow flag
- *n*-bit (4 to 128) Adder used
- Carry-out flag
- Three drive strength options for output

General Description

The Arithmetic Logic Unit builds an *n*-bit wide Arithmetic Logic Unit schematic. The schematic generated is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells.

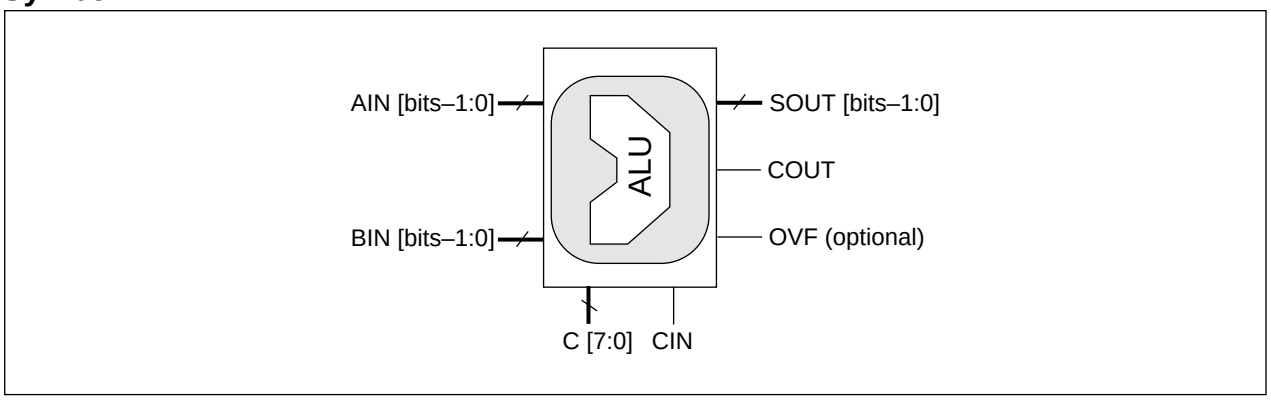
Design Description

The logic circuit produced by the generator performs 15 logical, 9 arithmetic operations. An *n*-bit wide operand (AIN), an *n*-bit wide operand (BIN), a 1-bit wide input carry signal(CIN), an *n*-bit wide output bus(SOUT) and 1-bit output carry signal(COUT) serve as the I/O signals to the module.

The Arithmetic Logic Unit is built with a carry-bypass chain. The carry-bypass chain has a unique grouping of bits which creates a high performance design. This scheme provides high performance for large data words arithmetic operations.

The overflow flag gets set if an overflow occurs while adding two positive or negative numbers. This flag is ignored for unsigned magnitude operations but is important when using the block in two’s complement arithmetic operations.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
overflow	Overflow flag for signed operation	0/1
drv	Drive strength	1/2/4

Function Table

Logical	Opcode	Arithmetic	Opcode
0	0x00	a + b + CIN	0x76
~a & ~b	0x01	a + ~b + CIN	0xb9
~a & b	0x02	b + ~a + CIN	0xd9
~a	0x03	~a + CIN	0xf3
a & ~b	0x04	~b + CIN	0xf5
~b	0x05	a + CIN	0xfc
a ^ b	0x06	b + CIN	0xfa
~a | ~b	0x07	a – ~CIN	0x33
a & b	0x08	b – ~CIN	0x55
~(a ^ b)	0x09	**NOTE**: While the ALU is not active, it is preferable to keep the opcode to “0x00”. If C input has an improper code, which is not in the above table, it can cause the undesirable power consumption.	
pass b	0x0a		
~a | b	0x0b		
pass a	0x0c		
a | ~b	0x0d		
a | b	0x0e		

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input for arithmetic/logical operations
BIN [bits–1:0]		Data input for arithmetic/logical operations
C [7:0]		Operational code control inputs. Refer to the function table.
CIN		Carry-in for arithmetic operations It must be maintained to ‘0’ in a logical operation.
SOUT [bits–1:0]	O	Result of an arithmetic/logical operation
COUT		Carry-out of an arithmetic operation
OVF		Overflow/underflow of a signed addition (optional when the parameter overflow = 1)

Pin Capacitance

Pin Name	Value (pF)
AIN	0.048
BIN	0.100
CIN	0.073
C	0.393

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: overflow = 1, drv =1					
Bit	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
	Width	**Height**	**T_{PLH}**	**T_{PHL}**	
8	240.9	159.2	3.171	2.867	0.108
16	452.1	155.7	3.468	3.158	0.212
24	663.3	157.4	3.841	3.537	0.308
32	874.5	159.1	4.068	3.745	0.410

Features

- Functional model, test-vector, schematic and layout generators
- Timing model with auto-characterization
- High speed and density
- Two's complement multiplication

General Description

The Array Multiplier can be optimized for multiple-targeted technologies. The Array Multiplier can build Multipliers from 6-bits to 64-bits with an accumulator, a configurable size of output buffer and a pipe.

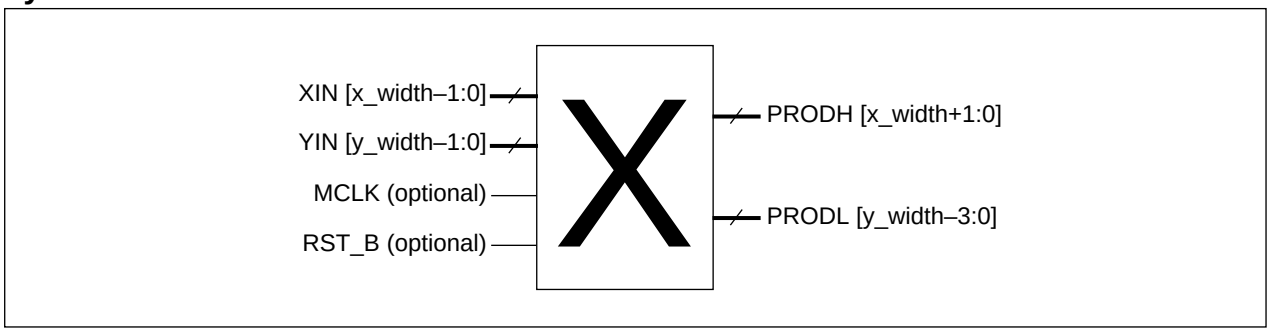
Design Description

The Array Multiplier uses the modified Booth's algorithm to encode the multiplier bits by partitioning the bits into three bit groups, with one bit shared between groups and performing the desired operation as required by the algorithm. The use of the modified Booth's algorithm reduces by half the number of partial products formed.

You can insert one pipeline stage, which increases the efficiency of the multiplier. The MSB adder used in the design is a fast group bypass adder and does not require pipes. The LSB adder is programmable to take pipes and is, therefore, the adder array. The clocks to the pipeline control how the internal data changes so that the data is always stable throughout the clock period and there is no hold problem.

The multiplier and the multiplicand are programmable in increments by the two bits from a minimum of 6 bits to a maximum of 64 bits.

Symbol



Parameter Description

Parameter Name	Description	Range
x_width*	Multiplicand bits (the x-input width)	6 to 64 even
y_width	Multiplier bits (the y-input width)	6 to 64 even
pipes	Pipeline stage	0/1
accum	0: none; n: (x_width+n) bit accumulator	0/1/2/3/4
obuff	1: 6x output buffer; 2: 12x output buffer	1/2

* x_width should be greater than or equal to y_width ($x \geq y$).

Pin Description

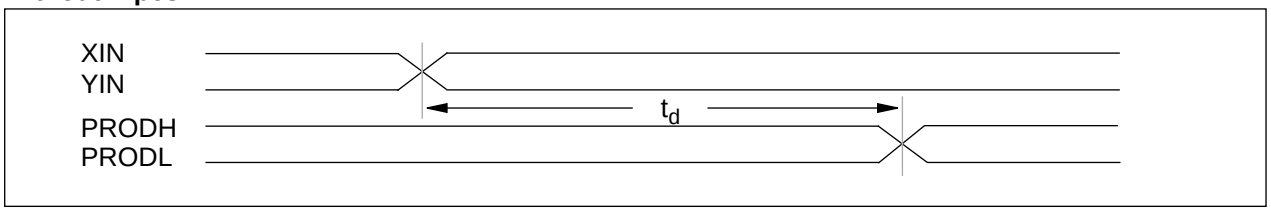
Pin Name	I/O	Description
XIN [x_width–1:0]	I	Data input – Multiplicand
YIN [y_width–1:0]		Data input – Multiplier
MCLK		Clock input to the latches used in the design (optional when pipes = 1 or accum ≥ 1)
RST_B		Input reset line for the latches (active high) If the multiplier has an accumulator, the reset lines ensure that the contents of the accumulator is zero before the first set of XIN * YIN arrives to the accumulator (optional when pipes = 1 or accum ≥ 1).
PRODH [x_width+1:0]	O	Data output lines from the MSB adder The values of these lines together with the prodL values gives the output data (product).
PRODL [y_width–3:0]		Data output lines from the LSB adder

Pin Capacitance

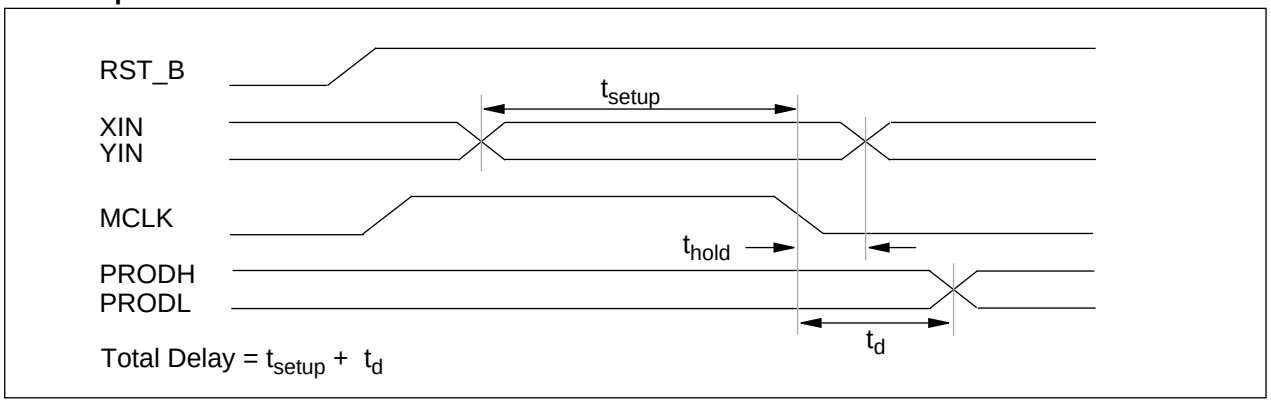
Pin Name	Value (pF)
XIN	0.088
YIN	0.083

Timing Diagram

Without Pipes



With 1 Pipe



Timing Parameters (With 1 Pipe)

Symbol	Description	Inputs	Outputs
t_{setup}	Input stage delay – Setup time	XIN, YIN	–
t_{hold}	Input state delay – Hold time	XIN, YIN	–
t_d	Output state delay	–	PRODH, PRODL

Timing Requirements

With 1 Pipe

Parameters: io_latch = 0, accum =0, obuff = 1, met_layer = 3, pipe=1		
Size	**Timing Field**	**Value (ns)**
8 x 8	min_pulse_width_high MCLK	0.617
	min_pulse_width_low MCLK	0.739
	min_pulse_width_low RST_B	0.922
	hold_falling XIN MCLK	0.407
	hold_falling YIN MCLK	0.064
	setup_falling XIN MCLK	3.050
	setup_falling YIN MCLK	3.790
16 x 8	min_pulse_width_high MCLK	0.920
	min_pulse_width_low MCLK	0.917
	min_pulse_width_low RST_B	1.350
	hold_falling XIN MCLK	0.497
	hold_falling YIN MCLK	0.064
	setup_falling XIN MCLK	3.050
	setup_falling YIN MCLK	3.880
16 x 16	min_pulse_width_high MCLK	0.920
	min_pulse_width_low MCLK	0.917
	min_pulse_width_low RST_B	1.350
	hold_falling XIN MCLK	0.457
	hold_falling YIN MCLK	0.064
	setup_falling XIN MCLK	0.385
	setup_falling YIN MCLK	4.610
24 x 8	min_pulse_width_high MCLK	0.741
	min_pulse_width_low MCLK	0.856
	min_pulse_width_low RST_B	1.160
	hold_falling XIN MCLK	0.479
	hold_falling YIN MCLK	0.064
	setup_falling XIN MCLK	3.050
	setup_falling YIN MCLK	3.930
24 x 16	min_pulse_width_high MCLK	0.741
	min_pulse_width_low MCLK	0.856
	min_pulse_width_low RST_B	1.160
	hold_falling XIN MCLK	0.438
	hold_falling YIN MCLK	0.064
	setup_falling XIN MCLK	3.850
	setup_falling YIN MCLK	4.670

Timing Requirements (Cont.)

With 1 Pipe (Cont.)

Parameters: io_latch = 0, accum =0, obuff = 1, met_layer = 3, pipe=1		
Size	**Timing Field**	**Value (ns)**
24 x 24	min_pulse_width_high MCLK	0.741
	min_pulse_width_low MCLK	0.856
	min_pulse_width_low RST_B	1.160
	hold_falling XIN MCLK	0.398
	hold_falling YIN MCLK	0.064
	setup_falling XIN MCLK	4.980
	setup_falling YIN MCLK	5.750
32 x 8	min_pulse_width_high MCLK	0.887
	min_pulse_width_low MCLK	0.949
	min_pulse_width_low RST_B	1.380
	hold_falling XIN MCLK	0.527
	hold_falling YIN MCLK	0.064
	setup_falling XIN MCLK	3.050
	setup_falling YIN MCLK	4.000
32 x 16	min_pulse_width_high MCLK	0.887
	min_pulse_width_low MCLK	0.949
	min_pulse_width_low RST_B	1.380
	hold_falling XIN MCLK	0.487
	hold_falling YIN MCLK	0.064
	setup_falling XIN MCLK	3.850
	setup_falling YIN MCLK	4.740
32 x 24	min_pulse_width_high MCLK	0.887
	min_pulse_width_low MCLK	0.949
	min_pulse_width_low RST_B	1.380
	hold_falling XIN MCLK	0.447
	hold_falling YIN MCLK	0.064
	setup_falling XIN MCLK	4.930
	setup_falling YIN MCLK	5.770
32 x 32	min_pulse_width_high MCLK	0.887
	min_pulse_width_low MCLK	0.949
	min_pulse_width_low RST_B	1.380
	hold_falling XIN MCLK	0.407
	hold_falling YIN MCLK	0.064
	setup_falling XIN MCLK	6.280
	setup_falling YIN MCLK	7.050

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Without Pipes

Parameters: io_latch = 0, accum =0, obuff = 1, met_layer = 3, pipe=0					
Bit	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
	Width	**Height**	**T_{PLH}**	**T_{PHL}**	
8 x 8	290.4	413.6	6.546	6.392	0.395
16 x 8	501.6	413.6	6.646	6.562	–
16 x 16	501.6	673.6	9.206	9.102	1.701
24 x 8	765.6	413.6	6.976	6.752	–
24 x 16	765.6	673.6	9.546	9.292	–
24 x 24	765.6	967.6	12.156	11.852	3.001
32 x 8	976.8	413.6	7.356	7.212	–
32 x 16	976.8	673.6	9.506	9.532	–
32 x 24	976.8	967.6	11.844	12.052	–
32 x 32	976.8	1237.6	14.656	14.652	4.720

With 1 Pipe

Parameters: io_latch = 0, accum =0, obuff = 1, met_layer = 3, pipe=1				
Bit	**Area (μm x μm)**		**Delay (ns)**	
	Width	**Height**	**T_{PLH}**	**T_{PHL}**
8 x 8	290.4	531.5	5.696	5.522
16 x 8	501.6	531.5	6.466	6.192
16 x 16	501.6	826.7	7.446	7.162
24 x 8	765.6	531.5	6.696	6.482
24 x 16	765.6	826.7	7.666	7.452
24 x 24	765.6	1163.2	8.866	8.602
32 x 8	976.8	531.5	7.176	7.042
32 x 16	976.8	826.7	8.156	8.012
32 x 24	976.8	1163.2	9.226	9.082
32 x 32	976.8	1469.8	10.376	10.402

Barrel Shifter

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- High performance Barrel Shifter
- *n*-bit (4 to 128) Shifter
- Transmission gate multiplexing scheme
- Bi-directional shift, fill vacant bits with data, or rotates
- Three drive strength options for output

General Description

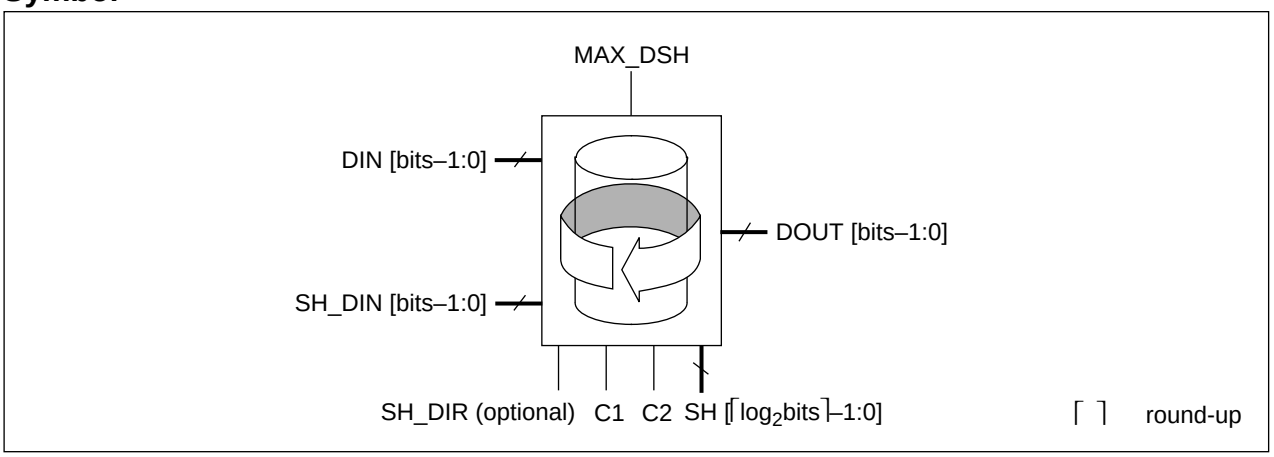
The Barrel Shifter builds an n-bit wide Barrel Shifter schematic. The schematic generated is used to drive a datapath placement and routing tool in combination with technology-specific layout leafcells. The Barrel Shifter can shift and rotate input signals in either direction. The direction of the shift can be chosen between MSB (LEFT) and LSB (RIGHT) of the bit string. The Barrel Shifter supports both arithmetic and logical shift operations.

Design Description

The Barrel Shifter is constructed as a series of cascaded 2-to-1 and 4-to-1 multiplexers. In its largest configuration (128 bits), three rows of 4-to-1 and one row of 2-to-1 MUXs are used. The architecture is based on a left-shifter block, a right-shifter block, a fill block and a direction block.

Data can be shifted left or right; the vacant bits are padded with zeros during a left shift and can be padded with MSB of the shift data bus during a right shift. A shift data bus (SH_DIN) fills the vacant bits during a shift operation. During a right shift, the shift data bus fills the vacant bits with data from the LSB of the shift data bus; during a left shift, the shift data bus fills the vacant bits with data from the MSB of the shift data bus (essentially a circular shift).

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Direction of shift	LEFT/RIGHT/BOTH
drv	Drive strength	1/2/4

Function Table

SH_DIR	C1	C2	DOUT
0	0	0	Shift right and fill with zeros
0	1	0	Shift right and fill with data bus (SH_DIN)
1	0	0	Shift left and fill with zeros
1	1	0	Shift left and fill with data bus (SH_DIN)
0	0	1	Shift right and fill with MSB
1	1	1	Left rotation
0	1	1	Right rotation

Pin Description

Pin Name	I/O	Description
DIN [bits–1:0]	I	Data input
SH_DIN [bits–1:0]		Shift data input
SH_DIR		Shift direction (Left/Right) (optional when the parameter type = BOTH)
C1, C2		Control signals
SH [$\lceil \log_2 bits \rceil$–1:0]		Shift amount (in binary)
MAX_DSH		It fills data output with filling information according to C1 and C2. It refreshes output with fill data.
DOUT [bits–1:0]	O	Data output

⌈ ⌉ round-up

Pin Capacitance

Pin Name	Value (pF)
C1	0.061
C2	0.087
DIN	0.283
MAX_DSH	0.077
SH	0.204
SH_DIN	0.045
SH_DIR	0.044

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: type = BOTH, drv = 1					
Bit	Area (μm x μm)		Delay (ns)		Current (mA)
	Width	Height	T_{PLH}	T_{PHL}	
8	264.0	295.0	1.929	1.568	0.079
16	475.2	376.9	2.549	2.102	0.152
24	686.4	481.1	3.069	2.538	0.302
32	897.6	517.1	3.339	2.768	0.639

Carry-Select Adder

Features

- Two’s complement or unsigned magnitude operation
- Functional model, test vector, schematic, and layout generators
- Timing model with auto-characterization
- Sophisticated double carry-select algorithm
- Two’s complement overflow flag
- *n*-bit (4 to 128) Adder
- Three drive strength options for output

General Description

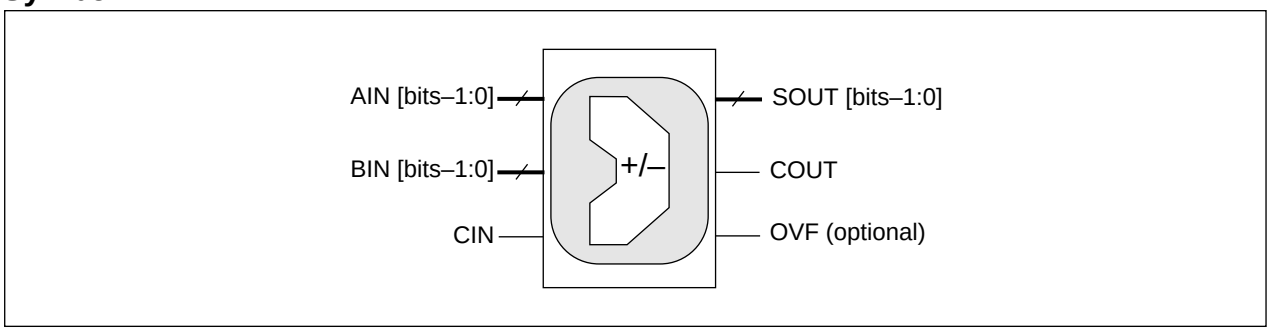
The Carry-Select Adder performs two’s complement addition or unsigned magnitude operation. The high performance Carry-Select Adder design can have layout leaf cells optimized for multiple-targeted technologies. The overflow flag gets set if an overflow occurs while adding two positive or negative numbers. The overflow is ignored for unsigned magnitude operations.

Design Description

The Carry-Select Adder performs high speed binary addition by using a sophisticated double carry-select algorithm with group delay equalization for carry propagation. The outer carry-select scheme is used to provide a short path between the low order inputs and the high order outputs. The internal carry-select schemes are placed within these blocks to reduce their block propagation delays. The sizes of the carry-select blocks increase along the carry propagation tree to produce a fast addition. An *n*-bit wide operand (AIN), an *n*-bit wide operand (BIN), a 1-bit wide input carry signal (CIN), and an *n*-bit wide output bus (SOUT) and 1-bit output carry signal (COUT) serve as the I/O signals to the module. The generated layout is constrained to four rows of cells for minimal area consumption.

This fast Carry-Select Adder is configured for your highest performance applications and outperforms normal Carry-Select Adders by modulating the size of the groups to equalize carry propagation delay, and by providing a second level of carry-select scheme.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of Carry-Select Adder instance to be generated	Any string
bits	Number of bits in the input data bus	4 to 128
overflow	It determines whether overflow output is present; 0: no overflow; 1: overflow	0/1
drv	Drive strength	1/2/4

Function Table

Type	Function
Adder	AIN + BIN + CIN
Overflow	(~SOUT [bits–1]) • (AIN [bits–1] • BIN [bits–1]) + (SOUT [bits–1]) • (~AIN [bits–1]) • (~BIN [bits–1])

Truth Table

Inputs			Outputs	
AIN	**BIN**	**CIN**	**SOUT**	**COUT**
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Input data word
BIN [bits–1:0]		Input data word
CIN		Carry-in
SOUT [bits–1:0]	O	Sum output (AIN + BIN + CIN)
COUT		Carry-out
OVF		Overflow output occurs during a signed addition (optional when the parameter overflow = 1).

Pin Capacitance

Pin Name	Value (pF)
AIN	0.083
BIN	0.077
CIN	0.065

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: overflow = 0, drv = 1					
Bit	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
	Width	**Height**	**T_{PLH}**	**T_{PHL}**	
8	240.5	146.8	2.508	2.134	0.212
16	451.7	149.5	3.028	2.654	0.447
24	662.9	151.3	3.338	2.982	0.689
32	874.1	151.3	3.468	3.104	0.929

Comparator

Features

- Functional model, test vector, schematic, and layout generators
- Timing model with auto-characterization
- Fast signed comparison
- Less than or equal and equal flags
- Greater than or equal and equal flags
- Greater than and equal flags
- Less than and equal flags
- *n*-bit (4 to 128) Comparator

General Description

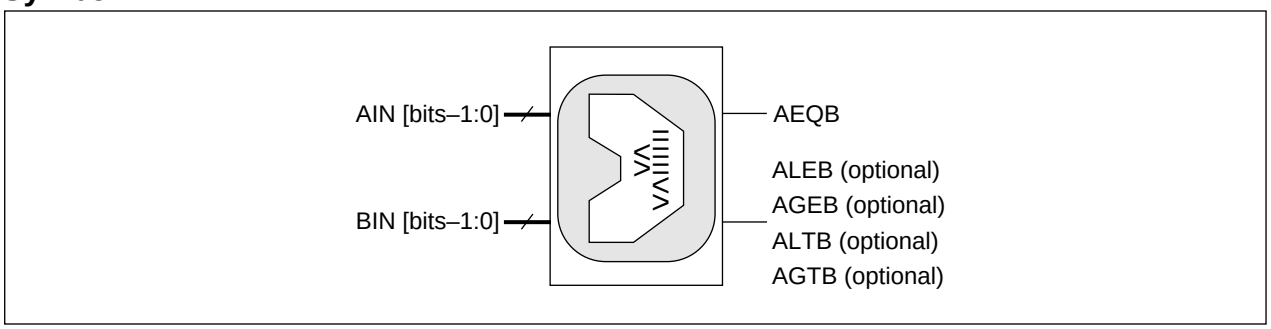
The Comparator builds an *n*-bit wide Comparator schematic. The schematic generated is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells. The Comparator supports signed comparisons.

Design Description

The logic circuit produced by the generator produces two different flags according to options.
In case of Greater than or Equal and Equal Flags (A ≥ B and A = B), two *n*-bit wide data operands (AIN, BIN) and two 1-bit wide outputs (AGEB, AEQB) serve as the I/O signals to the module. In case of Less than or Equal and Equal Flags (A ≤ B and A = B), two 1-bit wide outputs (ALEB, AEQB) serve as the I/O signals to the module. In case of Greater than and Equal Flags (A > B and A = B), two 1-bit wide outputs (AEQB, AGTB) serve as the I/O signals to the module. In case of Less than and Equal Flags (A < B and A = B), two 1-bit wide outputs (ALTB and AEQB) serve as the I/O signals to the module.

The Comparator is built with a unique carry-bypass chain. The carry-bypass chain has a unique grouping of bits which modulates the group sizes to minimize carry propagation delay, which creates a high performance design. This scheme is optimized for the comparison of large data words to attain high speed.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Type of flags to be generated – 0: LE, 1: GE, 2: LT, 3: GT	0/1/2/3
drv	Drive Strength	1/2/4

Function Table

Type	Function
AEQB (equal)	==
ALEB (less than or equal)	<=
AGEB (greater than or equal)	>=
ALTB (less than)	<
AGTB (greater than)	>

Truth Table

Inputs		Outputs				
AIN	**BIN**	**AEQB**	**ALEB**	**AGEB**	**AGTB**	**ALTB**
0	0	1	1	1	0	0
0	1	0	1	0	0	1
1	0	0	0	1	1	0
1	1	1	1	1	0	0

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input bus A
BIN [bits–1:0]		Data input bus B
AEQB	O	Equality flag (A = B) that specifies the signed equality of input busses
ALEB (optional)		Less than or Equal to flag (A ≤ B)
AGEB (optional)		Greater than or Equal to flag (A ≥ B)
ALTB (optional)		Less than flag (A < B)
AGTB (optional)		Greater than flag (A > B)

Pin Capacitance

Pin Name	Value (pF)
AIN	0.077
BIN	0.080

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: type = 1, drv = 1					
Bit	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
	Width	**Height**	**T_{PLH}**	**T_{PHL}**	
8	213.2	105.3	3.688	3.332	0.069
16	424.4	108.7	3.658	3.274	0.125
24	635.6	112.3	3.758	3.402	0.171
32	846.8	110.7	4.109	3.735	0.233

Decrementer

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Simple ripple and sophisticated carry-bypass scheme
- *n*-bit (4 to 128) Decrementer
- Buffered carry path
- Three drive strengths on output

General Description

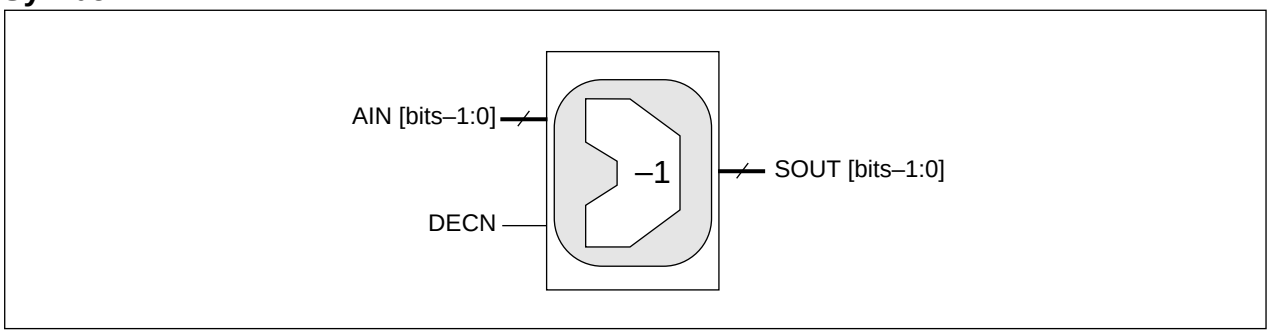
The Decrementer builds an *n*-bit wide Decrementer schematic. The schematic generated is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells. The Decrementer supports signed decrements.

Design Description

The logic circuit produced by the generator performs decrement functions. An *n*-bit wide operand (AIN), a 1-bit wide input carry signal (DECN), and an *n*-bit wide output bus (SOUT) serve as the I/O signals to the module.

The Decrementer is built with a unique carry-bypass chain. The carry-bypass chain has a unique grouping of bits which modulates the group sizes to minimize delay which creates a high performance design. This scheme is optimized for the decrement of large data words to attain high speed.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
nopass	0: group bypass; 1: ripple adder	0/1
drv	Drive strength	1/2/4

Function Table

Type	Function
Decrementer	AIN – 1

Truth Table

Inputs		Output
AIN	**DECN**	**SOUT**
0	1	0
1	1	1
0	0	1
1	0	0

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input
DECN		Decrement signal which is active low
SOUT [bits–1:0]	O	Data output – Result of decrementer

Pin Capacitance

Pin Name	Value (pF)
AIN	0.024
DECN	0.102

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: nopass = 0, drv = 1					
Bit	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
	Width	**Height**	**T_{PLH}**	**T_{PHL}**	
8	213.2	94.5	2.901	2.527	0.066
16	424.4	96.7	3.307	2.933	0.153
24	635.6	99.8	3.637	3.181	0.163
32	846.8	99.8	3.687	3.303	0.216

Fast Multiplier

Features

- Functional model, test vector, schematic and layout generator
- Timing model with auto-characterization
- Fastest architecture for large multipliers
- Supports two’s complement multiplication
- Three drive strength options for output

General Description

The Fast Multiplier can be optimized for multiple-targeted technologies. The Fast Multiplier can build Multipliers from 8-bits to 64-bits. There are output buffers which can be varied to three drive strengths.

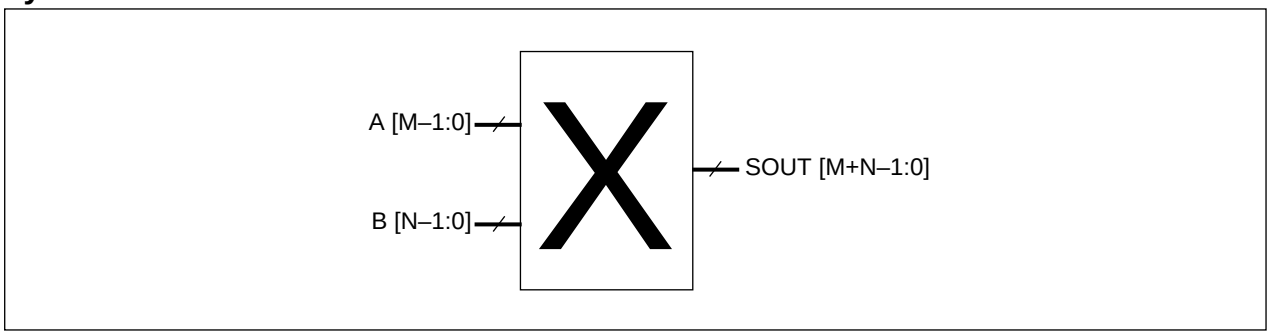
Design Description

The Fast Multiplier is based on a modified Wallace tree architecture, using the Baugh-Wooley algorithm to sum partial products for signed multiplication.

The traditional Wallace tree depends on a Carry Save Adder (CSA) which reduces three partial products to two redundant outputs (Sum, Carry). The modified Wallace tree architecture is based on a 4-2 Carry Save Adder (CSA42). The CSA42 reduces four partial products to two redundant outputs. This architecture reduces the number of partial products by two at each stage of the Wallace tree so that the core of a 32 x 32 multiplication can be achieved in four CSA42 delays.

The final sum (MSB) is generated by adding the final two redundant products from the multiplier core (Sum, Carry). The MSB adder uses a double carry select architecture to generate the final sum.

Symbol



Parameter Description

Parameter Name	Description	Range
M	Multiplicand bits (x-input width)	Refer to the note.
N	Multiplier bits (y-input width)	Refer to the note.
drv	1x/2x/4x output drive strength	1/2/4

NOTES: If M >= N, M = N, N+1, N+2, ..., 126 where N = 8, 12, 16, 20, 24, 32, 40 and 64
If M <= N, N = M, M+1, M+2, ..., 126 where M = 8, 12, 16, 20, 24, 32, 40 and 64

Pin Description

Pin Name	I/O	Description
A [M–1:0]	I	Data input – Multiplicand
B [N–1:0]		Data input – Multiplier
SOUT [M+N–1:0]	O	Data output – Result

Pin Capacitance

Pin Name	Value (pF)
A	0.043
B	0.043

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: drv = 1					
N x M	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
	Width	**Height**	**T_{PLH}**	**T_{PHL}**	
8 x 8	266.2	396.2	5.801	5.465	0.706
8 x 16	689.0	485.8	6.691	6.335	–
8 x 24	900.2	484.7	7.021	6.665	–
8 x 32	689.0	485.8	7.241	6.895	–
16 x 16	900.2	484.7	7.371	7.025	5.776
16 x 24	689.0	485.8	8.301	7.955	–
16 x 32	900.2	484.7	8.221	7.865	–
24 x 24	689.0	485.8	8.670	8.314	6.463
24 x 32	900.2	484.7	8.880	8.524	–
32 x 32	689.0	485.8	9.500	9.114	11.215

Incrementer

Features

- Functional model, test vector, schematic, and layout generators
- Timing model with auto-characterization
- Simple ripple and sophisticated carry-bypass scheme
- *n*-bit (4 to 128) Incrementer
- Buffered carry path
- Three drive strengths on output

General Description

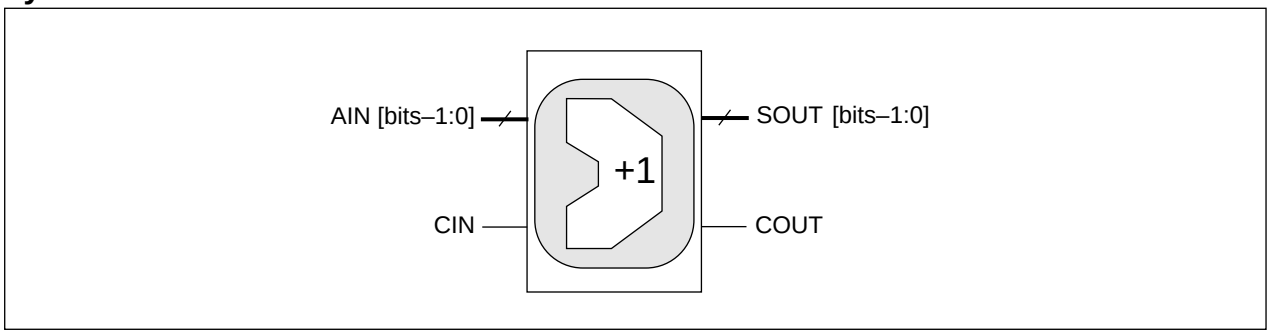
The Incrementer builds an *n*-bit wide Incrementer schematic. The schematic generated is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells. The Incrementer supports signed increments.

Design Description

The logic circuit produced by the generator performs increment functions. An *n*-bit wide operand (AIN), a 1-bit wide input carry signal (CIN), and an *n*-bit wide output bus (SOUT) and 1-bit output carry signal (COUT) serve as the I/O signals to the module.

The Incrementer can be built with two different carry chains allowing speed/area trade-offs. The ripple carry chain is high in density and low in performance. The carry-bypass chain has a unique grouping of bits which creates a high performance design. This scheme is preferable for the increment of high order bits to attain high performance.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
nopass	0: group bypass; 1: ripple adder	0/1
drv	Drive strength	1/2/4

Function Table

Type	Function
Incrementer	AIN + CIN

Truth Table

Inputs		Output
AIN	**CIN**	**SOUT**
0	0	0
1	0	1
0	1	1
1	1	0

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input
CIN		Carry-in increment signal
SOUT [bits–1:0]	O	Output data bus – Result of incrementer
COUT		Carry-out signal

Pin Capacitance

Pin Name	Value (pF)
AIN	0.150
CIN	0.116

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: nopass = 0, drv = 1				
Area (μm x μm)		**Delay (ns)**		**Current (mA)**
Width	**Height**	**T_{PLH}**	**T_{PHL}**	
213.2	88.7	2.333	1.959	0.060
424.4	94.9	2.387	2.013	0.108
635.6	92.3	2.617	2.261	0.154
846.8	92.5	2.757	2.383	0.201

Incrementer/Decrementer

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Simple ripple and sophisticated carry-bypass scheme
- *n*-bit (4 to 128) Incrementer/Decrementer
- Buffered carry path
- Three Multiple drive strengths options for output

General Description

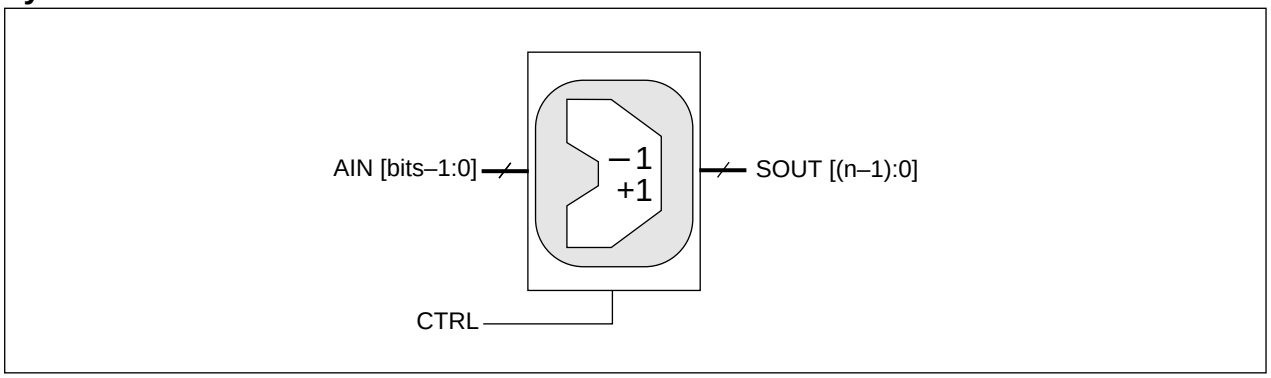
The Incrementer/Decrementer builds an *n*-bit wide Incrementer/Decrementer schematic. The schematic generated is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells. The Incrementer/Decrementer supports signed decrements.

Design Description

The logic circuit produced by the generator performs increment or decrement function by control signal. An *n*-bit wide operand (AIN), a 1-bit wide input control signal (CTRL), and an *n*-bit wide output bus (SOUT) serve as the I/O signals to the module.

The Incrementer/Decrementer is built with a unique carry-bypass chain. The carry-bypass chain has a unique grouping of bits which modulates the group sizes to minimize carry propagation delay, which creates a high performance design. This scheme is optimized for the incrementer/decrementer of large data words to attain high speed.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
nopass	0: group bypass; 1: ripple adder	0/1
drv	Drive strength	1/2/4

Function Table

Type	Function
Decrementer	AIN–1
Incrementer	AIN+1

Truth Table

Inputs		Output
AIN	**CTRL**	**SOUT**
0	1	1
1	1	0
0	0	1
1	0	0

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input
CTRL	I	Decrement signal which is active low, Increment signal which is active high
SOUT [bits–1:0]	O	Data output – Result of Incrementer or Decrementer

Pin Capacitance

Pin Name	Value (pF)
AIN	0.056
CTRL	0.869

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: nopass = 0, drv = 1					
Bit	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
	Width	**Height**	**T_{PLH}**	**T_{PHL}**	
8	213.2	100.6	3.111	2.737	0.04
16	424.4	107.5	3.353	2.979	0.05
24	635.6	106.1	3.583	3.227	0.07
32	846.8	106.3	3.790	3.426	0.09

Normalizer

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- *n*-bit (4 to 128) Normalizer
- High performance
- Outputs shift amount
- Three drive strength options for output

General Description

The Normalizer detects the number of leading zero's in the input data word, and outputs the data word so the left-most "1" appears in the MSB position, along with the shifted amount. If no "1" is detected in the data input, the ALL0 flag is set. The Normalizer is a high performance datapath function which can build normalizers between 4-128 bits in 1 bit increments.

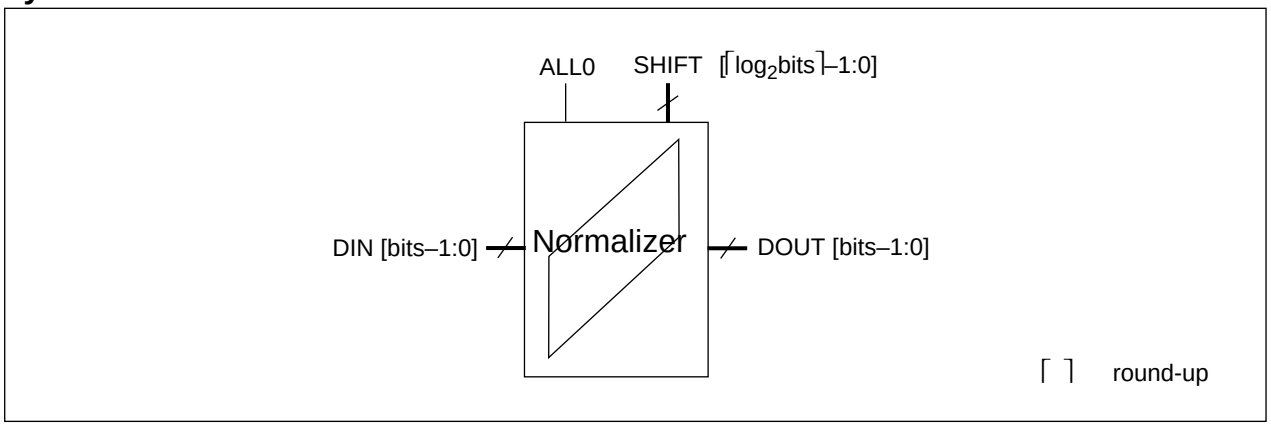
Design Description

The Normalizer is built from 2 sub-functions, an Priority Encoder, and a Left Shifter. The Priority Encoder detects the left-most "1" from the data input word and outputs the amount to be shifted. Then the amount is passed into the Left Shifter block and the leading "1" is shifted to the MSB position with the LSB filled with "0".

The priority encoder uses a parallel technique to calculate the high and low output address bits to speed up the leading "1" detection. A binary tree is used to determine the address of the high order bits, while a multiplexer tree is used to propagate the values of the low order bits.

The Left Shifter is constructed as a series of cascaded 2-to-1 and 4-to-1 multiplexers. In its largest configuration (128 bits), three rows of 4-to-1 and one row of 2-to-1 MUXs are used.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
drv	Drive strength	1/2/4

Pin Description

Pin Name	I/O	Description
DIN [bits–1:0]	I	Data input
ALL0	O	Output flag that zeros all bits on the data input bus
SHIFT [$\lceil \log_2 bits \rceil$–1:0]		Data output – Encoded address of the leading 1 bit
DOUT [bits–1:0]		Normalized data output

⌈ ⌉ round-up

Pin Capacitance

Pin Name	Bit	Value (pF)
DIN	8/24/32	0.196
	16	0.345

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: drv = 1					
Bit	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
	Width	**Height**	**T_{PLH}**	**T_{PHL}**	
8	266.5	177.5	1.855	1.820	0.078
16	477.7	205.0	2.196	2.160	0.154
24	688.9	262.6	2.326	2.500	0.258
32	900.1	297.6	2.526	2.500	0.348

One Detector

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Fast datapath one flag
- *n*-bit (4 to 128) one Detector
- Three drive strength options for output

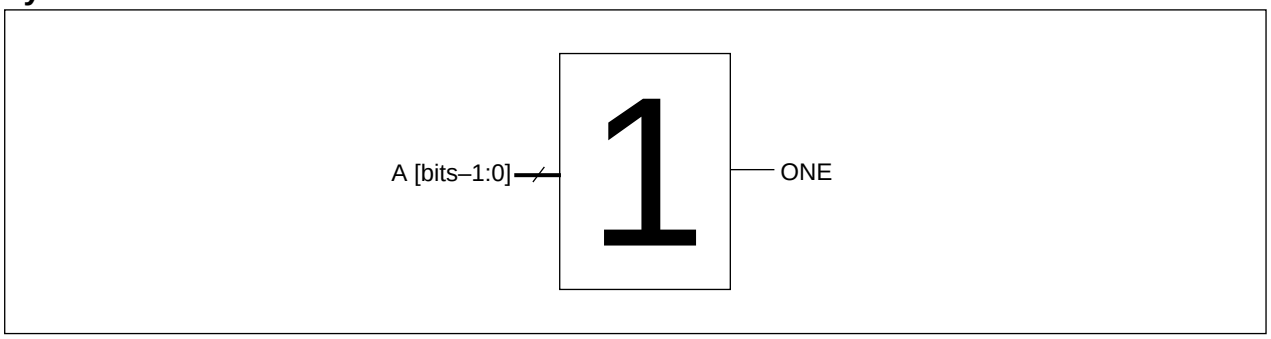
General Description

The One Detector builds an *n*-bit wide schematic that is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells. The One Detector detects “0” in the inputs and if there is no “0”, it sets ONE to “1.”

Design Description

The One Detector performs deciding whether the input is one or not. An *n*-bit wide operand (AIN) and a 1-bit wide one flag (ONE) serve as the I/O signals to the module. The One Detector can be built with simple AND gates.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
drv	Drive strength	1/2/4

Truth Table

A	ONE
All 1	1
Any 0	0

Pin Description

Pin Name	I/O	Description
A [bits–1:0]	I	Data input
ONE	O	It specifies whether all the bits in the input A are “0” or “1”.

Pin Capacitance

Pin Name	Value (pF)
A	0.038

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: drv = 1					
Bit	Area (μm x μm)		Delay (ns)		Current (mA)
	Width	Height	T_{PLH}	T_{PHL}	
8	213.3	61.3	1.766	1.157	0.021
16	424.5	64.6	2.066	1.311	0.024
24	662.0	68.0	2.356	1.467	0.048
32	846.9	71.4	2.376	1.465	0.047

Parity

Features

- Functional model, test-vector, schematic and layout generators
- Timing model with auto-characterization
- *n*-bit (4 to 128) Parity
- High speed and density
- Three drive strength options for output

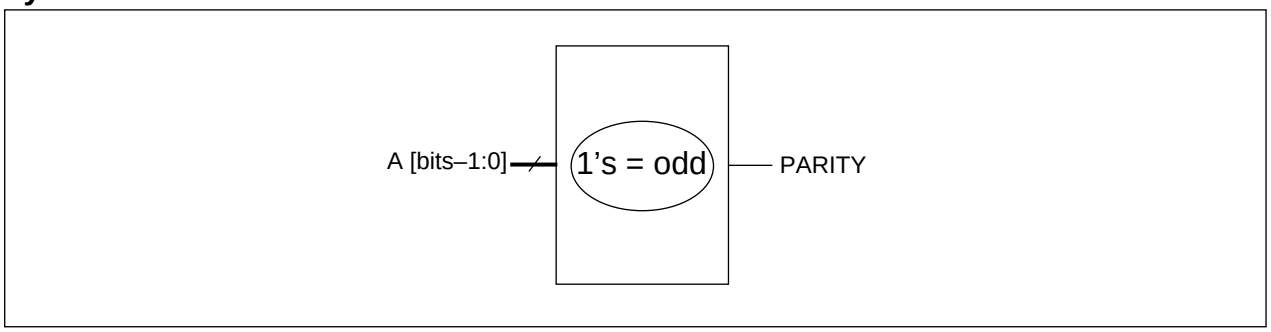
General Description

The Parity builds an n-bit wide Parity schematic. The Parity calculates the parity value of the specified input bits by performing the XOR function across all inputs. The design is optimized for multiple targeted technologies.

Design Description

The Parity uses a binary tree architecture for high speed calculations of the parity value. To minimize the area of the implementation, the layout cells used in the parity are placed in a single datapath row. It enables different drive strengths to be specified for the output.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of Parity generator to be created	Any string
bits	Number of bits in the input data bus	4 to 128
drv	Drive strength	1/2/4

Pin Description

Pin Name	I/O	Description
A [bits–1:0]	I	Data input bus for Parity generation
PARITY	O	Output parity value for inputs (odd parity)

Pin Capacitance

Pin Name	Value (pF)
A	0.035

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: drv = 1					
Bit	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
	Width	**Height**	**T_{PLH}**	**T_{PHL}**	
8	188.3	58.5	1.753	1.419	0.022
16	399.5	64.2	2.068	1.734	0.024
24	635.6	67.4	2.378	2.004	0.048
32	821.9	71.1	2.378	2.044	0.048

Priority Encoder

Features

- Functional Model, test-vectors, schematics and layout generators
- Timing model with auto characterization
- High speed and density
- *n*-bit (4 to 128) Priority Encoder

General Description

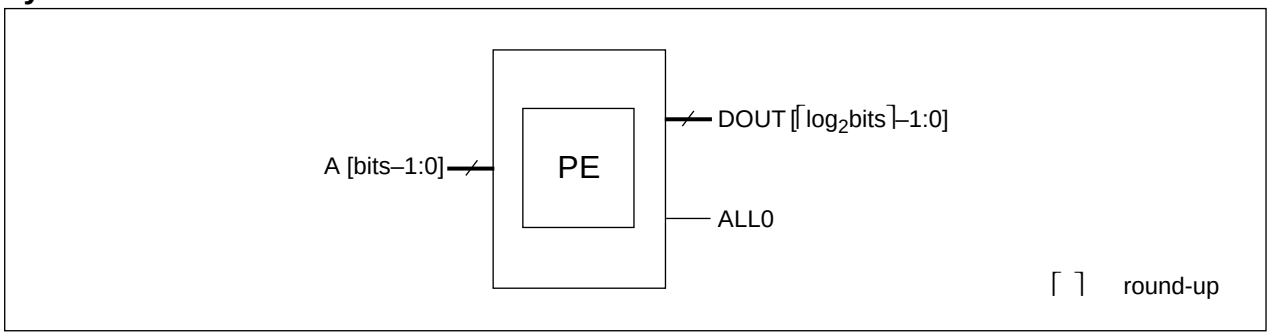
The Priority Encoder builds an n-bit wide schematic that is used to drive the datapath placement and routing tool in combination with technology-specific layout leafcells. The Priority Encoder detects the leading “1” on data bus.

Design Description

The priority encoder uses a parallel processing technique to calculate the high and low output address bits to speed up the leading “1” detection. A binary tree is used to determine the address of the high order bits, while a multiplexer tree is used to propagate the values of the low order bits.

This design supports a wide range of input data width with a narrow delay time spectrum. It can create either a leftmost one or a rightmost one Priority Encoder.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of Priority Encoder to be created	Any string
bits	Number of bits in the input data bus	4 to 128
type	0: detect from MSB; 1: detect from LSB	0/1
drv	Drive strength	1/2/4

Pin Description

Pin Name	I/O	Description
A [bits–1:0]	I	Data input bus for the leading one detection
DOUT [$\lceil \log_2 bits \rceil$–1:0]	O	Data output – Encoded address of the leading 1 bit
ALL0		Output flag that zeros all bits on the data input bus

⌈ ⌉ round-up

Pin Capacitance

Pin Name	Value (pF)
A	0.069

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: type = 0, drv = 1					
Bit	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
	Width	**Height**	**T_{PLH}**	**T_{PHL}**	
8	213.2	91.7	1.948	1.880	0.021
16	424.4	99.6	2.286	2.220	0.037
24	635.6	109.8	2.416	2.560	0.048
32	846.8	118.4	2.616	2.560	0.142

Register File

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Configurable read/write ports for macro block
- Address decoders on either side of the datapath block
- *n*-bit (4 to 128) Register File

General Description

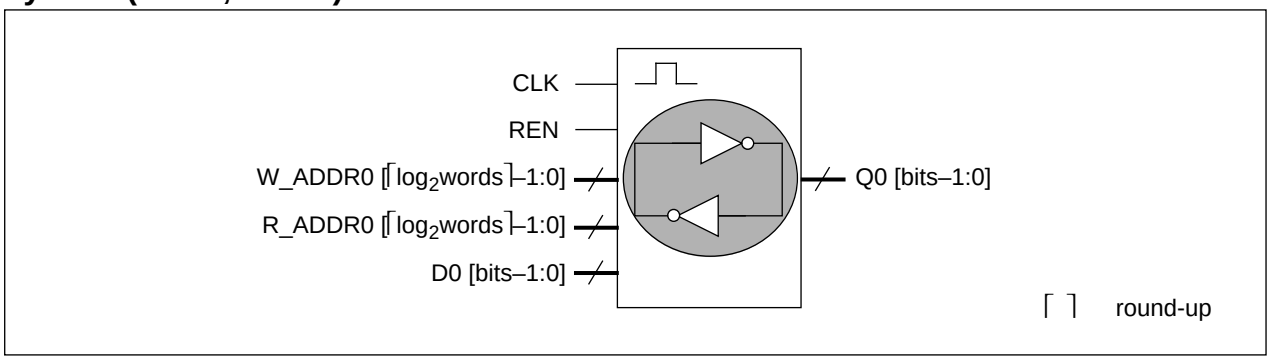
The Register File is optimized for multiple-targeted technologies. The Register File can be built with one to four read ports and with one to two write ports. The maximum number of words is 128 and there can be up to 128 bits per word.

Design Description

The Register File can be used as a stand-alone module or as part of a datapath block. To allow some flexibility, it allows you to place the control block to the right or left side of the register block.

All read and write ports are independent. The read ports always output data; data will be changed after the read address has been changed. The write ports are enabled by REN and data is latched into the memory location on the falling edge of the clock.

Symbol (1read, 1write)



Parameter Description

Parameter Name	Description	Range
words	Number of words in the Register File	8 to 128
bits	Number of bits per word	8 to 128
writes	Number of write ports	1/2
reads	Number of read ports	1/2/3/4
control	Where to place control with respect to memory	LEFT/RIGHT

Pin Description

Pin Name	I/O	Description
CLK (When # (write port) = 1.) CLK [1:0] (When # (write port) = 2.)	I	Clock signal (active-high) for each write port. When clock is high, data pass into the decoded memory location and is latched on the falling clock edge.
REN (When # (write port) = 1.) REN [1:0] (When # (write port) = 2.)		Register enable signal (active-low) for each write port. A high state prevents a write operation to the write port; a low state allows a write operation.
W_ADDR0 [$\lceil \log_2 words \rceil$–1:0]		Data input – Write address bus. There is one address bus for each write port and there can be from 1 to 2 write ports.
R_ADDR0 [$\lceil \log_2 words \rceil$–1:0]		Data input – Read address bus. There is one address bus for each read port and there can be from 1 to 4 read ports.
D0 <0>...D0 [bits–1:0]		Input – Word values written into the write port location during the write operation. There is one input bus for each write port.
Q0 <0>...Q0 [bits–1:0]	O	Output data previously written into the register file. Data are present at all times and the value depends on the read address. There is one output bus for each read port.

⌈ ⌉ round-up

Pin Capacitance

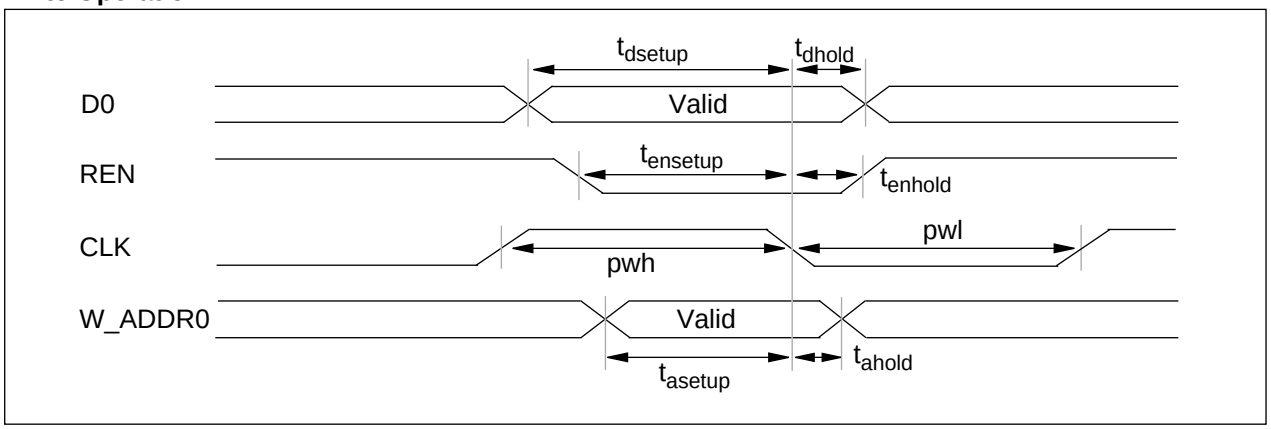
Word	Pin Name					
	CLK	D0	REN	R_ADDR0	R_ADDR1	W_ADDR0
8	0.183	0.035	0.067	0.034	0.034	0.035
16	0.265	0.035	0.067	0.034	0.034	0.035
24	0.347	0.035	0.067	0.034	0.034	0.035
32	0.405	0.035	0.067	0.034	0.034	0.035

Timing Parameters

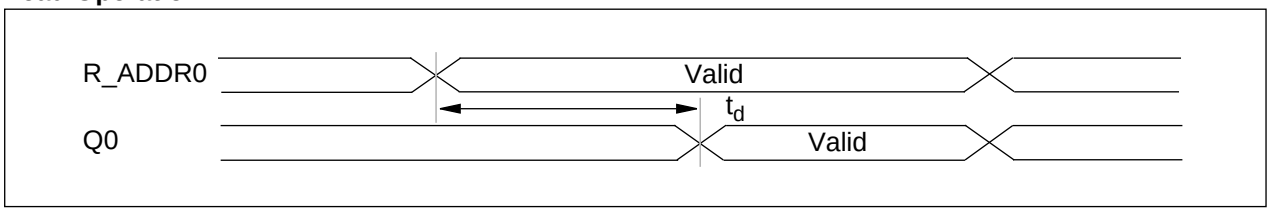
Symbol	Description	Input	Output
t_{dsetup}	Input data setup time	D0	–
t_{dhold}	Input data hold time	D0	–
$t_{ensetup}$	REN setup time	REN	–
t_{enhold}	REN hold time	REN	–
t_{asetup}	W_ADDR setup time	W_ADDR	–
t_{ahold}	W_ADDR hold time	W_ADDR	–
pwh	CLK pulse width high	CLK	–
pwl	CLK pulse width low	CLK	–
t_d	Read access time	R_ADDR	Q0

Timing Diagram

Write Operation



Read Operation



NOTE: Not allowed to read and write in the same location at the same time.

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Parameters: read = 1, write = 2, control = LEFT				
Words x Bit	**Area (μm x μm)**		**Delay (ns)**	
	Width	**Height**	**T_{PLH}**	**T_{PHL}**
8 x 8	237.6	343.2	2.612	2.312
8 x 16	448.8	343.2	2.712	2.422
8 x 24	660.0	343.2	2.802	2.522
8 x 32	871.2	343.2	2.892	2.632
16 x 8	237.6	549.9	3.032	2.762
16 x 16	448.8	549.9	3.122	2.872
16 x 24	660.0	549.9	3.212	2.972
16 x 32	871.2	549.9	3.302	3.082
24 x 8	237.6	740.5	3.231	3.001
24 x 16	448.8	740.5	3.321	3.111
24 x 24	660.0	740.5	3.411	3.211
24 x 32	871.2	740.5	3.501	3.312
32 x 8	237.6	924.1	3.522	3.341
32 x 16	448.8	924.1	3.621	3.442
32 x 24	660.0	924.1	3.711	3.551
32 x 32	871.2	924.1	3.801	3.652

Timing Requirements

Parameters: read = 1, write = 2, control = LEFT		
Words x Bit	**Timing Field**	**Value (ns)**
8 x 8	min_pulse_width_high CLK	0.609
	min_pulse_width_low CLK	0.634
	hold_rising D0 REN	0.151
	hold_falling D0 CLK	0.272
	hold_rising REN CLK	–0.656
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.511
	setup_falling D0 CLK	0.470
	setup_rising REN CLK	1.430
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000
8 x 16	min_pulse_width_high CLK	0.736
	min_pulse_width_low CLK	0.775
	hold_rising D0 REN	0.201
	hold_falling D0 CLK	0.324
	hold_rising REN CLK	–0.678
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.455
	setup_falling D0 CLK	0.411
	setup_rising REN CLK	1.430
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000
8 x 24	min_pulse_width_high CLK	0.864
	min_pulse_width_low CLK	0.916
	hold_rising D0 REN	0.251
	hold_falling D0 CLK	0.376
	hold_rising REN CLK	–0.699
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.401
	setup_falling D0 CLK	0.356
	setup_rising REN CLK	1.440
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000

Timing Requirements (Cont.)

Parameters: read = 1, write = 2, control = LEFT		
Words x Bit	**Timing Field**	**Value (ns)**
8 x 32	min_pulse_width_high CLK	0.991
	min_pulse_width_low CLK	1.060
	hold_rising D0 REN	0.301
	hold_falling D0 CLK	0.427
	hold_rising REN CLK	–0.720
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.351
	setup_falling D0 CLK	0.305
	setup_rising REN CLK	1.450
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000
16 x 8	min_pulse_width_high CLK	0.609
	min_pulse_width_low CLK	0.634
	hold_rising D0 REN	0.151
	hold_falling D0 CLK	0.272
	hold_rising REN CLK	–0.967
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.511
	setup_falling D0 CLK	0.470
	setup_rising REN CLK	1.710
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000
16 x 16	min_pulse_width_high CLK	0.736
	min_pulse_width_low CLK	0.775
	hold_rising D0 REN	0.201
	hold_falling D0 CLK	0.324
	hold_rising REN CLK	–0.988
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.455
	setup_falling D0 CLK	0.411
	setup_rising REN CLK	1.720
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000

Timing Requirements (Cont.)

Parameters: read = 1, write = 2, control = LEFT		
Words x Bit	**Timing Field**	**Value (ns)**
16 x 24	min_pulse_width_high CLK	0.864
	min_pulse_width_low CLK	0.916
	hold_rising D0 REN	0.251
	hold_falling D0 CLK	0.376
	hold_rising REN CLK	–1.010
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.401
	setup_falling D0 CLK	0.356
	setup_rising REN CLK	1.740
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000
16 x 32	min_pulse_width_high CLK	0.991
	min_pulse_width_low CLK	1.060
	hold_rising D0 REN	0.301
	hold_falling D0 CLK	0.427
	hold_rising REN CLK	–1.030
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.351
	setup_falling D0 CLK	0.305
	setup_rising REN CLK	1.760
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000
24 x 8	min_pulse_width_high CLK	0.609
	min_pulse_width_low CLK	0.634
	hold_rising D0 REN	0.151
	hold_falling D0 CLK	0.272
	hold_rising REN CLK	–1.280
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.511
	setup_falling D0 CLK	0.470
	setup_rising REN CLK	2.190
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000

Timing Requirements (Cont.)

Parameters: read = 1, write = 2, control = LEFT		
Words x Bit	**Timing Field**	**Value (ns)**
24 x 16	min_pulse_width_high CLK	0.736
	min_pulse_width_low CLK	0.775
	hold_rising D0 REN	0.201
	hold_falling D0 CLK	0.324
	hold_rising REN CLK	–1.300
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.455
	setup_falling D0 CLK	0.411
	setup_rising REN CLK	2.200
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000
24 x 24	min_pulse_width_high CLK	0.864
	min_pulse_width_low CLK	0.916
	hold_rising D0 REN	0.251
	hold_falling D0 CLK	0.376
	hold_rising REN CLK	–1.320
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.401
	setup_falling D0 CLK	0.356
	setup_rising REN CLK	2.220
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000
24 x 32	min_pulse_width_high CLK	0.991
	min_pulse_width_low CLK	1.060
	hold_rising D0 REN	0.301
	hold_falling D0 CLK	0.427
	hold_rising REN CLK	–1.340
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.351
	setup_falling D0 CLK	0.305
	setup_rising REN CLK	2.240
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000

Timing Requirements (Cont.)

Parameters: read = 1, write = 2, control = LEFT		
Wordsx Bit	**Timing Field**	**Value (ns)**
32 x 8	min_pulse_width_high CLK	0.609
	min_pulse_width_low CLK	0.634
	hold_rising D0 REN	0.151
	hold_falling D0 CLK	0.272
	hold_rising REN CLK	–1.590
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.511
	setup_falling D0 CLK	0.470
	setup_rising REN CLK	2.660
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000
32 x 16	min_pulse_width_high CLK	0.736
	min_pulse_width_low CLK	0.775
	hold_rising D0 REN	0.201
	hold_falling D0 CLK	0.324
	hold_rising REN CLK	–1.610
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.455
	setup_falling D0 CLK	0.411
	setup_rising REN CLK	2.680
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000
32 x 24	min_pulse_width_high CLK	0.864
	min_pulse_width_low CLK	0.916
	hold_rising D0 REN	0.251
	hold_falling D0 CLK	0.376
	hold_rising REN CLK	–1.630
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.401
	setup_falling D0 CLK	0.356
	setup_rising REN CLK	2.700
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000

Timing Requirements (Cont.)

Parameters: read = 1, write = 2, control = LEFT		
Words x Bit	**Timing Field**	**Value (ns)**
32 x 32	min_pulse_width_high CLK	0.991
	min_pulse_width_low CLK	1.060
	hold_rising D0 REN	0.301
	hold_falling D0 CLK	0.427
	hold_rising REN CLK	–1.650
	hold_falling REN CLK	0.000
	hold_falling W_ADDR0 CLK	0.000
	setup_rising D0 REN	0.351
	setup_falling D0 CLK	0.305
	setup_rising REN CLK	2.720
	setup_falling REN CLK	1.000
	setup_falling W_ADDR0 CLK	1.000

Features

- Functional model, test vector, schematic, and layout generators
- Timing model with auto-characterization
- High performance saturation scheme
- Two's complement overflow flag
- *n*-bit (4 to 128) Saturating Adder
- Three drive strength options for output

General Description

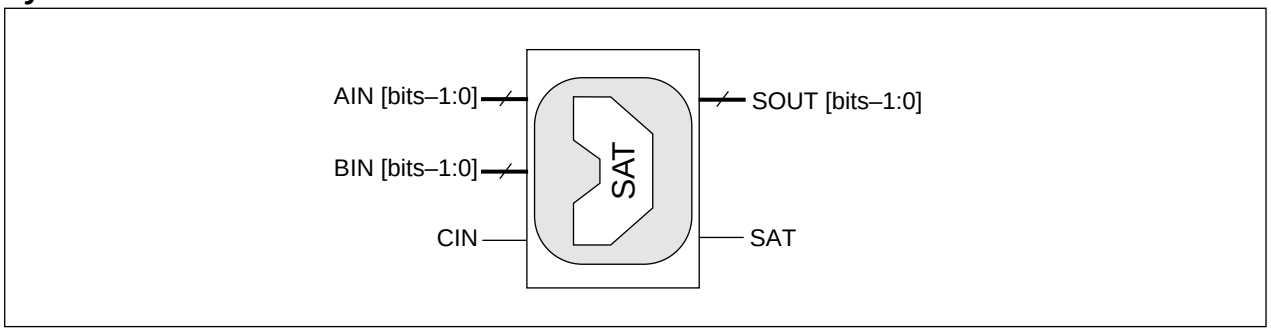
The Saturating Adder builds an *n*-bit wide adder schematic that is used to drive the datapath place and route tool in combination with technology-specific layout leaf cells. The saturate flag saturates the output to the largest positive number on an overflow or to the smallest negative number on an underflow.

Design Description

The Saturating Adder performs addition functions. An *n*-bit wide operand (AIN), an *n*-bit wide operand (BIN), a 1-bit wide input carry signal (CIN), and an *n*-bit wide output bus (SOUT) and a 1-bit saturation flag (SAT) serve as the I/O signals to the module.

The Saturating Adder can be built with two different carry chains allowing speed/area trade-offs. The ripple carry chain is high in density, with lower performance. The carry-bypass chain has a unique grouping of bits which creates a high performance design. This scheme is preferable for the addition of large data words to attain high speed.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
nopass	0: group bypass; 1: ripple adder	0/1
drv	Drive strength	1/2/4

Saturating Adder

Function Table

Type	Function

SOUT	AIN + BIN + CIN
	If (AIN and BIN have positive values, and SAT output becomes 1),
	then SOUT [bits–2:0] = 1, SOUT [bits–1] = 0.
	If (AIN and BIN have negative values, and SAT output becomes 1),
	then SOUT [bits–2:0] = 0, SOUT [bits–1] = 1.

SAT	If the result of two positive numbers addition is negative value or the result of two negative numbers addition is positive, then SAT is “1.”

Truth Table

Inputs			Outputs	
AIN	**BIN**	**CIN**	**SOUT**	**SAT**
0	0	0	0	0
0	0	0	1	1
0	1	0	0	0
1	1	0	1	0
0	0	1	1	0
1	0	1	0	0
0	1	1	0	1
1	1	1	1	0

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Data input
BIN [bits–1:0]		Data input
CIN		Carry-in
SAT	O	Saturate flag
SOUT		Output result of addition

Pin Capacitance

Pin Name	Value (pF)
AIN	0.052
BIN	0.042
CIN	0.102

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: nopass = 0, drv = 1					
Bit	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)**
	Width	**Height**	**T_{PLH}**	**T_{PHL}**	
8	266.4	134.9	4.238	3.802	0.228
16	477.6	135.1	4.798	4.352	0.436
24	688.8	138.2	5.158	4.702	0.623
32	900.0	137.4	5.568	5.102	0.824

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Fast datapath zero flag
- *n*-bit (4 to 128) zero Detector
- Three drive strength options for output

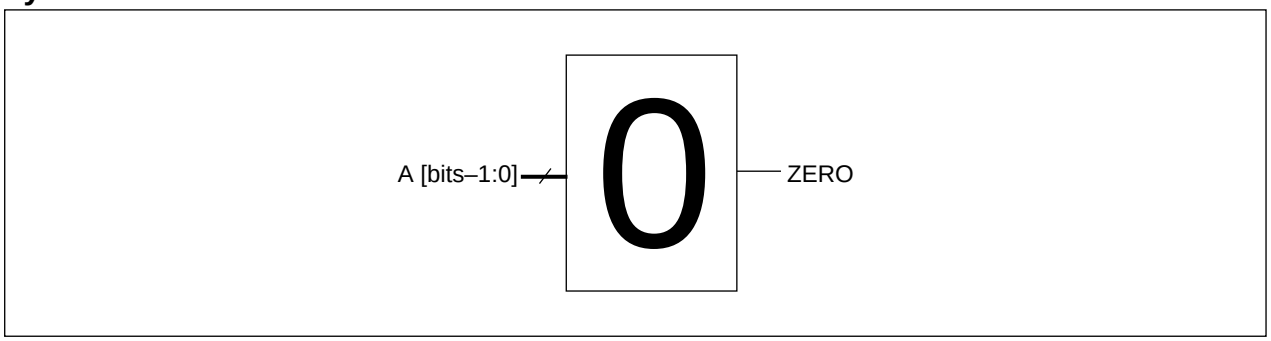
General Description

The Zero Detector builds an *n*-bit wide schematic that is used to drive the datapath placement and routing tool in combination with technology-specific layout leaf cells. The Zero Detector detects “1” in the inputs and if there is no “1”, it sets ZERO to “1.”

Design Description

The Zero Detector performs deciding whether the input is zero or not. An *n*-bit wide operand (AIN) and a 1-bit wide zero flag (ZERO) serve as the I/O signals to the module. The Zero Detector can be built with simple OR gates.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
drv	Drive strength	1/2/4

Zero Detector

Truth Table

A	ZERO
All 0	1
Any 1	0

Pin Description

Pin Name	I/O	Description
A [bits–1:0]	I	Data input
ZERO	O	It specifies whether all the bits in the input A are 0 or 1.

Pin Capacitance

Pin Name	Value (pF)
A	0.024

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF, f = 10MHz)

Parameters: drv = 1					
Bit	**Area (μm x μm)**		**Delay (ns)**		**Current (mA)fs**
	Width	**Height**	**T_{PLH}**	**T_{PHL}**	
8	213.3	59.6	1.728	0.933	0.021
16	424.5	61.6	1.962	1.118	0.024
24	662.0	65.1	2.202	1.285	0.048
32	846.9	68.4	2.202	1.302	0.047

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for types 21 and 22
- Two drive strength options for output

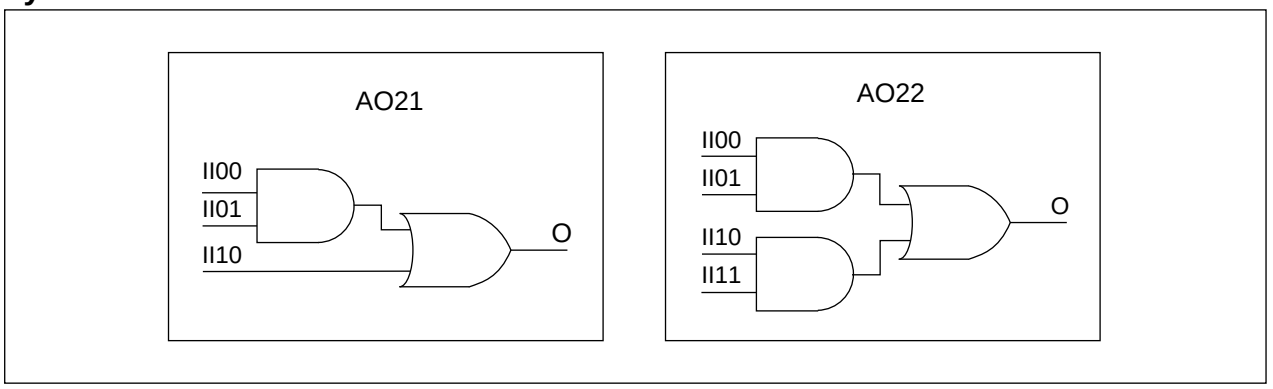
General Description

The high performance datapath AND-OR design can be optimized for multiple-targeted technologies. The generator can build AND-OR gates ranging from 4-bits to 128-bits for two different configurations (21 and 22) and two different drive strengths.

Design Description

The AND-OR design has schematic and layout generators that can build a variety of AND-OR gates. You have an option to build the different kinds of structure configurations by setting the “type” parameter to 21/22 depending on your application.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Configuration type	21/22
drv	Drive strength	1/2

Truth Table

AO21			
Inputs			Output
II00	II01	II10	O
x	x	1	1
x	0	0	0
0	x	0	0
1	1	0	1

AO22				
Inputs				Output
II00	II01	II10	II11	O
x	0	x	0	0
0	x	x	0	0
x	0	0	x	0
0	x	0	x	0
1	1	x	x	1
x	x	1	1	1

Pin Description

AO22		
Pin Name	I/O	Description
II00 [bits–1:0]	I	Data input
II01 [bits–1:0]		Data input
II10 [bits–1:0]		Data input
II11 [bits–1:0]		Data input
O	O	Data output

Pin Capacitance

AO21	
Pin Name	Value (pF)
II10	0.024
II01	0.025
II00	0.025

AO22	
Pin Name	Value (pF)
II11	0.024
II10	0.024
II01	0.025
II00	0.025

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	Bit	Area (μm x μm)		Delay (ns)	
		Width	Height	T_{PLH}	T_{PHL}
AO21	8/16/24/32	26.4 x bits	54.7	0.946	0.959
AO22	8/16/24/32	26.4 x bits	54.7	1.056	0.909

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for types 21 and 22
- Two drive strength options for output

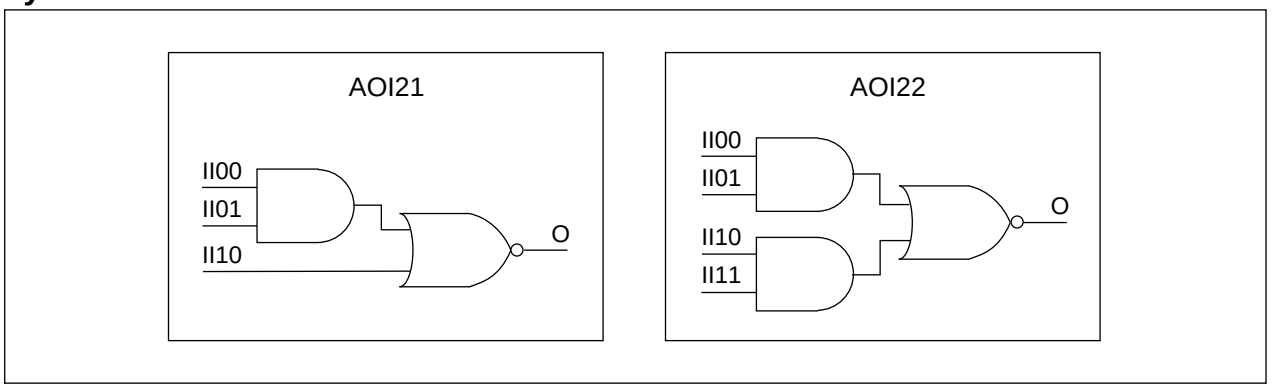
General Description

The high performance datapath AND-OR-INVERT design can be optimized for multiple-targeted technologies. The generator can build AND-OR-INVERT gates ranging from 4-bits to 128-bits for two different configurations (21 and 22) and two different drive strengths.

Design Description

The AND-OR-INVERT design has schematic and layout generators that can build a variety of AND-OR-INVERT gates. You have an option to build the different kinds of AND-OR-INVERT structure configurations by setting the “type” parameter to 21/22 depending on your application.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Configuration type	21/22
drv	Drive strength	1/2

Truth Table

AOI21			
Inputs			Output
II00	II01	II10	O
x	x	1	0
x	0	0	1
0	x	0	1
1	1	0	0

AOI22				
Inputs				Output
II00	II01	II10	II11	O
x	0	x	0	1
0	x	x	0	1
x	0	0	x	1
0	x	0	x	1
1	1	x	x	0
x	x	1	1	0

Pin Description

AOI22		
Pin Name	I/O	Description
II00 [bits–1:0]	I	Data input
II01 [bits–1:0]		Data input
II10 [bits–1:0]		Data input
II11 [bits–1:0]		Data input
O	O	Data output

Pin Capacitance

AOI21	
Pin Name	Value (pF)
II10	0.024
II01	0.025
II00	0.025

AOI22	
Pin Name	Value (pF)
II11	0.025
II10	0.025
II01	0.026
II00	0.025

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	Bit	Area (μm x μm)		Delay (ns)	
		Width	Height	T_{PLH}	T_{PHL}
AOI21	8/16/24/32	26.4 x bits	54.5	1.381	0.664
AOI22	8/16/24/32	26.4 x bits	58.4	1.351	0.788

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for Buffer/Inverter design
- Four drive strength options for output

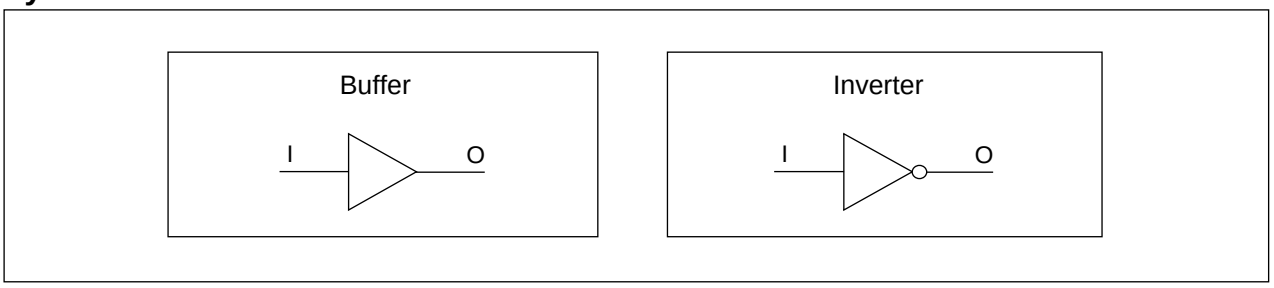
General Description

The high performance Buffer/Inverter design is optimized for multiple-targeted technologies. The generator design has the capability to build Buffers/Inverters ranging from 4-bits to 128-bits for various drive strength configurations.

Design Description

The Buffer/Inverter design has schematic and layout generators that can build a variety of Buffers and Inverters. You have an option to select either Buffer or Inverter by setting the “type” parameter to 1 or 0 respectively. The design supports four different drive strength options (1X, 2X, 4X and 8X).

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Type of a cell to be generated; 0: Inverter; 1: Buffer	0/1
drv	Drive strength	1/2/4/8

Buffer/Inverter

Truth Table

Buffer	
I	**O**
0	0
1	1

Inverter	
I	**O**
0	1
1	0

Pin Description

Pin Name	Description
I [bits–1:0]	Input
O [bits–1:0]	Output

Pin Capacitance

Pin Name	Value (pF)	
	Buffer	**Inverter**
I	0.024	0.033

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	Bit	Area (μm x μm)		Delay (ns)	
		Width	**Height**	T_{PLH}	T_{PHL}
Buffer	8/16/24/32	26.4 x bits	55.7	0.851	0.712
Inverter	8/16/24/32	26.4 x bits	53.6	1.001	0.447

Features

- Variable word width of 4 to 128 bits

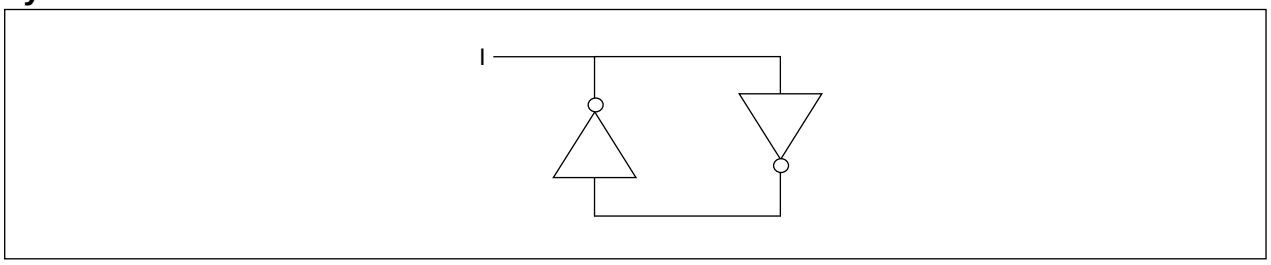
General Description

The high performance datapath Bus Holder design can be optimized for multiple-targeted technologies. The generator can build Bus Holders ranging from 4-bits to 128-bits.

Design Description

The Bus Holder design has schematic and layout generators that can build a variety of Bus Holders. The primary function of the Bus Holder is to hold the previous state, when the drivers on a bus go tri-stated.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128

Pin Description

Pin Name	Description
I [bits–1:0]	Data input

Pin Capacitance

Pin Name	Value (pF)
I	0.072

D Flip-Flop

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Separate load enable line
- Scan logic, set, reset and tri-stated output with enable high input options
- Clock edge specification option
- Tri-stated, normal and inverted outputs
- Two drive strength options for output

General Description

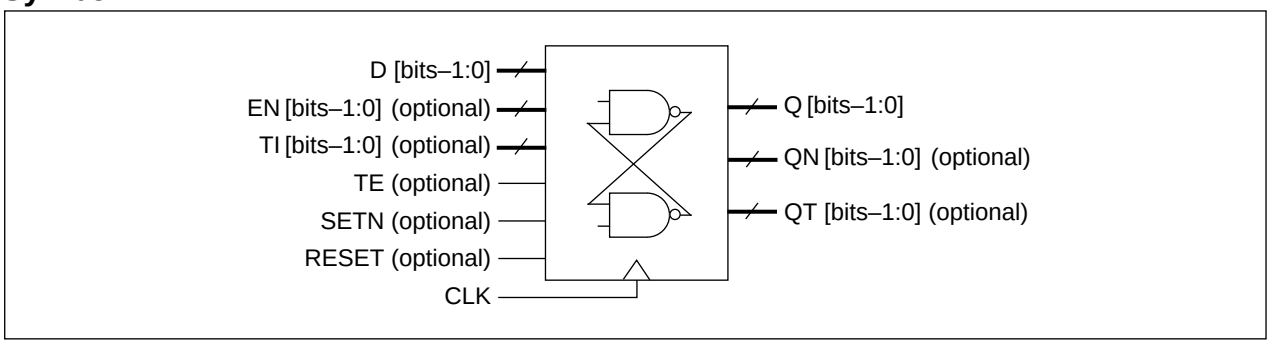
The high performance D Flip-Flop design can be optimized for multiple-targeted technologies. The generator can build D flip-flops ranging from 4-bits to 128-bits, with scan logic, set, reset and tri-stated output with enable high input options. The clock edge specification can also be controlled by users, either positive or negative edged. This generator supports a tri-state output and two different drive strengths.

Design Description

The D Flip-Flop design has schematic and layout generators that can build a variety of D flip-flops depending on the parameters set. The design supports scan inputs with test enable input. You can also have set, reset input along with the scan inputs, and tri-stated output with enable high input.

The clock edge can be specified by setting the clk parameter to 0 or 1 (negative clk or positive clk respectively). Both Q (normal data out), QN (inverted data out) and QT (tri-state data output) are available.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
scan	Scan inputs – 0: no scan; 1: scan	0/1
set	Set – 0: no; 1: set	0/1
rst	Reset – 0: no; 1: reset	0/1
tri	Tri-stated output with enable high input	0/1
q	Normal data output	0/1
qn	Inverted data output	0/1
clk	Clock edge spec. – 0: negative clk; 1: positive clk	0/1
drv	Drive strength	1/4

Truth Table

Positive edge trigger (clk = 1)									
Inputs							Outputs		
D	CLK	EN	SETN	RESET	TI	TE	Q (n+1)	QN (n+1)	QT (n+1)
x	x	0	x	x	x	x	x	x	Hi-Z
x	x	1	0	0	x	x	1	0	1
x	x	1	0	1	x	x	1	0	1
x	x	1	1	1	x	x	0	1	0
D	↓	1	1	0	x	0	Q (n)	QN (n)	QT (n)
D	↑	1	1	0	x	0	D	~D	D
x	↓	1	1	0	D	1	Q (n)	QN (n)	QT (n)
x	↑	1	1	0	D	1	D	~D	D

Negative edge trigger (clk = 0)									
Inputs							Outputs		
D	CLK	EN	SETN	RESET	TI	TE	Q (n+1)	QN (n+1)	QT (n+1)
x	x	0	x	x	x	x	x	x	Hi-Z
x	x	1	0	0	x	x	1	0	1
x	x	1	0	1	x	x	1	0	1
x	x	1	1	1	x	x	0	1	0
D	↑	1	1	0	x	0	Q (n)	QN (n)	QT (n)
D	↓	1	1	0	x	0	D	~D	D
x	↑	1	1	0	D	1	Q (n)	QN (n)	QT (n)
x	↓	1	1	0	D	1	D	~D	D

Pin Description

Pin Name	I/O	Description
D [bits–1:0]	I	Data input
EN [bits–1:0]		Enable input (optional when tri = 1)
TI [bits–1:0]		Test input (optional when scan = 1)
TE		Test enable input (optional when scan = 1)
SETN		Set input (optional when set = 1)
RESET		Reset input (optional when rst = 1)
CLK		Clock input (positive- or negative-edge)
Q [bits–1:0]	O	Normal data output
QN [bits–1:0]		Inverted data output (optional when qn = 1)
QT [bits–1:0]		Tri-stated data output (optional when tri = 1)

Pin Capacitance

Pin Name	Bit	Value (pF)
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan = 0, clk = 0, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
(Parameters: qn = 1, q = 1, tri = 0, rst = 0, set = 0, scan = 0, clk = 0, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 0, clk = 0, drv = 1)		
CLK	8	0.288
	16	0.576
	24	0.864
	32	1.152
D	8/16/24/32	0.033
EN	8/16/24/32	0.024
QT	8/16/24/32	0.028
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 0, scan = 0, clk = 0, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
RESET	8	0.448
	16	0.896
	24	1.344
	32	1.792

Pin Name	Bit	Value (pF)
(Parameters: qn = 0, q = 1, tri = 1, rst =1, set = 0, scan = 0, clk = 0, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
EN	8/16/24/32	0.023
RESET	8	0.432
	16	0.864
	24	1.296
	32	1.728
QT	8/16/24/32	0.029
(Parameters: qn = 0, q = 1, tri = 0, rst = 1, set = 1, scan = 0, clk = 0, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
RESET	8	0.456
	16	0.912
	24	1.368
	32	1.824
SETN	8	0.440
	16	0.880
	24	1.320
	32	1.760

Pin Capacitance (Cont.)

Pin Name	Bit	Value (pF)
(Parameters: qn = 1, q = 1, tri = 0, rst =1, set = 1, scan = 0, clk = 0, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
RESET	8	0.456
	16	0.912
	24	1.368
	32	1.824
SETN	8	0.448
	16	0.896
	24	1.344
	32	1.792
(Parameters: qn = 0, q = 1, tri = 1, rst =1, set = 1, scan = 0, clk = 0, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
EN	8/16/24/32	0.024
RESET	8	0.448
	16	0.896
	24	1.344
	32	1.792
SETN	8	0.432
	16	0.864
	24	1.296
	32	1.728
QT	8/16/24/32	0.029

Pin Name	Bit	Value (pF)
(Parameters: qn = 0, q = 1, tri = 1, rst =1, set = 1, scan = 1, clk = 0, drv = 1)		
CLK	8	0.264
	16	0.528
	24	0.792
	32	1.056
D	8/16/24/32	0.049
EN	8/16/24/32	0.023
TE	8	0.192
	16	0.384
	24	0.576
	32	0.768
TI	8/16/24/32	0.050
QT	8/16/24/32	0.028
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 1, clk = 0, drv = 1)		
CLK	8	0.264
	16	0.528
	24	0.792
	32	1.056
D	8/16/24/32	0.051
EN	8/16/24/32	0.023
RESET	8	0.416
	16	0.832
	24	1.248
	32	1.664
SETN	8	0.408
	16	0.816
	24	1.224
	32	1.632
TE	8	0.200
	16	0.400
	24	0.600
	32	0.800
TI	8/16/24/32	0.050
QT	8/16/24/32	0.029

Pin Capacitance (Cont.)

Pin Name	Bit	Value (pF)
(Parameters: qn = 1, q = 1, tri = 0, rst =0, set = 0, scan = 0, clk = 1, drv = 1)		
CLK	8	0.272
	16	0.544
	24	0.816
	32	1.088
D	8/16/24/32	0.033
(Parameters: qn = 0, q = 1, tri = 1, rst =0, set = 0, scan = 0, clk = 1, drv = 1)		
CLK	8	0.272
	16	0.544
	24	0.816
	32	1.088
D	8/16/24/32	0.033
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 0, clk = 1, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
EN	8/16/24/32	0.024
QT	8/16/24/32	0.028
(Parameters: qn = 1, q = 1, tri = 0, rst 01, set = 0, scan = 0, clk = 1, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
RESET	8	0.424
	16	0.848
	24	1.272
	32	1.696

Pin Name	Bit	Value (pF)
(Parameters: qn = 0, q = 1, tri = 1, rst =1, set = 0, scan = 0, clk = 1, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
EN	8/16/24/32	0.024
RESET	8	0.416
	16	0.832
	24	1.248
	32	1.664
QT	8/16/24/32	0.029
(Parameters: qn = 1, q = 1, tri = 0, rst =1, set = 1, scan = 0, clk = 1, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
RESET	8	0.432
	16	0.864
	24	1.296
	32	1.728
SETN	8	0.432
	16	0.864
	24	1.296
	32	1.728

Pin Capacitance (Cont.)

Pin Name	Bit	Value (pF)
(Parameters: qn = 0, q = 1, tri = 0, rst = 1, set = 1, scan = 0, clk = 1, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
RESET	8	0.448
	16	0.896
	24	1.344
	32	1.792
SETN	8	0.432
	16	0.864
	24	1.296
	32	1.728
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 0, clk = 1, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
EN	8/16/24/32	0.024
RESET	8	0.432
	16	0.864
	24	1.296
	32	1.728
SETN	8	0.432
	16	0.864
	24	1.296
	32	1.728
QT	8/16/24/32	0.029

Pin Name	Bit	Value (pF)
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 1, clk = 1, drv = 1)		
CLK	8	0.272
	16	0.544
	24	0.816
	32	1.088
D	8/16/24/32	0.055
EN	8/16/24/32	0.024
TE	8	0.208
	16	0.416
	24	0.624
	32	0.832
TI	8/16/24/32	0.025
QT	8/16/24/32	0.028
(Parameters: qn = 0, q = 1, tri = 1, rst =1, set = 1, scan = 1, clk = 1, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.055
EN	8/16/24/32	0.024
RESET	8	0.440
	16	0.880
	24	1.320
	32	1.760
SETN	8	0.432
	16	0.864
	24	1.296
	32	1.728
TE	8	0.208
	16	0.416
	24	0.624
	32	0.832
TI	8/16/24/32	0.025
QT	8/16/24/32	0.029

D Flip-Flop

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Parameters		Value
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan = 0, clk = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	73.6
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_low CLK	0.300
		hold_falling D CLK	0.300
		setup_falling D CLK	0.600
		T_{PLH}	1.413
		T_{PHL}	1.168
(Parameters: qn = 1, q = 1, tri = 0, rst = 0, set = 0, scan = 0, clk = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	77.8
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_low CLK	0.300
		hold_falling D CLK	0.300
		setup_falling D CLK	0.600
		T_{PLH}	1.477
		T_{PHL}	1.216
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 0, clk = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	88.3
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_low CLK	0.300
		hold_falling D CLK	0.300
		setup_falling D CLK	0.600
		T_{PLH}	2.249
		T_{PHL}	1.450
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 0, scan = 0, clk = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	84.1
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_high RESET	0.300
		min_pulse_width_low CLK	0.300
		hold_falling D CLK	0.300
		setup_falling D CLK	0.600
		T_{PLH}	1.573
		T_{PHL}	1.206

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Parameters		Value
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 0, scan = 0, clk = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	92.5
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_high RESET	0.300
		min_pulse_width_low CLK	0.300
		hold_falling D CLK	0.300
		setup_falling D CLK	0.600
		T_{PLH}	2.343
		T_{PHL}	1.440
(Parameters: qn = 0, q = 1, tri = 0, rst = 1, set = 1, scan = 0, clk = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	79.9
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_low CLK	0.300
		min_pulse_width_high RESET	0.300
		min_pulse_width_low SETN	0.300
		hold_falling D CLK	0.300
		setup_falling D CLK	0.600
		T_{PLH}	1.499
		T_{PHL}	1.222
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 1, scan = 0, clk = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	84.1
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_low CLK	0.300
		min_pulse_width_high RESET	0.300
		min_pulse_width_low SETN	0.300
		hold_falling D CLK	0.300
		setup_falling D CLK	0.600
		T_{PLH}	1.569
		T_{PH}	1.272

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Parameters		Value
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 0, clk = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	92.5
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_low CLK	0.300
		min_pulse_width_high RESET	0.300
		min_pulse_width_low SETN	0.300
		hold_falling D CLK	0.200
		setup_falling D CLK	0.600
		T_{PLH}	2.339
		T_{PHL}	1.500
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 1, clk = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	94.6
	Delay (ns)	min_pulse_width_high CLK	0.250
		min_pulse_width_low CLK	0.300
		hold_falling D CLK	0.200
		hold_falling TI CLK	0.200
		setup_falling D CLK	0.700
		setup_falling TI CLK	0.700
		T_{PLH}	2.249
		T_{PHL}	1.435
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 1, clk = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	100.5
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_low CLK	0.300
		min_pulse_width_high RESET	0.300
		min_pulse_width_low SETN	0.300
		hold_falling D CLK	0.200
		hold_falling TI CLK	0.200
		setup_falling D CLK	0.700
		setup_falling TI CLK	0.700
		T_{PLH}	2.339
		T_{PHL}	1.490

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Parameters		Value
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan = 0, clk = 1, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	73.6
	Delay (ns)	min_pulse_width_high CLK	0.250
		min_pulse_width_low CLK	0.300
		hold_falling D CLK	–0.100
		setup_falling D CLK	0.600
		T_{PLH}	1.293
		T_{PHL}	0.882
(Parameters: qn = 1, q = 1, tri = 0, rst = 0, set = 0, scan = 0, clk = 1, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	77.8
	Delay (ns)	min_pulse_width_high CLK	0.250
		min_pulse_width_low CLK	0.300
		hold_falling D CLK	–0.100
		setup_falling D CLK	0.600
		T_{PLH}	1.329
		T_{PHL}	0.922
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 0, clk = 1, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	88.3
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_low CLK	0.300
		hold_falling D CLK	–0.100
		setup_falling D CLK	0.600
		T_{PLH}	2.119
		T_{PHL}	1.150
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 0, scan = 0, clk = 1, drv 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	84.1
	Delay (ns)	min_pulse_width_high CLK	0.250
		min_pulse_width_low CLK	0.300
		min_pulse_width_high RESET	0.250
		hold_falling D CLK	–0.100
		setup_falling D CLK	0.600
		T_{PLH}	1.429
		T_{PHL}	0.935

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Parameters		Value
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 0, scan = 0, clk = 1, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	92.5
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_low CLK	0.300
		min_pulse_width_high RESET	0.300
		hold_falling D CLK	–0.100
		setup_falling D CLK	0.600
		T_{PLH}	2.203
		T_{PHL}	1.150
(Parameters: qn = 0, q = 1, tri = 0, rst = 1, set = 1, scan =0, clk = 1, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	79.9
	Delay (ns)	min_pulse_width_high CLK	0.250
		min_pulse_width_low CLK	0.300
		min_pulse_width_high RESET	0.250
		min_pulse_width_low SETN	0.300
		hold_falling D CLK	–0.100
		setup_falling D CLK	0.600
		T_{PLH}	1.379
		T_{PHL}	0.928
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 1, scan = 0, clk = 1, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	84.1
	Delay (ns)	min_pulse_width_high CLK	0.250
		min_pulse_width_low CLK	0.300
		min_pulse_width_high RESET	0.250
		min_pulse_width_low SETN	0.300
		hold_rising D CLK	–0.100
		T_{PLH}	1.445
		T_{PHL}	0.972

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Parameters		Value
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 0, clk = 1, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	92.5
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_low CLK	0.300
		min_pulse_width_high RESET	0.300
		min_pulse_width_low SETN	0.300
		hold_rising D CLK	–0.100
		setup_rising D CLK	0.600
		T_{PLH}	2.223
		T_{PHL}	1.204
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 1, clk = 1, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	94.6
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_low CLK	0.300
		hold_falling D CLK	–0.100
		hold_rising TI CLK	–0.100
		setup_rising D CLK	0.700
		setup_falling TI CLK	0.700
		T_{PLH}	2.119
		T_{PHL}	1.145
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 1, clk = 1, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	100.5
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_low CLK	0.300
		min_pulse_width_high RESET	0.300
		min_pulse_width_low SETN	0.300
		hold_falling D CLK	–0.100
		hold_rising TI CLK	–0.100
		setup_rising D CLK	0.700
		setup_falling TI CLK	0.700
		T_{PLH}	2.213
		T_{PHL}	1.200

Full Adder

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Two drive strength options for output

General Description

The high performance datapath Full Adder design can be optimized for multiple-targeted technologies. This generator can build Full Adders ranging from 4-bits to 128-bits, supporting two different drive strengths.

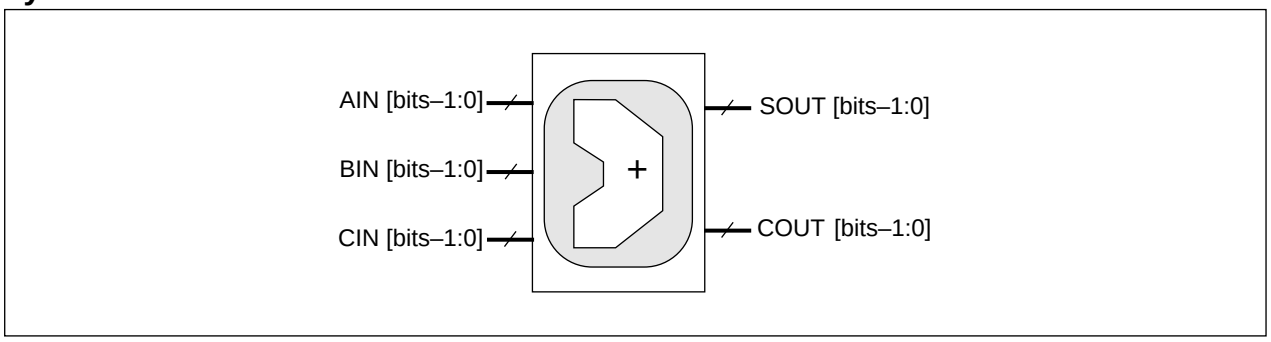
Design Description

The Full Adder design has schematic and layout generators that can build a variety of Full Adders. The design supports two different drive strengths (1X and 2X).

The sum output is expressed as: **SOUT = AIN ⊕ BIN ⊕ CIN**

The carry output is expressed as: **COUT = {(AIN | BIN) & CIN} | (AIN & BIN)**

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
drv	Drive strength	1/2

Truth Table

Inputs			Outputs	
AIN	**BIN**	**CIN**	**SOUT**	**COUT**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Pin Description

Pin Name	I/O	Description
AIN [bits–1:0]	I	Input AIN
BIN [bits–1:0]		Input BIN
CIN [bits–1:0]		Carry-in CIN
SOUT [bits–1:0]	O	Sum output
COUT [bits–1:0]		Carry output

Pin Capacitance

Pin Name	Value (pF)
AIN	0.060
BIN	0.072
CIN	0.071

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Area (μm x μm)		Delay (ns)	
	Width	**Height**	T_{PLH}	T_{PHL}
8/16/24/32	26.4 x bits	75.7	1.443	1.045

Latch

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Separate load enable line
- Scan logic, set, reset and tri-stated output with enable high input options
- Tri-stated, normal and inverted output
- Two drive strength options for output

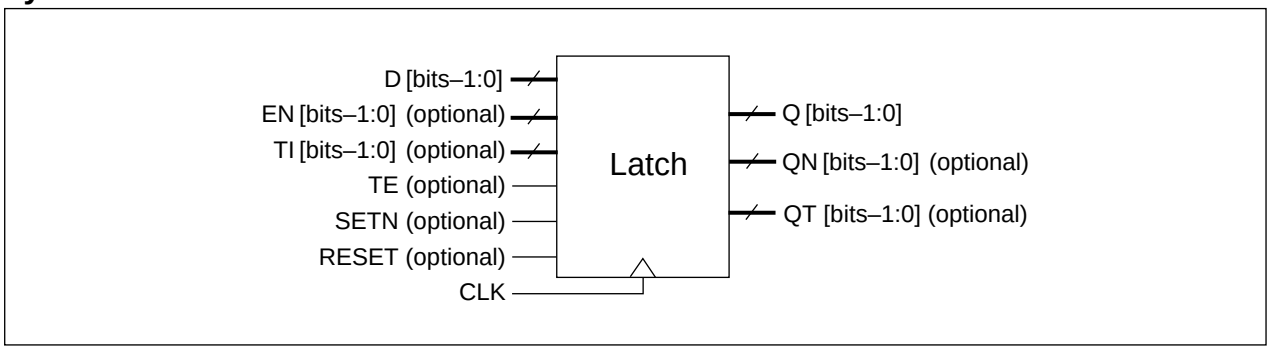
General Description

The high performance Latch design can be optimized for multiple-targeted technologies. The generator can build Latches ranging from 4-bits to 128-bits, with scan logic and set, reset and tri-stated output with enable high input options.This generator supports two different drive strengths.

Design Description

The Latch design has schematic and layout generators that can build a variety of Latches depending on the parameters set. The design supports scan inputs with test enable input. You can also have set or reset input, and tri-stated output with enable high input.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
scan	Scan inputs – 0: no scan; 1: scan	0/1
set	Set – 0: no; 1: set	0/1
rst	Reset – 0: no; 1: reset	0/1
tri	Tri-stated output with enable high input	0/1
q	Normal data output	0/1
qn	Inverted data output	0/1
drv	Drive strength	1/4

Truth Table

Inputs							Outputs		
D	CLK	EN	SETN	RESET	TI	TE	Q (n+1)	QN (n+1)	QT (n+1)
x	x	0	x	x	x	x	x	x	HI-Z
x	x	1	0	0	x	x	1	0	1
x	x	1	0	1	x	x	1	0	1
x	x	1	1	1	x	x	0	1	0
D	0	1	1	0	x	0	Q (n)	QN (n)	QT (n)
D	1	1	1	0	x	0	D	~D	D
x	0	1	1	0	D	1	Q (n)	QN (n)	QT (n)
x	1	1	1	0	D	1	D	~D	D

Pin Description

Pin Name	I/O	Description
D [bits–1:0]	I	Data input
EN [bits–1:0]		Enable input (optional when tri = 1)
TI [bits–1:0]		Test input (optional when scan = 1)
TE		Test enable input (optional when scan = 1)
SETN		Set input (optional when set = 1)
RESET		Reset input (optional when rst = 1)
CLK		Clock input
Q [bits–1:0]	O	Normal data output
QN [bits–1:0]		Inverted data output (optional when qn = 1)
QT [bits–1:0]		Tri-stated data output (optional when tri = 1)

Pin Capacitance

Pin Name	Bit	Value (pF)
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan = 0, drv = 1)		
CLK	8	0.272
	16	0.544
	24	0.816
	32	1.088
D	8/16/24/32	0.033
(Parameters: qn = 1, q = 1, tri = 0, rst =0, set = 0, scan = 0, drv = 1)		
CLK	8	0.272
	16	0.544
	24	0.816
	32	1.088
D	8/16/24/32	0.033

Pin Name	Bit	Value (pF)
(Parameters: qn = 0, q = 0, tri = 1, rst =0, set = 0, scan = 0, drv = 1)		
CLK	8	0.272
	16	0.544
	24	0.816
	32	1.088
D	8/16/24/32	0.033
EN	8/16/24/32	0.024
QT	8/16/24/32	0.030

Pin Capacitance (Cont.)

Pin Name	Bit	Value (pF)
(Parameters: qn = 0, q = 1, tri = 1, rst =0, set = 0, scan = 0, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.034
EN	8/16/24/32	0.024
QT	8/16/24/32	0.030
(Parameters: qn = 0, q = 1, tri = 0, rst = 1, set = 0, scan = 0, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
RESET	8	0.264
	16	0.528
	24	0.792
	32	1.056
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 0, scan = 0, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.034
RESET	8	0.264
	16	0.528
	24	0.792
	32	1.056

Pin Name	Bit	Value (pF)
(Parameters: qn = 0, q = 0, tri = 1, rst = 1, set = 0, scan = 0, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
EN	8/16/24/32	0.024
RESET	8	0.264
	16	0.528
	24	0.792
	32	1.056
QT	8/16/24/32	0.030
(Parameters: qn = 0, q = 1, tri =1, rst =1, set = 0, scan = 0, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.033
EN	8/16/24/32	0.024
RESET	8	0.272
	16	0.544
	24	0.816
	32	1.088
QT	8/16/24/32	0.030

Pin Capacitance (Cont.)

Pin Name	Bit	Value (pF)
(Parameters: qn = 0, q = 1, tri =1, rst =1, set = 1, scan = 0, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.034
EN	8/16/24/32	0.024
RESET	8	0.272
	16	0.544
	24	0.816
	32	1.088
SETN	8	0.264
	16	0.528
	24	0.792
	32	1.056
QT	8/16/24/32	0.029
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan = 1, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.055
TE	8	0.200
	16	0.400
	24	0.600
	32	0.800
TI	8/16/24/32	0.056

Pin Name	Bit	Value (pF)
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 1, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.055
EN	8/16/24/32	0.024
TE	8	0.248
	16	0.496
	24	0.744
	32	0.992
TI	8/16/24/32	0.055
QT	8/16/24/32	0.031
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan = 1, drv = 1)		
CLK	8	0.280
	16	0.560
	24	0.840
	32	1.120
D	8/16/24/32	0.049
EN	8/16/24/32	0.024
RESET	8	0.256
	16	0.512
	24	0.768
	32	1.024
SETN	8	0.264
	16	0.528
	24	0.792
	32	1.056
TE	8	0.248
	16	0.496
	24	0.744
	32	0.992
TI	8/16/24/32	0.048
QT	8/16/24/32	0.029

Latch

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Parameters		Value
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan =0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	64.6
	Delay (ns)	min_pulse_width_high CLK	0.300
		hold_falling D CLK	0.200
		setup_falling D CLK	0.600
		T_{PLH}	1.259
		T_{PHL}	0.897
(Parameters: qn = 1, q = 1, tri = 0, rst = 0, set = 0, scan = 0, drv = 1)			
8/16/24/3	Area (µm x µm)	Width	26.4 x bits
		Height	69.4
	Delay (ns)	min_pulse_width_high CLK	0.300
		hold_falling D CLK	0.200
		setup_falling D CLK	0.600
		T_{PLH}	1.313
		T_{PHL}	1.014
(Parameters: qn = 0, q = 0, tri = 1, rst = 0, set = 0, scan = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	75.7
	Delay (ns)	min_pulse_width_high CLK	0.300
		hold_falling D CLK	0.200
		setup_falling D CLK	0.600
		T_{PLH}	2.073
		T_{PHL}	1.136
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	82.0
	Delay (ns)	min_pulse_width_high CLK	0.300
		hold_falling D CLK	0.200
		setup_falling D CLK	0.600
		T_{PLH}	2.093
		T_{PHL}	1.156

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Parameters		Value
+(Parameters: qn = 0, q = 1, tri = 0, rst = 1, set = 0, scan =0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	67.3
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_high RESET	0.300
		hold_falling D CLK	0.200
		setup_falling D CLK	0.600
		T_{PLH}	1.329
		T_{PHL}	1.022
(Parameters: qn = 1, q = 1, tri = 0, rst = 1, set = 0, scan = 0, drv = 1)			
8/16/24/3	Area (µm x µm)	Width	26.4 x bits
		Height	71.5
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_high RESET	0.300
		hold_rising D CLK	–1.700
		setup_rising D CLK	2.100
		T_{PLH}	1.395
		T_{PHL}	0.970
(Parameters: qn = 0, q = 0, tri = 1, rst = 1, set = 0, scan = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	77.8
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_high RESET	0.300
		hold_rising D CLK	–2.100
		setup_rising D CLK	2.100
		T_{PLH}	2.149
		T_{PHL}	1.144
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 0, scan = 0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	82.0
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_high RESET	0.300
		hold_rising D CLK	–2.100
		setup_rising D CLK	2.300
		T_{PLH}	2.209
		T_{PHL}	1.220

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Parameters		Value
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan =0, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	82.2
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_high RESET	0.300
		min_pulse_width_low SETN	0.300
		hold_rising D CLK	–2.100
		setup_rising D CLK	2.200
		T_{PLH}	2.163
		T_{PHL}	1.365
(Parameters: qn = 0, q = 1, tri = 0, rst = 0, set = 0, scan = 1, drv = 1)			
8/16/24/3	Area (µm x µm)	Width	26.4 x bits
		Height	71.0
	Delay (ns)	min_pulse_width_high CLK	0.300
		hold_rising D CLK	–2.100
		hold_rising TI CLK	–2.100
		setup_rising D CLK	2.200
		setup_rising TI CLK	2.200
		T_{PLH}	1.319
		T_{PHL}	1.308
(Parameters: qn = 0, q = 1, tri = 1, rst = 0, set = 0, scan = 1, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	88.3
	Delay (ns)	min_pulse_width_high CLK	0.300
		hold_rising D CLK	–2.100
		hold_rising TI CLK	–2.100
		setup_rising D CLK	2.200
		setup_rising TI CLK	2.200
		T_{PLH}	2.373
		T_{PHL}	1.360

Performance Table (Cont.)

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	Parameters		Value
(Parameters: qn = 0, q = 1, tri = 1, rst = 1, set = 1, scan =1, drv = 1)			
8/16/24/32	Area (µm x µm)	Width	26.4 x bits
		Height	93.8
	Delay (ns)	min_pulse_width_high CLK	0.300
		min_pulse_width_low CLK	0.300
		min_pulse_width_high RESET	0.300
		min_pulse_width_low SETN	0.300
		hold_rising D CLK	–2.200
		hold_rising TI CLK	–2.200
		setup_rising D CLK	2.300
		setup_rising TI CLK	2.300
		T_{PLH}	2.423
		T_{PHL}	1.429

Multiplexer

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for 2:1 to 8:1 multiplexing inputs with a variable number of bits
- Inverting and non-inverting options
- Configurable select inputs according to decoding and non-decoding options
- Three drive strength options for output

General Description

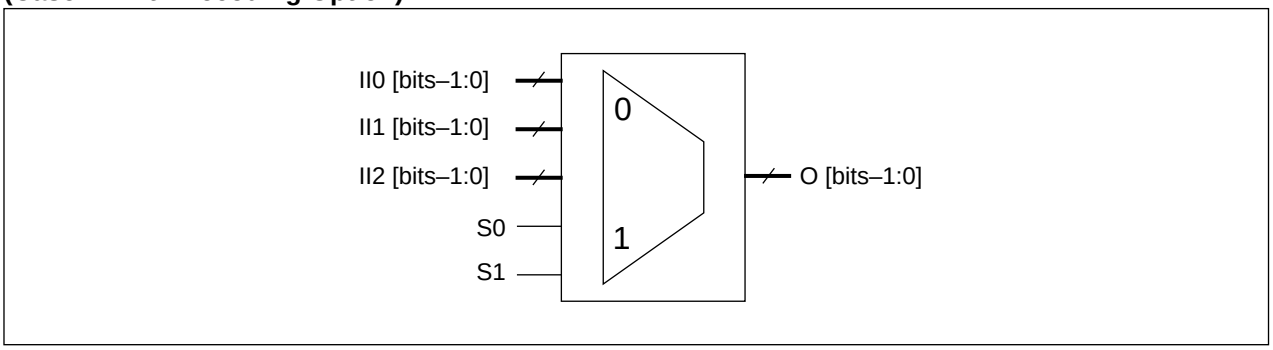
The multiplexer is optimized for multiple-targeted technologies. The generator n has the capability to build 2:1, 3:1, 4:1 and 8:1 multiplexer configurations from 4 to 128 bits range, with inverting and non-inverting, decoding and non-decoding options and three different drive strength capability.

Design Description

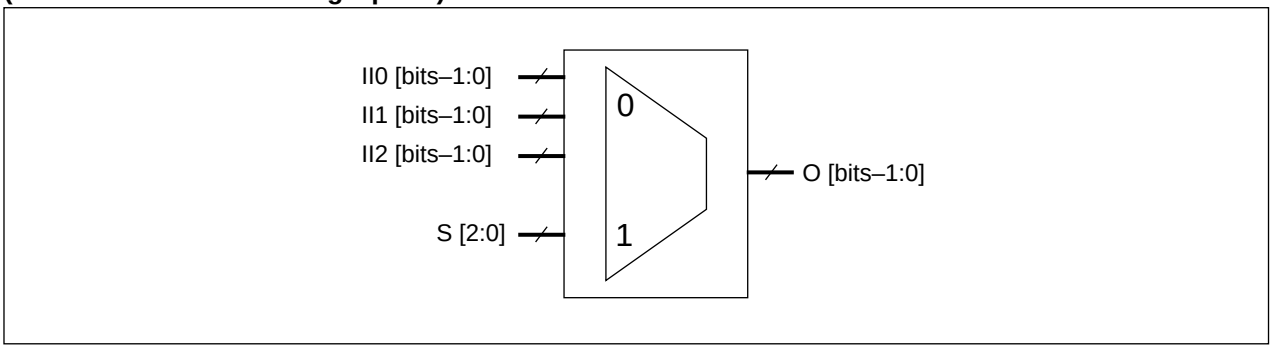
The Multiplexer has schematic and layout generators that can build a variety of multiplexers. You have options to select among two types of output buffering (inverting and non-inverting), two types of select inputs (decoding and non-decoding), three different sizes of output buffers, variable number of bits (4 to 128), and inputs ranging from 2 to 8.

Symbol (In case of 3:1 MUX)

(Case 1: With Decoding Option)



(Case 2: Without Decoding Option)



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
ins	Number of inputs	2/3/4/8
type	Output buffering: inverting or non-inverting	0/1
sel	Select controlling: decoding of non-decoding	0/1
drv	Drive strengths	1/2/4

Truth Table

(Case 1)

Non-Inverted Output					
Inputs					Output
II0	II1	II2	S0	S1	O
1	0	0	0	0	1
0	1	0	0	1	1
0	0	1	1	x	1

Inverted Output					
Inputs					Output
II0	II1	II2	S0	S1	O
1	0	0	0	0	0
0	1	0	0	1	0
0	0	1	1	x	0

(Case 2)

Non-Inverted Output						
Inputs						Output
II0	II1	II2	S[0]	S[1]	S[2]	O
1	0	0	1	0	0	1
0	1	0	0	1	0	1
0	0	1	0	0	1	1

Inverted Output						
Inputs						Output
II0	II1	II2	S[0]	S[1]	S[2]	O
1	0	0	1	0	0	0
0	1	0	0	1	0	0
0	0	1	0	0	1	0

Pin Description

(Case 1)

Pin Name	I/O	Description
II0/II1/II2 [bits–1:0]	I	Data input
S0, S1		Select lines
O	O	Data output – The Multiplexer generator can produce an inverted or non-inverted output.

(Case 2)

Pin Name	I/O	Description
II0/II1/II2 [bits–1:0]	I	Data input
S [$\lceil \log_2 ins \rceil$–1:0]		Select lines
O	O	Data output – The Multiplexer generator can produce an inverted or non-inverted output.

⌈ ⌉ round-up

Pin Capacitance

3-1 MUX With Decoding Option		
Pin Name	**Bit**	**Value (pF)**
II2	8/16/24/32	0.055
II1	8/16/24/32	0.056
II0	8/16/24/32	0.056
S1	8/16/24/32	0.035
S0	8/16/24/32	0.033

3-1 MUX Without Decoding Option		
Pin Name	**Bit**	**Value (pF)**
II2	8/16/24/32	0.055
II1	8/16/24/32	0.056
II0	8/16/24/32	0.056
S	8	0.192
	16	0.384
	24	0.576
	32	0.768

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Bit	**Area (μm x μm)**		**Delay (ns)**	
	Width	**Height**	**T_{PLH}**	**T_{PHL}**
3-1 MUX With Decoding Option				
8	26.4 x bits	71.5	1.690	1.256
16			1.836	1.391
24			1.983	1.527
32			2.133	1.667
3-1 MUX Without Decoding Option				
8/16/24/32	26.4 x bits	65.2	0.973	0.658

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for 2, 3 and 4 inputs
- Three drive strength options for input

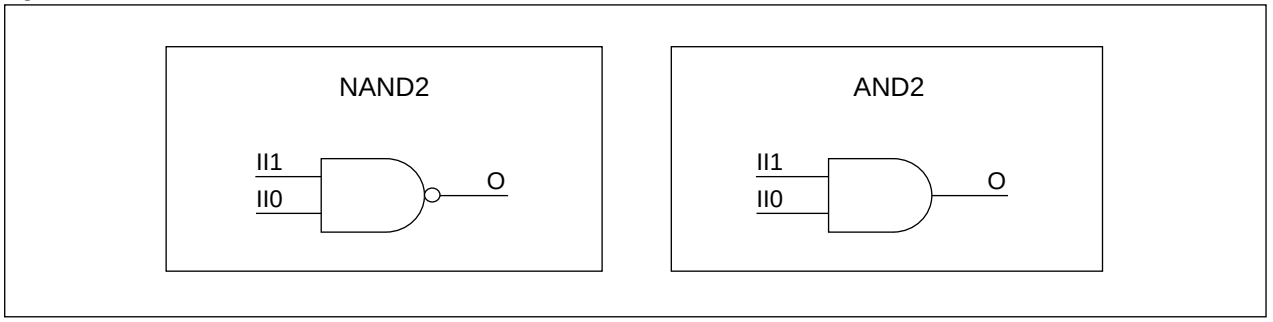
General Description

The high performance datapath NAND/AND design can be optimized for multiple-targeted technologies. This generator can build NAND/AND gates ranging from 4-bits to 128-bits for 2, 3 and 4 input configurations, supporting three different drive strengths.

Design Description

The NAND/AND design has schematic and layout generators that can build a variety of NAND and AND gates. You have an option to select either NAND or AND by setting the "type" parameter to 0 or 1 respectively. The design supports three different drive strengths (1X, 2X and 4X) and is also configured to build 2, 3 and 4-input gates.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
ins	Number of inputs	2/3/4
type	0: NAND; 1: AND	0/1
drv	Drive strength	1/2/4

NAND/AND

Truth Table

NAND2		
Inputs		Output
II0	II1	O
0	0	1
0	1	1
1	0	1
1	1	0

AND2		
Inputs		Output
II0	II1	O
0	0	0
0	1	0
1	0	0
1	1	1

Pin Description

Pin Name	I/O	Description
II0 [bits–1:0]	I	Input pin – 2, 3, 4 input NAND/AND
II1 [bits–1:0]		Input pin – 2, 3, 4 input NAND/AND
II2 [bits–1:0]		Input pin – 3, 4 input NAND/AND
II3 [bits–1:0]		Input pin – 4 input NAND/AND
O	O	Output pin

Pin Capacitance

Pin Name	Value (pF)	
	NAND4	AND4
II3	0.036	0.034
II2	0.036	0.033
II1	0.035	0.033
II0	0.033	0.033

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	Bit	Area (μm x μm)		Delay (ns)	
		Width	Height	T_{PLH}	T_{PHL}
NAND4	8/16/24/32	26.4 x bits	59.6	1.051	1.231
AND4	8/16/24/32	26.4 x bits	59.0	1.115	0.712

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for 2, 3 and 4 inputs
- Three drive strength options for output

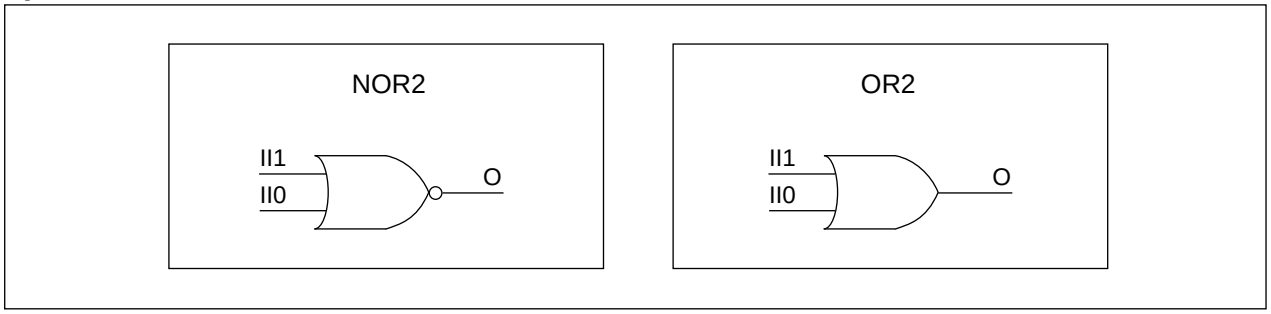
General Description

The high performance datapath NOR/OR design can be optimized for multiple-targeted technologies. This generator can build NOR/OR gates ranging from 4-bits to 128-bits for 2, 3 and 4 input configurations, supporting three different drive strengths.

Design Description

The NOR/OR design has schematic and layout generators that can build a variety of NOR and OR gates. You have an option to select either NOR or OR by setting the "type" parameter to 0 or 1 respectively. The design supports three different drive strengths (1X, 2X and 4X) and is also configured to build 2, 3 and 4-input gates.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
ins	Number of inputs	2/3/4
type	0: NOR; 1: OR	0/1
drv	Drive strength	1/2/4

NOR/OR

Truth Table

NOR2		
Inputs		Output
II0	II1	O
0	0	1
0	1	0
1	0	0
1	1	0

OR2		
Inputs		Output
II0	II1	O
0	0	0
0	1	1
1	0	1
1	1	1

Pin Description

Pin Name	I/O	Description
II0 [bits–1:0]	I	Input pin – 2-, 3-, 4-input NOR/OR
II1 [bits–1:0]		Input pin – 2-, 3-, 4-input NOR/OR
II2 [bits–1:0]		Input pin – 3-, 4-input NOR/OR
II3 [bits–1:0]		Input pin – 4-input NOR/OR
O	O	Output pin

Pin Capacitance

Pin Name	Value (pF)	
	NOR4	OR4
II3	0.037	0.028
II2	0.038	0.030
II1	0.039	0.031
II0	0.039	0.030

Performance Table

(T = 25℃, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	Bit	Area (μm x μm)		Delay (ns)	
		Width	Height	T_{PLH}	T_{PHL}
NOR4	8/16/24/32	26.4 x bits	58.9	2.308	0.487
OR4	8/16/24/32	26.4 x bits	58.9	1.031	0.970

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for types 21 and 22
- Two drive strength options for output

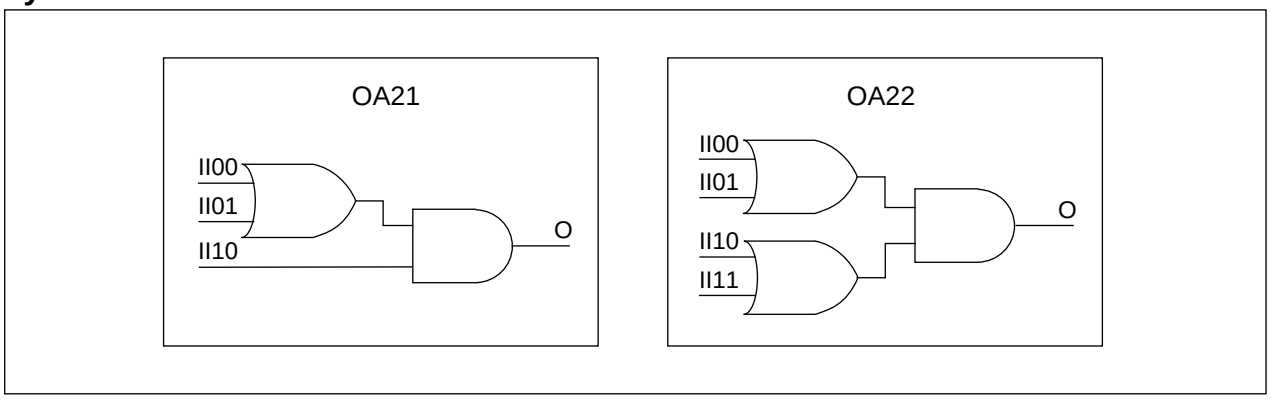
General Description

The high performance datapath OR-AND design can be optimized for multiple-targeted technologies. This generator can build OR-AND gates ranging from 4-bits to 128-bits for two different configurations (21 and 22) and two different drive strengths (1X and 2X).

Design Description

The OR-AND design has schematic and layout generators that can build a variety of OR-AND gates. You have an option to build the different kinds of OA structure configurations by setting the "type" parameter to 21 or 22 depending on your application.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Configuration type	21/22
drv	Drive strength	1/2

Truth Table

OA21			
Inputs			Output
II00	II01	II10	O
1	x	1	1
x	1	1	1
x	x	0	0
0	0	x	0

OA22				
Inputs				Output
II00	II01	II10	II11	0
1	x	1	x	1
x	1	1	x	1
1	x	x	1	1
x	1	x	1	1
0	0	x	x	0
x	x	0	0	0

Pin Description

OA22		
Pin Name	I/O	Description
II00 [bits–1:0]	I	Data input
II01 [bits–1:0]		Data input
II10 [bits–1:0]		Data input
II11 [bits–1:0]		Data input
O	O	Data output

Pin Capacitance

OA21	
Pin Name	Value (pF)
II10	0.035
II01	0.033
II00	0.034

OA22	
Pin Name	Value (pF)
II11	0.033
II10	0.036
II01	0.032
II00	0.033

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	Bit	Area (μm x μm)		Delay (ns)	
		Width	Height	T_{PLH}	T_{PHL}
OA21	8/16/24/32	26.4 x bits	56.8	0.941	0.782
OA22	8/16/24/32	26.4 x bits	58.9	0.934	1.155

Features

- Functional model, test vector, schematic and layout generators
- Timing model with auto-characterization
- Variable word width of 4 to 128 bits
- Configurable for types 21 and 22
- Two drive strength options for output

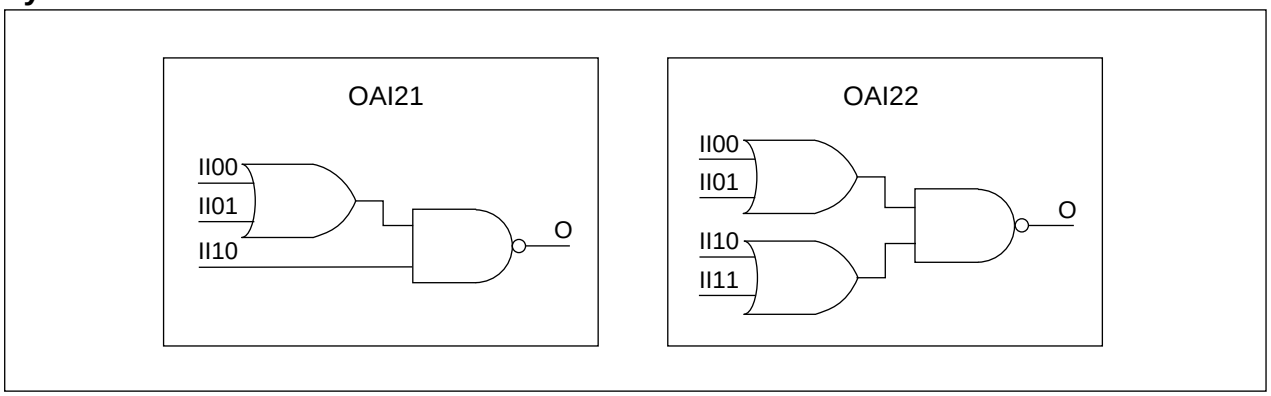
General Description

The high performance datapath OR-AND-INVERT design can be optimized for multiple-targeted technologies. This generator can build OR-AND-INVERT gates ranging from 4-bits to 128-bits for two different configurations (21 and 22) and two different drive strengths (1X and 2X).

Design Description

The OR-AND-INVERT design has schematic and layout generators that can build a variety of OR-AND-INVERT gates. You have an option to build the different kinds of OAI structure configurations by setting the "type" parameter to 21 or 22 depending on your application.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	Configuration type	21/22
drv	Drive strength	1/2

Truth Table

OAI21			
Inputs			Output
II00	II01	II10	O
1	x	1	0
x	1	1	1
x	x	0	1
0	0	x	1

OAI22				
Inputs				Output
II00	II01	II10	II11	O
1	x	1	x	0
x	1	1	x	0
1	x	x	1	0
x	1	x	1	0
0	0	x	x	1
x	x	0	0	1

Pin Description

OA22		
Pin Name	I/O	Description
II00 [bits–1:0]	I	Data input
II01 [bits–1:0]		Data input
II10 [bits–1:0]		Data input
II11 [bits–1:0]		Data input
O	O	Data output

Pin Capacitance

OAI21	
Pin Name	Value (pF)
II10	0.025
II01	0.026
II00	0.025

OAI22	
Pin Name	Value (pF)
II11	0.024
II10	0.023
II01	0.024
II00	0.025

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	Bit	Area (μm x μm)		Delay (ns)	
		Width	Height	T_{PLH}	T_{PHL}
OAI21	8/16/24/32	26.4 x bits	54.5	1.331	0.714
OAI22	8/16/24/32	26.4 x bits	58.4	1.471	0.694

Features

- Technology-independent generator
- Variable word width of 4 to 128 bits
- Configurable for tri-state buffer/inverter design
- Four drive strength options for output

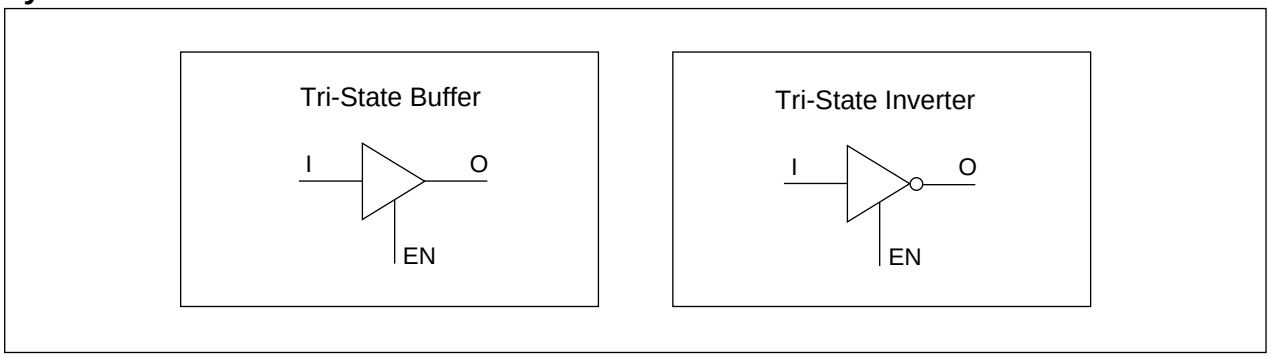
General Description

The high performance Tri-State Buffer/Inverter design is optimized for multiple-targeted technologies. The generator design has the capability to build tri-state buffers/inverters ranging from 4-bits to 128-bits for various drive strength configurations.

Design Description

The Tri-State Buffer/Inverter design has schematic and layout generators that can build a variety of tri-state buffers and inverters. You have an option to select either Tri-State Buffer or a Tri-State Inverter by setting the "type" parameter to 1 or 0 respectively. The design supports 4 different drive strength options (1X, 2X, 4X, 8X) for the tri-state buffer and 2 drive strength options (1X and 2X) for the tri-state inverter.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
type	0: Tri-State Inverter; 1: Tri-State Buffer	0/1
drv	Drive strength	1/2/4/8

NOTE: For type = 0, only 1X and 2X supported.

Tri-State Buffer/Inverter

Truth Table

Tri-State Buffer		
Inputs		Output
I	EN	O
x	0	Hi-Z
0	1	0
1	1	1

Tri-State Inverter		
Inputs		Output
I	EN	O
x	0	Hi-Z
0	1	1
1	1	0

Pin Description

Pin Name	Description
I [bits–1:0]	Input
EN [bits–1:0]	High enable
O [bits–1:0]	Output

Pin Capacitance

Pin Name	Value (pF)	
	Tri-State Buffer	Tri-State Inverter
EN	0.051	0.035
I	0.054	0.052
O	0.028	0.060

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	Bit	Area (μm x μm)		Delay (ns)	
		Width	Height	T_{PLH}	T_{PHL}
Tri-State Buffer	8/16/24/32	26.4 x bits	63.7	0.897	0751
Tri-State Inverter	8/16/24/32	26.4 x bits	61.0	0.989	0.520

Features

- Technology-independent generator
- Variable word width of 4 to 128 bits
- Configurable for 2 and 3 inputs
- Configurable for XNOR/XOR design
- Three drive strength options for output

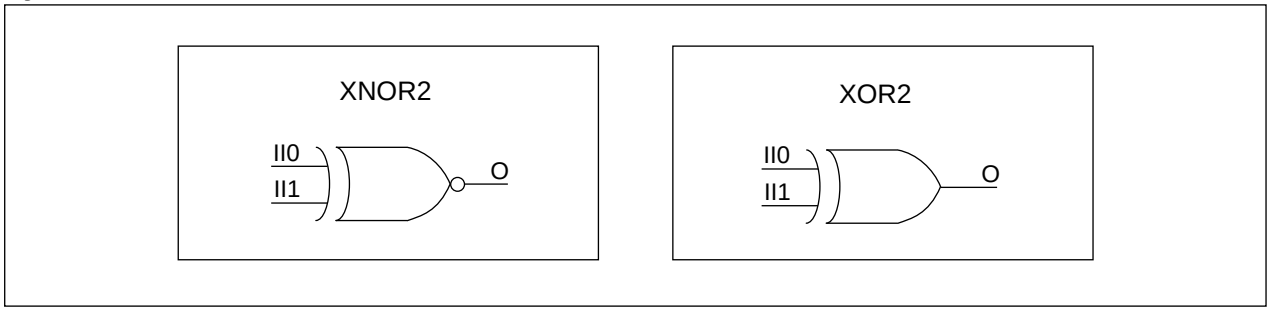
General Description

The high performance datapath XNOR/XOR design can be optimized for multiple targeted technologies. The generator can build XNOR/XOR gates ranging from 4-bits to 128-bits for 2 and 3 input configurations, supporting three different drive strengths.

Design Description

The XNOR/XOR design has schematic and layout generators that can build a variety of XNOR and XOR gates. You have an option to select either XNOR or XOR by setting the “type” parameter to 0 or 1 respectively. The design supports three different drive strengths (1X, 2X and 4X) and is also configured to build 2- and 3-input gates.

Symbol



Parameter Description

Parameter Name	Description	Range
instance_name	Name of the instance	Any string
bits	Number of bits in the input data bus	4 to 128
ins	Number of inputs	2/3
type	0: XNOR; 1: XOR	0/1
drv	Drive strength	1/2/4

NOTE: When ins = 3, only drv = 1 and 2 are supported.

Truth Table

XNOR2		
Inputs		Output
II0	II1	O
0	0	1
0	1	0
1	0	0
1	1	1

XOR2		
Inputs		Output
II0	II1	O
0	0	0
0	1	1
1	0	1
1	1	0

Pin Description

Pin Name	I/O	Description
II0 [bits–1:0]	I	Input pin – 2-, 3-input XNOR/XOR
II1 [bits–1:0]		Input pin – 2-, 3-input XNOR/XOR
II2 [bits–1:0]		Input pin – 3-input XNOR/XOR
O	O	Output pin

Pin Capacitance

Pin Name	Value (pF)	
	XNOR3	XOR3
II2	0.029	0.034
II1	0.031	0.031
II0	0.037	0.036

Performance Table

(T = 25°C, Slope = 1.0ns, Cap. = 0.4pF)

Cell Name	Bit	Area (μm x μm)		Delay (ns)	
		Width	Height	T_{PLH}	T_{PHL}
XNOR3	8/16/24/32	26.4 x bits	65.2	1.497	1.074
XOR3	8/16/24/32	26.4 x bits	65.2	1.142	0.972

JTAG Boundary Scans 7

Contents

OVERVIEW

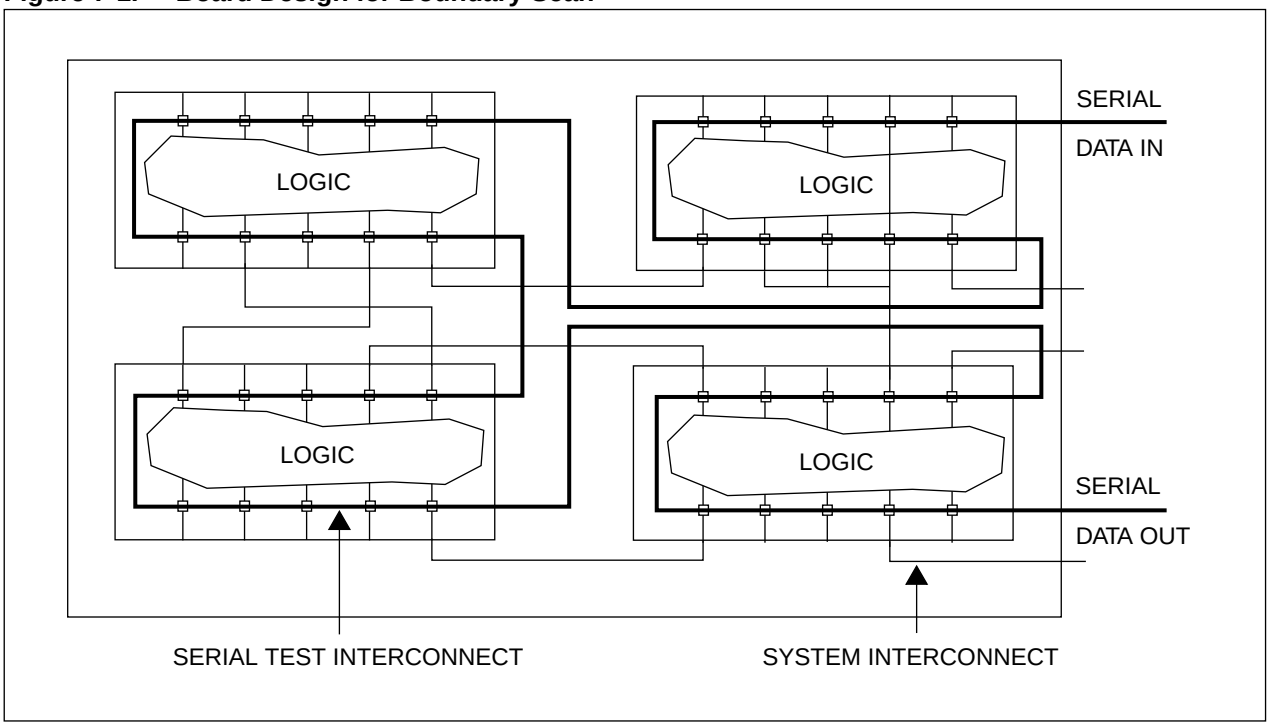
A board test is typically achieved by using in-circuit test techniques. However, in-circuit test techniques demonstrate significant limitations for Surface Mount Technology (SMT) and Fine Pitch Technology (FPT) boards. The pin and pad spacings getting tighter make it difficult to test boards with traditional methods economically and reliably.

A boundary scan design reduces the cost of a function test. A boundary scan design circuitry allows boards to be tested using the equivalent in-circuit test technique without bed-of-nails fixture. In recognition of the increasing acceptance of the boundary scan test, IEEE and JTAG (Joint Test Action Group) developed IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std 1149.1).

A boundary scan technique requires to place a boundary scan cell adjacent to each component pin so that signals at component boundaries can be controlled and observed using scan testing principles. Each boundary scan cell for a given component is able to capture data from an input pin or from its internal logic, and to drive its internal logic or an output pin. Boundary scan cells for the pins of a given component are interconnected so as to form a shift-register chain around the border of the design, known as a boundary scan register. Boundary scan registers for individual components can be connected in series to form a single path through the complete design as shown in the figure 9-1. Alternatively, a board design can contain several independent boundary scan paths that allow individual components to be tested as well as the interconnections between components.

To test component interconnections, test data are first shifted into all boundary scan register cells associated with component output test pins. Test data are then loaded into parallel inputs of boundary scan cells associated with input pins through the component interconnections, and data captured in these cells are shifted out from the boundary cells for evaluation. For an individual component test, a boundary scan register is used to isolate on-chip system logic from stimuli received from surrounding components. An actual test can be performed through the boundary scan path or the built-in self-test hardware.

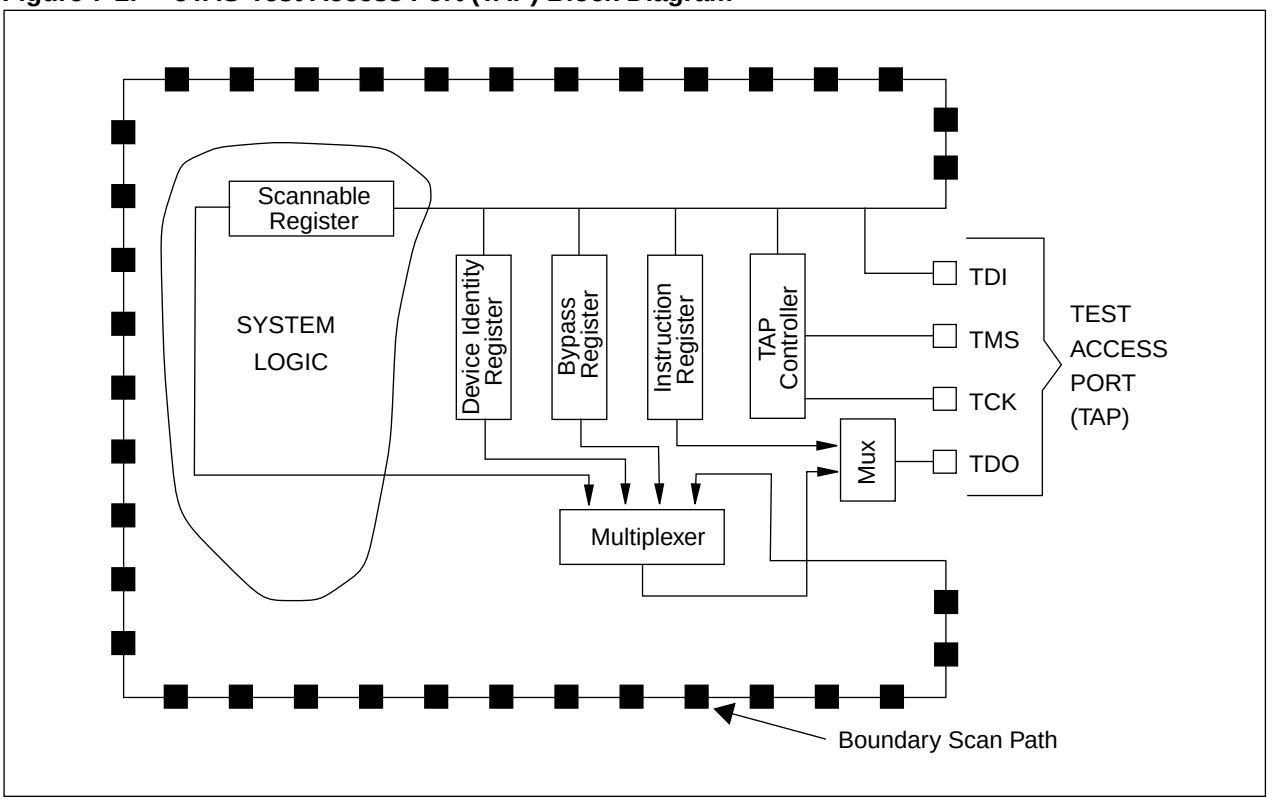
Figure 7-1. Board Design for Boundary Scan



BOUNDARY SCAN ARCHITECTURE

A boundary scan architecture contains TAP (Test Access Port), TAP controller, instruction register and a group of test data registers. The instruction and test data registers are separate shift-register-based paths connected in parallel with a common serial data input and a common serial data output which are connected to TAP, TDI and TDO signals. TAP controller selects the alternative instruction and test data register paths between TDI and TDO. The schematic view of the top level design of the test logic architecture is shown in the figure 9-2.

Figure 7-2. JTAG Test Access Port (TAP) Block Diagram



Boundary Scan Functional Block Descriptions

TAP (Test Access Port)

TAP is a general-purpose port that can provide with an access to many test support functions built into a component, including the test logic. It includes three inputs (TCK; Test Clock Signal, TMS; Test Mode Signal and TDI; Test Data Input) and one output (TDO; Test Data Output) required by the test logic. An optional fourth input (TRSTN; Test Reset) is provided for the asynchronous initialization of the test logic. The values applied at TMS and TDI pins are sampled on the rising edge of TCK, and the value placed on TDO pin changes on the falling edge of TCK.

TAP Controller

TAP controller receives TCK, interprets the signals on TMS, and generates clock and control signals for both instruction and test data registers and for other parts of the test circuitries as required.

Instruction Register/Instruction Decoder

Test instructions are shifted into and held by the instruction register. Test instructions include a selection of tests to be performed or the test data register to be accessed. A basic 3-bit instruction register and its instruction decoder are provided as macrofunctions in the library.

Test Data Registers

Data registers include a bypass register, a boundary scan register, a device identification register and other design specific registers. Only the bypass- and boundary scan registers are mandatory; the rest are optional.

Bypass register:	The bypass register provides a single-bit serial connection through the circuit when none of the other test data registers is selected. It can be used to allow test data to flow through a given device to the other components in a product without affecting a normal operation.
Boundary scan register:	The boundary scan register detects typical production defects in board interconnects, such as opens, shorts, etc. It also allows an access to component inputs and outputs when you test their logic or sample flow-through signals. Special boundary scan register macrocells are provided for this purpose. These special registers is discussed in the next section of next pages.
Design-specific test data register:	These optional registers may be provided to allow an access to design-specific test support features in the integrated circuit, such as self-test, scan test.
Device identification register:	This is an optional test data register that allows the manufacturer part number and variant of a components to be identified. The 32-bit identification register is partitioned into four fields:

Device version identifier	1st field	The first four bits beginning from MSB
Device part number	2nd field	16 bits
Manufacturer's JEDEC number	3rd field	11 bits
LSB	4th field	1 bit —tied in High

The ASIC designer is free to fill the version and part number in any manner as long as the total twenty bits are used.

SEC's JEDEC code:	78 decimal = 1001110 Continuation field (4 bits) = 0000
Contents of device identification register:	XXXX XXXXXXXXXXXXXXX 0000 1001110 1 Users can define these two fields.

BOUNDARY SCAN REGISTER MACROCELLS

The boundary scan register allows testing of circuitry external to the integrated circuit and provides for defined conditions to be established at the periphery of the on-chip system logic while it is tested itself. It also permits signals flowing through system pins to be sampled and examined without interfering with the operation of the on-chip system logic. The boundary scan register has four capabilities:

Capture: Loads data into the boundary scan register in parallel on the rising edge of TCK. It does not affect the output until Update is executed.

Shift: Shifts data from one boundary scan register to the next register towards the serial data output pin on the rising edge of TCK.

Update: Loads data in the boundary scan register into the parallel data output pin on the falling edge of TCK when EXTEST or INTEST instruction is selected.

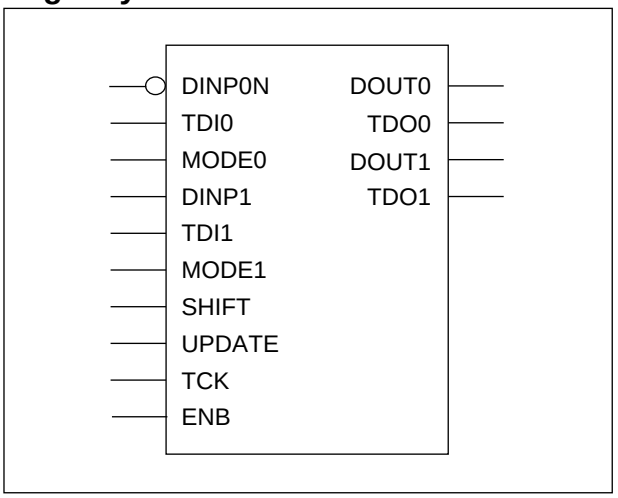
Set: Sets the parallel output pin.

SEC supports five types of boundary scan registers. Four of them, JTCK, JTBI1, JTIN1 and JTOUT1 are to be implemented around the periphery of the die next to I/O cells. For this reason, two I/O pads at each corner, that is, the total of eight I/O pads for the entire chip are not scannable. An implementation is automatically performed during a placement to achieve the most optimum placement with a minimum performance penalty. The fifth cell, JTINT1, is to be placed in the core area of the die for tri-state I/O control. Applications for each type of boundary scan register cell are summarized as follows.

Cell List

Cell Name	Function Description	Page
JTBI1	Bi-directional I/O Boundary Scan Cell	7-5
JTCK	Special Input (such as Clock Input) Boundary Scan Cell	7-10
JTIN1	Input Boundary Scan Cell	7-12
JTINT1	Tri-State I/O Control Boundary Scan Cell	7-15
JTOUT1	Output Boundary Scan Cell	7-19

Logic Symbol



Cell Data

Input Loading (SL)	
DINP0N	4
TDI0	0
MODE0	1
DINP1	3
TDI1	0
MODE1	1
SHIFT	2
UPDATE	3
TCK	1
ENB	0
Gate Count	
22	

Pin Description

Pin name	I/O	Description
DINP0N	I	Parallel Data Input Active Low for the Input Part of the Bi-Directional Pin
TDI0	I	Serial Test Data Input for Input Part of the Bi-Directional Pin
MODE0	I	Mode Select for Input Part—Low for Data Input and High for Internal Register Data Value
DINP1	I	Parallel Data Input Active Low for the Output Part of the Bi-Directional Pin
TDI1	I	Serial Test Data Input for Input Part of the Bi-Directional Pin
MODE1	I	Mode Select for Output Part—Low for Data Input and High for Internal Register Data Value
SHIFT	I	Active High Shift Control Input
UPDATE	I	Update Latch Input—Low for Update
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable
DOUT0	O	Parallel Data Output for Input Part of the Bi-Directional Pin
TDO0	O	Serial Test Data Output for Input Part of the Bi-Directional Pin
DOUT1	O	Parallel Data Output for Output Part of the Bi-Directional Pin
TDO1	O	Serial Test Data Output for Output Part of the Bi-Directional Pin

JTBI1

Bi-directional I/O Scan Cell with Capture, Shift and Update

Truth Table

DINP0N	TDI0	MODE0	SHIFT	UPDATE	TCK	ENB	OUTPUT
							DOUT0
0	X	0	X	X	X	X	1
1	X	0	X	X	X	X	0
X	X	1	X	X	X	X	LatchQN
							TDO0
X	X	X	X	X	↗	0	TDO0o
0	X	0	0	X	↗	1	1
1	X	0	0	X	↗	1	0
X	X	1	0	X	↗	1	LatchQN
X	0	X	1	X	↗	1	0
X	1	X	1	X	↗	1	1
X	X	X	X	X	0	X	TDO0o
X	X	X	X	X	1	X	TDO0o
X	X	X	X	X	↘	X	TDO0o
							LatchQN
X	X	X	X	0	X	X	TDO0
X	X	X	X	1	X	X	LatchQNo

DINP1	TDI1	MODE1	SHIFT	UPDATE	TCK	ENB	OUTPUT
							DOUT1
0	X	0	X	X	X	X	0
1	X	0	X	X	X	X	1
X	X	1	X	X	X	X	LatchQ
							TDO1
X	X	X	X	X	↗	0	TDO1o
0	X	X	0	X	↗	1	0
1	X	X	0	X	↗	1	1
X	0	X	1	X	↗	1	0
X	1	X	1	X	↗	1	1
X	X	X	X	X	0	X	TDO1o
X	X	X	X	X	1	X	TDO1o
X	X	X	X	X	↘	X	TDO1o
							LatchQ
X	X	X	X	0	X	X	TDO1
X	X	X	X	1	X	X	LatchQo

NOTES:

1. Outputs are defined in separate truth tables. In addition, the internal states known as “LatchQ” and “LatchQN” are defined as the output of the latch in the logic diagram.
2. JTBI1 has a similar truth table to JTIN1 and JTOUT1 macrocells without SETN input. It has similar delays to JTIN1 and JTOUT1.

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Input Setup Time (TDI0 to TCK)	t_{SU}	0.49
Input Hold Time (TDI0 to TCK)	t_{HD}	0.40
Input Setup Time (TDI0 to ENB)	t_{SU}	0.49
Input Hold Time (TDI0 to ENB)	t_{HD}	0.40
Input Setup Time (TDI1 to TCK)	t_{SU}	0.49
Input Hold Time (TDI1 to TCK)	t_{HD}	0.40
Input Setup Time (TDI1 to ENB)	t_{SU}	0.49
Input Hold Time (TDI1 to ENB)	t_{HD}	0.40
Input Setup Time (DINP0N to TCK)	t_{SU}	0.82
Input Hold Time (DINP0N to TCK)	t_{HD}	0.33
Input Setup Time (DINP0N to ENB)	t_{SU}	0.82
Input Hold Time (DINP0N to ENB)	t_{HD}	0.33
Input Setup Time (DINP1 to TCK)	t_{SU}	0.82
Input Hold Time (DINP1 to TCK)	t_{HD}	0.33
Input Setup Time (DINP1 to ENB)	t_{SU}	0.82
Input Hold Time (DINP1 to ENB)	t_{HD}	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.66
Input Hold Time (SHIFT to TCK)	t_{HD}	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.66
Input Hold Time (SHIFT to ENB)	t_{HD}	0.33
Input Setup Time (MODE0 to TCK)	t_{SU}	0.90
Input Hold Time (MODE0 to TCK)	t_{HD}	0.33
Input Setup Time (MODE0 to ENB)	t_{SU}	0.90
Input Hold Time (MODE0 to ENB)	t_{HD}	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO0	t_{PLH}	1.06	1.00 + 0.031*SL	1.01 + 0.026*SL	1.00 + 0.027*SL
	t_{PHL}	0.89	0.81 + 0.040*SL	0.83 + 0.035*SL	0.85 + 0.033*SL
	t_R	0.24	0.13 + 0.054*SL	0.12 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.25	0.12 + 0.061*SL	0.12 + 0.063*SL	0.10 + 0.065*SL
ENB to TDO0	t_{PLH}	1.07	1.01 + 0.032*SL	1.02 + 0.029*SL	1.03 + 0.027*SL
	t_{PHL}	0.90	0.82 + 0.040*SL	0.84 + 0.035*SL	0.86 + 0.033*SL
	t_R	0.24	0.13 + 0.051*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.25	0.12 + 0.063*SL	0.12 + 0.063*SL	0.09 + 0.066*SL
TCK to TDO1	t_{PLH}	1.03	0.97 + 0.031*SL	0.98 + 0.027*SL	0.98 + 0.027*SL
	t_{PHL}	0.85	0.77 + 0.039*SL	0.78 + 0.034*SL	0.79 + 0.033*SL
	t_R	0.23	0.13 + 0.051*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.10 + 0.066*SL	0.11 + 0.065*SL
ENB to TDO1	t_{PLH}	1.04	0.98 + 0.030*SL	0.99 + 0.027*SL	0.99 + 0.027*SL
	t_{PHL}	0.87	0.79 + 0.039*SL	0.81 + 0.034*SL	0.82 + 0.033*SL
	t_R	0.22	0.12 + 0.054*SL	0.11 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.11 + 0.062*SL	0.11 + 0.065*SL	0.10 + 0.065*SL
DINP0N to DOUT0	t_{PLH}	0.19	0.16 + 0.015*SL	0.17 + 0.014*SL	0.17 + 0.014*SL
	t_{PHL}	0.21	0.11 + 0.046*SL	0.18 + 0.021*SL	0.23 + 0.017*SL
	t_R	0.19	0.14 + 0.027*SL	0.14 + 0.025*SL	0.11 + 0.029*SL
	t_F	0.23	0.12 + 0.059*SL	0.20 + 0.030*SL	0.18 + 0.031*SL
MODE0 to DOUT0	t_{PLH}	0.28	0.24 + 0.018*SL	0.25 + 0.014*SL	0.26 + 0.013*SL
	t_{PHL}	0.41	0.35 + 0.031*SL	0.38 + 0.020*SL	0.40 + 0.017*SL
	t_R	0.21	0.12 + 0.044*SL	0.18 + 0.023*SL	0.13 + 0.029*SL
	t_F	0.21	0.15 + 0.030*SL	0.14 + 0.033*SL	0.15 + 0.032*SL
UPDATE to DOUT0	t_{PLH}	0.67	0.61 + 0.032*SL	0.66 + 0.014*SL	0.66 + 0.014*SL
	t_{PHL}	1.02	0.95 + 0.036*SL	0.98 + 0.027*SL	1.06 + 0.018*SL
	t_R	0.21	0.15 + 0.028*SL	0.15 + 0.027*SL	0.14 + 0.028*SL
	t_F	0.38	0.30 + 0.037*SL	0.32 + 0.033*SL	0.33 + 0.031*SL
TCK to DOUT0	t_{PLH}	1.58	1.54 + 0.019*SL	1.55 + 0.016*SL	1.58 + 0.013*SL
	t_{PHL}	1.56	1.49 + 0.033*SL	1.51 + 0.027*SL	1.59 + 0.019*SL
	t_R	0.21	0.17 + 0.021*SL	0.15 + 0.027*SL	0.14 + 0.029*SL
	t_F	0.38	0.31 + 0.033*SL	0.31 + 0.035*SL	0.35 + 0.031*SL
ENB to DOUT0	t_{PLH}	1.61	1.57 + 0.017*SL	1.58 + 0.016*SL	1.60 + 0.013*SL
	t_{PHL}	1.57	1.50 + 0.034*SL	1.52 + 0.026*SL	1.60 + 0.019*SL
	t_R	0.21	0.15 + 0.027*SL	0.15 + 0.029*SL	0.15 + 0.028*SL
	t_F	0.38	0.30 + 0.040*SL	0.32 + 0.032*SL	0.33 + 0.031*SL
DINP1 to DOUT1	t_{PLH}	0.30	0.24 + 0.033*SL	0.26 + 0.026*SL	0.25 + 0.027*SL
	t_{PHL}	0.41	0.35 + 0.034*SL	0.33 + 0.039*SL	0.39 + 0.033*SL
	t_R	0.23	0.12 + 0.055*SL	0.11 + 0.059*SL	0.10 + 0.060*SL
	t_F	0.27	0.13 + 0.070*SL	0.15 + 0.063*SL	0.13 + 0.065*SL

(Continued)

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

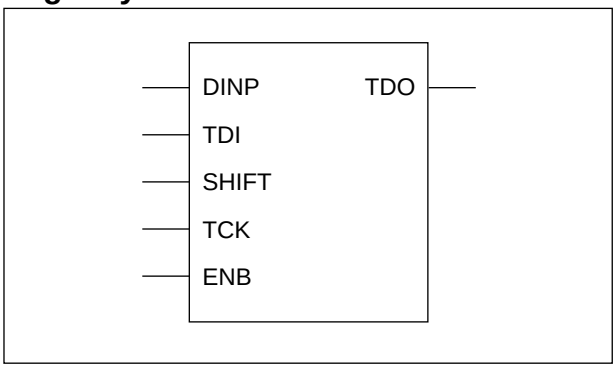
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
MODE1 to DOUT1	t_{PLH}	0.25	0.18 + 0.033*SL	0.20 + 0.026*SL	0.19 + 0.027*SL
	t_{PHL}	0.40	0.33 + 0.036*SL	0.32 + 0.038*SL	0.38 + 0.033*SL
	t_R	0.24	0.12 + 0.061*SL	0.13 + 0.057*SL	0.10 + 0.060*SL
	t_F	0.27	0.13 + 0.071*SL	0.15 + 0.064*SL	0.15 + 0.065*SL
UPDATE to DOUT1	t_{PLH}	0.86	0.80 + 0.034*SL	0.80 + 0.031*SL	0.85 + 0.027*SL
	t_{PHL}	0.78	0.69 + 0.044*SL	0.71 + 0.037*SL	0.75 + 0.033*SL
	t_R	0.24	0.15 + 0.047*SL	0.12 + 0.058*SL	0.10 + 0.060*SL
	t_F	0.29	0.16 + 0.061*SL	0.16 + 0.064*SL	0.15 + 0.065*SL
TCK to DOUT1	t_{PLH}	1.76	1.70 + 0.031*SL	1.71 + 0.027*SL	1.72 + 0.027*SL
	t_{PHL}	1.53	1.44 + 0.044*SL	1.46 + 0.037*SL	1.50 + 0.033*SL
	t_R	0.24	0.13 + 0.056*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.29	0.15 + 0.067*SL	0.17 + 0.062*SL	0.14 + 0.065*SL
ENB to DOUT1	t_{PLH}	1.78	1.71 + 0.030*SL	1.72 + 0.029*SL	1.74 + 0.027*SL
	t_{PHL}	1.53	1.44 + 0.045*SL	1.47 + 0.037*SL	1.51 + 0.033*SL
	t_R	0.24	0.15 + 0.047*SL	0.11 + 0.060*SL	0.12 + 0.059*SL
	t_F	0.28	0.16 + 0.064*SL	0.15 + 0.066*SL	0.17 + 0.064*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

JTCK

Special Input Scan Cell with Capture and Shift

Logic Symbol



Cell Data

Input Loading (SL)	
DINP	1
TDI	0
SHIFT	1
TCK	1
ENB	0
Gate Count	
7	

General Description

JTCK is a special input boundary scan cell for clock pad. It has capture and shift capabilities only. JTCK doesn't have update and set capabilities, but has clock enable capability.

Pin Description

Pin name	I/O	Description
DINP	I	Parallel System Data Input
TDI	I	Serial Test Data Input
SHIFT	I	Active High Shift Control Input
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable Input
TDO	O	Serial Test Data Output

Truth Table

DINP	TDI	SHIFT	TCK	ENB	TDO
X	X	X	↑	0	TDOo
0	X	0	↑	1	0
1	X	0	↑	1	1
X	0	1	↑	1	0
X	1	1	↑	1	1
X	X	X	0	X	TDOo
X	X	X	1	X	TDOo
X	X	X	↓	X	TDOo

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Input Setup Time (TDI to TCK)	t_{SU}	0.90
Input Hold Time (TDI to TCK)	t_{HD}	0.33
Input Setup Time (TDI to ENB)	t_{SU}	0.90
Input Hold Time (TDI to ENB)	t_{HD}	0.33
Input Setup Time (DINP to TCK)	t_{SU}	0.76
Input Hold Time (DINP to TCK)	t_{HD}	0.33
Input Setup Time (DINP to ENB)	t_{SU}	0.79
Input Hold Time (DINP to ENB)	t_{HD}	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.68
Input Hold Time (SHIFT to TCK)	t_{HD}	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.74
Input Hold Time (SHIFT to ENB)	t_{HD}	0.33

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

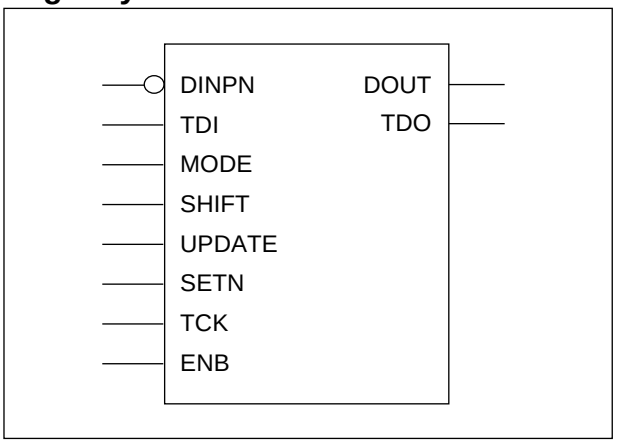
Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.71	0.65 + 0.030*SL	0.66 + 0.028*SL	0.67 + 0.027*SL
	t_{PHL}	0.78	0.71 + 0.038*SL	0.72 + 0.034*SL	0.73 + 0.033*SL
	t_R	0.23	0.11 + 0.057*SL	0.10 + 0.062*SL	0.13 + 0.059*SL
	t_F	0.23	0.11 + 0.062*SL	0.11 + 0.063*SL	0.09 + 0.066*SL
ENB to TDO	t_{PLH}	0.70	0.64 + 0.030*SL	0.64 + 0.028*SL	0.65 + 0.027*SL
	t_{PHL}	0.78	0.70 + 0.039*SL	0.72 + 0.034*SL	0.73 + 0.033*SL
	t_R	0.23	0.12 + 0.059*SL	0.12 + 0.057*SL	0.09 + 0.060*SL
	t_F	0.24	0.11 + 0.068*SL	0.12 + 0.062*SL	0.09 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

JTIN1

Input Scan Cell with Capture, Shift, Update and Set

Logic Symbol



Cell Data

Input Loading (SL)	
DINPN	4
TDI	0
MODE	1
SHIFT	1
UPDATE	1
SETN	0
TCK	1
ENB	0
Gate Count	
13	

Pin Description

Pin name	I/O	Description
DINPN	I	Parallel Data Input Active Low
TDI	I	Serial Test Data Input
MODE	I	Mode Select Input—Low for Data Input and High for Internal Register Data Value
SHIFT	I	Active High Shift Control Input
UPDATE	I	Update Latch Input—Low for Update
SETN	I	Active Low Set Input
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable Input
DOUT	O	Parallel Data Output
TDO	O	Serial Test Data Output

Truth Table

DINPN	TDI	MODE	SHIFT	UPDATE	TCK	ENB	OUTPUT
							DOUT
0	X	0	X	X	X	X	1
1	X	0	X	X	X	X	0
X	X	1	X	X	X	X	LatchQ
							TDO
X	X	X	X	X	↗	0	TDOo
0	X	0	0	X	↗	1	1
1	X	0	0	X	↗	1	0
X	X	1	0	X	↗	1	LatchQ
X	0	X	1	X	↗	1	0
X	1	X	1	X	↗	1	1
X	X	X	X	X	0	X	TDOo
X	X	X	X	X	1	X	TDOo
X	X	X	X	X	↘	X	TDOo
							LatchQ
X	X	X	X	0	X	X	0
X	X	X	X	1	0	X	TDO
X	X	X	X	1	1	X	LatchQo

NOTE: Outputs are defined in separate truth tables. In addition, an internal state known as “LatchQ” is defined as the output of the latch in the logic diagram.

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Input Setup Time (TDI to TCK)	t_{SU}	0.49
Input Hold Time (TDI to TCK)	t_{HD}	0.33
Input Setup Time (TDI to ENB)	t_{SU}	0.58
Input Hold Time (TDI to ENB)	t_{HD}	0.33
Input Setup Time (DINPN to TCK)	t_{SU}	0.96
Input Hold Time (DINPN to TCK)	t_{HD}	0.33
Input Setup Time (DINPN to ENB)	t_{SU}	0.96
Input Hold Time (DINPN to ENB)	t_{HD}	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.68
Input Hold Time (SHIFT to TCK)	t_{HD}	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.74
Input Hold Time (SHIFT to ENB)	t_{HD}	0.33
Input Setup Time (MODE to TCK)	t_{SU}	0.96
Input Hold Time (MODE to TCK)	t_{HD}	0.33
Input Setup Time (MODE to ENB)	t_{SU}	0.98
Input Hold Time (MODE to ENB)	t_{HD}	0.33
Recovery Time (SETN)	t_{RC}	0.48

JTIN1

Input Scan Cell with Capture, Shift, Update and Set

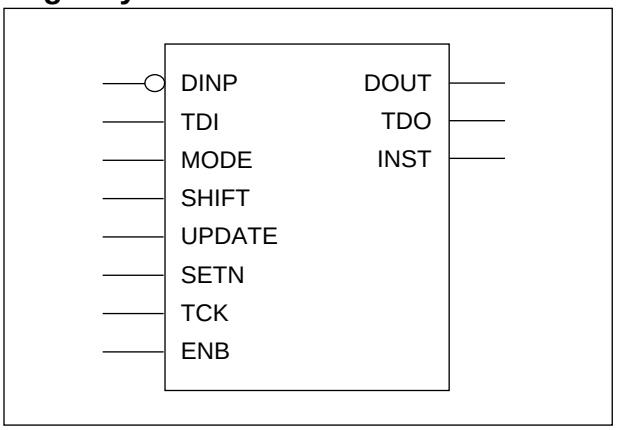
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.68	0.62 + 0.030*SL	0.63 + 0.028*SL	0.63 + 0.027*SL
	t_{PHL}	0.75	0.67 + 0.039*SL	0.69 + 0.034*SL	0.70 + 0.033*SL
	t_R	0.23	0.12 + 0.051*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.23	0.11 + 0.064*SL	0.11 + 0.064*SL	0.09 + 0.065*SL
ENB to TDO	t_{PLH}	0.73	0.67 + 0.030*SL	0.68 + 0.026*SL	0.67 + 0.027*SL
	t_{PHL}	0.79	0.71 + 0.039*SL	0.73 + 0.034*SL	0.74 + 0.033*SL
	t_R	0.22	0.12 + 0.050*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.23	0.11 + 0.064*SL	0.11 + 0.064*SL	0.09 + 0.065*SL
DINPN to DOUT	t_{PLH}	0.19	0.16 + 0.016*SL	0.17 + 0.014*SL	0.33 + -0.003*SL
	t_{PHL}	0.21	0.16 + 0.028*SL	0.17 + 0.022*SL	0.43 + -0.005*SL
	t_R	0.19	0.15 + 0.024*SL	0.14 + 0.027*SL	0.44 + -0.005*SL
	t_F	0.24	0.16 + 0.040*SL	0.18 + 0.033*SL	0.56 + -0.007*SL
MODE to DOUT	t_{PLH}	0.36	0.32 + 0.017*SL	0.34 + 0.013*SL	0.48 + -0.003*SL
	t_{PHL}	0.41	0.36 + 0.025*SL	0.37 + 0.021*SL	0.62 + -0.005*SL
	t_R	0.16	0.11 + 0.025*SL	0.08 + 0.033*SL	0.45 + -0.006*SL
	t_F	0.21	0.15 + 0.035*SL	0.15 + 0.033*SL	0.53 + -0.007*SL
UPDATE to DOUT	t_{PLH}	0.87	0.83 + 0.019*SL	0.84 + 0.017*SL	1.04 + -0.004*SL
	t_{PHL}	0.88	0.81 + 0.030*SL	0.83 + 0.024*SL	1.12 + -0.006*SL
	t_R	0.20	0.16 + 0.024*SL	0.14 + 0.028*SL	0.47 + -0.006*SL
	t_F	0.28	0.22 + 0.034*SL	0.22 + 0.034*SL	0.61 + -0.007*SL
SETN to DOUT	t_{PLH}	0.60	0.56 + 0.020*SL	0.57 + 0.017*SL	0.76 + -0.004*SL
	t_{PHL}	0.63	0.56 + 0.031*SL	0.59 + 0.024*SL	0.87 + -0.006*SL
	t_R	0.21	0.15 + 0.030*SL	0.16 + 0.026*SL	0.46 + -0.006*SL
	t_F	0.28	0.21 + 0.037*SL	0.22 + 0.033*SL	0.60 + -0.007*SL
TCK to DOUT	t_{PLH}	1.48	1.45 + 0.018*SL	1.45 + 0.016*SL	1.64 + -0.004*SL
	t_{PHL}	1.52	1.46 + 0.030*SL	1.48 + 0.024*SL	1.76 + -0.006*SL
	t_R	0.20	0.15 + 0.025*SL	0.14 + 0.028*SL	0.46 + -0.006*SL
	t_F	0.29	0.22 + 0.035*SL	0.22 + 0.034*SL	0.61 + -0.007*SL
ENB to DOUT	t_{PLH}	1.53	1.49 + 0.018*SL	1.51 + 0.014*SL	1.67 + -0.004*SL
	t_{PHL}	1.56	1.51 + 0.029*SL	1.52 + 0.024*SL	1.80 + -0.006*SL
	t_R	0.21	0.15 + 0.026*SL	0.15 + 0.028*SL	0.47 + -0.006*SL
	t_F	0.28	0.21 + 0.036*SL	0.22 + 0.033*SL	0.60 + -0.007*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Cell Data

Input Loading (SL)	
DINP	3
TDI	0
MODE	1
SHIFT	1
UPDATE	1
SETN	0
TCK	1
ENB	0
Gate Count	
13	

Pin Description

Pin name	I/O	Description
DINP	I	Parallel Data Input Active Low
TDI	I	Serial Test Data Input
MODE	I	Mode Select Input—Low for Data Input and High for Internal Register Data Value
SHIFT	I	Active High Shift Control Input
UPDATE	I	Update Latch Input—Low for Update
SETN	I	Active Low Set Input
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable Input
DOUT	O	Parallel Data Output
TDO	O	Serial Test Data Output
INST	O	Updated Instruction Output

JTINT1

Tri-State I/O Control Scan Cell with Capture, Shift, Update and Set

Truth Table

DINP	TDI	MODE	SHIFT	UPDATE	SETN	TCK	ENB	OUTPUT
								DOUT
0	X	0	X	X	X	X	X	0
1	X	0	X	X	X	X	X	1
X	X	1	X	X	X	X	X	INST
								TDO
X	X	X	X	X	X	↑	0	TDOo
0	X	X	0	X	X	↑	1	0
1	X	X	0	X	X	↑	1	1
X	0	X	1	X	X	↑	1	0
X	1	X	1	X	X	↑	1	1
X	X	X	X	X	X	0	X	TDOo
X	X	X	X	X	X	1	X	TDOo
X	X	X	X	X	X	↓	X	TDOo
								INST
X	X	X	X	X	0	X	X	1
X	X	X	X	0	1	X	X	TDO
X	X	X	X	1	1	X	X	INSTo

NOTE: Outputs are defined in separate truth tables.

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Input Setup Time (TDI to TCK)	t_{SU}	0.57
Input Hold Time (TDI to TCK)	t_{HD}	0.33
Input Setup Time (TDI to ENB)	t_{SU}	0.60
Input Hold Time (TDI to ENB)	t_{HD}	0.33
Input Setup Time (DINPN to TCK)	t_{SU}	0.57
Input Hold Time (DINPN to TCK)	t_{HD}	0.33
Input Setup Time (DINPN to ENB)	t_{SU}	0.57
Input Hold Time (DINPN to ENB)	t_{HD}	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.68
Input Hold Time (SHIFT to TCK)	t_{HD}	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.68
Input Hold Time (SHIFT to ENB)	t_{HD}	0.33
Recovery Time (SETN)	t_{RC}	0.48

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.71	0.65 + 0.030*SL	0.66 + 0.028*SL	0.67 + 0.027*SL
	t_{PHL}	0.75	0.67 + 0.039*SL	0.68 + 0.034*SL	0.70 + 0.033*SL
	t_R	0.23	0.12 + 0.051*SL	0.11 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.11 + 0.063*SL	0.08 + 0.066*SL
ENB to TDO	t_{PLH}	0.70	0.64 + 0.030*SL	0.64 + 0.030*SL	0.68 + 0.026*SL
	t_{PHL}	0.79	0.72 + 0.039*SL	0.73 + 0.034*SL	0.74 + 0.033*SL
	t_R	0.23	0.12 + 0.052*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.10 + 0.063*SL	0.09 + 0.065*SL
DINP to DOUT	t_{PLH}	0.31	0.25 + 0.027*SL	0.29 + 0.014*SL	0.29 + 0.014*SL
	t_{PHL}	0.41	0.36 + 0.027*SL	0.38 + 0.021*SL	0.42 + 0.017*SL
	t_R	0.19	0.14 + 0.023*SL	0.12 + 0.029*SL	0.13 + 0.028*SL
	t_F	0.23	0.16 + 0.033*SL	0.16 + 0.033*SL	0.17 + 0.032*SL
MODE to DOUT	t_{PLH}	0.41	0.39 + 0.009*SL	0.37 + 0.019*SL	0.42 + 0.013*SL
	t_{PHL}	0.35	0.27 + 0.038*SL	0.32 + 0.023*SL	0.37 + 0.017*SL
	t_R	0.21	0.21 + 0.000*SL	0.13 + 0.028*SL	0.12 + 0.029*SL
	t_F	0.23	0.16 + 0.036*SL	0.16 + 0.035*SL	0.19 + 0.032*SL
UPDATE to DOUT	t_{PLH}	0.89	0.84 + 0.021*SL	0.86 + 0.016*SL	0.89 + 0.013*SL
	t_{PHL}	0.86	0.81 + 0.028*SL	0.82 + 0.024*SL	0.89 + 0.017*SL
	t_R	0.20	0.14 + 0.028*SL	0.13 + 0.030*SL	0.15 + 0.028*SL
	t_F	0.24	0.18 + 0.033*SL	0.18 + 0.032*SL	0.18 + 0.032*SL
SETN to DOUT	t_{PLH}	0.62	0.55 + 0.032*SL	0.60 + 0.016*SL	0.62 + 0.013*SL
	t_{PHL}	0.61	0.56 + 0.028*SL	0.57 + 0.022*SL	0.62 + 0.017*SL
	t_R	0.19	0.15 + 0.023*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.24	0.17 + 0.034*SL	0.17 + 0.034*SL	0.20 + 0.031*SL
TCK to DOUT	t_{PLH}	1.49	1.46 + 0.018*SL	1.46 + 0.015*SL	1.48 + 0.013*SL
	t_{PHL}	1.51	1.46 + 0.027*SL	1.47 + 0.022*SL	1.52 + 0.017*SL
	t_R	0.20	0.14 + 0.028*SL	0.14 + 0.027*SL	0.13 + 0.028*SL
	t_F	0.24	0.18 + 0.033*SL	0.18 + 0.032*SL	0.19 + 0.032*SL
ENB to DOUT	t_{PLH}	1.53	1.49 + 0.019*SL	1.50 + 0.016*SL	1.52 + 0.013*SL
	t_{PHL}	1.56	1.50 + 0.029*SL	1.52 + 0.022*SL	1.57 + 0.017*SL
	t_R	0.20	0.14 + 0.027*SL	0.14 + 0.027*SL	0.12 + 0.029*SL
	t_F	0.24	0.18 + 0.031*SL	0.17 + 0.035*SL	0.20 + 0.032*SL
UPDATE to INST	t_{PLH}	0.77	0.70 + 0.035*SL	0.72 + 0.029*SL	0.74 + 0.027*SL
	t_{PHL}	0.75	0.66 + 0.046*SL	0.69 + 0.033*SL	0.69 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.10 + 0.059*SL	0.09 + 0.060*SL
	t_F	0.23	0.11 + 0.062*SL	0.11 + 0.064*SL	0.09 + 0.065*SL
SETN to INST	t_{PLH}	0.52	0.46 + 0.030*SL	0.47 + 0.027*SL	0.47 + 0.027*SL
	t_{PHL}	0.45	0.37 + 0.039*SL	0.39 + 0.034*SL	0.40 + 0.033*SL
	t_R	0.22	0.11 + 0.056*SL	0.10 + 0.059*SL	0.09 + 0.060*SL
	t_F	0.24	0.12 + 0.060*SL	0.11 + 0.064*SL	0.09 + 0.066*SL

(Continued)

JTINT1

Tri-State I/O Control Scan Cell with Capture, Shift, Update and Set

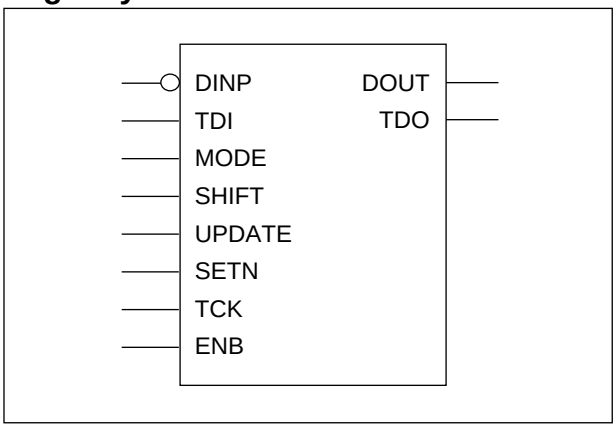
Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to INST	t_{PLH}	1.42	1.36 + 0.028*SL	1.37 + 0.027*SL	1.37 + 0.027*SL
	t_{PHL}	1.39	1.31 + 0.040*SL	1.33 + 0.034*SL	1.34 + 0.033*SL
	t_R	0.22	0.11 + 0.057*SL	0.10 + 0.059*SL	0.09 + 0.060*SL
	t_F	0.24	0.10 + 0.070*SL	0.12 + 0.064*SL	0.11 + 0.065*SL
ENB to INST	t_{PLH}	1.41	1.35 + 0.027*SL	1.35 + 0.029*SL	1.37 + 0.027*SL
	t_{PHL}	1.44	1.36 + 0.039*SL	1.37 + 0.034*SL	1.38 + 0.033*SL
	t_R	0.22	0.11 + 0.054*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.10 + 0.068*SL	0.11 + 0.064*SL	0.10 + 0.065*SL

*Group1 : SL < 3, *Group2 : 3 ≦ SL ≦ 10, *Group3 : 10 < SL

Logic Symbol



Cell Data

Input Loading (SL)	
DINP	3
TDI	0
MODE	1
SHIFT	1
UPDATE	1
SETN	0
TCK	1
ENB	0
Gate Count	
12	

Pin Description

Pin name	I/O	Description
DINP	I	Parallel Data Input Active Low
TDI	I	Serial Test Data Input
MODE	I	Mode Select Input—Low for Data Input and High for Internal Register Data Value
SHIFT	I	Active High Shift Control Input
UPDATE	I	Update Latch Input—Low for Update
SETN	I	Active Low Set Input
TCK	I	Test Clock Input
ENB	I	Active High Test Clock Enable Input
DOUT	O	Parallel Data Output
TDO	O	Serial Test Data Output

JTOUT1

Output Scan Cell with Capture, Shift, Update and Set

Truth Table

DINP	TDI	MODE	SHIFT	UPDATE	SETN	TCK	ENB	OUTPUT
								DOUT
0	X	0	X	X	X	X	X	0
1	X	0	X	X	X	X	X	1
X	X	1	X	X	X	X	X	LatchQ
								TDO
X	X	X	X	X	X	↑	0	TDOo
0	X	X	0	X	X	↑	1	0
1	X	X	0	X	X	↑	1	1
X	0	X	1	X	X	↑	1	0
X	1	X	1	X	X	↑	1	1
X	X	X	X	X	X	0	X	TDOo
X	X	X	X	X	X	1	X	TDOo
X	X	X	X	X	X	↓	X	TDOo
								LatchQ
X	X	X	X	X	0	X	X	1
X	X	X	X	0	1	X	X	TDO
X	X	X	X	1	1	X	X	LatchQo

NOTE: Outputs are defined in separate truth tables. In addition, an internal state known as “LatchQ” is defined as the output of the latch in the logic diagram.

Timing Requirements

(Typical process, 25°C, 3.3V)

Parameter	Symbol	Value (ns)
Input Setup Time (TDI to TCK)	t_{SU}	0.49
Input Hold Time (TDI to TCK)	t_{HD}	0.33
Input Setup Time (TDI to ENB)	t_{SU}	0.58
Input Hold Time (TDI to ENB)	t_{HD}	0.33
Input Setup Time (DINP to TCK)	t_{SU}	0.57
Input Hold Time (DINP to TCK)	t_{HD}	0.33
Input Setup Time (DINP to ENB)	t_{SU}	0.57
Input Hold Time (DINP to ENB)	t_{HD}	0.33
Input Setup Time (SHIFT to TCK)	t_{SU}	0.68
Input Hold Time (SHIFT to TCK)	t_{HD}	0.33
Input Setup Time (SHIFT to ENB)	t_{SU}	0.74
Input Hold Time (SHIFT to ENB)	t_{HD}	0.33
Recovery Time (SETN)	t_{RC}	0.48

Switching Characteristics

(Typical process, 25°C, 3.3V, t_R/t_F = 0.35ns, SL: Standard Load)

Path	Parameter	Delay [ns] SL = 2	Delay Equations [ns]		
			Group1*	Group2*	Group3*
TCK to TDO	t_{PLH}	0.68	0.62 + 0.030*SL	0.63 + 0.028*SL	0.64 + 0.027*SL
	t_{PHL}	0.75	0.67 + 0.039*SL	0.69 + 0.034*SL	0.70 + 0.033*SL
	t_R	0.23	0.12 + 0.051*SL	0.10 + 0.058*SL	0.08 + 0.060*SL
	t_F	0.24	0.11 + 0.063*SL	0.11 + 0.063*SL	0.09 + 0.066*SL
ENB to TDO	t_{PLH}	0.72	0.66 + 0.031*SL	0.67 + 0.027*SL	0.67 + 0.027*SL
	t_{PHL}	0.79	0.72 + 0.039*SL	0.73 + 0.034*SL	0.74 + 0.033*SL
	t_R	0.22	0.11 + 0.055*SL	0.11 + 0.057*SL	0.08 + 0.060*SL
	t_F	0.23	0.11 + 0.064*SL	0.11 + 0.063*SL	0.09 + 0.065*SL
DINP to DOUT	t_{PLH}	0.31	0.25 + 0.027*SL	0.29 + 0.014*SL	0.29 + 0.014*SL
	t_{PHL}	0.41	0.36 + 0.027*SL	0.38 + 0.021*SL	0.42 + 0.017*SL
	t_R	0.19	0.14 + 0.023*SL	0.12 + 0.029*SL	0.13 + 0.028*SL
	t_F	0.23	0.16 + 0.033*SL	0.16 + 0.033*SL	0.17 + 0.032*SL
MODE to DOUT	t_{PLH}	0.42	0.38 + 0.020*SL	0.39 + 0.016*SL	0.42 + 0.013*SL
	t_{PHL}	0.36	0.30 + 0.028*SL	0.32 + 0.022*SL	0.37 + 0.017*SL
	t_R	0.20	0.15 + 0.028*SL	0.15 + 0.028*SL	0.14 + 0.028*SL
	t_F	0.23	0.16 + 0.036*SL	0.17 + 0.032*SL	0.17 + 0.032*SL
UPDATE to DOUT	t_{PLH}	0.85	0.79 + 0.032*SL	0.84 + 0.015*SL	0.85 + 0.013*SL
	t_{PHL}	0.84	0.79 + 0.025*SL	0.79 + 0.024*SL	0.85 + 0.017*SL
	t_R	0.19	0.15 + 0.023*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.25	0.18 + 0.038*SL	0.19 + 0.032*SL	0.21 + 0.031*SL
SETN to DOUT	t_{PLH}	0.61	0.57 + 0.019*SL	0.58 + 0.016*SL	0.61 + 0.013*SL
	t_{PHL}	0.60	0.54 + 0.029*SL	0.56 + 0.023*SL	0.61 + 0.017*SL
	t_R	0.19	0.13 + 0.031*SL	0.15 + 0.026*SL	0.13 + 0.028*SL
	t_F	0.25	0.17 + 0.038*SL	0.18 + 0.033*SL	0.20 + 0.031*SL
TCK to DOUT	t_{PLH}	1.47	1.43 + 0.017*SL	1.44 + 0.016*SL	1.46 + 0.013*SL
	t_{PHL}	1.49	1.44 + 0.026*SL	1.45 + 0.022*SL	1.49 + 0.017*SL
	t_R	0.19	0.14 + 0.026*SL	0.14 + 0.027*SL	0.12 + 0.028*SL
	t_F	0.25	0.17 + 0.037*SL	0.18 + 0.033*SL	0.20 + 0.032*SL
ENB to DOUT	t_{PLH}	1.51	1.47 + 0.019*SL	1.48 + 0.015*SL	1.50 + 0.013*SL
	t_{PHL}	1.56	1.50 + 0.029*SL	1.52 + 0.022*SL	1.56 + 0.017*SL
	t_R	0.19	0.15 + 0.024*SL	0.13 + 0.028*SL	0.13 + 0.028*SL
	t_F	0.25	0.17 + 0.037*SL	0.19 + 0.031*SL	0.18 + 0.032*SL

*Group1 : SL < 3, *Group2 : 3 ≦SL≦ 10, *Group3 : 10 < SL

JTAG TAP CONTROLLER MACROFUNCTION

TAP controller macrofunction consists of instruction register and data register scan paths, a bypass register, multiplexers and a 16-state finite state machine. The bypass register and instruction register are JTAG devices. TAP controller uses the largest available internal buffers (IVD8) to drive data register control signals.

Instruction register/decoder are external to TAP controller since the register length and instruction codes vary from one ASIC design to another. The instruction register consists of three JTINT1 macrocells. The instruction decoder is used to implement a minimum TAP configuration with a boundary scan register and an optional identification register.

TAP Controller Input Pin Description

Name	Mandatory	Description
BPSEL		Bypass select
DREGDI		Data register scan path data-in
IREGDI		Instruction register scan path data-in
TCK	•	Test clock
TDI	•	Test data input to the bypass register
TMS	•	Test mode select controlling state transitions of a finite state machine
TRSTN		Test reset input

TAP Controller Output Pin Description

Name	Mandatory	Description
DRE		Data register enable control output
IRE		Instruction register enable control output
RSTO		Reset output
SHFDR		Data register shift control output
SHFIR		Instruction register shift control output
TDO	•	Test data output
TDOE		TDO tri-state enable output
UPDATEDR		Data register update control output
UPDATEIR		Instruction register update control output

The bulleted pins (TCK, TDI, TMS and TDO) are mandatory pins associated with the IEEE P1149.1 standard test bus interface. TRSTN is an optional test reset input. It is possible to implement TAP without the test reset input indicated in the IEEE P1149.1 standard by setting TRSTN pin to high logic state. Alternatively, if a power-on reset capability is desired, TRSTN pin should be set to active low and connected to the power-on reset circuitry.

The 16 states of the finite state machine, diagrammed in the figure 9-3, also comply with the proposed IEEE P1149.1 standard. State transitions occur on the rising edge of TCK and are controlled by TMS. To ensure stable state transitions, TMS transitions occur on the falling edges of TCK. Capture, shift or update of test data take place on the next rising edge of TCK after the state transition or on each subsequent rising edge of TCK if no state transition occurs.

Figure 7-3. TAP Controller I/O Pin-Out Diagram

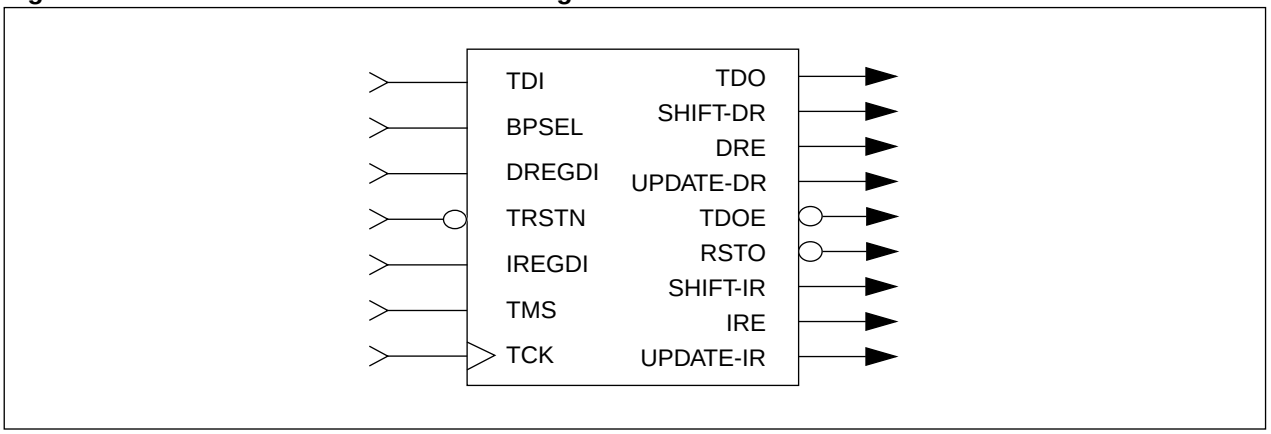
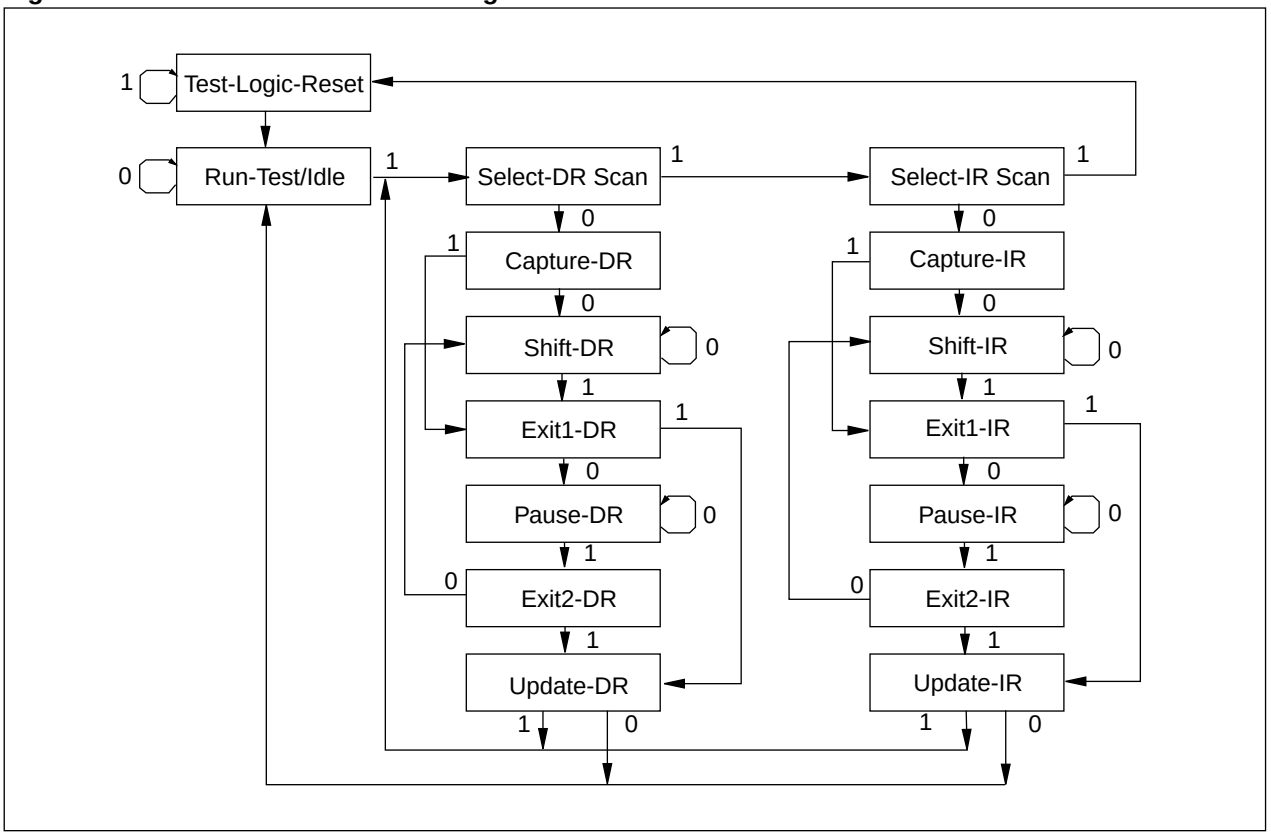


Figure 7-4. TAP Controller State Diagram



Behavior of TAP Controller States

Test-Logic-Reset

An initialization of the instruction register disables the test logic, allowing the on-chip system logic to operate normally. Irrespective of its original state, TAP controller reverts to Test-Logic-Reset when TMS is maintained high for five rising edges of TCK.

Run-Test/Idle

Idles in the state between scan operations or self-tests.

Capture-DR

Loads data parallelly into test data registers selected by the current instruction on the rising edge of TCK.

Shift-DR

Shifts data in the test data register between TDI and TDO one stage towards its serial output on each rising edge of TCK.

Pause-DR

Temporarily halts test data register shifts in the serial path between TDI and TDO.

Update-DR

Latches the data from the shift register path to the parallel output of test data registers on the falling edge of TCK.

Capture-IR

The shift-register contained in the instruction register loads a pattern of fixed logic value on the rising edge of TCK. It is possible to load design-specific data into shift-register stages that are not set to fixed values.

Shift-IR

Shifts data contained in the shift-register of the instruction register between TDI and TDO one stage towards its serial output on each rising edge of TCK.

Pause-IR

Temporarily halts shifting of the instruction register.

Update-IR

Latches the instruction shifted into the instruction register to the parallel output from the shift register path on the falling edge of TCK.

Select-DR-Scan, Select-IR-Scan, Exit1-DR, Exit2-DR, Exit1-IR, Exit2-IR

They are temporary controller states.

State Assignments for TAP Controller

Table 7-1. State Assignments

Controller State	State [3:0]	Controller State	State [3:0]
Exit2-DR	0	Exit2-IR	8
Exit1-DR	1	Exit1-IR	9
Shift-DR	2	Shift-IR	A
Pause-DR	3	Pause-IR	B
Select-IR Scan	4	Run-Test/Idle	C
Update-DR	5	Update-IR	D
Capture-DR	6	Capture-IR	E
Select-DR-Scan	7	Test-Logic-Reset	F

The bypass circuitry captures a low state during the data capture state of the finite state machine data cycle, as required by the proposed IEEE 1149.1 standard.

INSTRUCTION REGISTER/DECODER MACROFUNCTION

Instruction Register Macrofunction

The instruction register provides eight instructions in a minimum 3-bit device. These 3 bits are sufficient for operations of boundary scan cells and an instruction register, and three other operations such as the internal scan chains. Devices requiring more than eight instructions need a customer-specific design.

The instruction register allows an instruction to be shifted into the design. The instruction defines the test to be performed or the test data register to access or both. If a device identification register is present, the output register must be initialized to IDCODE instruction when TAP controller is in the Test-Logic-Reset state. Alternatively, it may be initialized to the bypass instruction. To support a fault isolation at the board-level, a constant binary ‘01’ pattern is loaded into the least significant bits of the instruction register when it is in the Capture-IR state.

Instruction Decoder Macrofunction

The instruction decoder operates with the instruction register to provide boundary scan control. Designs requiring other options need a customer-specific design.

Instruction Decoder Input Pin Description:

Name	Description
INST (2:0)	Instruction register input

Instruction Decoder Output Pin Description:

Name	Description
0_Mode	Boundary scan output mode control
I_Mode	Boundary scan input mode control

The instruction decoder has the following truth table.

INST(2)	INST(1)	INST(0)	I_Mode	0_Mode
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

IMPLEMENTATION OF IEEE P1149.1/JTAG

The following design procedures should be followed for ASIC implementation of IEEE P1149.1/JTAG using SEC boundary scan cells:

1. Allocate four (optionally five) package pins for testing.
2. Generate a bonding diagram, including provision for the corner pads that cannot be used for boundary scan I/Os.
3. Configure the top level device symbol with the same pin-out sequence as the packaged device.
4. Select appropriate boundary scan macrocells, JTBI1, JTCK, JTIN1 and JTOUT1, for the boundary-scan I/O pads. JTCK and JTIN1 must be associated with inputs; JTOUT1 with outputs and JTBI1 with bi-directional inputs and outputs.
5. ASIC clock inputs generally use JTCK macrocell, but it may be used for other critical inputs where performance considerations dominate. JTOUT1 macrocells are used for each output pin and JTBI1 macrocells are used by bi-directional pins.
6. JTAG inputs (TDI, TCK, TMS), output (TDO) and optional TRSTN are connected to TAP controller. The boundary scan register and the instruction register are connected to TDI and TCK inputs. Inputs, TDI, TMS and TRSTN should have input pull-up resistors.
7. To start the boundary scan chain sequence, connect any TDI input to JTBI1, JTCK, JTIN1, or JTOUT1 macrocells. The chain sequence proceeds to each adjacent macrocell I/O pad until terminated. TDO output of the final macrocell is connected to DREGDI input of TAP controller. Similarly, the terminal TDO output of the instruction register is connected to IREGDI of TAP controller.
8. Instruction register and data register control signals are connected to the instruction register and boundary scan registers, and INST signal lines from the instruction register are connected to the instruction decoder which supplies the control signals BPSEL, I_Mode and O_Mode for TAP controller and the boundary scan register. I_Mode is connected to JTIN1 macrocells and O_Mode is connected to JTOUT1 macrocells. I_Mode, O_Mode and MODE1 are also connected to the appropriate inputs of JTBI1 macrocells.
9. I_MODE output is connected to a IVD8 macrocell and TN inputs of the bi-directional and tri-state output buffers associated with the respective I/O pads. Other buffers may be required if there are a large number of bi-directional or tri-state pads.
10. If the design requires internal tri-state enable control signals, an additional JTINT1 macrocell is needed for each enable. Internal enable macrocells should be connected to TAP controller RSTO signal and O_MODE control line. JTIN1 macrocell is used for external tri-state enable input signals and should be connected to TAP controller RSTO signal and I_MODE control line.
11. Generate the test patterns to test JTAG portion of the design.

SYSTEM CLOCK CONSIDERATIONS

Test and system clocks must be synchronized carefully. All phases of the system clock should be gated on and off at a central point within the system. When TMS input is high, TCK can run continuously and test modes is disabled.