Ordering number : ENN7183

N-Channel and P-Channel Silicon MOSFETs

CPH6605

Load Switching Applications

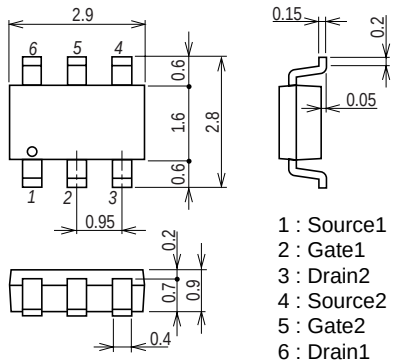
Features

- Dual chip device for high-density mounting.
  One of the encapsulated devices is a P-channel MOSFET featuring low ON-resistance and high-speed switching. The other is an N-channel small signal MOSFET used for driving the P-channel MOSFET.
- Optimal for load switch use.
- Excellent ON-resistance characteristic.
- 2.5V drive.

Package Dimensions

unit : mm
2202

[CPH6605]



1 : Source1
2 : Gate1
3 : Drain2
4 : Source2
5 : Gate2
6 : Drain1

SANYO : CPH6

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	N-channel	P-channel	Unit
Drain-to-Source Voltage	V_{DSS}		30	–20	V
Gate-to-Source Voltage	V_{GSS}		±10	±10	V
Drain Current (DC)	I_D		0.65	–1.5	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	2.6	–6.0	A
Allowable Power Dissipation	P_D	Mounted on a ceramic board (900mm²X0.8mm)1unit	0.8		W
Channel Temperature	Tch		150		°C
Storage Temperature	Tstg		–55 to +150		°C

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[N-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0	30			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0			10	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±8V, V_{DS}=0			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=10V, I_D=100μA	0.4		1.3	V
Forward Transfer Admittance	|yfs|	V_{DS}=10V, I_D=150mA	400	560		mS
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=150mA, V_{GS}=4V		0.9	1.2	Ω
	R_{DS}(on)2	I_D=80mA, V_{GS}=2.5V		1.2	1.7	Ω
	R_{DS}(on)3	I_D=10mA, V_{GS}=1.5V		2.6	5.2	Ω

Marking : FQ

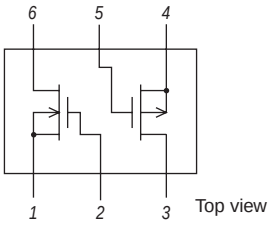
Continued on next page.

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input Capacitance	Ciss	V_{DS}=10V, f=1MHz		30		pF
Output Capacitance	Coss	V_{DS}=10V, f=1MHz		15		pF
Reverse Transfer Capacitance	Crss	V_{DS}=10V, f=1MHz		10		pF
Turn-ON Delay Time	t_{d}(on)	See specified Test Circuit.		32		ns
Rise Time	t_{r}	See specified Test Circuit.		110		ns
Turn-OFF Delay Time	t_{d}(off)	See specified Test Circuit.		250		ns
Fall Time	t_{f}	See specified Test Circuit.		160		ns
Total Gate Charge	Qg	V_{DS}=10V, V_{GS}=10V, I_{D}=300mA		2.34		nC
Gate-to-Source Charge	Qgs	V_{DS}=10V, V_{GS}=10V, I_{D}=300mA		0.38		nC
Gate-to-Drain “Miller” Charge	Qgd	V_{DS}=10V, V_{GS}=10V, I_{D}=300mA		0.45		nC
Diode Forward Voltage	V_{SD}	I_{S}=300mA, V_{GS}=0		0.8	1.2	V
[P-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_{D}=−1mA, V_{GS}=0	−20			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=−20V, V_{GS}=0			−1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±8V, V_{DS}=0			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=−10V, I_{D}=−1mA	−0.4		−1.3	V
Forward Transfer Admittance	|yfs|	V_{DS}=−10V, I_{D}=−800mA	1.6	2.3		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_{D}=−800mA, V_{GS}=−4V		180	235	mΩ
	R_{DS}(on)2	I_{D}=−400mA, V_{GS}=−2.5V		240	340	mΩ
Input Capacitance	Ciss	V_{DS}=−10V, f=1MHz		290		pF
Output Capacitance	Coss	V_{DS}=−10V, f=1MHz		40		pF
Reverse Transfer Capacitance	Crss	V_{DS}=−10V, f=1MHz		25		pF
Turn-ON Delay Time	t_{d}(on)	See specified Test Circuit.		10		ns
Rise Time	t_{r}	See specified Test Circuit.		35		ns
Turn-OFF Delay Time	t_{d}(off)	See specified Test Circuit.		32		ns
Fall Time	t_{f}	See specified Test Circuit.		27		ns
Total Gate Charge	Qg	V_{DS}=−10V, V_{GS}=−4V, I_{D}=−1.5A		3.2		nC
Gate-to-Source Charge	Qgs	V_{DS}=−10V, V_{GS}=−4V, I_{D}=−1.5A		0.8		nC
Gate-to-Drain “Miller” Charge	Qgd	V_{DS}=−10V, V_{GS}=−4V, I_{D}=−1.5A		0.6		nC
Diode Forward Voltage	V_{SD}	I_{S}=−1.5A, V_{GS}=0		−0.82	−1.2	V

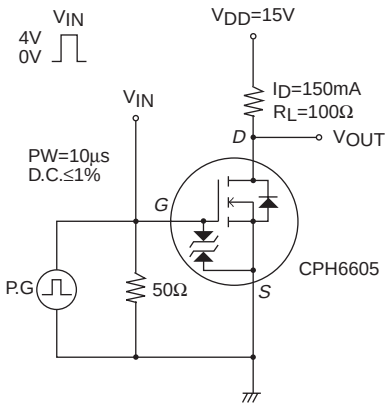
Electrical Connection



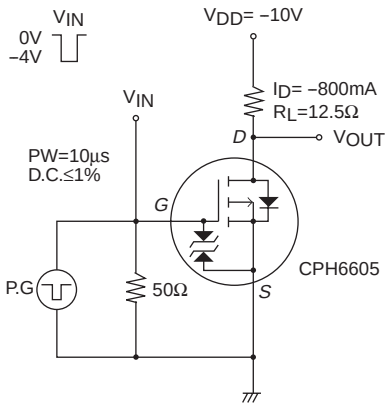
1 : Source1
2 : Gate1
3 : Drain2
4 : Source2
5 : Gate2
6 : Drain1

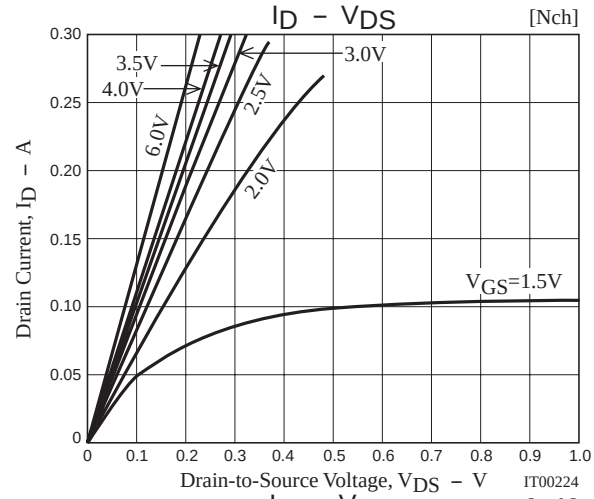
Switching Time Test Circuit

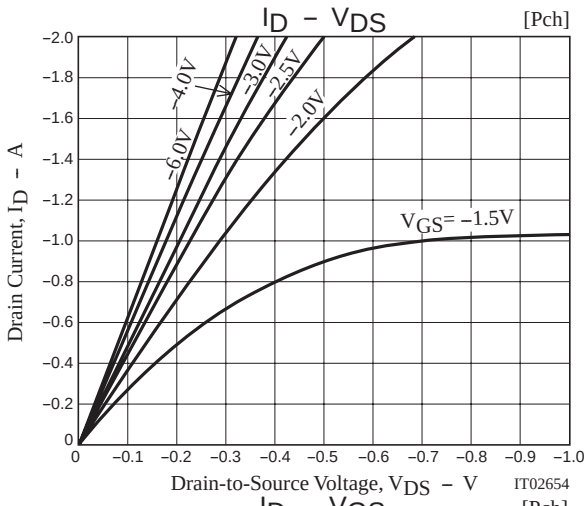
[N-channel]

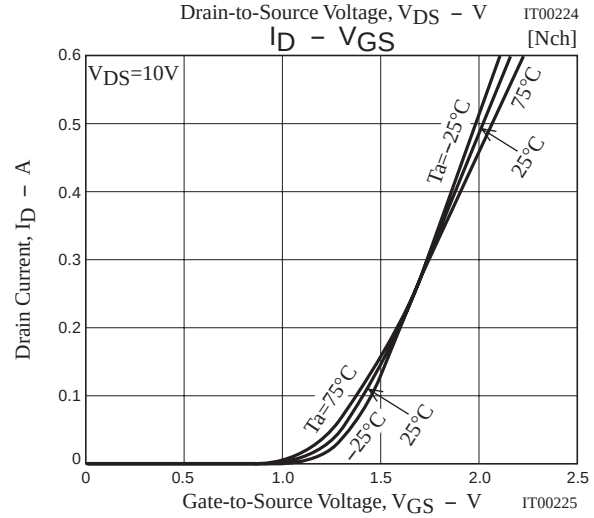


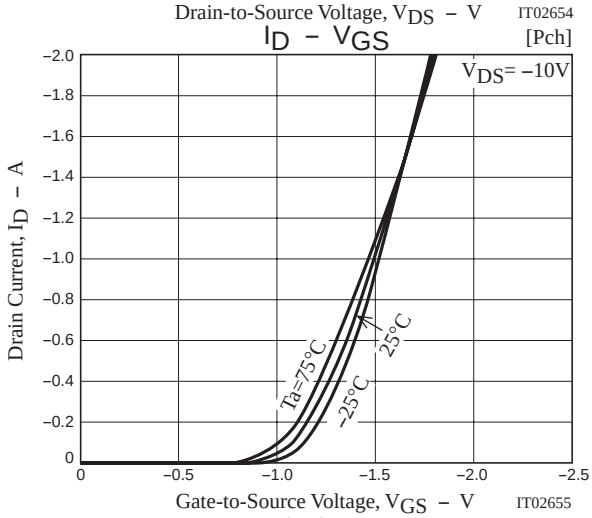
[P-channel]

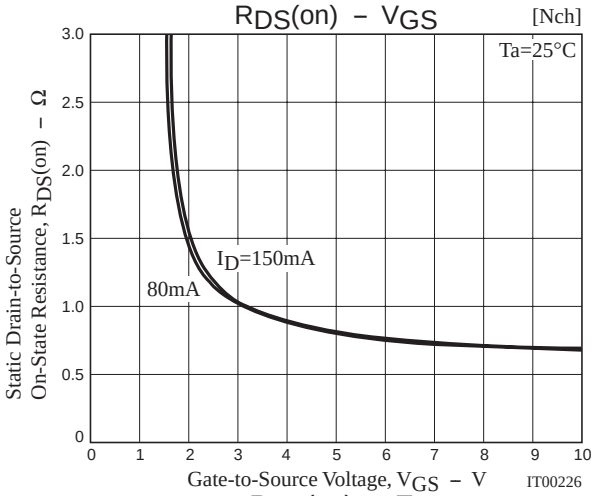


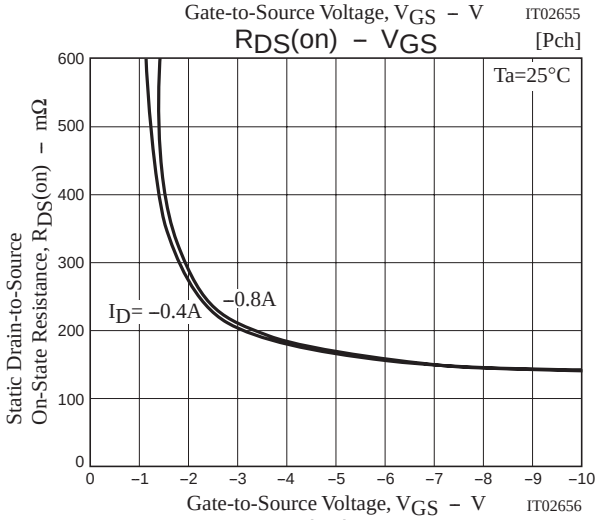

ID – VDS
[Nch]
3.5V
4.0V
3.0V
2.5V
6.0V
2.0V
VGS=1.5V
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT00224

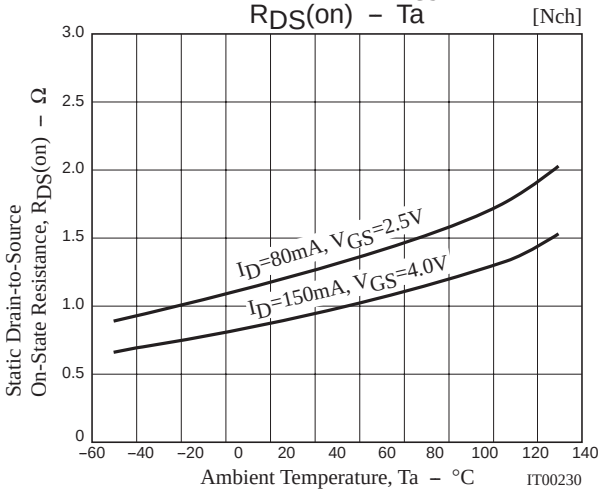

ID – VDS
[Pch]
–4.0V
–3.0V
–2.5V
–6.0V
–2.0V
VGS= –1.5V
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT02654

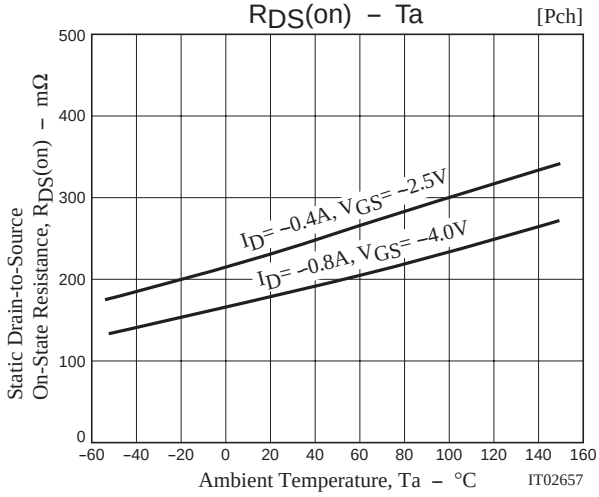

ID – VGS
[Nch]
VDS=10V
75°C
Ta=–25°C
25°C
Ta=75°C
–25°C
25°C
Drain Current, ID – A
Gate-to-Source Voltage, VGS – V
IT00225

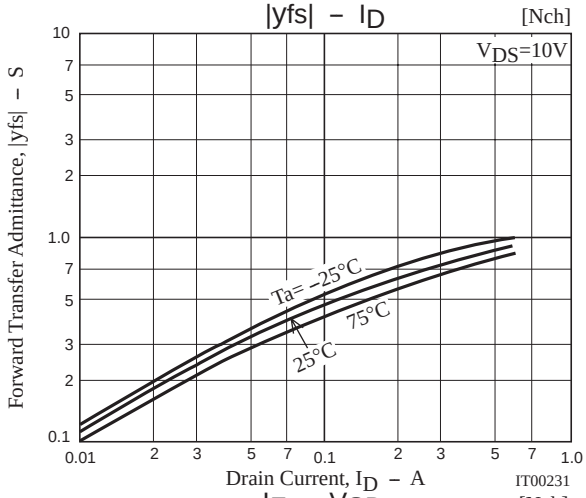

ID – VGS
[Pch]
VDS= –10V
25°C
Ta=75°C
–25°C
Drain Current, ID – A
Gate-to-Source Voltage, VGS – V
IT02655

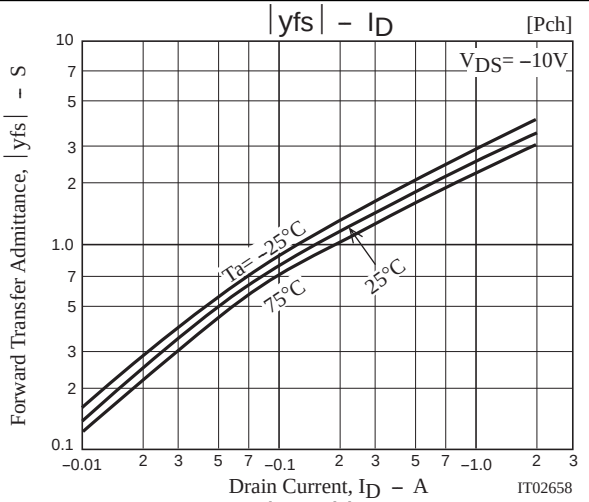

RDS(on) – VGS
[Nch]
Ta=25°C
ID=150mA
80mA
Static Drain-to-Source On-State Resistance, RDS(on) – Ω
Gate-to-Source Voltage, VGS – V
IT00226

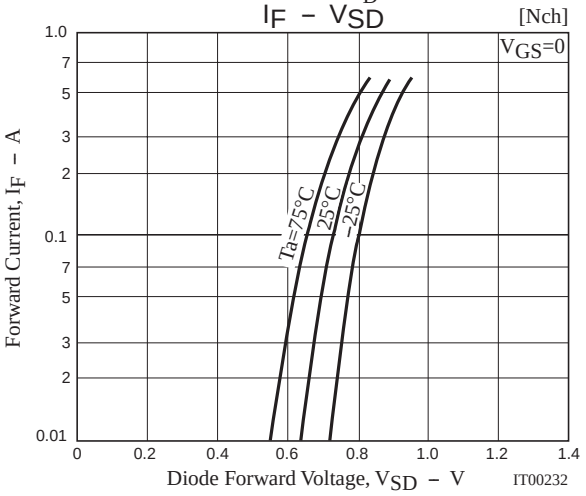

RDS(on) – VGS
[Pch]
Ta=25°C
ID= –0.4A
–0.8A
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage, VGS – V
IT02656

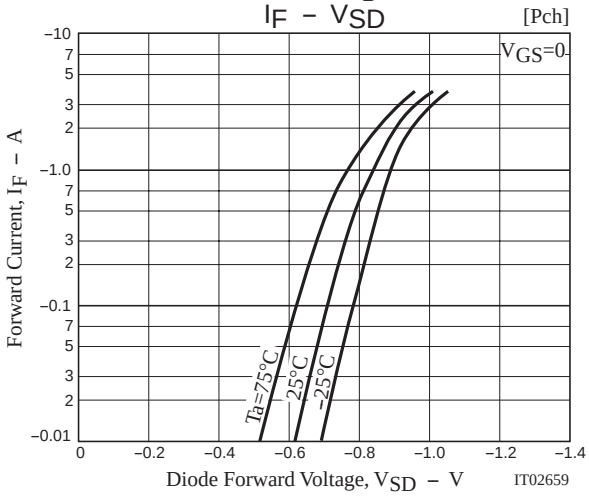

RDS(on) – Ta
[Nch]
ID=80mA, VGS=2.5V
ID=150mA, VGS=4.0V
Static Drain-to-Source On-State Resistance, RDS(on) – Ω
Ambient Temperature, Ta – °C
IT00230

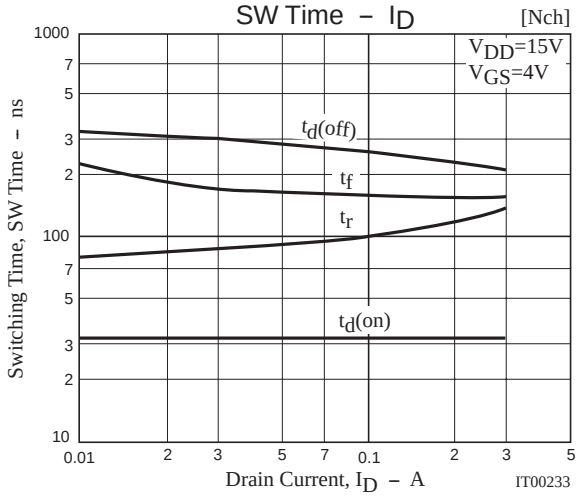

RDS(on) – Ta
[Pch]
ID= –0.4A, VGS= –2.5V
ID= –0.8A, VGS= –4.0V
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Ambient Temperature, Ta – °C
IT02657

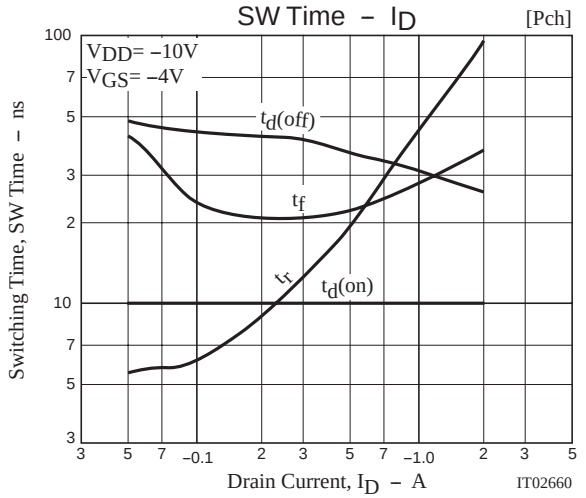

|yfs| – ID
[Nch]
VDS=10V
Ta= –25°C
75°C
25°C
Forward Transfer Admittance, |yfs| – S
Drain Current, ID – A
IT00231

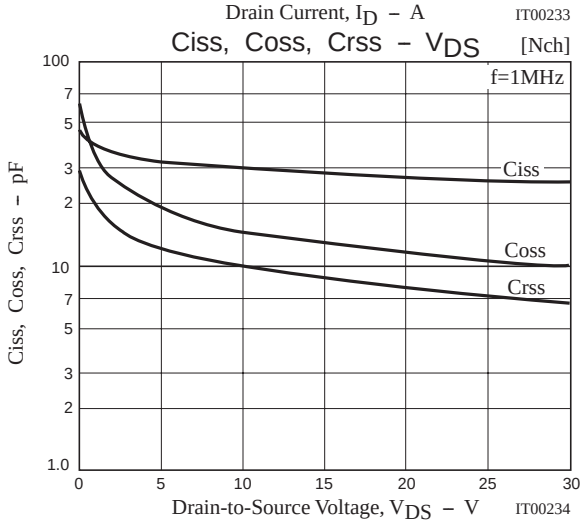

|yfs| – ID
[Pch]
VDS= –10V
Ta= –25°C
75°C
25°C
Forward Transfer Admittance, |yfs| – S
Drain Current, ID – A
IT02658

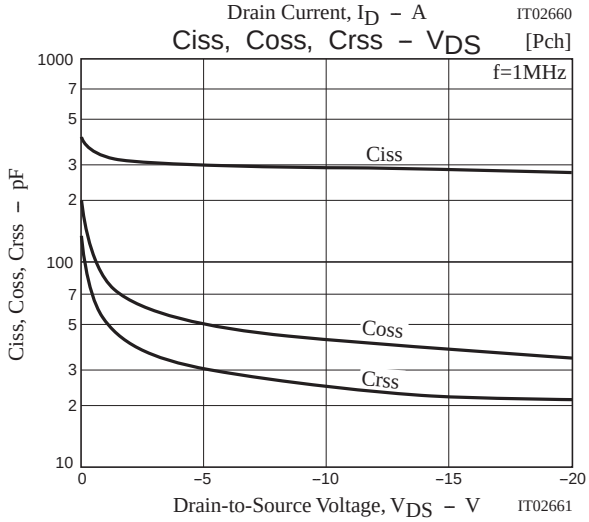

IF – VSD
[Nch]
VGS=0
Ta=75°C
25°C
–25°C
Forward Current, IF – A
Diode Forward Voltage, VSD – V
IT00232

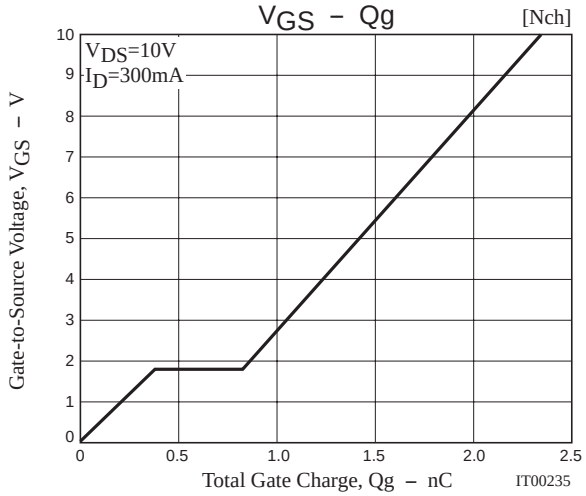

IF – VSD
[Pch]
VGS=0
Ta=75°C
25°C
–25°C
Forward Current, IF – A
Diode Forward Voltage, VSD – V
IT02659

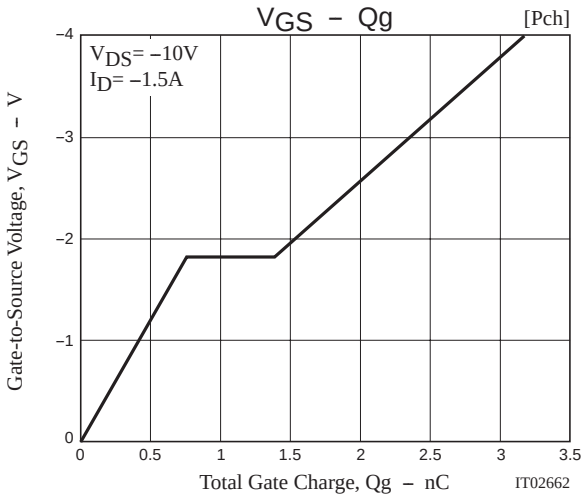

SW Time – ID
[Nch]
VDD=15V
VGS=4V
td(off)
tf
tr
td(on)
Switching Time, SW Time – ns
Drain Current, ID – A
IT00233

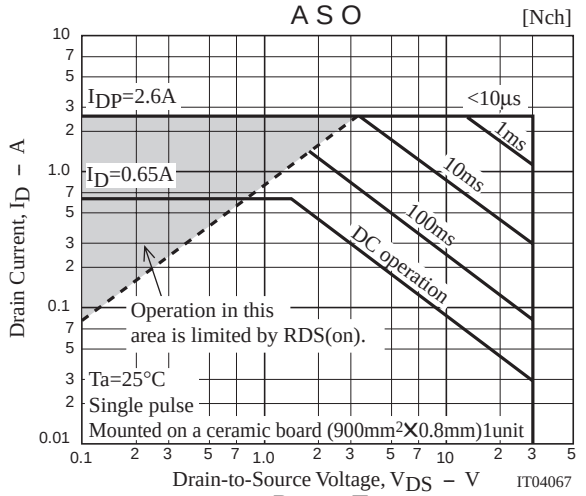

SW Time – ID
[Pch]
VDD= –10V
VGS= –4V
td(off)
tf
tr
td(on)
Switching Time, SW Time – ns
Drain Current, ID – A
IT02660

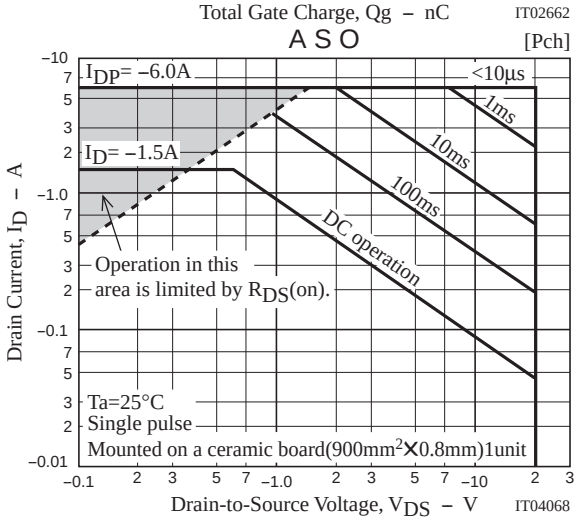

Ciss, Coss, Crss – VDS
[Nch]
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT00234

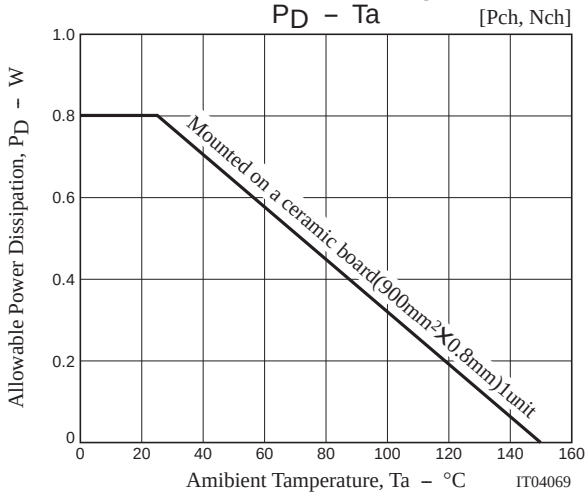

Ciss, Coss, Crss – VDS
[Pch]
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT02661


VGS – Qg
[Nch]
VDS=10V
ID=300mA
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT00235


VGS – Qg
[Pch]
VDS= –10V
ID= –1.5A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT02662


A S O
[Nch]
IDP=2.6A
ID=0.65A
<10µs
1ms
10ms
100ms
DC operation
Operation in this
area is limited by RDS(on).
Ta=25°C
Single pulse
Mounted on a ceramic board (900mm2×0.8mm)1unit
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT04067


A S O
[Pch]
IDP= –6.0A
ID= –1.5A
<10µs
1ms
10ms
100ms
DC operation
Operation in this
area is limited by RDS(on).
Ta=25°C
Single pulse
Mounted on a ceramic board(900mm2×0.8mm)1unit
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT04068


PD – Ta
[Pch, Nch]
Mounted on a ceramic board(900mm2×0.8mm)1unit
Allowable Power Dissipation, PD – W
Amibient Tamperature, Ta – °C
IT04069

Note on usage : Since the CPH6605 is designed for high-speed switching applications, please avoid using this device in the vicinity of highly charged objects.