Ordering number : ENN6471

Monolithic Linear IC

LA8519M

I/O Switch/Voice Signal-Processing IC for Cordless Telephones

Overview

The LA8519M is a cordless telephone base unit IC that provides I/O switching, voice signal processing, and other functions. It integrates, on a single chip, crosspoint switch, power amplifier, electronic volume and tone control, microphone amplifier, speech network, and other functions.

Functions

- Speech network block
  - — Impedance matching, 2-wire/4-wire converter, line driver, BN circuit network switching circuit, transmitter amplifier, BTL receiver amplifier, DTMF input, key tone input, receiver volume level switching, and power supply switching circuit.

- Audio signal-processing block
  - — Power amplifier, electronic volume and tone control, preamplifier with ALC, voice level detection (VOX), beep tone input, ring tone (OSC) input, ring tone level switching, line volume level switching, microphone amplifier, crosspoint switch (10 × 9 point equivalent), and serial interface.

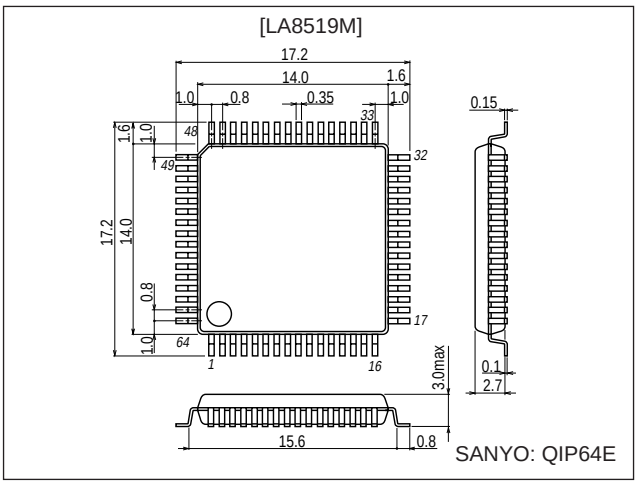
Features

- Allows switching between two anti-sidetone networks (near terminal/far terminal) depending on the line current, and thus achieves excellent sidetone characteristics over a wide range of line currents.
- Built-in transmitter/receiver amplifier driver power supply switching circuit allows communication using extension without power from the telephone network.
- The receiver amplifier supports both ceramic receivers (BTL) and dynamic receiver (single).
- Built-in power amplifier (load: 8 to 32 Ω): V_{CC} = 5 V, R_L = 8 Ω, Pomax = 200 mW
- The power amplifier signal path includes an electronic volume control (7 steps of about 3.8 dB each)
- Includes a 10-input/9-output crosspoint switch that provides mixing functions for easy implementation of systems that support a diverse range of signal path switching functions.

Package Dimensions

Unit:mm

3159-QIP64E



SANYO Electric Co.,Ltd. Semiconductor Company

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		15	V
	V_L max		15	V
Line current	I_L max		130	mA
Allowable power dissipation	Pd max	Ta ≤ 70°C (Mounted on a glass epoxy board: 120 × 120 × 1.6 mm^3)	1000	mW
Operating temperature	Topr		–20 to +70	°C
Storage temperature	Tstg		–40 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}	Other than the speech network	5.0	V
Allowable operating supply voltage range	V_{CC} op	Pin 17	4.5 to 6.5	V
	V_{CC} oppwr	Pin 28	4.5 to 9.5	V

Electrical Characteristics

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
[Speech Network Block] at Ta = 25°C, Power supplied: V_{CC} = 5 V, f_{IN} = 1 kHz						
Line voltage (20 mA, power supplied/power off)	V_L1	I_L = 20 mA	3.3	3.8	4.3	V
Line voltage (50 mA, power supplied/power off)	V_L2	I_L = 50 mA	4.5	5.2	6.0	V
Line voltage (120 mA, power supplied)	EV_L3	I_L = 120 mA	7.1	8.5	9.9	V
Line voltage (120 mA, power off)	L_V3	I_L = 120 mA	7.0	8.4	9.8	V
Transmitter gain (20 mA, power supplied)	EGt1	I_L = 20 mA, V_{IN} = –55 dBV	42.5	44.5	46.5	dB
Transmitter gain (20 mA, power off)	Gt1	I_L = 20 mA, V_{IN} = –55 dBV	42.3	44.3	46.3	dB
Transmitter gain (120 mA, power supplied/power off)	Gt2	I_L = 120 mA, V_{IN} = –55 dBV	38.3	40.3	42.3	dB
Receiver gain (20 mA, power supplied)	EGr1	I_L = 20 mA, V_{IN} = –20 dBV	–0.9	1.1	3.1	dB
Receiver gain (120 mA, power supplied)	EGr2	I_L = 120 mA, V_{IN} = –20 dBV	–7.4	–5.4	–3.4	dB
Receiver gain (20 mA, power off)	Gr1	I_L = 20 mA, V_{IN} = –20 dBV	–5.4	–3.4	–1.4	dB
Receiver gain (120 mA, power off)	Gr2	I_L = 120 mA, V_{IN} = –20 dBV	–8.7	–6.7	–4.7	dB
DTMF gain (20 mA, power supplied/power off)	Gmf1	I_L = 20 mA, V_{IN} = –30 dBV	27.7	29.7	31.7	dB
DTMF gain (120 mA, power supplied/power off)	Gmf2	I_L = 120 mA, V_{IN} = –30 dBV	23.6	25.6	27.6	dB
KT gain (power supplied)	EGkt	I_L = 20 mA/120 mA, V_{IN} = –40 dBV	10.0	12.0	14.0	dB
KT gain (20 mA, power off)	Gkt1	I_L = 20 mA, V_{IN} = –40 dBV	5.8	7.8	9.8	dB
KT gain (120 mA, power off)	Gkt2	I_L = 120 mA, V_{IN} = –40 dBV	9.0	11.0	13.0	dB
Transmitter dynamic range (20 mA, power supplied/power off)	DRt1	I_L = 20 mA, THD = 4%	2.5	5.6		Vp-p
Transmitter dynamic range (120 mA, power supplied/power off)	DRt2	I_L = 120 mA, THD = 4%	4.5	7.7		Vp-p
Receiver dynamic range (power supplied)	EDRs	I_L = 20 mA/120 mA, R_L = 150 Ω, THD = 10%	0.5	1.5		Vp-p
Receiver dynamic range (20 mA, power off)	DRs1	R_L = 150 Ω, I_L = 20 mA, THD = 10%	0.3	0.55		Vp-p
Receiver dynamic range (120 mA, power off)	DRs2	R_L = 150 Ω, I_L = 120 mA, THD = 10%	0.5	1.4		Vp-p

Continued on next page.

Continued from preceding page.

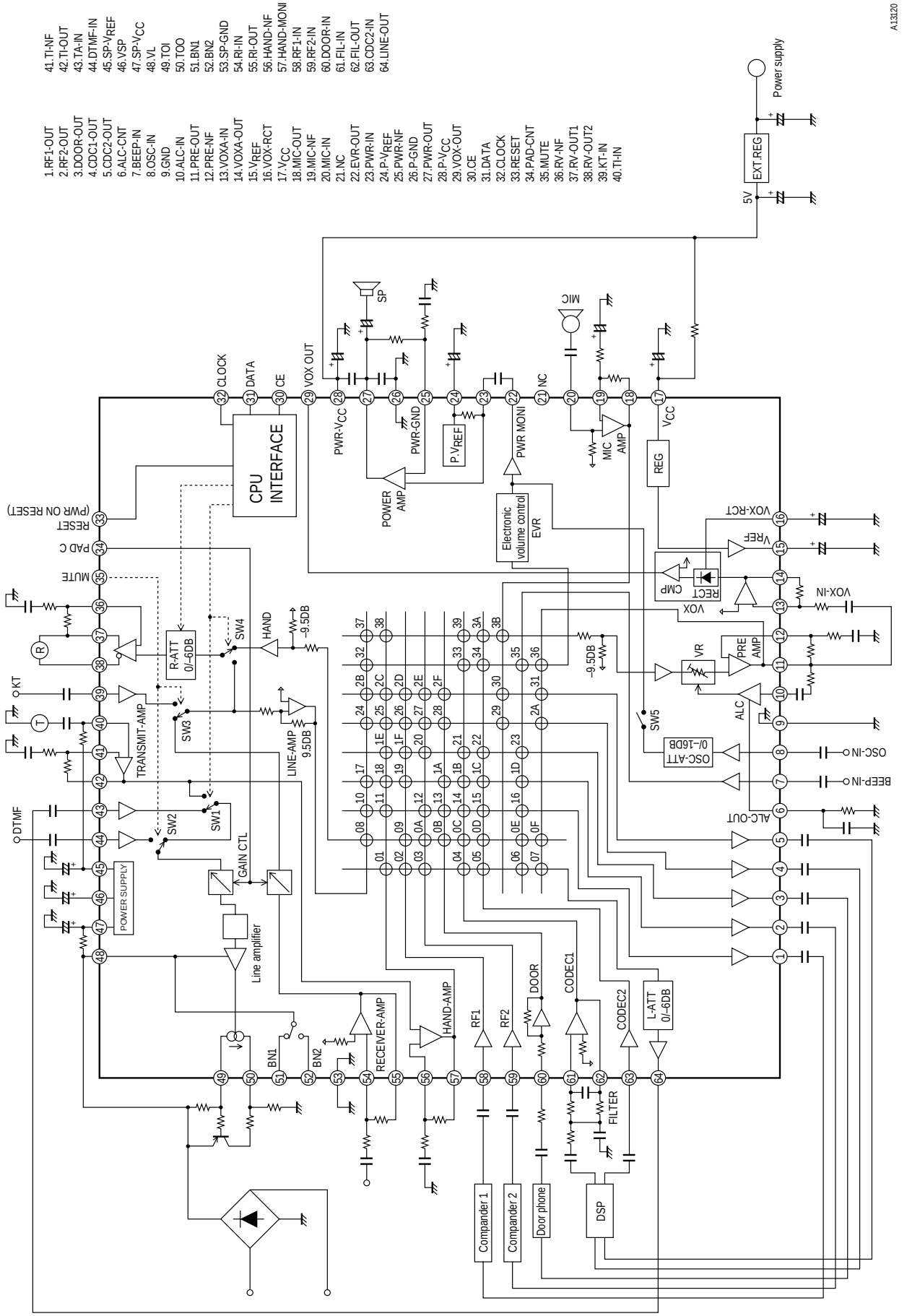
Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Receiver BTL dynamic range (power supplied)	EDRb	I_L = 20 mA/120 mA, R_L = 3 kΩ, THD = 10%	5	10		Vp-p
Receiver BTL dynamic range (20 mA, power off)	DRb1	R_L = 3 kΩ, I_L = 20 mA, THD = 10%	2	3.4		Vp-p
Receiver BTL dynamic range (120 mA, power off)	DRb2	R_L = 3 kΩ, I_L = 120 mA, THD = 10%	5	8.4		Vp-p
MUTE input high-level voltage (power supplied/power off)	V_{IH}	I_L = 20 mA to 120 mA	0.6 VSP			V
MUTE input low-level voltage (power supplied/power off)	V_{IL}	I_L = 20 mA to 120 mA	0		0.4	V
Transmitter PADC attenuation (power supplied/power off)	ΔGt	I_L = 40 mA, pin 34: grounded through 24 Ω		4.0		dB
Receiver PADC attenuation (power supplied/power off)	ΔGr	I_L = 40 mA, pin 34: grounded through 24 Ω		6.0		dB
Internal supply voltage (power supplied)	EV_{SP}	I_L = 20 mA/120 mA		4.75		V
Internal supply voltage (20 mA, power off)	$V_{SP}1$	I_L = 20 mA		1.92		V
Internal supply voltage (120 mA, power off)	$V_{SP}2$	I_L = 120 mA		4.74		V
Internal reference voltage (power supplied)	ES-V_{REF}	I_L = 20 mA/120 mA		2.26		V
Internal reference voltage (20 mA, power off)	S-$V_{REF}1$	I_L = 20 mA		0.79		V
Internal reference voltage (120 mA, power off)	S-$V_{REF}2$	I_L = 120 mA		1.92		V
[Voice Signal-Processing Block] at Ta = 25°C, V_{CC} = 5 V, f_{IN} = 1 kHz, R_L = 10 kΩ						
(Crosspoint switch)						
Voltage gain	G_{SW}	V_{IN} = –13 dBV, pin 58 input, pin 2 output	–2.5	–0.5	1.5	dB
Maximum input level	V_{IN} max	THD = 1.5%	–13.5	–7.5		dBV
Output noise voltage	V_{NOSW}	Rg = 620 Ω, 20 to 20 kHz		7.0	40	μVrms
(Preamplifier: input from the crosspoint switch)						
Voltage gain	VG_C	V_{IN} = –45 dBV	8.5	10.5	12.5	dB
Total harmonic distortion	THD	V_{IN} = –20 dBV		0.26	1.0	%
ALC saturated output level	V_{OS}	V_{IN} = –20 dBV	93	115	137	mVrms
ALC range	ALC_W	From the point the ALC circuit turns on to the point the THD reaches 1%.	15			dB
Output noise voltage	V_{NO}	Rg = 620 Ω, 20 to 20 kHz		65	250	μVrms
(Microphone amplifier)						
Voltage gain	VGm	V_{IN} = –40 dBV	27.5	29.5	31.5	dB
Total harmonic distortion	THD	V_{IN} = –40 dBV		0.05	1.0	%
Output noise voltage	V_{NO}	Rg = 620 Ω, 20 to 20 kHz		65	250	μVrms
(Power amplifier)						
Voltage gain	VGp	R_L = 8 Ω, V_{IN} = –30 dBV	27.5	29.5	31.5	dB
Maximum output power	Po	R_L = 8 Ω, THD = 10%	200	275		mW
Total harmonic distortion	THD	V_{IN} = –30 dBV		0.8	1.5	%
Ripple rejection ratio	SVRR	Rg = 620 Ω, fr = 100 kHz, Vr = –20 dBV	40	50		dB
Output noise voltage	V_{NO}	Rg = 620 Ω, 20 to 20 kHz		35	100	μVrms
(VOX)						
Sensitivity 1 low level	$V_{OX}L$	V_{IN} = –40 dBV, R_L = 100 kΩ		0.1	0.3	V
Sensitivity 2 high level	$V_{OX}H$	V_{IN} = –44 dBV, R_L = 100 kΩ	4.8	4.95		V
(Electronic volume control)						
Step width	Evrw		2.9	3.8	4.7	dB
(Attenuator)						
R-ATT attenuation	ΔGR		5.4	6.4	7.4	dB
LINE-ATT attenuation	ΔGL		4.6	5.6	6.6	dB
OSC-ATT attenuation	ΔGO		13.1	14.6	16.1	dB

Continued on next page.

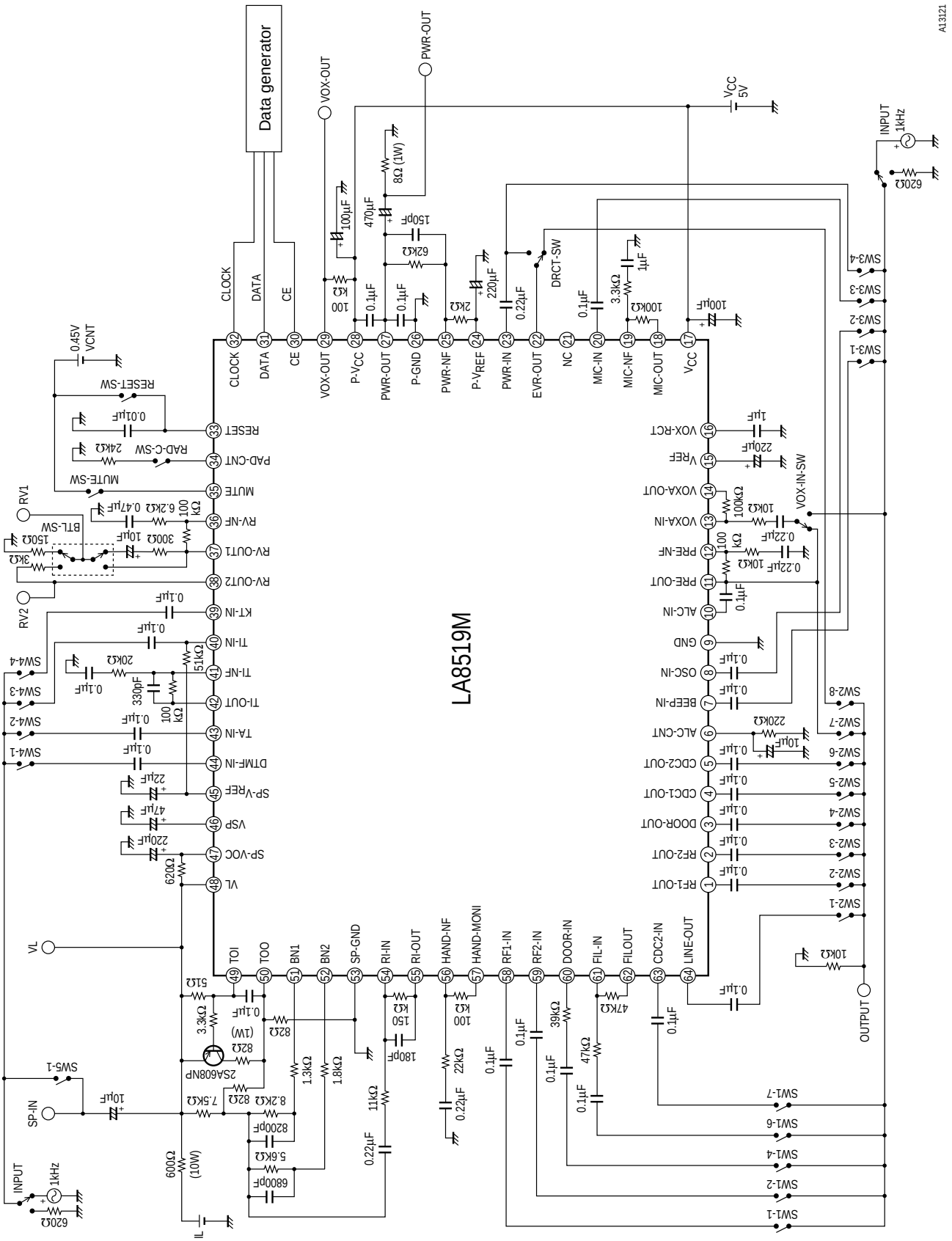
Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
(V_{REF})						
Output voltage	V_{REF}		2.07	2.27	2.47	V
(Serial Control)						
Clock frequency	Fck				500	kHz
Input signal high level	V_H		2.3			V
Input signal low level	V_L				1.0	V
(Power Supply Switching)						
Pin 17 voltage 1	Vch1	The voltage applied to pin 17 is valid.	3.5			V
Pin 17 voltage 2	Vch2	The voltage supplied from pin 48 is valid.			1.0	V
Quiescent current	I_{CCO}	With the power amplifier on		24	33.5	mA

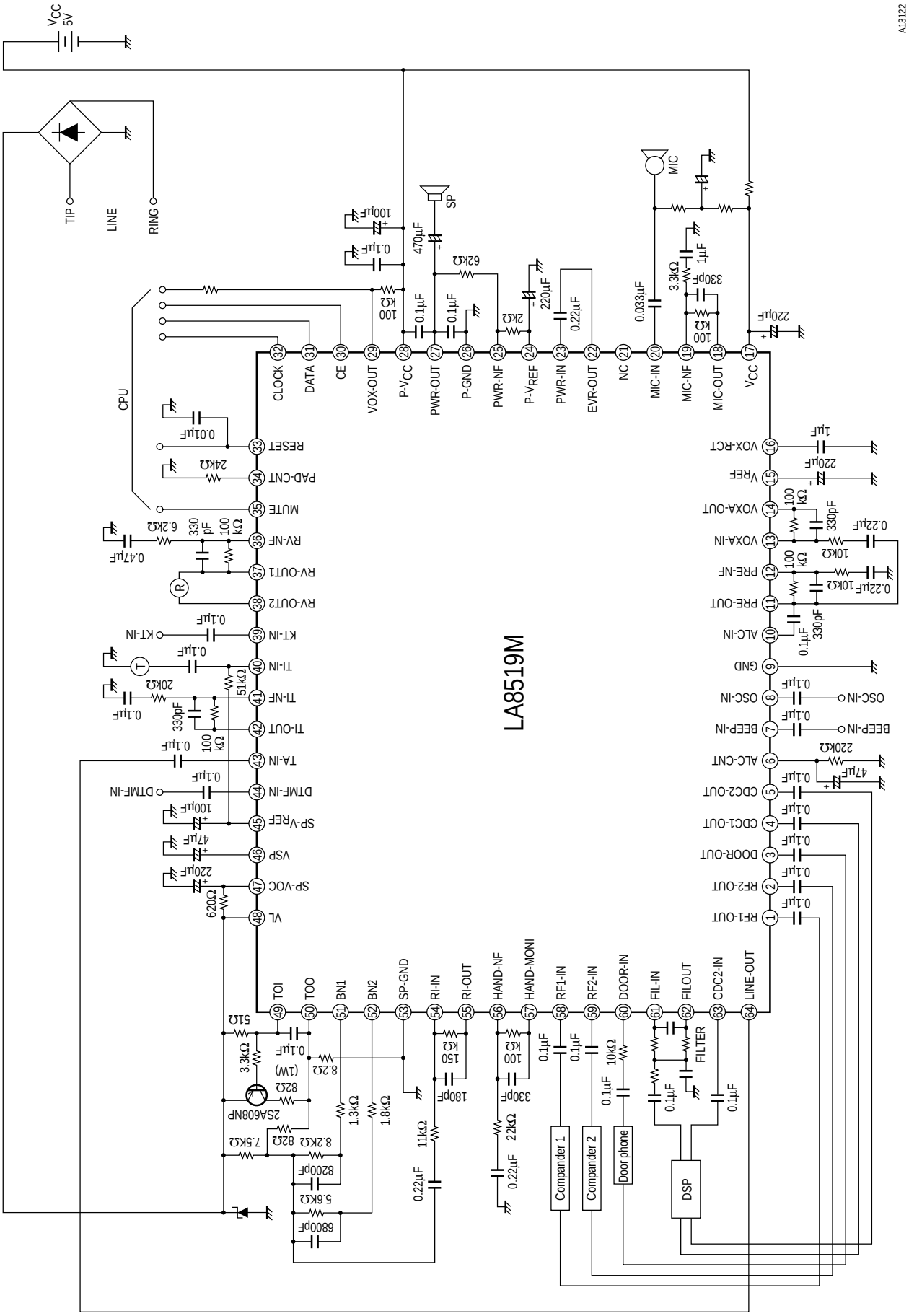
Block Diagram



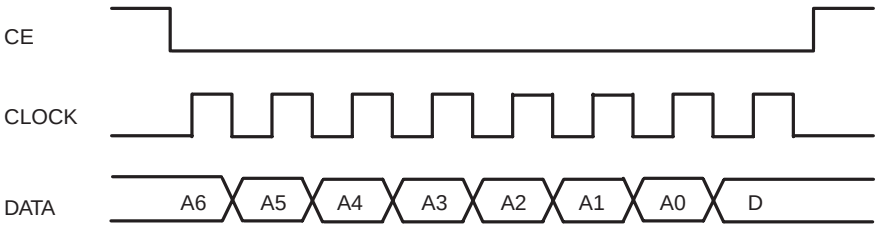
Test Circuit Diagram



Sample Application Circuit



Serial Data Format



A6 to A0 ⇒ Sets the address of the crosspoint switch or control switch (hexadecimal ⇒ binary number)
D ⇒ Sets the on/off state of the crosspoint switch or control switch.
(The switch is set to the on state when D is 1, and to the off state when 0.)

Address Table

Input \ Output	LINE	HAND	RF1	RF2	DOOR	CDC1	CDC2	EVR	PRE
LINE	—	08	10	17	—	24	2B	32	37
HAND	01	—	11	18	1E	25	2C	—	38
RF1	02	09	—	19	1F	26	2D	—	—
RF2	03	0A	12	—	20	27	2E	—	—
DOOR	—	0B	13	1A	—	28	2F	—	—
CDC1	04	0C	14	1B	21	—	—	33	39
CDC2	05	0D	15	1C	22	—	—	34	3A
MIC	—	—	—	—	—	29	30	—	3B
BEEP	06	0E	16	1D	23	—	—	35	—
PRE	07	0F	—	—	—	2A	31	36	—

Other addresses

Address No.	Mode		
00	Sets all crosspoint and control switches to the off state. *2		
3C	ALC control (D = 1: Off, D = 0: On)		
3D	Transmitter/receiver control (SW1 and SW4 in the block diagram) *1		
3E	OSC input (SW5) control (D = 1: On, D = 0: Off)		
3F	Power amplifier control (D = 1: On, D = 0: Off)		
40	Electronic volume control	0 dB	⇒ (Default value)
41	Electronic volume control	–4 dB	
42	Electronic volume control	–8 dB	
43	Electronic volume control	–12 dB	*2
44	Electronic volume control	–16 dB	
45	Electronic volume control	–20 dB	
46	Electronic volume control	–24 dB	
47	Electronic volume control	–28 dB	
7D	Line attenuator (L-ATT) setting (D = 1: –6 dB, D = 0: 0 dB)		
7E	Receiver attenuator (R-ATT) setting (D = 1: 0 dB, D = 0: –6 dB)		
7F	Oscillator attenuator (OSC-ATT) setting (D = 1: 0 dB, D = 0: –16 dB)		

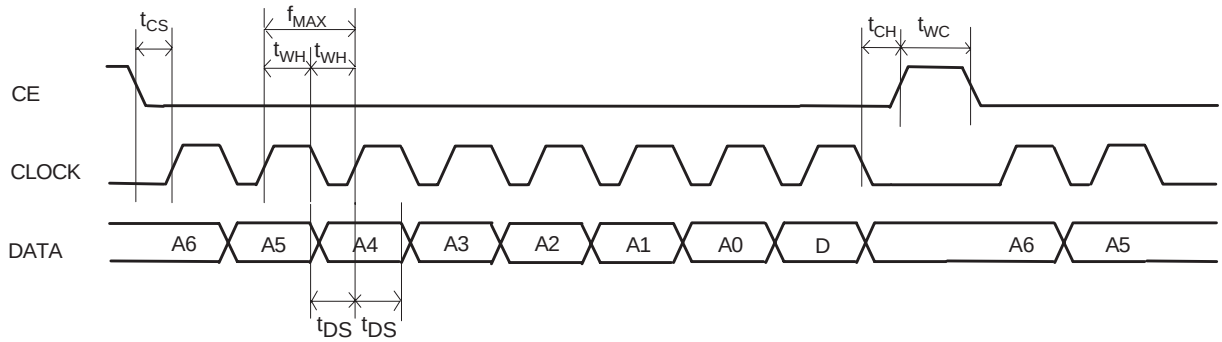
* With address 3D set to the on state, SW1 is set to enable the transmitter amplifier output (pin 42) and SW4 is set to enable either the receiver amplifier output (pin 55) or the KT (pin 39) signal. If a voltage is not supplied to V_{CC} (pin 17) (i.e. the power off state), SW1 and SW4 are set to the same states as when address 3D is set to the on state.

** For addresses 00 and 40 to 47, the data D may be either 0 or 1.

Notes: 1. The receiver attenuator (R-ATT) is set to –6 dB at power on or after a reset (pin 33 set to low, or address 00 accessed).
2. The line attenuator (L-ATT) is set to 0 dB at power on or after a reset (pin 33 set to low, or address 00 accessed).
3. The oscillator attenuator (OSC-ATT) is set to –16 dB at power on or after a reset (pin 33 set to low, or address 00 accessed).
4. The electronic volume control is set to 0 dB at power on or after a reset (pin 33 set to low, or address 00 accessed).
5. Addresses are expressed as hexadecimal numbers.
6. Since the LA8519M includes a power on reset function, all the crosspoint and control switches are reset to their default states when external power (pin 17: V_{CC}) is applied.
7. Switches SW2 and SW3 in the block diagram are controlled by the MUTE pin (pin 35). The table lists the signals enabled by this pin.

MUTE pin (pin 35)	SW2	SW3
High/Open	Transmitter (pin 42) and TA-IN (pin 43)	Receiver (pin 55)
Low	DTMF pin (pin 44)	KT pin (pin 39)

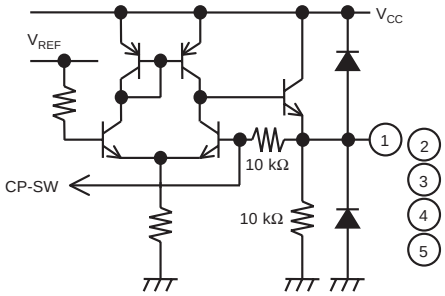
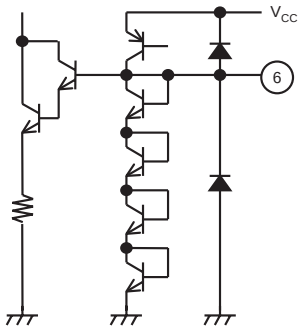
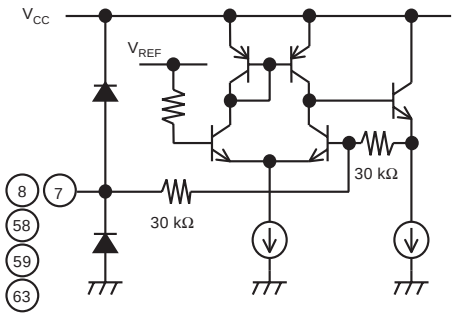
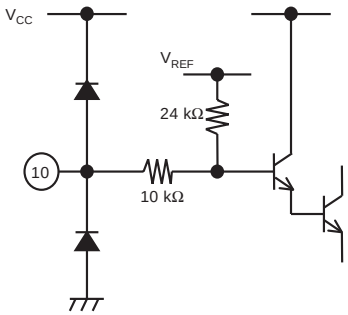
Serial Data Timing



- f_{MAX} (maximum clock frequency) 500 kHz
- t_{WL} (clock low-level pulse width) At least 1 µs
- t_{WH} (clock high-level pulse width) At least 1 µs
- t_{CS} (chip enable setup time) At least 1 µs
- t_{CH} (chip enable hold time) At least 1 µs
- t_{DS} (data setup time) At least 1 µs
- t_{DH} (data hold time) At least 1 µs
- t_{WC} (chip enable pulse width) At least 1 µs

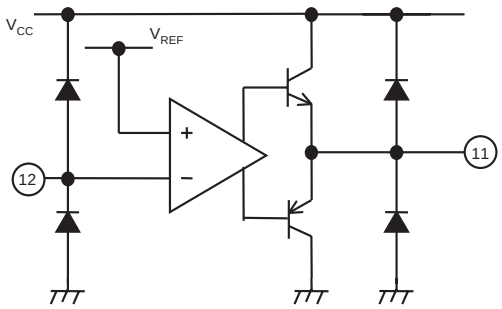
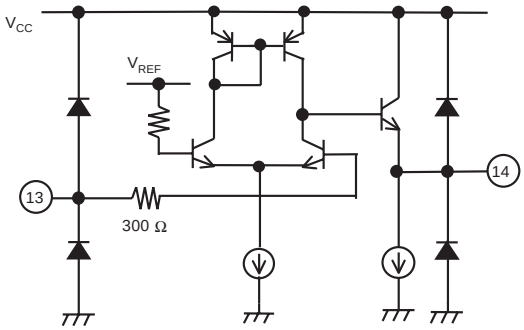
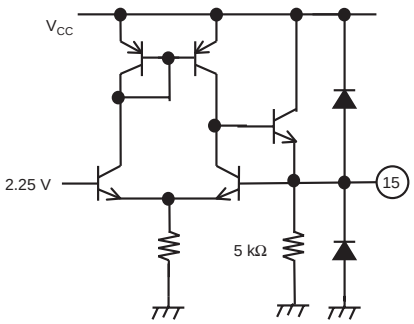
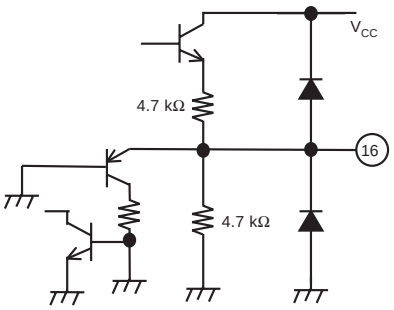
Note: The control data must be input at least 400 ms after the supply voltage is applied to the V_{CC} pin (pin 17).

Pin Functions

Pin No.	Pin	Notes	Equivalent circuit
1 2 3 4 5	RF1-OUT RF2-OUT DOOR-OUT CDC1-OUT CDC2-OUT	• These are the IC outputs.	
6	ALC-CNT	• Adjusts the ALC time constants This pin can be used to adjust the ALC attack time and recovery time.	
7 8 58 59 63	BEEP-IN OSC-IN RF1-IN RF2-IN CDC2-IN	• Beep tone amplifier input • Oscillator amplifier input • Compander 1 input • Compander 2 input • CDC2 amplifier input	
9	GND	Signal-processing system ground	
10	ALC-IN	• ALC input. The PRE output (pin 11) is input to this pin through a coupling capacitor. The ALC level can be adjusted by inserting a resistor in series.	

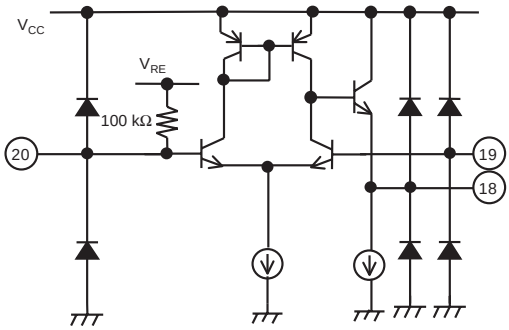
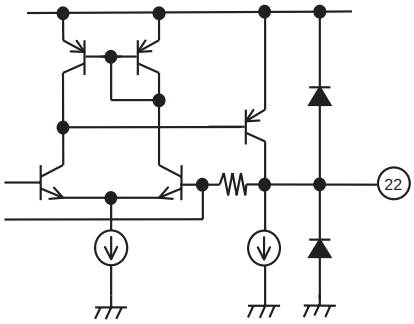
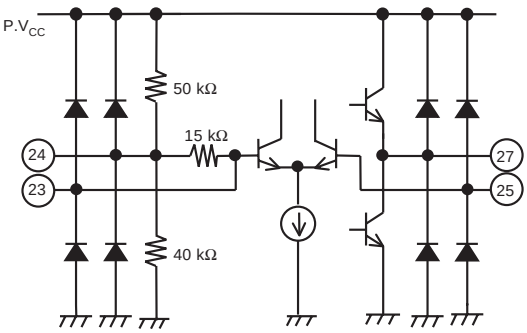
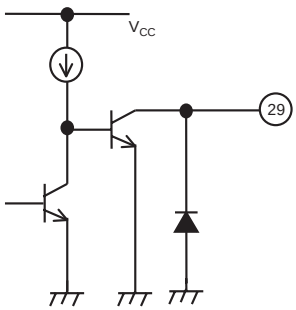
Continued on next page.

Continued from preceding page.

Pin No.	Pin	Notes	Equivalent circuit
11 12	PRE-OUT PRE-NF	• Preamplifier output	
13 14	VOXA-IN VOXA-OUT	• VOX amplifier input • VOX amplifier output	
15	VREF	• Internal reference voltage output	
16	VOX-RCT	• VOX detection output. This circuit can also be used as a waveform shaping circuit by forcibly setting this pin to the high state.	
17	V_{CC}	• External power supply input. This voltage is supplied to the signal-processing system and V_{SP} (pin 46).	

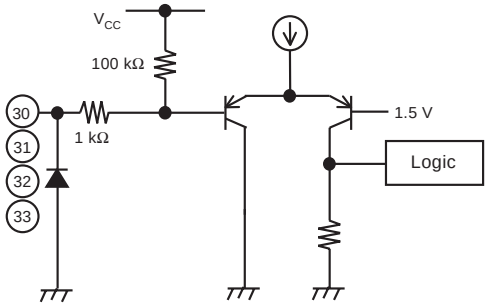
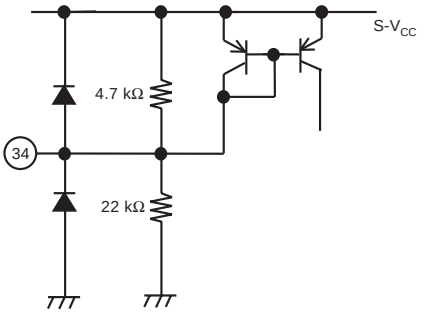
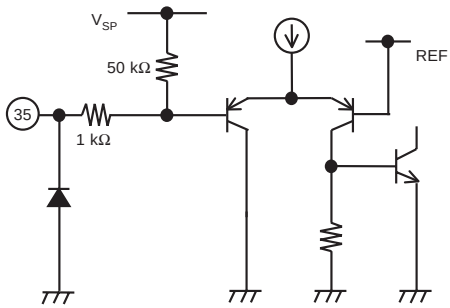
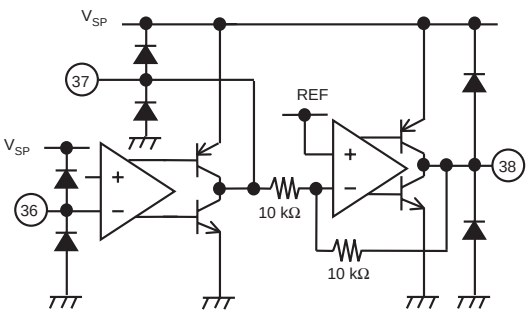
Continued on next page.

Continued from preceding page.

Pin No.	Pin	Notes	Equivalent circuit
18 19 20	MIC-OUT MIC-NF MIC-IN	• Microphone amplifier output • Microphone amplifier minus input • Microphone amplifier plus input	
21	NC	• Unused.	
22	EVR-OUT	• EVR amplifier output	
23 24 25 27	PWR-IN P-VREF PWR-NF PWR-OUT	• Power amplifier plus input • Power amplifier reference voltage (about 4/9 × P-V_{CC}) • Power amplifier minus input • Power amplifier output	
26	P-GND	• Power system ground	
28	P-V_{CC}	• Power system power supply	
29	VOX-OUT	• VOX output This is an open-collector output.	

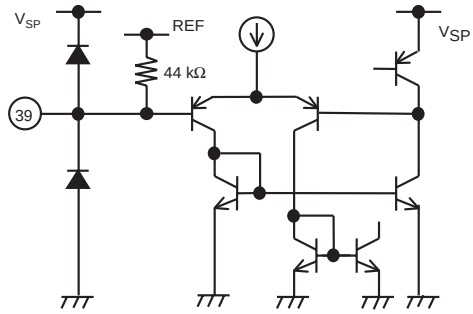
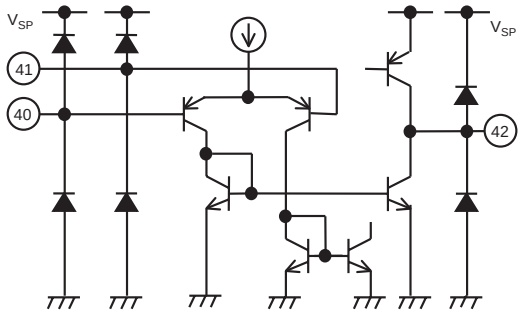
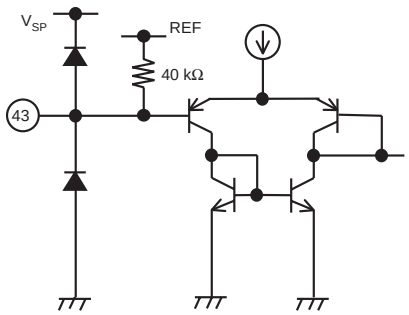
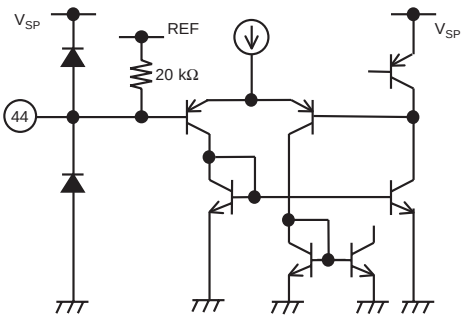
Continued on next page.

Continued from preceding page.

Pin No.	Pin	Notes	Equivalent circuit
30 31 32 33	CE DATA CLOCK RESET	• Chip enable input • Data input • Clock input • Reset Power on reset.	
34	PAD C	• Pad control. The gain control based on line current and the BN switching operating current can be controlled by connecting this pin through a resistor to either ground or S-V_{CC} (pin 47).	
35	MUTE	• Muting control. This pin switches the transmitted audio and DTMF signals in the transmitter system and the KT and received signals in the receiver system. (Switches SW2 and SW3 in the block diagram.) When low, the DTMF and KT signals are enabled.	
36 37 38	RV-NF RV-OUT1 RV-OUT2	• Receiver amplifier noise figure connection • Receiver amplifier 1 output • Receiver amplifier 2 output	

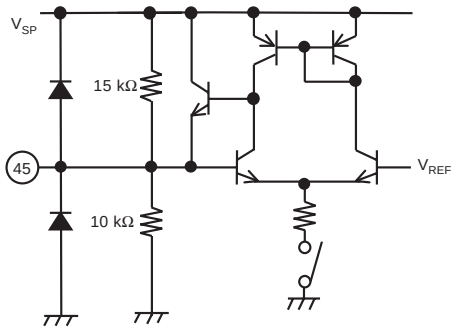
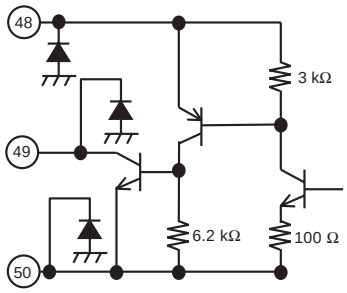
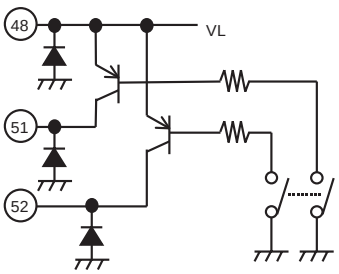
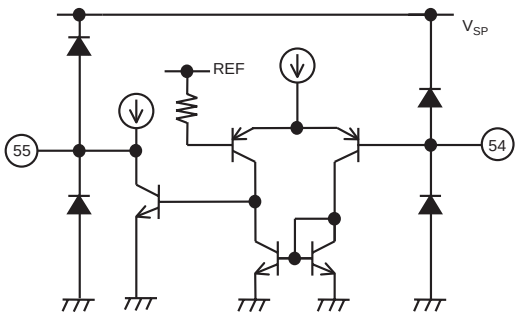
Continued on next page.

Continued from preceding page.

Pin No.	Pin	Notes	Equivalent circuit
39	KT-IN	• Key tone input	
40 41 42	TI-IN TI-NF TI-OUT	• Transmitter input amplifier plus input. Since no bias voltage is applied internally, a bias voltage must be applied through a resistor from the REF pin (pin 61). • Transmitter input amplifier minus input • Transmitter input amplifier output	
43	TA-IN	• Input for the line output	
44	DTMF-IN	• DTMF input	

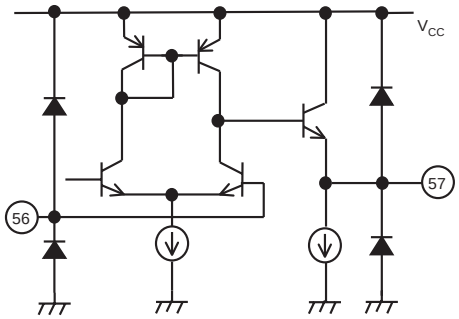
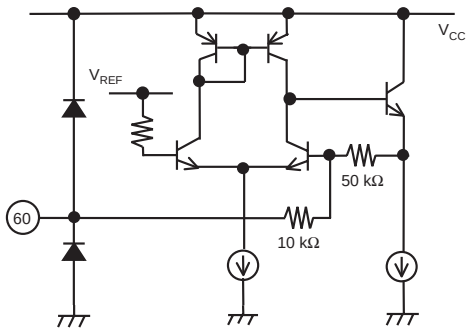
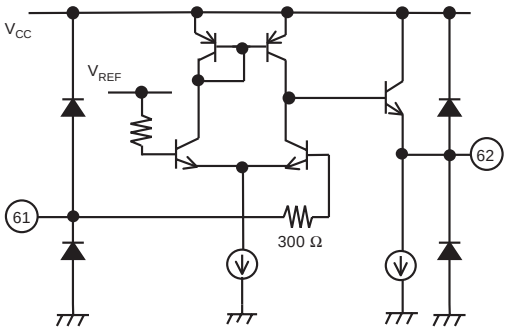
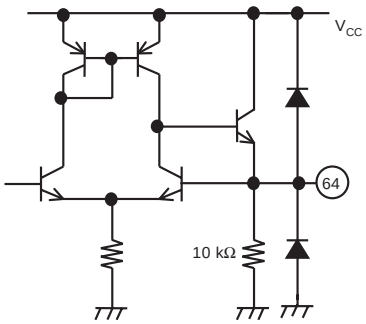
Continued on next page.

Continued from preceding page.

Pin No.	Pin	Notes	Equivalent circuit
45	REF	• Speech network system internal reference voltage output. When the V_{CC} (pin 17) voltage is over 3.5 V, the reference voltage is output from V_{REF} (pin 15). When the V_{CC} voltage is under 1.2 V, a voltage of about (2/5) × V is output.	
46	VSP	• Speech network system internal power supply. A voltage of about 0.3 V less than the voltage applied to V_{CC} is output when the V_{CC} (pin 17) voltage is over 3.5 V. When the V_{CC} voltage is under 1.2 V, a voltage of about 0.3 V less than the S-V_{CC} (pin 47) voltage is output.	
47	S-V_{CC}	• Speech network system power supply. When the V_{CC} voltage is under 1.2 V, power is supplied to V_{SP} (pin 46) based on the line power.	
48 49 50	VL TOI TOO	• Line current input and line voltage • Current input for the transmitter output current • Transmitter output current output	
51 52	BN1 BN2	• First BN switching control input • Second BN switching control input Connect these inputs when two balancing networks are used. When unused, leave these pins open.	
53	SP-GND	• Speech network system ground	
54 55	RI-IN RI-OUT	• Receiver input amplifier minus input • Receiver input amplifier output	

Continued on next page.

Continued from preceding page.

Pin No.	Pin	Notes	Equivalent circuit
56 57	HAND-NF HAND-MONI	• Handset amplifier minus input • Handset amplifier output	
60	DOOR-IN	• Door phone input	
61 62	FIL-IN FIL-OUT	• FIL amplifier input • FIL amplifier output	
64	LINE-OUT	• Line amplifier output	

Usage Notes

Speech Network Circuit Block

• External driver transistor

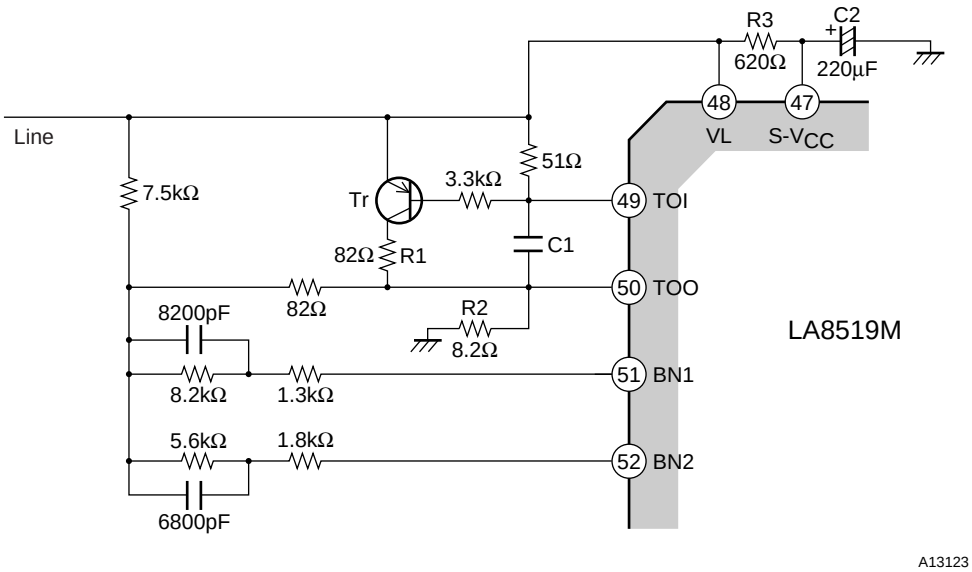


Figure 1

Since the IC includes a built-in power amplifier, due to the allowable power dissipation limits, include a heat dissipation transistor as shown in figure 1, and dissipate the circuit current outside the IC. Set the allowable power dissipation for R1 and R2 according to the maximum expected circuit current. (The values shown are for reference purposes only.)

Note: If oscillation occurs due to the load state between VL and ground, insert the capacitor C1 (about 0.1 µF) shown in the figure.

• Changing the DC resistance

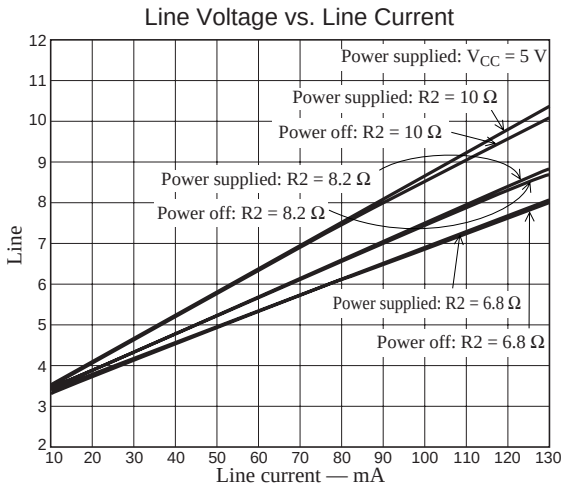
The DC resistance can be modified by using a variable resistor for R2 in figure 1. (See the figure below.)

Note: Note that changing R2 will also change the transmitter gain and the balancing network conditions.

• Determining the AC impedance

The AC impedance is basically determined by R3 (620 Ω) and C2 (220 µF) shown in figure 1 above page. Since in actual operation there will be other AC loads in addition to the speech network, adjust the total AC impedance for the whole system in combination with the speech network impedance.

Note: Note that if R3 is changed, the DC resistance will change as well.



• Anti-sidetone network

The LA8519M can switch between two anti-sidetone networks, one for the near terminal and one for the far terminal, depending on the circuit current. (See figure 1 for the connections used.) The switching point can be changed by connecting PADC (pin 34) through a resistor to either ground or S-V_{CC} (pin 47).

If only one anti-sidetone network is used, short pin 51 to pin 52 as shown in figure 2. (The component values shown are for reference purposes only.)

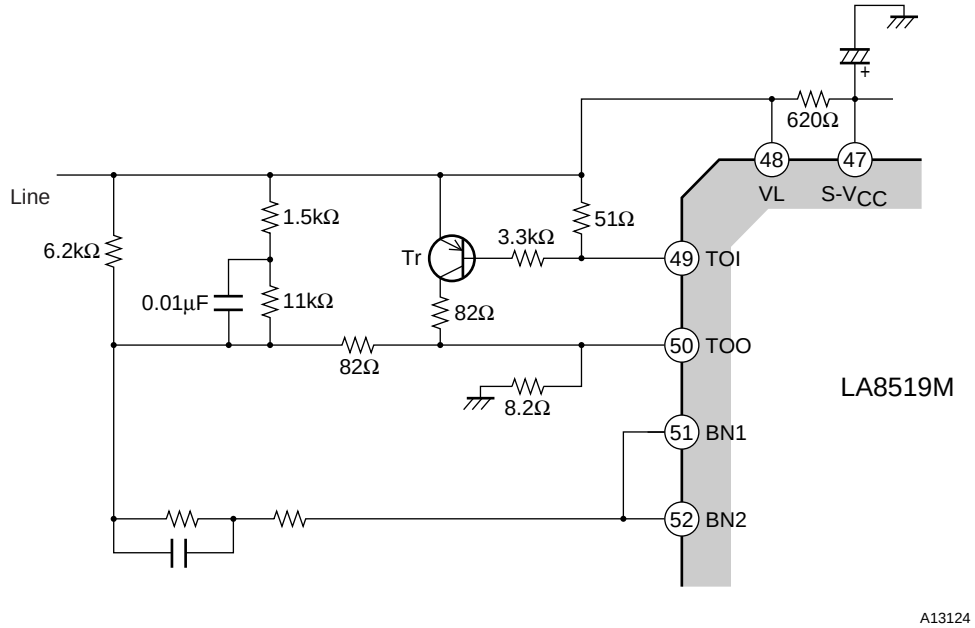
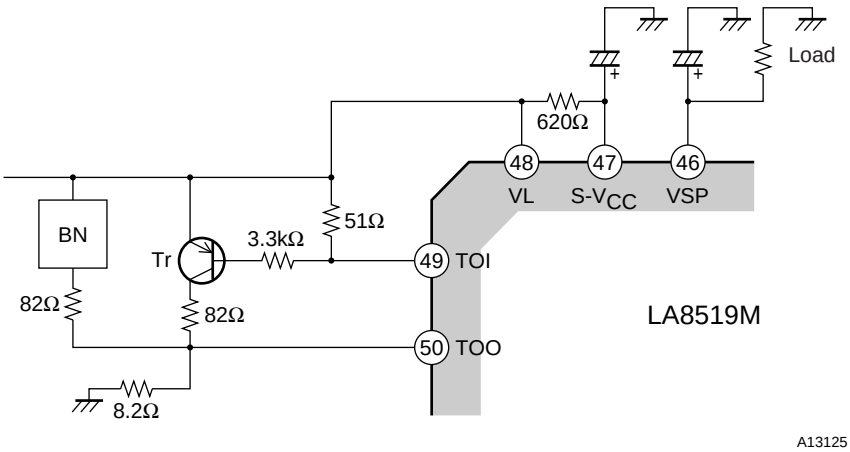


Figure 2

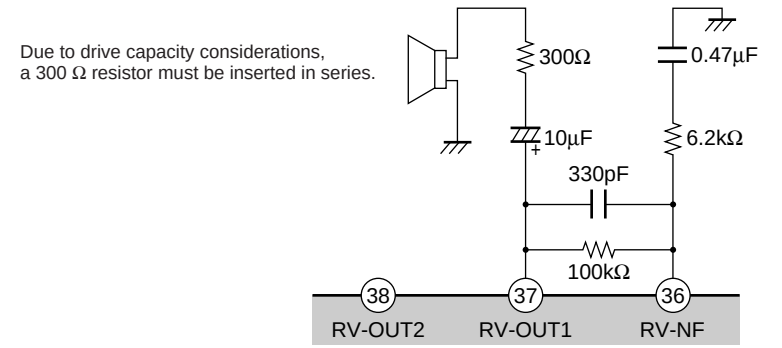
• Line voltage VL DC characteristics when V_{CC} is not applied (Values shown are for reference purposes only.)



The slope of the DC characteristics when V_{CC} is not applied can be increased without changing the DC characteristics when V_{CC} is applied by applying a load to V_{SP} (pin 46).

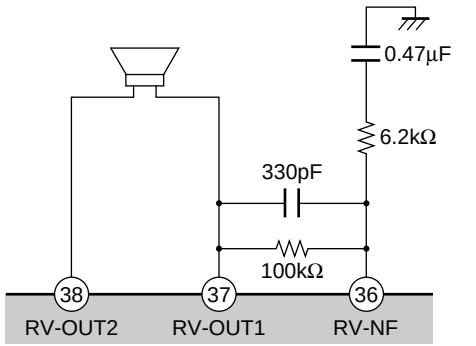
• Receiver amplifier application circuits

(1) When a dynamic receiver is used (Values shown are for reference purposes only.)



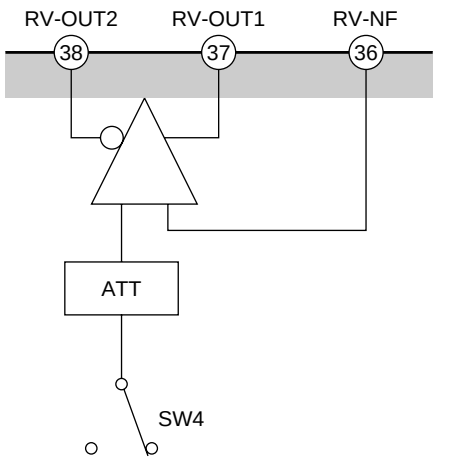
A13126

(2) When a ceramic receiver is used (Values shown are for reference purposes only.)



A13127

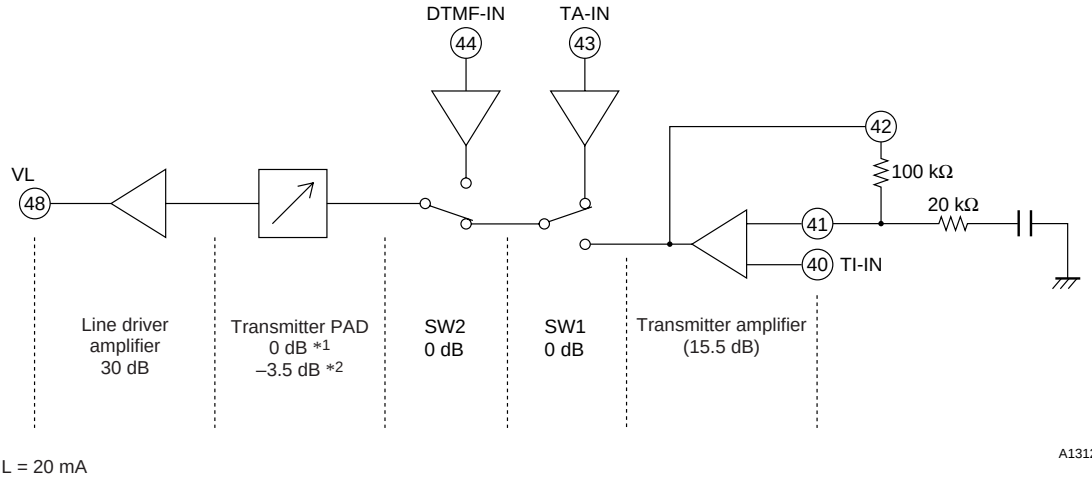
• Receiver attenuator



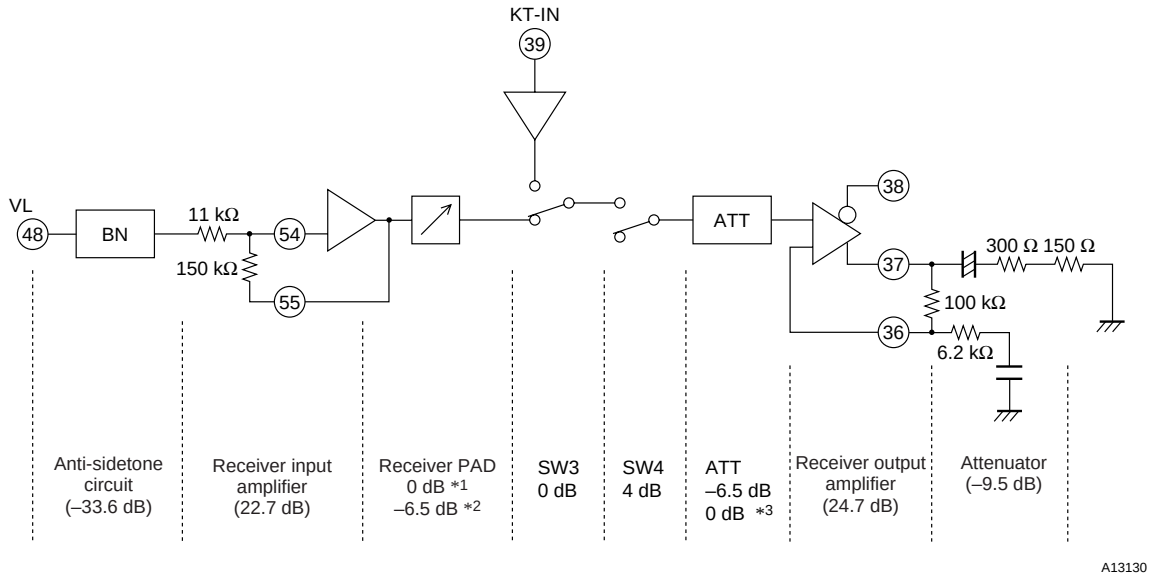
A13128

Normally, the receiver attenuator is set to –6 dB. It can be set to 0 dB by setting address 7E to the on state with a serial data transfer.

• Speech network gain distribution

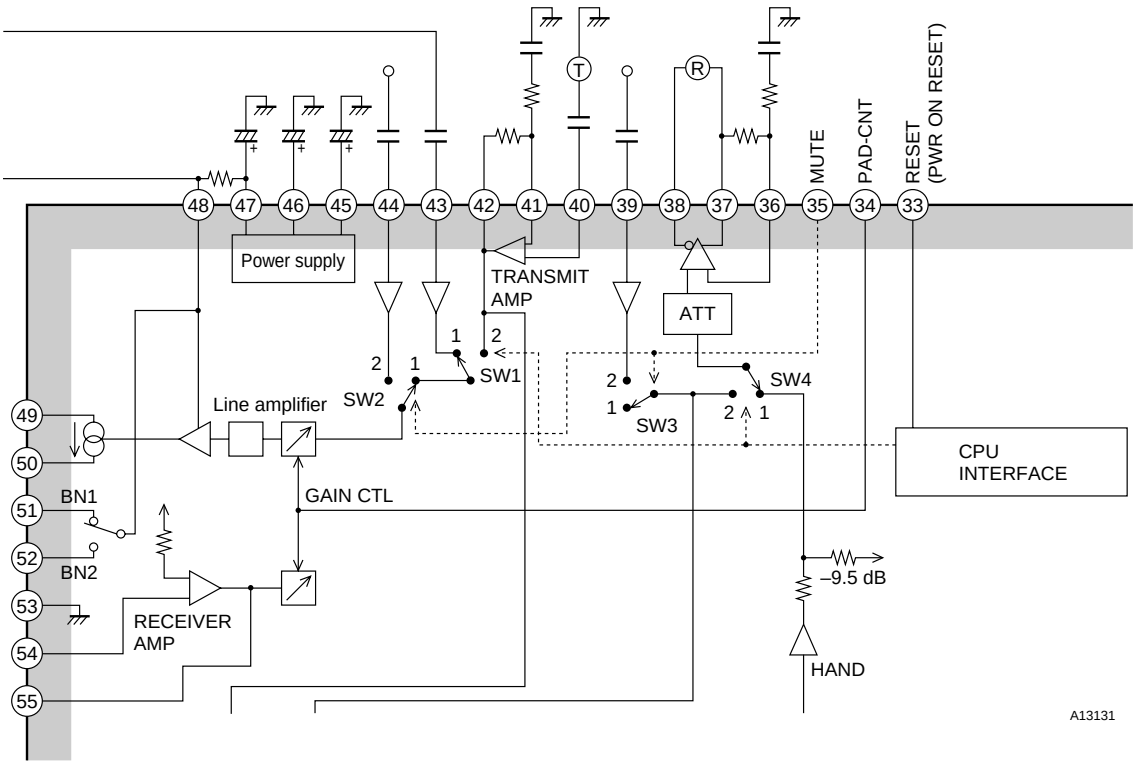


* IL = 20 mA
** IL = 120 mA
Note: For a 600 Ω line termination



* IL = 20 mA
** IL = 120 mA
*** When address 7E is set to the on state with a serial data transfer.
Notes: 1. The gain values are rough values, and should be seen as target values during the design process.
2. Values in parentheses can be modified by external components.

• Speech network internal analog switch operation



Note: Switches SW2 and SW3 are controlled by the MUTE pin (pin 35). Switches SW1 and SW4 are controlled by address 3D as set by serial data transfers. Note that switches SW2 and SW3 operate together, as do switches SW1 and SW4.

SW1 and SW4 Operation

State	SW1	SW4
Power supplied (initial state)	1	1
Address 3D	2	2
Power off	2	2

Note: When the power is off, SW1 and SW4 go to the "2" positions, and their states cannot be changed.

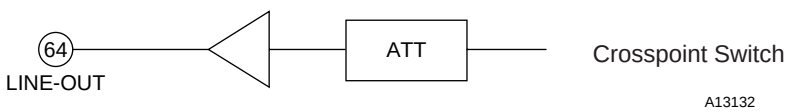
SW2 and SW3 Operation

Pin 35 (MUTE)	SW2	SW3
High	1	1
Low	2	2

Note: SW2 and SW3 operate as described above regardless of the power supplied/off state.

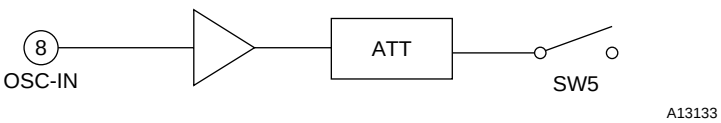
• Line amplifier attenuator

Normally, the line attenuator is set to 0 dB. It can be set to –6 dB by setting address to 7D and mode to D = 1 with a serial data transfer.



• Oscillator amplifier attenuator

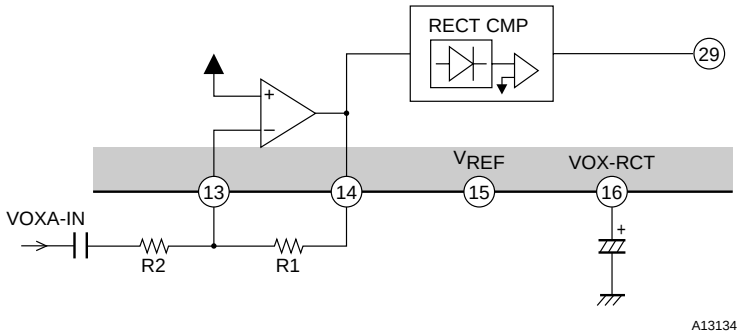
Normally, the oscillator amplifier attenuator is set to –16 dB. It can be set to 0 dB by setting address to 7F and mode to D = 1 with a serial data transfer.



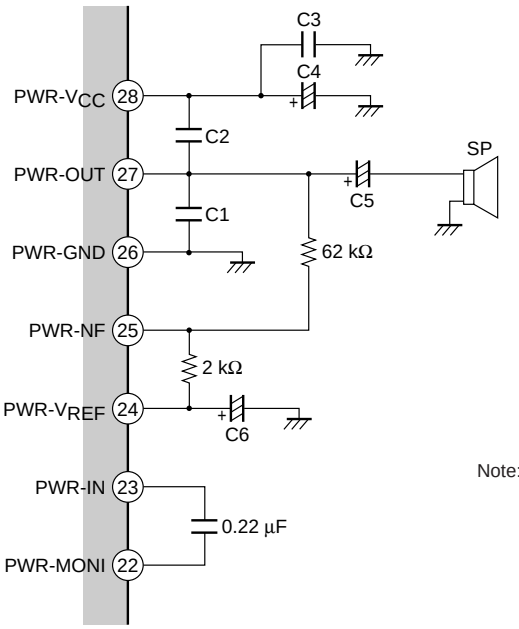
• VOX circuit

(1) The VOX circuit detects whether there is conversation or not. When the signal level in the VOXA input block (when the application constants in the application circuit diagram are used) becomes over about –42 dBV, the VOX output pin (pin 29) goes low. The detection level can be set by setting the gain of the VOX input amplifier with resistors R1 and R2.

(2) This circuit can be used as a waveform shaping circuit if VOX-RCT (pin 16) is connected to V_{CC}, i.e. if pin 16 is set to the high level. Thus this circuit can also be used to recognize a 400 Hz beep tone. In this mode, there is no need to connect a capacitor to pin 16.



• Power amplifier circuit applications (The component values are for reference purposes only.)



C1: 0.1 µF
C2: 0.1 µF
C3: 0.1 µF
C4: 220 µF
C5: 100 to 470 µF
C6: 220 µF
SP: 8 to 32 Ω

• Voltage gain: 20 to 30 dB
• A frequency characteristics adjustment capacitor cannot be attached to the feedback resistor.

Note: The power amplifier output goes to the high-impedance state in the muted state, i.e. when address 3F has been set to the off state.

• Power amplifier phase compensation capacitors

Of the external components, the capacitors C1 between pin 27 (output) and pin 26 (ground) and C2 between pin 27 and pin 28 (V_{CC}) are power amplifier phase compensation capacitors. If these components are separated from their pins in the PCB layout, their phase compensation effect may be reduced and high-frequency oscillation may occur.

We therefore strongly recommend using a layout in which the capacitors C1 and C2 are located as close as possible to their respective IC pins. In particular, C1, which is connected to ground, should be given priority in positioning close to the IC. Note that phase compensation not with capacitors alone, but with series resistors (on the order of 1 to 2.2 Ω) inserted is also possible. While this can increase the phase compensation effect, since it increases the parts count, we recommend using capacitors only. However, we do recommend phase compensation with resistors inserted if, due to the details of the layout, the power amplifier is subject to oscillation.

Also note that the ceramic capacitor C3 between pins 26 and 28 has only a minimal phase compensation effect on normal power amplifiers, so is not required. However, there are cases where it does have a large effect due to the pattern layout, so we recommend creating a dummy pattern for this capacitor and handling it as a reserve component.

• Power amplifier VREF (pin 24) line

Pin 24 is the reference voltage pin for the power amplifier, and is connected to pin 23 (the input) by an internal bias resistor. This means that pin 24 is part of the power amplifier plus input line system. If this line is affected by the power amplifier output or the V_{CC} line, the resultant positive feedback can cause oscillation.

Therefore, if at all possible, the pin 24 line should not be routed around other lines. If it must be routed around other lines, do not rout it adjacent to output or V_{CC} lines, but rout it adjacent to ground lines to prevent interference.

• LA8519M ground line rerouting (See the figure on the next page.)

The LA8519M circuit blocks can be classified into three systems: (1) power amplifier, (2) speech network system, and (3) crosspoint switch and other small-signal processing systems. Since the IC itself, naturally, has a three-block structure, each block has independent V_{CC} and ground pins. The best possible ground system design, is for external components that are connected to ground to be connected to the ground for the block to which they belong, and for the pattern to be formed so that these three lines are independent and connect to the ground of the power supply (regulator) that is the reference.

However, since there are limitations on the area available on the printed circuit board, there are cases where a single line is connected to the reference ground. In this case, ground lines must be routed so that the ground lines that carry larger currents (power amplifier and line connection blocks) are closer to the power supply ground (and thus have a lower impedance)than ground lines for circuits with a lower current drain.

If the large currents used by the power amplifier or other high-current system flow in the ground lines that handle the smaller currents from small-signal system or other low-current system, a loop may be formed and low band oscillation may occur.

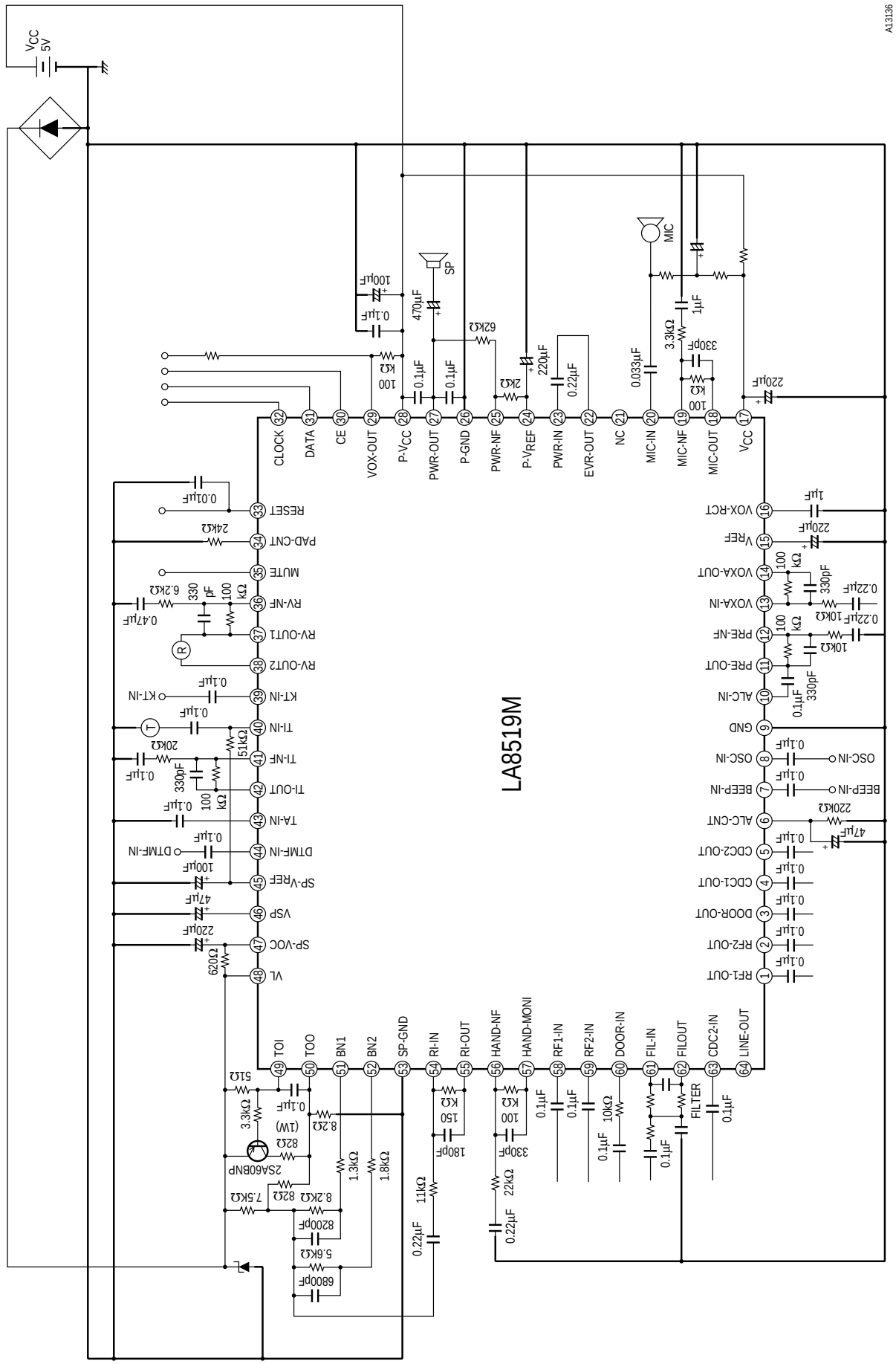
Therefore we recommend that the ground lines are designed, as described above, so that lines in which large currents flow are routed closest to the power supply ground.

IC Usage Notes

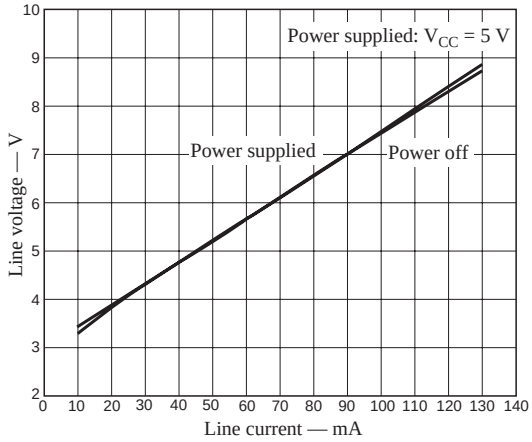
1. If the LA8519M is used in the vicinity of its maximum ratings, even slight variations in operating conditions may result in the maximum ratings being exceeded. Since this can lead to damage to or destruction of the device, provide adequate margin in the fluctuations in the supply voltage and other parameters, and do not allow the maximum ratings to be exceeded.
2. Pin shorting

   If the LA8519M is left with output loads shorted for extended periods, it may be damaged or destroyed. Always use this device in a manner such that output loads are never shorted.

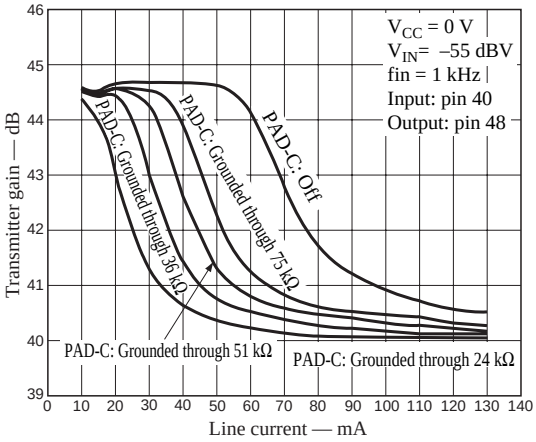
Ground Line Routing



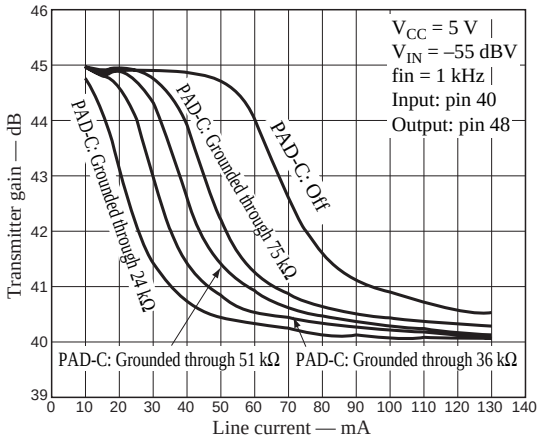
Line Voltage vs. Line Current



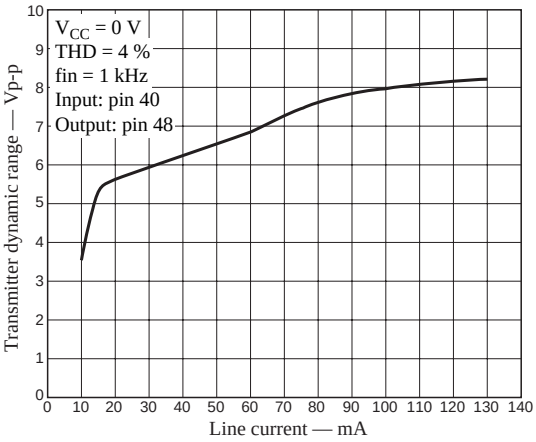
Transmitter Gain vs. Line Current (Power off)



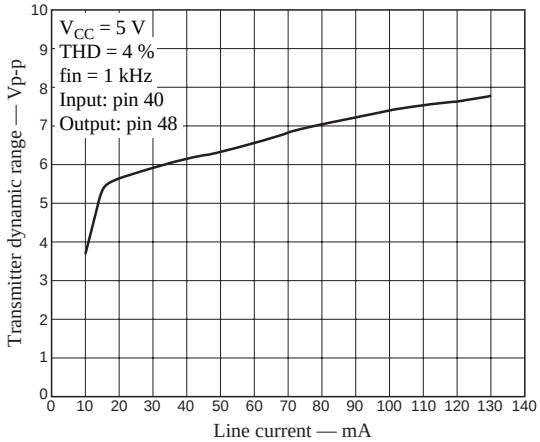
Transmitter Gain vs. Line Current (Power supplied)



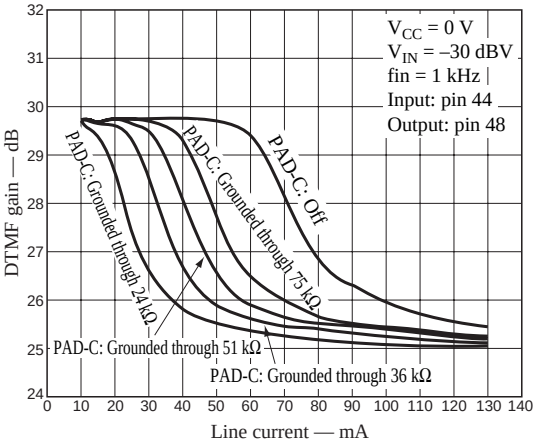
Transmitter Dynamic Range vs. Line Current (Power off)



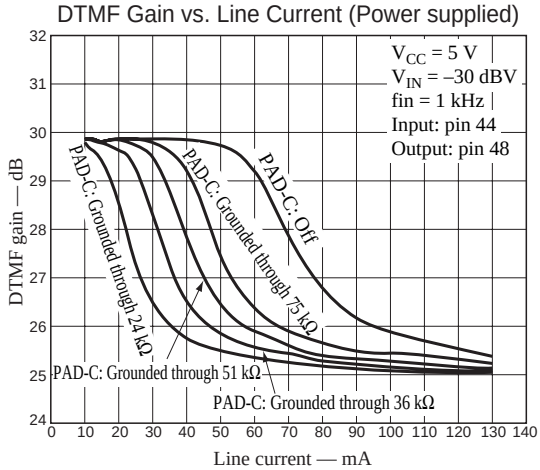
Transmitter Dynamic Range vs. Line Current (Power supplied)



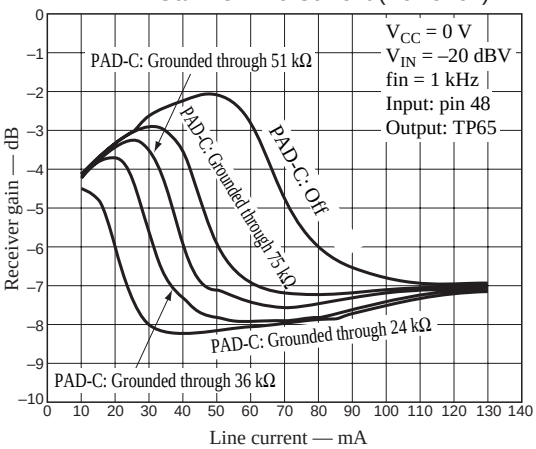
DTMF Gain vs. Line Current (Power off)



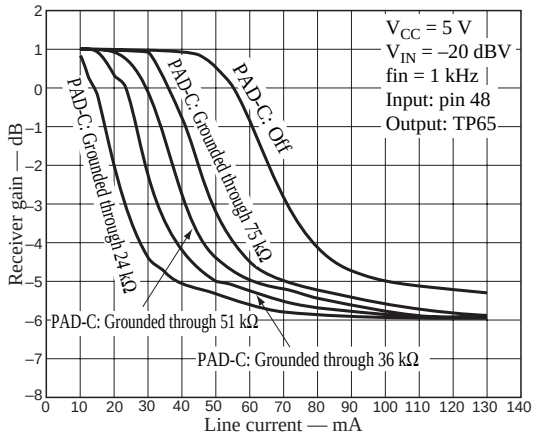
DTMF Gain vs. Line Current (Power supplied)



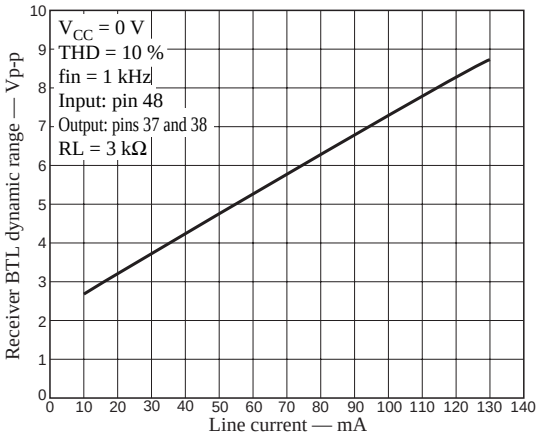
DTMF Gain vs. Line Current (Power off)



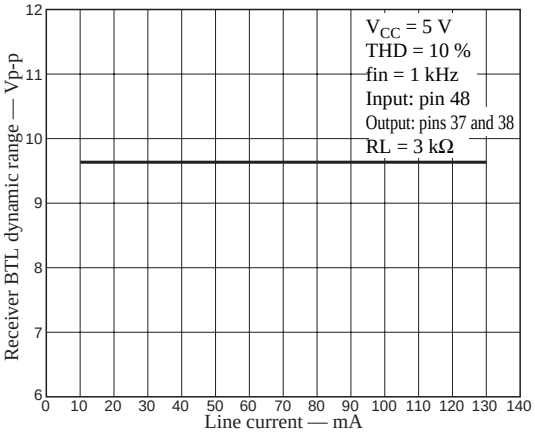
Receiver Characteristics vs. Line Current (Power supplied)



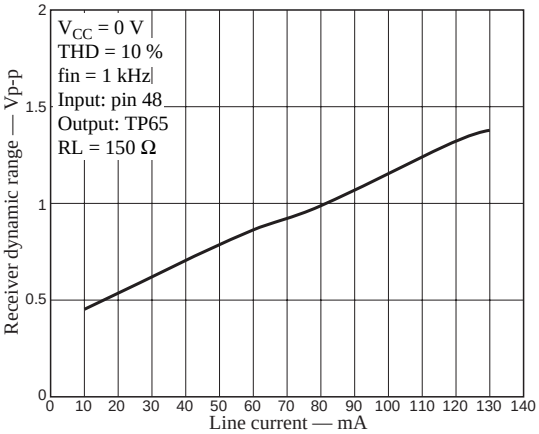
Receiver BTL Dynamic Range vs. Line Current (Power off)



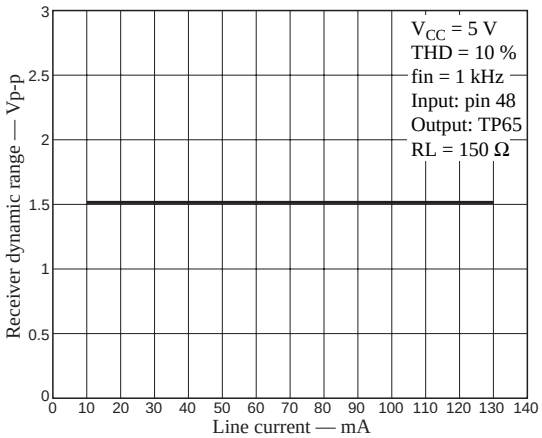
Receiver BTL Dynamic Range vs. Line Current (Power supplied)



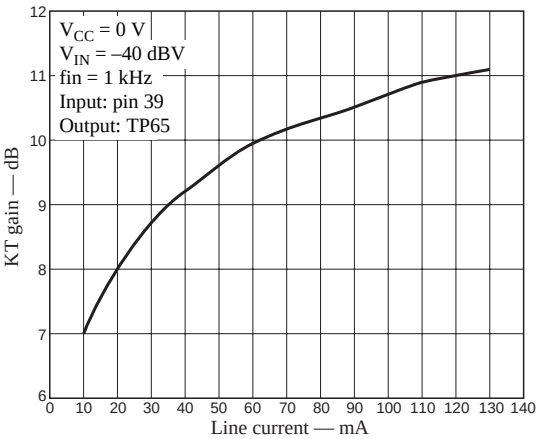
Receiver Dynamic Range vs. Line Current (Power off)



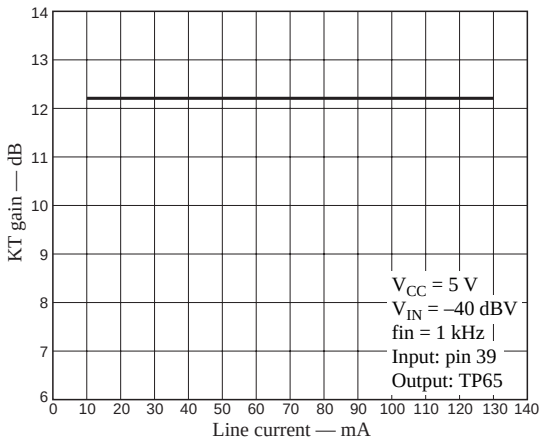
Receiver Dynamic Range vs. Line Current (Power supplied)



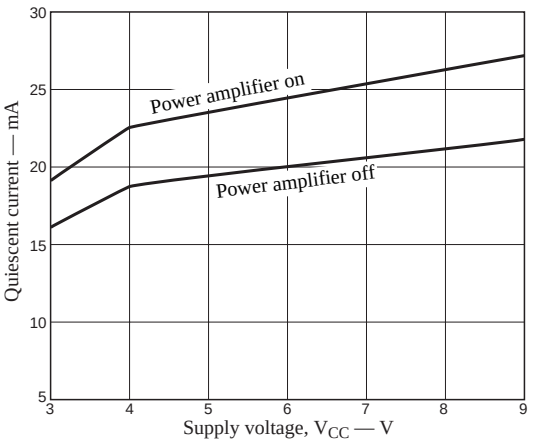
KT Gain vs. Line Current (Power off)



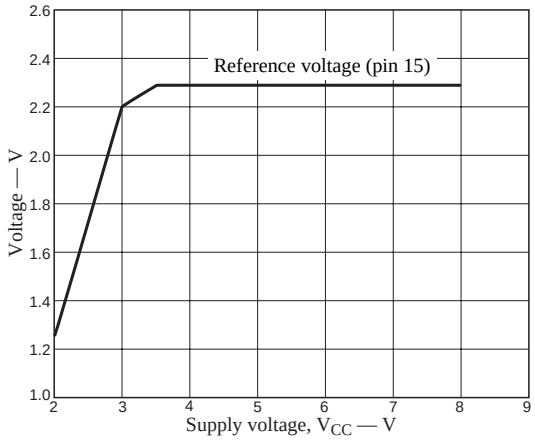
KT Gain vs. Line Current (Power supplied)



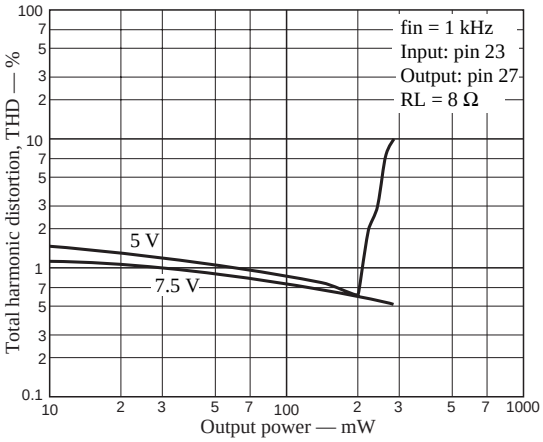
Quiescent Current vs. Supply Voltage



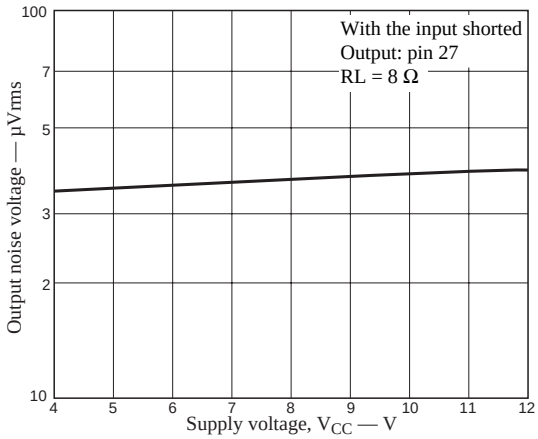
Reference Voltage (pin 15) vs. Supply Voltage



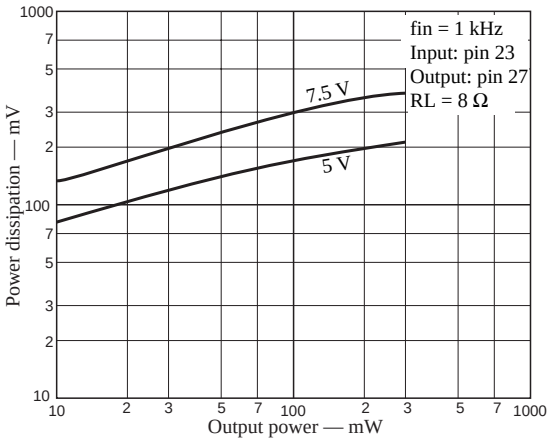
Power Amplifier: Output Power vs. Distortion



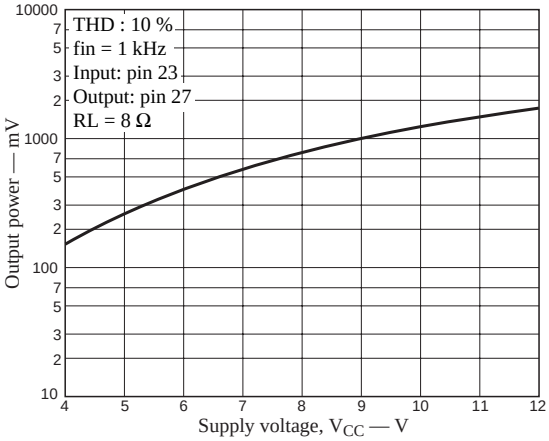
Power Amplifier: Output Noise Voltage vs. Supply Voltage



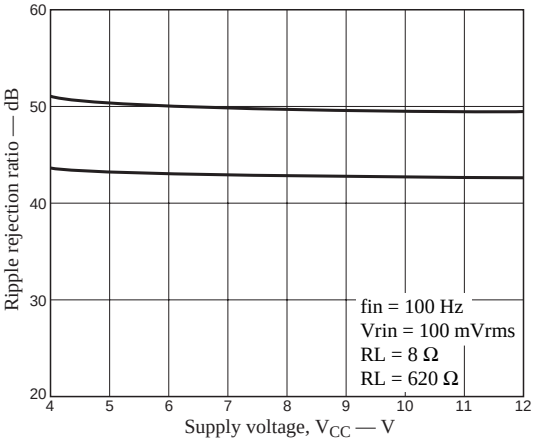
Power Amplifier: Output Power vs. Power Dissipation



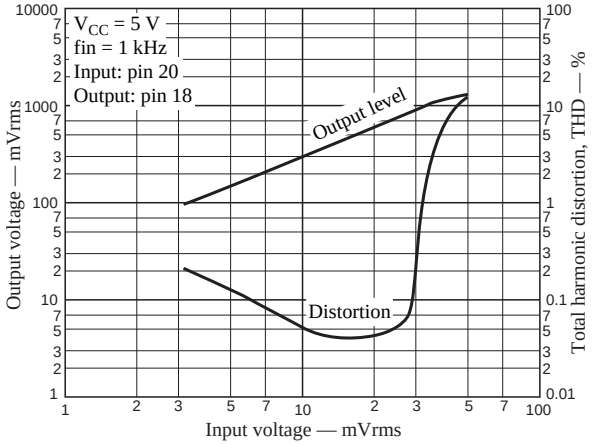
Power Amplifier: Supply Voltage vs. Output Power



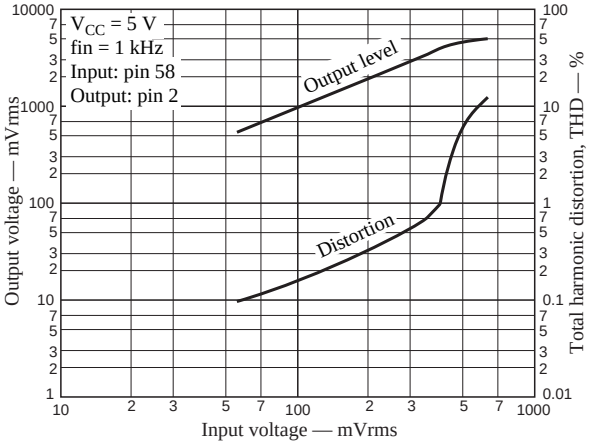
Power Amplifier Ripple Rejection Ratio vs. Supply Voltage



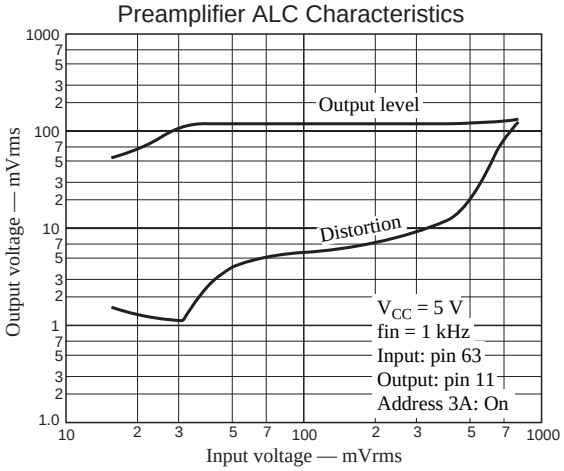
Microphone Amplifier Input/Output Characteristics



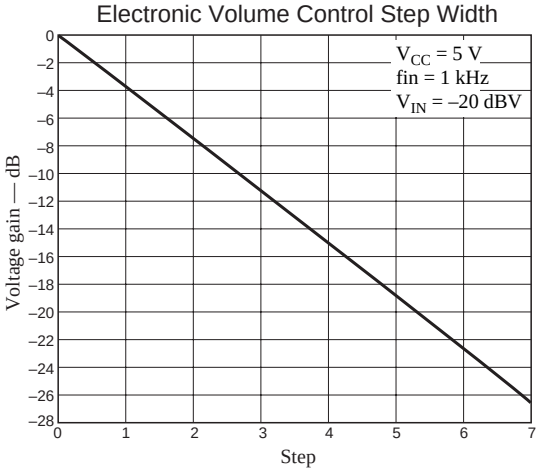
Crosspoint Switch Input/Output Characteristics



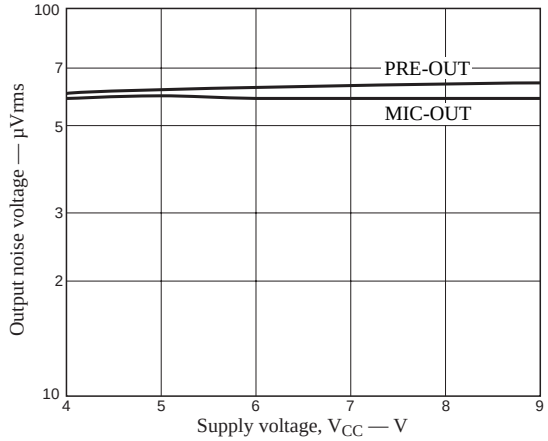
Preamplifier ALC Characteristics



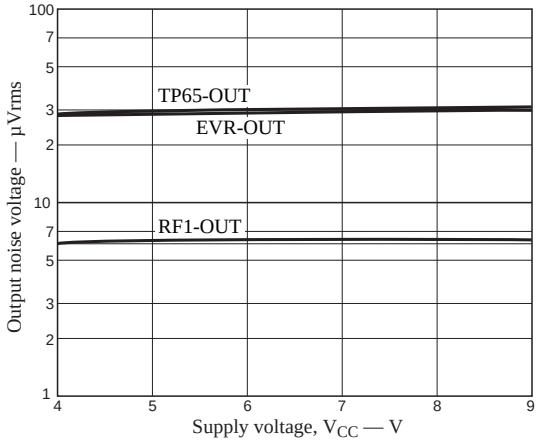
Electronic Volume Control Step Width



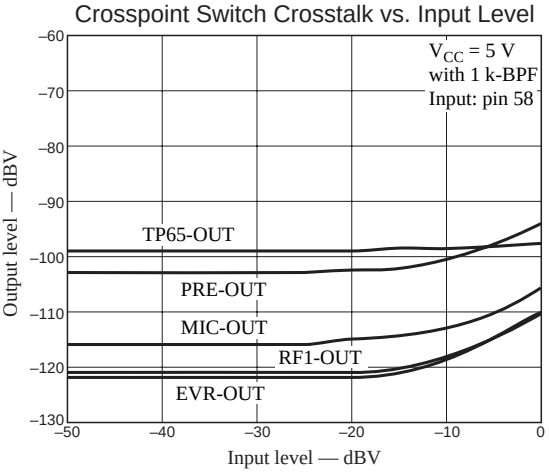
PRE/Microphone Amplifier Output Noise Voltage vs. Supply Voltage



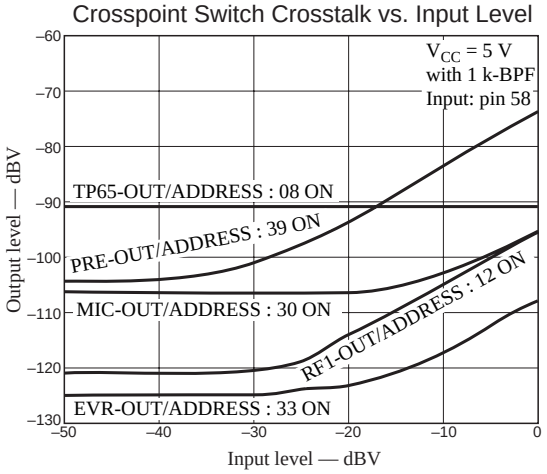
Crosspoint Switch Output Noise Voltage vs. Supply Voltage



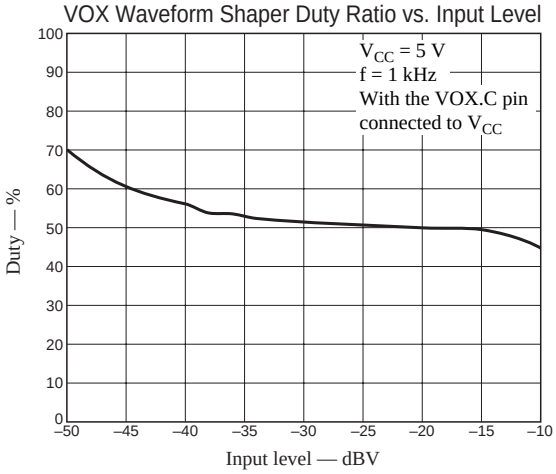
Crosspoint Switch Crosstalk vs. Input Level



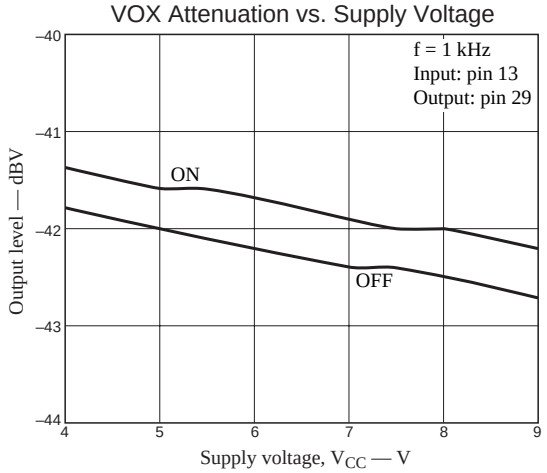
Crosspoint Switch Crosstalk vs. Input Level



VOX Waveform Shaper Duty Ratio vs. Input Level



VOX Attenuation vs. Supply Voltage



Equivalent Input Noise Voltage vs. Supply Voltage