Ordering number: EN2258E

SANYO

No. 2258E

LC6543C, 6543H, 6546C, 6546H

CMOS LSI
SINGLE-CHIP 4-BIT MICROCOMUPTER FOR SMALL-SCALE CONTROL-ORIENTED APPLICATIONS

The LC6543C/H, LC6546C/H belong to our single-chip 4-bit microcomputer LC6500 series fabricated using CMOS process technology and are suited for use in small-scale control-oriented applications. Their basic architecture and instruction set are the same. Application areas include audio equipment (tape deck, player, etc.), office equipment, communications equipment, car equipment, home appliances as well as circuits so far formed with standard logic circuits and applications where the number of controls is small.

Features

1) CMOS technology for low-power operation (with instruction-controlled standby function)
2) ROM/RAM
   LC6543C/H ROM: 2K x 8 bits, RAM: 128 x 4 bits
   LC6546C/H ROM: 1K x 8 bits, RAM: 64 x 4 bits
3) Instruction set: 80 instructions common to the LC6500 series
4) Wide operating voltage range from 3.0 V to 6.0 V (C version)
5) Instruction cycle time of 0.92 usec. (H version)
6) On-chip serial I/O port
7) Flexible I/O ports
   - Number of ports: 7 ports/25 pins max.
   - All ports: Input/output common
     Input/output voltage 15 V max. (open drain type)
     Output current 20 mA max. (sink current) (LED direct drivable)
   - Option selectable for your intended system
     (A) Open drain output, pull-up resistor: Single-bit select for all ports
     (B) Output level at the reset mode: 4-bit select of H/L level for port C/D
8) Interrupt function
   Vectored interrupt by timer overflow (instruction-testable)
   Vectored interrupt by $\overline{\text{INT}}$ pin or completion of transmit/receive at serial I/O port (instruction-testable)
9) Stack level: 4 levels (common with interrupt)
10) Timer: 4-bit prescaler + 8 bit programmable timer
11) Clock oscillation option selectable for your intended system
    - Oscillator option: 1-pin C oscillation (with R), 2-pin RC oscillation (C version), 2-pin ceramic resonator oscillation, 1-pin external clock (C version and H version), crystal oscillation (C version and H version constants being checked)
    - Predivider option: No predivider, 1/3 predivider, 1/4 predivider (C version)
12) Burst pulse (64 x cycle time, duty 50%) output function

SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
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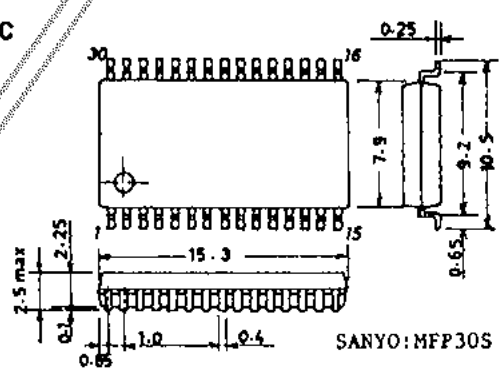
Item		LC6543C	LC6543H	LC6546C	LC6546H
Memory	ROM	2048 x 8 bits	2048 x 8 bits	1024 x 8 bits	1024 x 8 bits
	RAM	128 x 4 bits	128 x 4 bits	64 x 4 bits	64 x 4 bits
Instruction	Instruction set	80	80	80	80
	Table read	With	With	With	With
On-chip function	Interrupt	External 1, Internal 1	External 1, Internal 1	External 1, Internal 1	External 1, Internal 1
	Timer	4-bit prescaler + 8-bit timer	4-bit prescaler + 8-bit timer	4-bit prescaler + 8-bit timer	4-bit prescaler + 8-bit timer
	Stack level	4	4	4	4
	Standby function	Standby available by HALT instruction	Standby available by HALT instruction	Standby available by HALT instruction	Standby available by HALT instruction
Input/output port	Number of ports	I/O 25 max.	I/O 25 max.	I/O 25 max.	I/O 25 max.
	Serial port	4/8-bit I/O	4/8-bit I/O	4/8-bit I/O	4/8-bit I/O
	I/O voltage	15V max.	15V max.	15V max.	15V max.
	Output current	10mA typ. 20mA max.	10mA typ. 20mA max.	10mA typ. 20mA max.	10mA typ. 20mA max.
	I/O circuit configuration	Open drain (N channel) or pull-up resistor-provided output selectable bit by bit.			
	Output level at reset mode	"H" or "L" level selectable port by port (port C, D only)			
	Burst pulse output	Available	Available	Available	Available
Characteristic	Minimum cycle time	2.77μs (V_{DD}≧4V) 6.0μs (V_{DD}≧3V)	0.92μs	2.77μs (V_{DD}≧4V) 6.0μs (V_{DD}≧3V)	0.92μs
	Supply voltage	3 to 6V	4.5 to 6V	3 to 6V	4.5 to 6V
	Current dissipation	2.5mA typ.	4mA typ.	2.5mA typ.	4mA typ.
Oscillation	Resonator	RC (600kHz typ.) Ceramic (400k, 800k, 1MHz, 4MHz)	Ceramic 4MHz	RC (600kHz typ.) Ceramic (400k, 800k, 1MHz, 4MHz)	Ceramic 4MHz
	Predivider option	1/1, 1/3, 1/4	1/1	1/1, 1/3, 1/4	1/1
Other	Package	DIP30 shrink type, MFP30S	DIP30 shrink type, MFP30S	DIP30 shrink type, MFP30S	DIP30 shrink type MFP30S

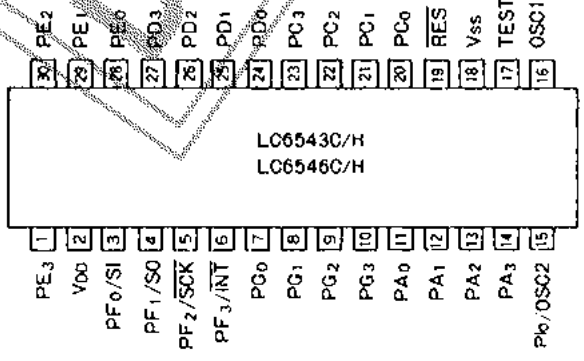
Note) Information on the resonator and oscillation circuit constants will be presented as soon as the recommended circuit is determined.

Case Outline 3073A-M30IC
(unit: mm)

When mounting the MFP version on the board, do not dip it in solder.

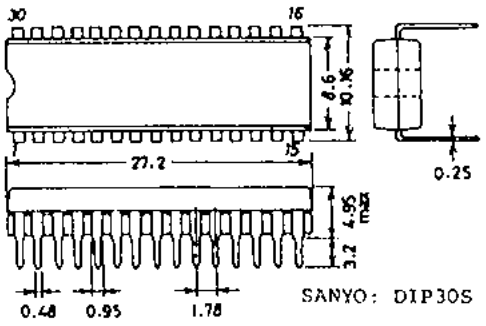


Pin Assignment



Common to DIP/MFP

Case Outline 3061-D30SIC
(unit: mm)



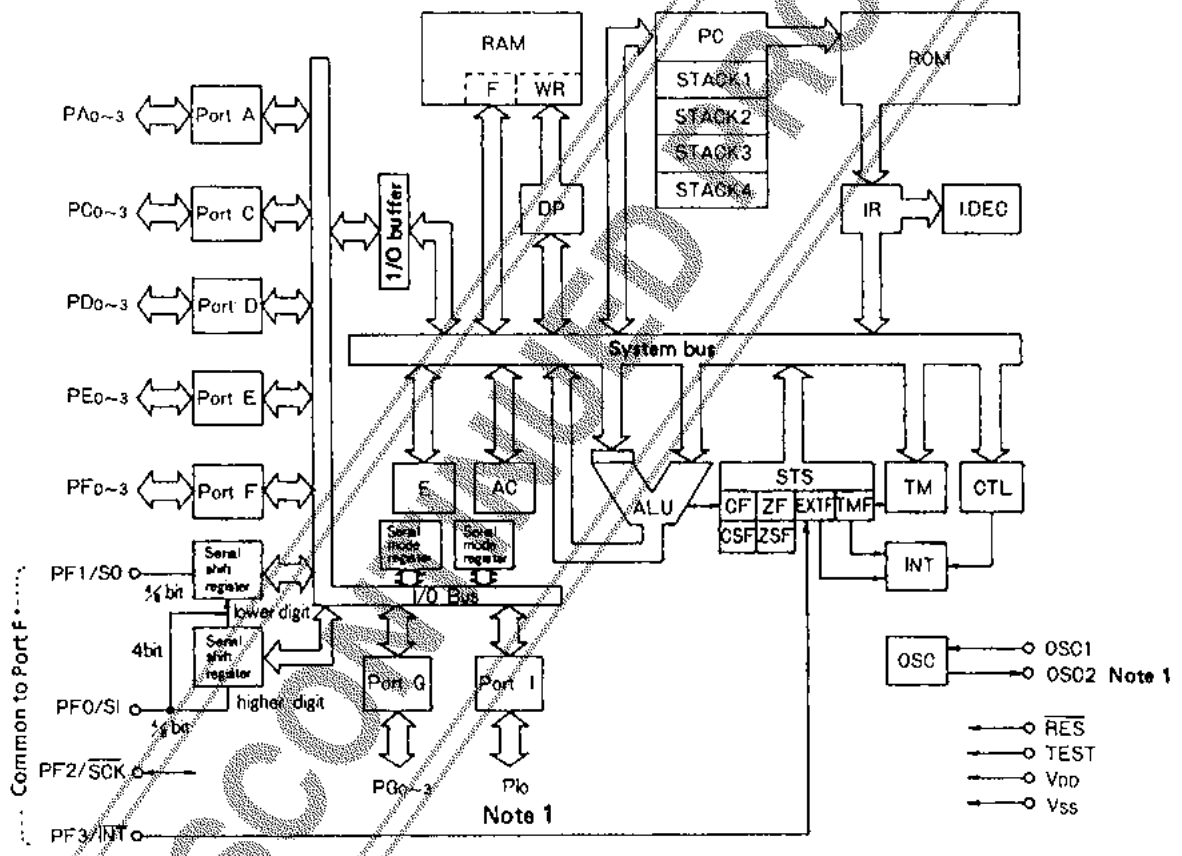
Pin Name

OSC1, OSC2	: R, C or ceramic resonator for OSC	TEST	: Test
$\overline{RES}$	: Reset	$\overline{INT}$	: Interrupt request pin
$PA_{0 \text{ to } 3}$	: Input/output common port A_0 to 3	SI	: Serial input pin
$PC_{0 \text{ to } 3}$	: Input/output common port C_0 to 3	SO	: Serial output pin
$PD_{0 \text{ to } 3}$	: Input/output common port D_0 to 3	$\overline{SCK}$	: Serial clock input/output pin
$PE_{0 \text{ to } 3}$	: Input/output common port E_0 to 3		
$PF_{0 \text{ to } 3}$	: Input/output common port F_0 to 3		
$PG_{0 \text{ to } 3}$	: Input/output common port G_0 to 3		
PI_0	: Input/output common port I_0		

Note) • The SI, SO, $\overline{SCK}$, and $\overline{INT}$ pins are common to the PF_0 to PF_3 pins respectively.
• The OSC2 pin and PI_0 pin are common to each other, but are mutually exclusive. Either pin is user-selectable.

System Block Diagram

LC6543C/H, LC6546C/H



Note 1. The OSC2 pin and PI_0 pin are common to each other, but are mutually exclusive. Either pin is user-selectable.

RAM	: Data memory	ROM	: Program memory
F	: Flag	PC	: Program counter
WR	: Working register	INT	: Interrupt control
AC	: Accumulator	IR	: Instruction register
ALU	: Arithmetic and logic unit	I.DEC	: Instruction decoder
DP	: Data pointer	CF, CSF	: Carry flag, carry save flag
E	: E register	ZF, ZSF	: Zero flag, zero save flag
CTL	: Control register	EXTF	: External interrupt request flag
OSC	: Oscillator	TMF	: Internal interrupt request flag
TM	: Timer		
STS	: Status register		

Development Support Tools

The following are available to support the program development for the LC6543, LC6546.

(1) User's Manual
"LC6554 Series User's Manual" No. E21B (Issued in December, 1987)

(2) Development Tool Manual
For the EVA-410 system, refer to the description of Development support tool in "LC6554 Series User's Manual".
For the EVA-800 system, refer to "EVA-800 · LC6554 Series Development Tool Manual".

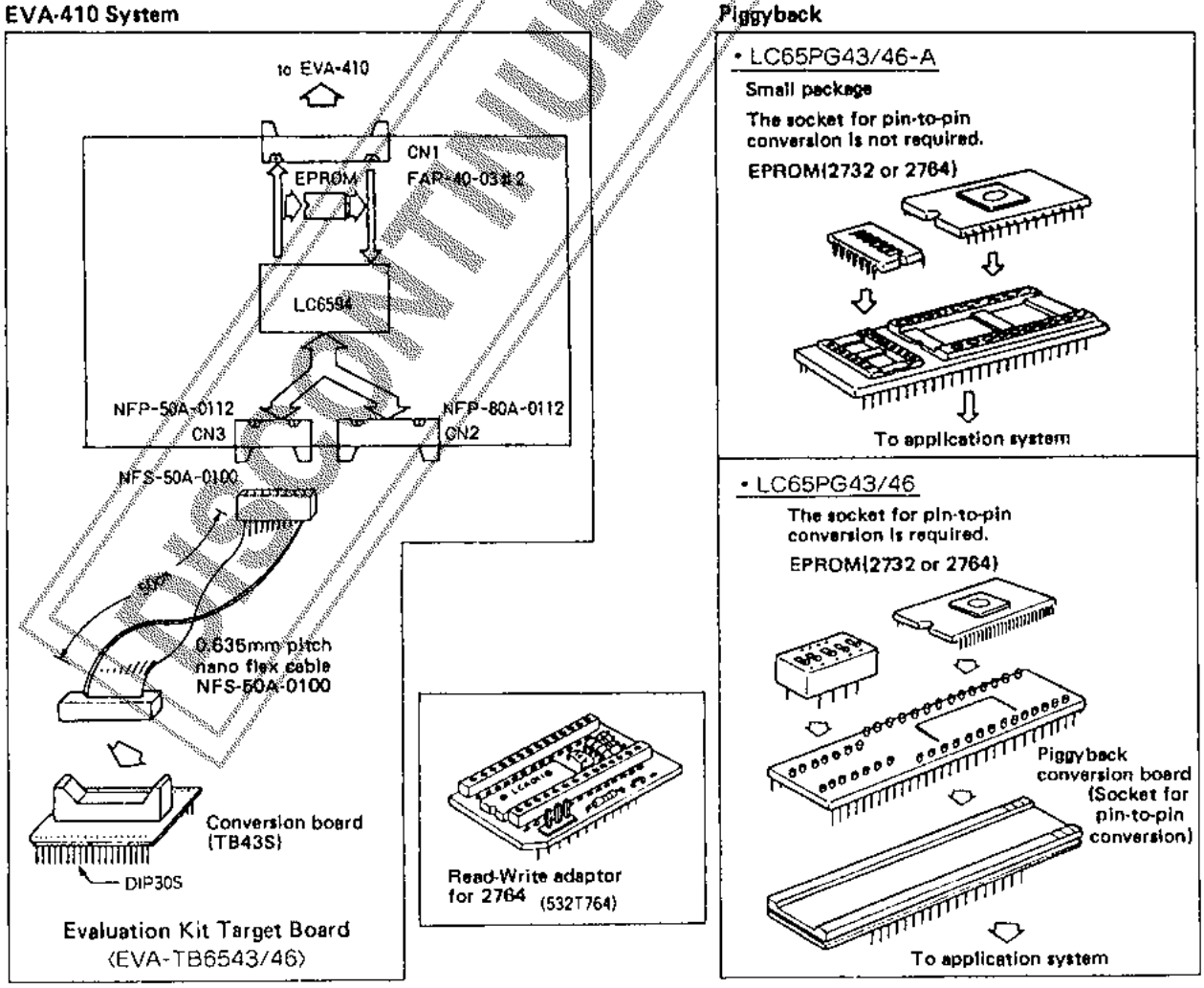
(3) Development Tools

1) For program development (EVA-410 system)
   i. MS-DOS for host system (Note 1)
   ii. MS-DOS base cross assembler: < LC65S.EXE >
   iii. Evaluation kit (EVA-410C)
   iv. Evaluation kit target board (EVA-TB6543/46), evaluation chip (LC6594)

2) For program evaluation
   i. New piggyback (LC65PG43/46-A)
   - Small package
   - The socket for pin-to-pin conversion is not required.
   - For detailed information on how to use it, refer to page 33 of this catalog.

   ii. Piggyback (LC65PG43/46)
   - The socket for pin-to-pin conversion is required.

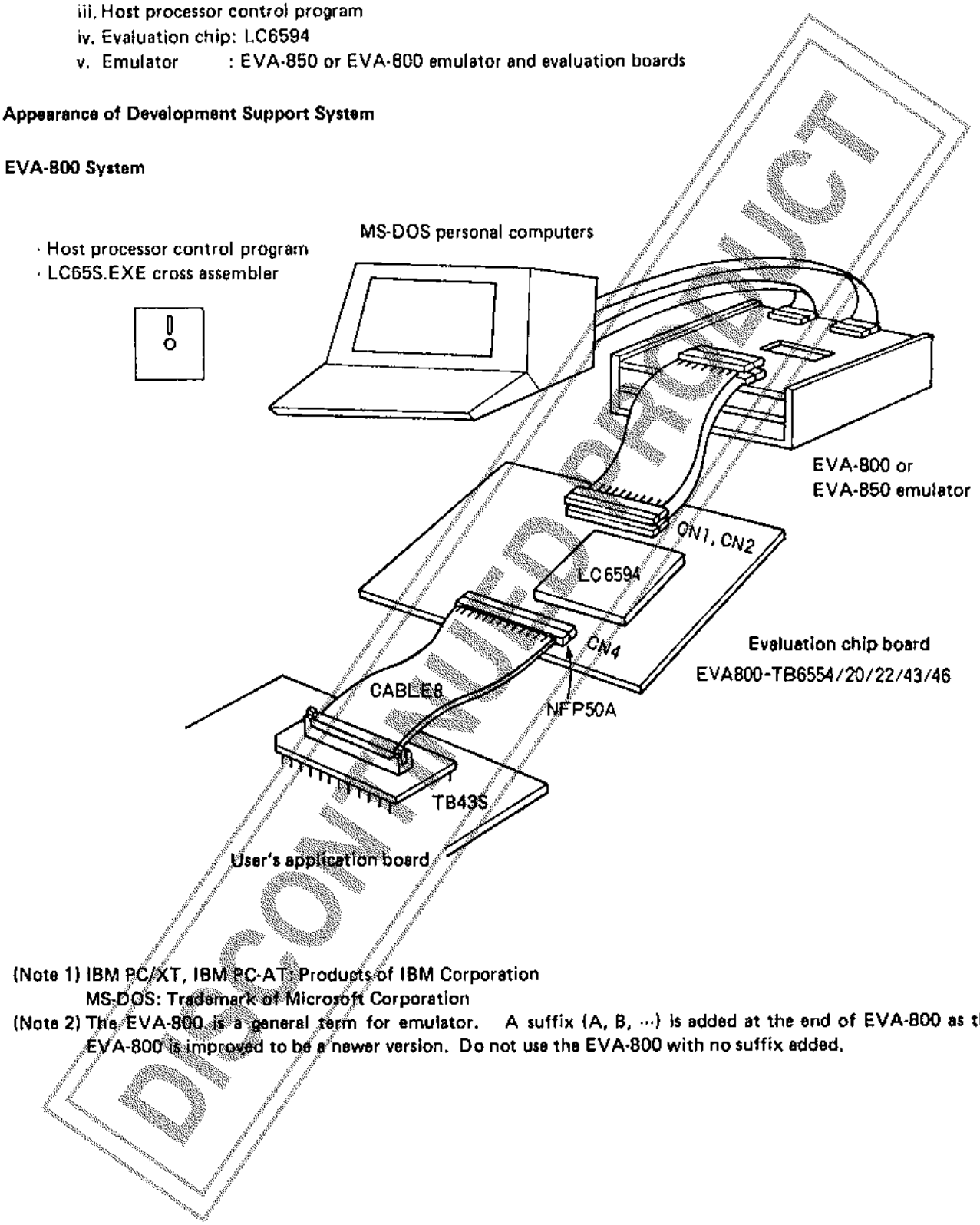
Note. For notes for program evaluation, do not fail to refer to "5-3-4. Notes when evaluating programs for the LC6543/46" in "LC6554 Series User's Manual".



3) For program development (EVA-800 system)
   i. MS-DOS personal computers compatible with IBM PC/XT and IBM PC-AT (Note 1)
   ii. Cross assembler ·····MS-DOS base cross assembler: < LC65S.EXE >
   iii. Host processor control program
   iv. Evaluation chip: LC6594
   v. Emulator : EVA-850 or EVA-800 emulator and evaluation boards

Appearance of Development Support System

EVA-800 System



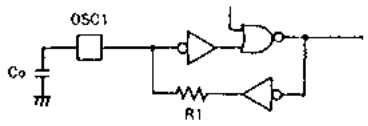
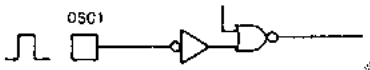
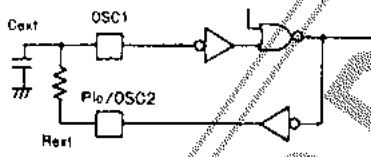
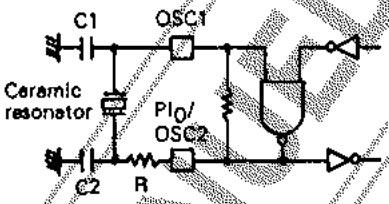
(Note 1) IBM PC/XT, IBM PC-AT: Products of IBM Corporation
MS-DOS: Trademark of Microsoft Corporation
(Note 2) The EVA-800 is a general term for emulator. A suffix (A, B, ···) is added at the end of EVA-800 as the EVA-800 is improved to be a newer version. Do not use the EVA-800 with no suffix added.

Pin Description

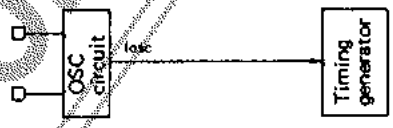
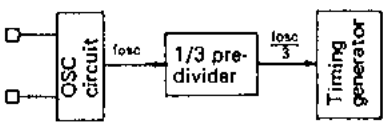
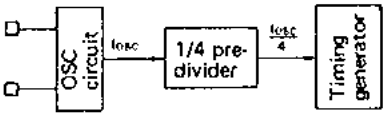
Pin Name	Pins	I/O	Function	Option	When in the Reset Mode
V_{DD} V_{SS}	1 1	— —	Power supply	—	—
OSC1	1	Input	• Pin for externally connecting C, RC, ceramic resonator for system clock generation. • For 1-pin external clock input, 1-pin C OSC, the PI_0/OSC2 pin is used as I/O port PI_0 • For 2-pin RC OSC, 2-pin ceramic resonator OSC, the PI_0/OSC2 pin is used as OSC pin OSC2.	1) 1-pin external clock input 2) 1-pin C OSC 3) 2-pin RC OSC 4) 2-pin ceramic resonator OSC 5) Predivider option 1. No predivider 2. 1/3 predivider 3. 1/4 predivider	—
PA_0 PA_1 PA_2 PA_3	4	Input/ output	• I/O port A_0 to 3. 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit decision (BP, BNP instruction) Single-bit set/reset (SPB, RPB Instruction) • Standby is controlled by PA_3 (or $PA_{0\text{ to }3}$). • The PA_3 (or $PA_{0\text{ to }3}$) pin must be free from chattering during the HALT instruction execution cycle.	1) Open drain type output 2) With pull-up resistor 1), 2): Specified bit by bit	• "H" output (Output Nch transistor: OFF)
PC_0 PC_1 PC_2 PC_3	4	Input/ output	• I/O port $C_{0\text{ to }3}$ Same as for $PA_{0\text{ to }3}$ (Note) • Option permits output at the reset mode to be "H" or "L". (Note) No standby control function is provided.	1) Open drain type output 2) With pull-up resistor 3) Output at the reset mode: "H" 4) Output at the reset mode: "L" • 1), 2): Specified bit by bit • 3), 4): Specified in a group of 4 bits	• "H" output • "L" output (Option-selectable)
PD_0 PD_1 PD_2 PD_3	4	Input/ output	• I/O port $D_{0\text{ to }3}$ Same as for $PC_{0\text{ to }3}$	Same as for $PC_{0\text{ to }3}$	Same as for $PC_{0\text{ to }3}$
PE_0 PE_1 PE_2 PE_3	4	Input/ output	• I/O port $E_{0\text{ to }3}$ 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit decision (BP, BNP instruction) Single-bit set/reset (SPB, RPB instruction) • PE_0: With burst pulse ($64T_{CYC}$) output function	1) Open drain type output 2) With pull-up resistor 1), 2): Specified bit by bit	"H" output (Output Nch transistor OFF)

Pin Name	Pins	I/O	Function	Option	When in the Reset Mode
PF_0/SI PF_1/SO PF_2/$\overline{SCK}$ PF_3/$\overline{INT}$	4	Input/ output	•I/O port $F_{0 \text{ to } 3}$ Same as for $PE_{0 \text{ to } 3}$ (Note) •$PF_{0 \text{ to } 3}$: Common with serial interface, $\overline{INT}$ input. Program-selectable SI ----- Serial input port SO ----Serial output port $\overline{SCK}$--Serial clock Input/output $\overline{INT}$---Interrupt request input 4-bit/8-bit serial input/output is program-selectable. (Note) No burst pulse output function is provided.	Same as for $PE_{0 \text{ to } 3}$	Same as for $PE_{0 \text{ to } 3}$ Serial port: Disable Interrupt source: $\overline{INT}$
PG_0 PG_1 PG_2 PG_3	4	Input/ output	•I/O port $G_{0 \text{ to } 3}$ Same as for $PE_{0 \text{ to } 3}$ (Note) (Note) No burst pulse output function is provided.	Same as for $PE_{0 \text{ to } 3}$	Same as for $PE_{0 \text{ to } 3}$
PI_0/OSC2	1	Input· output/ output	•I/O port I_0 Same as for $PG_{0 \text{ to } 3}$ •Single-bit configuration •For 2-pin OSC, this pin is used as the OSC2 pin, providing no function as I/O port.	Same as for $PG_{0 \text{ to } 3}$	Same as for $PG_{0 \text{ to } 3}$
$\overline{RES}$	1	Input	•System reset input •For power-up reset, C is connected externally. •For reset restart, "L" level is applied for 4 clock cycles or more.		
TEST	1	Input	•LSI test pin Normally connected to V_{SS}		

Oscillator Circuit Option

Option Name	Circuit	Conditions, etc.
1. 1-pin C OSC		The PI_0/OSC2 pin is used as port PI_0.
2. External clock		The PI_0/OSC2 pin is used as port PI_0.
3. 2-pin RC OSC		The PI_0/OSC2 pin is used as OSC pin OSC2, providing no function as port.
4. Ceramic resonator OSC		The PI_0/OSC2 pin is used as OSC pin OSC2, providing no function as port.

Predivider Option

Option Name	Circuit	Conditions, etc.
1. No predivider (1/1)		●Applicable to all of 4 OSC options. ●The OSC frequency, external clock do not exceed 1444kHz. (LC6543C, 6546C) ●The OSC frequency, external clock do not exceed 4330kHz (LC6543H, 6546H).
2. 1/3 predivider		●Applicable to only 2 options of external clock, ceramic resonator OSC. ●The OSC frequency, external clock do not exceed 4330kHz.
3. 1/4 predivider		●Applicable to only 2 options of external clock, ceramic resonator OSC. ●The OSC frequency, external clock do not exceed 4330kHz.

Note: The OSC option and predivider option are summarized below. Full care must be exercised.

Table of OSC, Predivider Option of LC6543C/46C,43H/46H

LC6543C, LC6546C

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	V_{DD} Range	Remarks
Ceramic resonator OSC	400kHz	1/1 (10μs)	3 to 6V	Unusable with 1/3, 1/4 predivider
	800kHz	1/1 (5μs) 1/3 (15μs) 1/4 (20μs)	4 to 6V 4 to 6V 4 to 6V	
	1MHz	1/1 (4μs) 1/3 (12μs) 1/4 (16μs)	4 to 6V 4 to 6V 4 to 6V	
	4MHz	1/3 (3μs) 1/4 (4μs)	4 to 6V 4 to 6V	Unusable with 1/1 predivider
1-pin external clock	200k to 667kHz 600k to 2000kHz 800k to 2667kHz 200k to 1444kHz 600k to 4330kHz 800k to 4330kHz	1/1 (20 to 6μs) 1/3 (20 to 6μs) 1/4 (20 to 6μs) 1/1 (20 to 2.77μs) 1/3 (20 to 2.77μs) 1/4 (20 to 3.70μs)	3 to 6V 3 to 6V 3 to 6V 4 to 6V 4 to 6V 4 to 6V	
External clock by 2-pin RC OSC circuit	Same as above			
1-pin C	Used with 1/1 predivider, recommended constants		4 to 6V	
	If used with other than recommended constants, the frequency, predivider option, V_{DD} range must be the same as for 1/pin external clock.			
2-pin RC	Same as above		3 to 6V 4 to 6V	
External clock input to the ceramic oscillation circuit	The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the external clock option or the 2-pin RC option.			

LC6543H, LC6546H

Circuit Configuration	Frequency	Predivider Option (Cycle Time)	V_{DD} Range	Remakrs
Ceramic resonator OSC	4MHz	1/1 (1μs)	4.5 to 6V	
1-pin external clock	200k to 4330kHz	1/1 (20 to 0.92μs)	4.5 to 6V	
External clock by ceramic resonator OSC circuit	The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the external clock option.			

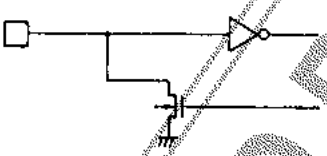
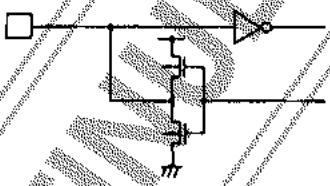
Option of Ports C, D Output Level at the Reset Mode

For input/output common ports C, D, either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions, etc.
1. Output at the reset mode: "H" level	All of 4 bits of ports C, D
2. Output at the reset mode: "L" level	All of 4 bits of ports C, D

Option of Port Output Configuration

For each input/output common port, either of the following two output configurations may be selected by option (Bitwise).

Option Name	Circuit	Conditions, etc.
1. Open drain output		●Unapplicable to port PI_0/OSC2 when 2-pin RC OSC or ceramic resonator OSC is selected.
2. Output with pull-up resistor		

LC6543C, 6546C

1. Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

					unit
Maximum Supply Voltage	V_{DD} max		V_{DD}	−0.3 to +7.0	V
Output Voltage	V_O		OSC2	Allowable up to voltage generated	V
Input Voltage	$V_{I(1)}$		OSC1 (*1)	−0.3 to V_{DD}+0.3	V
	$V_{I(2)}$		TEST, $\overline{RES}$	−0.3 to V_{DD}+0.3	V
Input/Output Voltage	$V_{IO(1)}$		Port of OD type	−0.3 to +15	V
	$V_{IO(2)}$		Port of PU type OSC1 for 1-pin C OSC	−0.3 to V_{DD}+0.3	V
Peak Output Current	I_{OP}		I/O port	−2 to +20	mA
Average Output Current	I_{OA}	Per pin over the period of 100msec.	I/O port	−2 to +20	mA
	$\Sigma I_{OA(1)}$	Total current of PC_0 to 3, PD_0 to 3, PE_0 to 3 (*2)		−15 to +100	mA
	$\Sigma I_{OA(2)}$	Total current of PF_0 to 3, PG_0 to 3, PA_0 to 3, PI_0 (*2)		−15 to +100	mA
Allowable Power Dissipation	Pd max (1)	Ta=−30 to +70°C (DIP package)		400	mW
	Pd max (2)	Ta=−30 to +70°C (MFP package)		200	mW
Operating Temperature	Topg			−30 to +70	°C
Storage Temperature	Tstg			−55 to +125	°C

LC6543C, 6546C

2. Allowable Operating Conditions at Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=3.0 to 6.0V

				min	typ	max	unit
Operating Supply Voltage	V_{DD}		V_{DD}	3.0		6.0	V
Standby Supply Voltage	Vst	RAM, register hold (*3)	V_{DD}	1.8		6.0	V
"H"-Level Input Voltage	$V_{IH}(1)$	Output Nch Tr OFF	Port of OD type (except I_0)	0.7V_{DD}		+13.5	V
	$V_{IH}(2)$	Output Nch Tr OFF	Port of PU type (except I_0)	0.7V_{DD}		V_{DD}	V
	$V_{IH}(3)$	Output Nch Tr OFF	$\overline{INT}$, SCK, SI, I_0 of OD type	0.8V_{DD}		+13.5	V
	$V_{IH}(4)$	Output Nch Tr OFF	$\overline{INT}$, SCK SI, I_0 of PU type	0.8V_{DD}		V_{DD}	V
	$V_{IH}(5)$		$\overline{RES}$	0.8V_{DD}		V_{DD}	V
	$V_{IH}(6)$	External clock mode	OSC1	0.8V_{DD}		V_{DD}	V
"L"-Level Input Voltage	$V_{IL}(1)$	Output Nch Tr OFF	V_{DD}=4 to 6V, Port	V_{SS}		0.3V_{DD}	V
	$V_{IL}(2)$	Output Nch Tr OFF	Port	V_{SS}		0.25V_{DD}	V
	$V_{IL}(3)$	Output Nch Tr OFF	V_{DD}=4 to 6V, $\overline{INT}$, SCK, SI	V_{SS}		0.25V_{DD}	V
	$V_{IL}(4)$	Output Nch Tr OFF	$\overline{INT}$, SCK, SI	V_{SS}		0.2V_{DD}	V
	$V_{IL}(5)$	External clock mode	V_{DD}=4 to 6V, OSC1	V_{SS}		0.25V_{DD}	V
	$V_{IL}(6)$	External clock mode	OSC1	V_{SS}		0.2V_{DD}	V
	VIL(7)		V_{DD}=4 to 6V, TEST	V_{SS}		0.3V_{DD}	V
	$V_{IL}(8)$		TEST	V_{SS}		0.25V_{DD}	V
	$V_{IL}(9)$		V_{DD}=4 to 6V, $\overline{RES}$	V_{SS}		0.25V_{DD}	V
	$V_{IL}(10)$		$\overline{RES}$	V_{SS}		0.2V_{DD}	V
Operating Frequency (Cycle Time)	f_{op} (T_{CYC})	When the 1/3 or 1/4 predivider option is selected, clock must not exceed 4.33MHz.	V_{DD}=4 to 6V	200 (20)		1444 (2.77)	kHz (μs)
				200 (20)		667 (6.0)	kHz (μs)
External Clock Conditions							
Frequency	fext	Fig. 1. When clock exceeds 1.444MHz, the 1/3 or 1/4 predivider option is selected.	V_{DD}=4 to 6V, OSC1	200		4330	kHz
				200		667	kHz
Pulse Width	t_{extH}, t_{extL}		V_{DD}=4 to 6V, OSC1	69			ns
				180			ns
Rise/Fall Time	t_{extR}, t_{extF}		V_{DD}=4 to 6V, OSC1			50	ns
						100	ns
Oscillation Guaranteed Constants							
1-pin C Oscillation	C_O	Fig. 2	V_{DD}=4 to 6V, OSC1		180±5%		pF
2-pin RC Oscillation	Cext	Fig. 3	OSC1, OSC2		270±5%		pF
	Rext	Fig. 3	OSC1, OSC2		12±1%		kohm
	Cext	Fig. 3	V_{DD}=4 to 6V, OSC1, OSC2		270±5%		pF
	Rext	Fig. 3	V_{DD}=4 to 6V, OSC1, OSC2		4.7±1%		kohm
Ceramic Resonator Oscillation		Fig. 4			Table 1		

3. Electrical Characteristics at Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=3.0 to 6.0V

				min	typ	max	unit
"H"-Level Input Current	$I_{IH}(1)$	Output Nch Tr OFF (including OFF leak current of Nch Tr) V_{IN}=+13.5V	Port of OD type			+5.0	μA
	$I_{IH}(2)$	External clock mode, V_{IN}=V_{DD}	OSC1			+1.0	μA
"L"-Level Input Current	$I_{IL}(1)$	Output Nch Tr OFF V_{IN}=V_{SS}	Port of OD type	−1.0			μA
	$I_{IL}(2)$	Output Nch Tr OFF V_{IN}=V_{SS}	Port of PU type	−1.3	−0.35		mA

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				min	typ	max	unit
	$I_{IL(3)}$	$V_{IN}=V_{SS}$	$\overline{RES}$	−45	−10		μA
	$I_{IL(4)}$	External clock mode, $V_{IN}=V_{SS}$	OSC1	−1.0			μA
"H"-Level Output Voltage	$V_{OH(1)}$	I_{OH}=−50μA, V_{DD}=4.0 to 6.0V	Port of PU type	V_{DD}−1.2			V
	$V_{OH(2)}$	I_{OH}=−10μA	Port of PU type	V_{DD}−0.5			V
"L"-Level Output Voltage	$V_{OL(1)}$	I_{OL}=10mA, V_{DD}=4.0 to 6.0V	Port			1.5	V
	$V_{OL(2)}$	I_{OL}=1mA, I_{OL} of each port: 1mA or less	Port			0.5	V
Hysteresis Voltage	V_{HYS}		$\overline{RES}$, $\overline{INT}$, SCK, SI, OSC1 of Schmitt type (*6)	0.1V_{DD}			V
Current Dissipation							
1-Pin C Oscillation	$I_{DDOP(1)}$	Fig. 2 f_{OSC}=600kHz (TYP)	V_{DD}=4 to 6V, V_{DD}		1.5	5	mA
2-Pin RC Oscillation	$I_{DDOP(2)}$	Fig. 3 f_{OSC}=750kHz (TYP)	V_{DD}=4 to 6V, V_{DD}		1.5	5	mA
	$I_{DDOP(3)}$	Fig. 3 f_{OSC}=350kHz (TYP)	V_{DD}		1.0	4	mA
Ceramic Resonator Oscillation	$I_{DDOP(4)}$	Fig. 4 4MHz, 1/3 predivider	V_{DD}=4 to 6V, V_{DD}		2.5	8	mA
	$I_{DDOP(5)}$	Fig. 4 4MHz, 1/4 predivider	V_{DD}=4 to 6V, V_{DD}		2.0	6	mA
	$I_{DDOP(6)}$	Fig. 4 400kHz	V_{DD}		0.5	2	mA
	$I_{DDOP(7)}$	Fig. 4 800kHz	V_{DD}=4 to 6V, V_{DD}		1.5	4	mA
External Clock	$I_{DDOP(8)}$	200kHz to 667kHz, 1/1 predivider 600kHz to 2000kHz, 1/3 predivider 800kHz to 2667kHz, 1/4 predivider	V_{DD}		1.5	5	mA
	$I_{DDOP(9)}$	200kHz to 1444kHz, 1/1 predivider 800kHz to 4330kHz, 1/3 predivider 800kHz to 4330kHz, 1/4 predivider	V_{DD}=4 to 6V, V_{DD}		2.5	8	mA
Standby Mode	I_{DDSt}	Output Nch Tr OFF, Port=V_{DD}	V_{DD}=6V, V_{DD}		0.05	10	μA
			V_{DD}=3V, V_{DD}		0.025	5	μA
Oscillation Characteristics							
Ceramic Resonator Oscillation							
Oscillation Frequency	f_{CFOSC} (*4)	Fig. 4, fo=400kHz	OSC1, OSC2	384	400	416	kHz
		Fig. 4, fo=800kHz	V_{DD}=4 to 6V, OSC1, OSC2	768	800	832	kHz
		Fig. 4, fo=1MHz	V_{DD}=4 to 6V, OSC1, OSC2	960	1000	1040	kHz
		Fig. 4, fo=4MHz, 1/3 predivider, 1/4 predivider	V_{DD}=4 to 6V, OSC1, OSC2	3840	4000	4160	kHz
Oscillation Stabilizing Period	t_{CFS}	Fig. 5, fo=400kHz				10	ms
		Fig. 5, fo=800kHz, 1MHz, 4MHz, 1/3 predivider, 1/4 predivider	V_{DD}=4 to 6V			10	ms
1-Pin C OSC Oscillation Frequency	f_{COSC}	Fig. 2, Co=180pF±5%	V_{DD}=4 to 6V, OSC1	310	600	1141	kHz
2-Pin RC OSC Oscillation Frequency	f_{MOSC}	Fig. 3, Cext=270pF±5% Fig. 3, Rext=4.7kohms±1%	V_{DD}=4 to 6V, OSC1, OSC2	612	850	1159	kHz
		Fig. 3, Cext=270pF±5% Fig. 3, Rext=12kohms±1%	OSC1, OSC2	275	400	642	kHz

Operating mode, Output Nch Tr OFF, Port=V_{DD}

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						min	typ	max	unit
Pull-up/Pull-down Resistance									
I/O Port Pull-up Resistance	R_{PP}		V_{DD}=5V, Port of PU type				14		kohm
External Reset Characteristics									
Reset Time	t_{RST}						See Fig. 6.		
Pin Capacitance	C_P	f=1MHz, Other than pins to be tested, $V_{IN}=V_{SS}$					10		pF
Serial Clock									
Input Clock Cycle Time	$t_{CKCY(1)}$	Fig. 7	V_{DD}=4 to 6V	$\overline{SCK}$		3.0			µs
				$\overline{SCK}$		12.0			µs
Output Clock Cycle Time	$t_{CKCY(2)}$	Fig. 7		$\overline{SCK}$		64 x T_{CYC} (T_{CYC}=4xSystem clock period)			µs
Input Clock "L"-Level Pulse Width	$t_{CKL(1)}$	Fig. 7	V_{DD}=4 to 6V	$\overline{SCK}$		1.0			µs
				$\overline{SCK}$		4.0			µs
Output Clock "L"-Level Pulse Width	$t_{CKL(2)}$	Fig. 7		$\overline{SCK}$		32 x T_{CYC}			µs
Input Clock "H"-Level Pulse Width	$t_{CKH(1)}$	Fig. 7	V_{DD}=4 to 6V	$\overline{SCK}$		1.0			µs
				$\overline{SCK}$		4.0			µs
Output Clock "H"-Level Pulse Width	$t_{CKH(2)}$	Fig. 7		$\overline{SCK}$		32 x T_{CYC}			µs
Serial Input									
Data Setup Time	t_{ICK}	Specified for ↑ of $\overline{SCK}$		SI		0.5			µs
Data Hold Time	t_{CKI}	Fig. 7		SI		0.5			µs
Serial Output									
Output Delay Time	t_{CKO}	Specified for ↓ of $\overline{SCK}$	V_{DD}=4 to 6V	SO				0.5	µs
		Nch OD only, External 1kohm, external 50pF, Fig. 7		SO				2.0	µs
Pulse Output									
Period	t_{PCY}	Fig. 8		PE_0		64 x T_{CYC}			µs
"H"-Level Pulse Width	t_{PH}	T_{CYC}=4 x System clock period		PE_0		32 x T_{CYC}		±10%	µs
"L"-Level Pulse Width	t_{PL}	Nch OD only, External 1kohm, External 50pF		PE_0		32 x T_{CYC}		∓10%	µs

(*1) When oscillated internally under the oscillating conditions in Fig. 4, up to the oscillation amplitude generated is allowable.

(*2) Average over the period of 100msec.

(*3) Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction.
The PA_3 (or PA_0 to 3) pin must be free from chattering during the HALT instruction execution cycle.

(*4) f_{CFOSC}: Oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic resonator mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

(*5) When mounting the MFP version on the board, do not dip it in solder.

(*6) The OSC1 pin can be schmitt-triggered when the 1-pin oscillation option, 2-pins oscillation option, or external clock oscillation option has been selected.

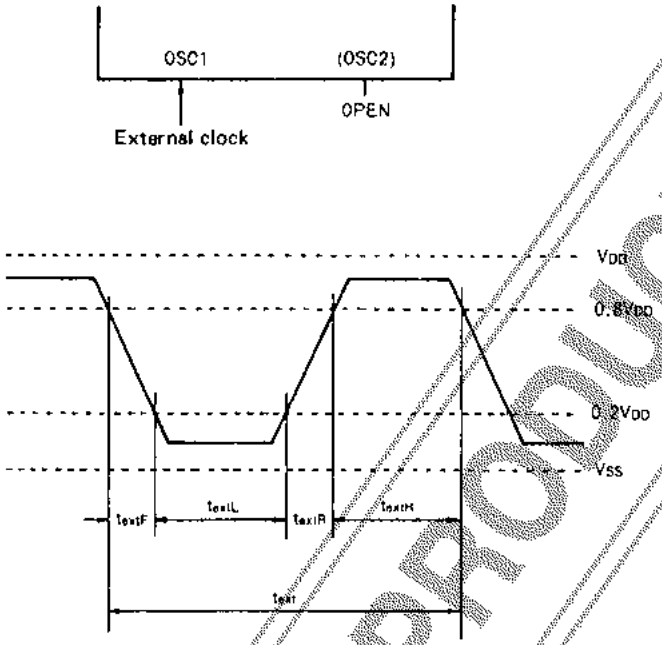


Fig. 1 External Clock Input Waveform

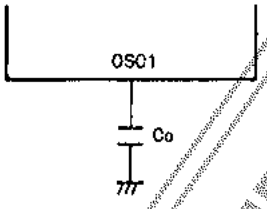


Fig. 2 1-Pin C Oscillation Circuit

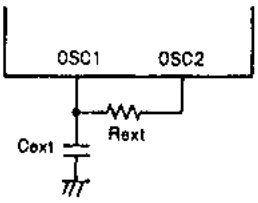


Fig. 3 2-Pin RC Oscillation Circuit

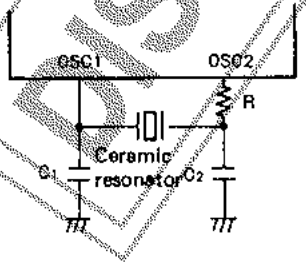


Fig. 4 Ceramic Resonator Oscillation Circuit

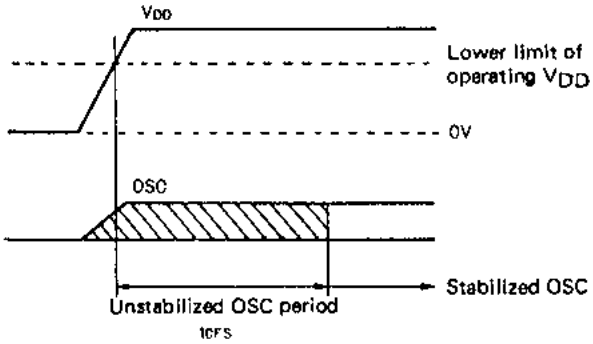


Fig. 5 Oscillation Stabilizing Period

4 MHz CSA4.00MG (Murata)	C_1	33pF±10%
	C_2	33pF±10%
	R	0Ω
4 MHz KBR4.0MS (Kyocera)	C_1	33pF±10%
	C_2	33pF±10%
	R	0Ω
1 MHz CSB1000K (Murata) CSB1000D (Murata)	C_1	220pF±10%
	C_2	220pF±10%
	R	0Ω
1 MHz KBR1000H (Kyocera)	C_1	100pF±10%
	C_2	100pF±10%
	R	0Ω
800KHz CSB800D (Murata)	C_1	220pF±10%
	C_2	220pF±10%
	R	0Ω
800KHz KBR800H (Kyocera)	C_1	220pF±10%
	C_2	220pF±10%
	R	0Ω
400KHz CSB400P (Murata)	C_1	330pF±10%
	C_2	330pF±10%
	R	0Ω
400KHz KBR400B (Kyocera)	C_1	330pF±10%
	C_2	330pF±10%
	R	0Ω

Table 1 Constants Guaranteed for Ceramic Resonator OSC

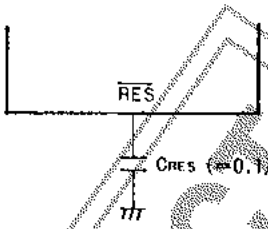
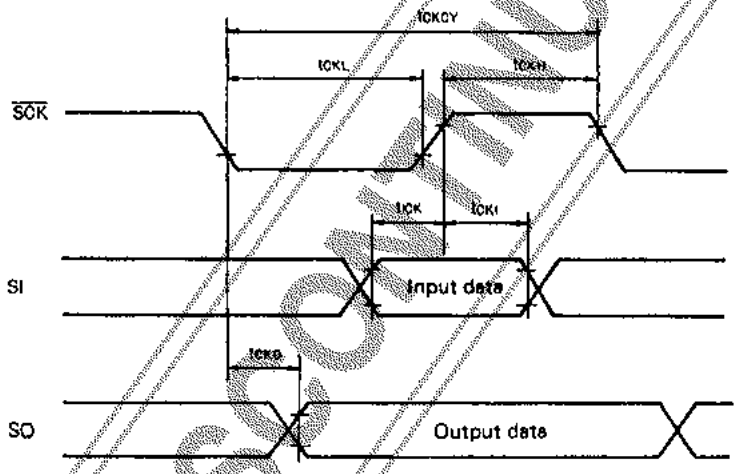


Fig. 6 Reset Circuit

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at C_{RES}=0.1μF. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or more.



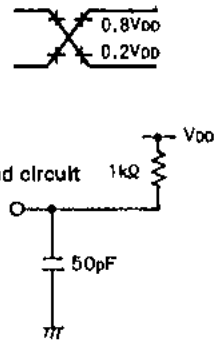
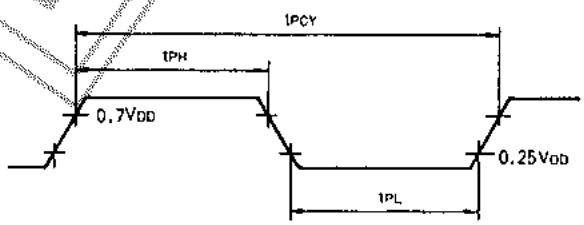


Fig. 7 Serial Input/Output Timing



The load conditions are the same as in Fig. 7.

Fig. 8 Pulse Output Timing at Port PE_0

RC Oscillation Characteristic of the LC6543C, 6546C

Fig. 9 shows the RC oscillation characteristic of the LC6543C, 6546C. For the variation range of RC OSC frequency of the LC6543C, 6546C, the following are guaranteed at the external constants only shown below.

i) V_{DD}=3.0V to 6.0V, Ta=−30°C to +70°C
External constants Cext=270pF
Rext=12kohms
275kHz ≦ f_{MOSC} ≦ 642kHz

ii) V_{DD}=4.0V to 6.0V, Ta=−30°C to +70°C
External constants Cext=270pF
Rext=4.7kohms
612kHz ≦ f_{MOSC} ≦ 1159kHz

If any other constants than specified above are used, the range of Rext=3kohms to 20kohms, Cext=150pF to 390pF must be observed. (See Fig. 9.)

(*7): The oscillation frequency at V_{DD}=5.0V, Ta=25°C must be in the range of 350kHz to 750kHz.

(*8): The oscillation frequency at V_{DD}=4.0V to 6.0V, Ta=−30°C to +70°C and V_{DD}=3.0V to 6.0V, Ta=−30°C to +70°C must be within the operation clock frequency range.

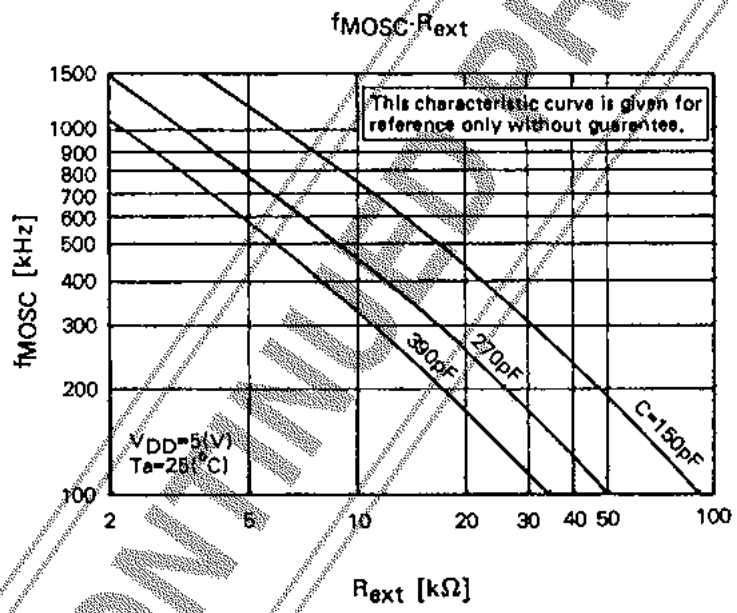


Fig. 9 RC Oscillation Frequency Data (Typ.)

LC6543H, 6546H

1. Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

					unit
Maximum Supply Voltage	V_{DD} max		V_{DD}	−0.3 to +7.0	V
Output Voltage	V_O		OSC2	Allowable up to voltage generated	V
Input Voltage	$V_{I(1)}$		OSC1 (*1)	−0.3 to V_{DD}+0.3	V
	$V_{I(2)}$		TEST, $\overline{RES}$	−0.3 to V_{DD}+0.3	V
Input/Output Voltage	$V_{IO(1)}$		Port of OD type	−0.3 to +15	V
	$V_{IO(2)}$		Port of PU type	−0.3 to V_{DD}+0.3	V
Peak Output Current	I_{OP}		I/O port	−2 to +20	mA
Averate Output Current	I_{OA}	Per pin over the period of 100msec.	I/O port	−2 to +20	mA
	$\Sigma I_{OA(1)}$	Total current of PC_0 to 3, PD_0 to 3, PE_0 to 3 (*2)		−15 to +100	mA
	$\Sigma I_{OA(2)}$	Total current of PF_0 to 3, PG_0 to 3, PA_0 to 3, PI_0 (*2)		−15 to +100	mA
Allowable Power Dissipation	Pd max (1)	Ta=−30 to +70°C (DIP)		400	mW
	Pd max (2)	Ta=−30 to +70°C (MFP)		200	mW
Operating Temperature	Topg			−30 to +70	°C
Storage Temperature	Tstg			−55 to +125	°C

2. Allowable Operating Conditions at Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=4.5 to 6.0V

				min	typ	max	unit
Operating Supply Voltage	V_{DD}		V_{DD}	4.5		6.0	V
Standby Supply Voltage	V_{St}	RAM, register hold(*3)	V_{DD}	1.8		6.0	V
"H"-Level Input Voltage	$V_{IH(1)}$	Output Nch Tr OFF	Port of OD type (except I_0)	0.7V_{DD}		+13.5	V
	$V_{IH(2)}$	Output Nch Tr OFF	Port of PU type (except I_0)	0.7V_{DD}		V_{DD}	V
	$V_{IH(3)}$	Output Nch Tr OFF	$\overline{INT}$, $\overline{SCK}$ SI, I_0 of OD type	0.8V_{DD}		+13.5	V
	$V_{IH(4)}$	Output Nch Tr OFF	$\overline{INT}$, $\overline{SCK}$, SI, I_0 of PU type	0.8V_{DD}		V_{DD}	V
	$V_{IH(5)}$		$\overline{RES}$	0.8V_{DD}		V_{DD}	V
	$V_{IH(6)}$	External clock mode	OSC1	0.8V_{DD}		V_{DD}	V
"L"-Level Input Voltage	$V_{IL(1)}$	Output Nch Tr OFF	Port	V_{SS}		0.3V_{DD}	V
	$V_{IL(2)}$	Output Nch Tr OFF	$\overline{INT}$, $\overline{SCK}$, SI	V_{SS}		0.25V_{DD}	V
	$V_{IL(3)}$	External clock mode	OSC1	V_{SS}		0.25V_{DD}	V
	$V_{IL(4)}$		TEST	V_{SS}		0.3V_{DD}	V
	$V_{IL(5)}$		$\overline{RES}$	V_{SS}		0.25V_{DD}	V
Operating Frequency (Cycle Time)	fop (t_{CYC})			200 (20)		4330 (0.92)	kHz (μs)
External Clock Conditions							
Frequency	f_{ext}		OSC1	200		4330	kHz
Pulse Width	t_{extH}, t_{extL}	Fig. 1	OSC1	69			ns
Rise/Fall Time	t_{extR}, t_{extF}		OSC1			50	ns
Oscillation Guaranteed Constants							
Ceramic Resonator Oscillation		Fig. 2			See Table 1.		

(*1) When oscillated internally under the oscillating conditions in Fig. 2, up to the oscillation amplitude generated is allowable.

(*2) Average over the period of 100msec.

(*3) Operating supply voltage V_{DD} must be held until the standby mode is entered after the execution of the HALT instruction.
The PA_3 (or $PA_{0\ to\ 3}$) pin must be free from chattering during the HALT instruction execution cycle.

(*4) When mounting the MFP version on the board, do not dip it in solder.

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3. Electrical Characteristics at Ta=−30 to +70°C, V_{SS}=0V, V_{DD}=4.5 to 6.0V

				min	typ	max	unit
"H"-Level Input Currnt	$I_{IH(1)}$	Output Nch Tr OFF (including OFF leak current of Nch Tr) V_{IN}=+13.5V	Port of OD type			+5.0	μA
	$I_{IH(2)}$	External clock mode, $V_{IN}=V_{DD}$	OSC1			+1.0	μA
"L"-Level Input Current	$I_{IL(1)}$	Output Nch Tr OFF $V_{IN}=V_{SS}$	Port of OD type	−1.0			μA
	$I_{IL(2)}$	Output Nch Tr OFF $V_{IN}=V_{SS}$	Port of PU type	−1.3	−0.35		mA
	$I_{IL(3)}$	$V_{IN}=V_{SS}$	$\overline{RES}$	−45	−10		μA
	$I_{IL(4)}$	External clock mode, $V_{IN}=V_{SS}$	OSC1	−1.0			μA
"H"-Level Output Voltage	$V_{OH(1)}$	I_{OH}=−50uA	Port of PU type	V_{DD}−1.2			V
	$V_{OH(2)}$	I_{OH}=−10uA	Port of PU type	V_{DD}−0.5			V
"L"-Level Output Voltage	$V_{OL(1)}$	I_{OL}=10mA	Port			1.5	V
	$V_{OL(2)}$	I_{OL}=1mA, I_{OL} of each port: 1mA or less	Port			0.5	V
Hysteresis Voltage	V_{HYS}		$\overline{RES}$, $\overline{INT}$, $\overline{SCK}$, SI, OSC1 of Schmitt type (*5)	0.1V_{DD}			V
Current Dissipation							
Ceramic Resonator Oscillation	$I_{DDOP(1)}$	Fig. 2, 4MHz	Operating mode, V_{DD} Output Nch Tr OFF, Port=V_{DD} V_{DD}		4.0	10	mA
External Clock	$I_{DDOP(2)}$	200kHz to 4330kHz			4.0	10	mA
Standby Mode	I_{DDSt}	Output Nch Tr OFF, Port=V_{DD}	V_{DD}=6V V_{DD}		0.05	10	μA
			V_{DD}=3V V_{DD}		0.025	5	μA
Oscillation Characteristics							
Ceramic Resonator Oscillation							
Oscillation Frequency	f_{CFOSC}	Fig. 2, fo=4MHz (*6)	OSC1, OSC2	3840	4000	4160	kHz
Oscillation Stabilizing Period	t_{CFS}	Fig. 3, fo=4MHz				10	ms
Pull-up/Pull-down Reistance							
I/O Port Pull-up Reistance	R_{PP}		V_{DD}=5V, Port of PU type		14		kohm
External Reset Characteristics							
Reset Time	t_{RST}				See Fig. 4.		
Pin Capacitance	C_P	f=1MHz, other than pins to be tested, $V_{IN}=V_{SS}$			10		pF
Serial Clock							
Input Clock Cycle Time	$t_{CKCY(1)}$	Fig. 5	$\overline{SCK}$	3.0			μs
Output Clock Cycle Time	$t_{CKCY(2)}$	Fig. 5	$\overline{SCK}$		64 x T_{CYC} (T_{CYC}=4 x System clock period)		μs
Input Clock "L"-Level Pulse Width	$t_{CKL(1)}$	Fig. 5	$\overline{SCK}$	1.0			μs
Output Clock "L"-Level Pulse Width	$t_{CKL(2)}$	Fig. 5	$\overline{SCK}$		32 x T_{CYC}		μs
Input Clock "H"-Level Pulse Width	$t_{CKH(1)}$	Fig. 5	$\overline{SCK}$	1.0			μs
Output Clock "H"-Level Pulse Width	$t_{CKH(2)}$	Fig. 5	$\overline{SCK}$		32 x T_{CYC}		μs

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LC6543H, 6546H

				min	typ	max	unit
Serial Input							
Data Setup Time	t_{ICK}	Specified for ↑ of $\overline{SCK}$	SI	0.5			μs
Data Hold Time	t_{CKI}	Fig. 5	SI	0.5			μs
Serial Output							
Output Delay Time	t_{CKO}	Specified for ↓ of $\overline{SCK}$ Nch OD only, External 1kohm, external 50pF, Fig. 5	SO			0.5	μs
Pulse Output							
Period	t_{PCY}	Fig. 6	PE_0		64 x T_{CYC}		μs
"H"-Level Pulse Width	t_{PH}	T_{CYC}=4 x System clock period, Nch OD only, External 1kohm, External 50pF	PE_0		32 x T_{CYC}	±10%	μs
"L"-Level Pulse Width	t_{PL}		PE_0		32 x T_{CYC}	±10%	μs

(*5) The OSC1 pin can be schmitt-triggered when the external clock oscillation option has been selected.

(*6) f_{CFOSC}: Oscillatable frequency

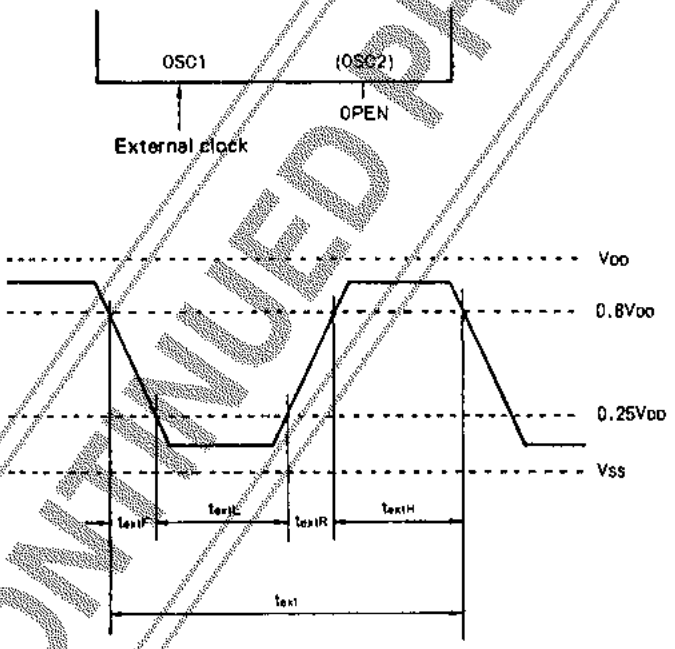


Fig. 1 External Clock Input Waveform

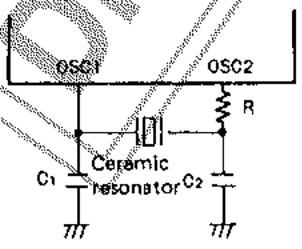


Fig. 2 Ceramic Resonator Oscillation Circuit

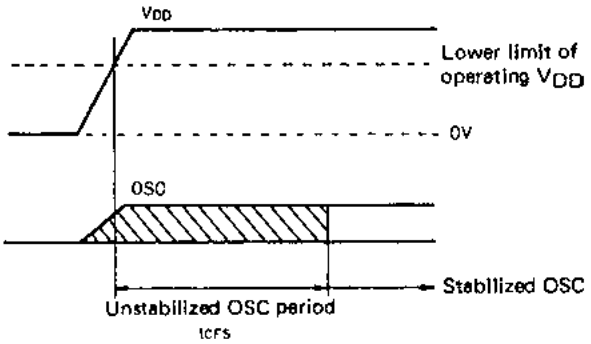


Fig. 3 Oscillation Stabilizing Period

4 MHz CSA4.00MG (Murata)	C_1	33PF ±10%
	C_2	33PF ±10%
	R	0Ω
4 MHz KBR4.0MS (Kyocera)	C_1	33PF ±10%
	C_2	33PF ±10%
	R	0Ω

Table 1 Constants Guaranteed for Ceramic Resonator OSC

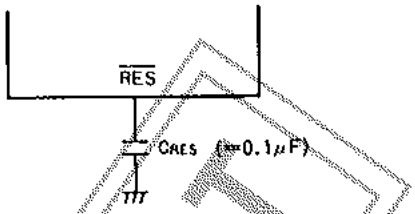


Fig. 4 Reset Circuit

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at C_{RES}=0.1μF. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or more.

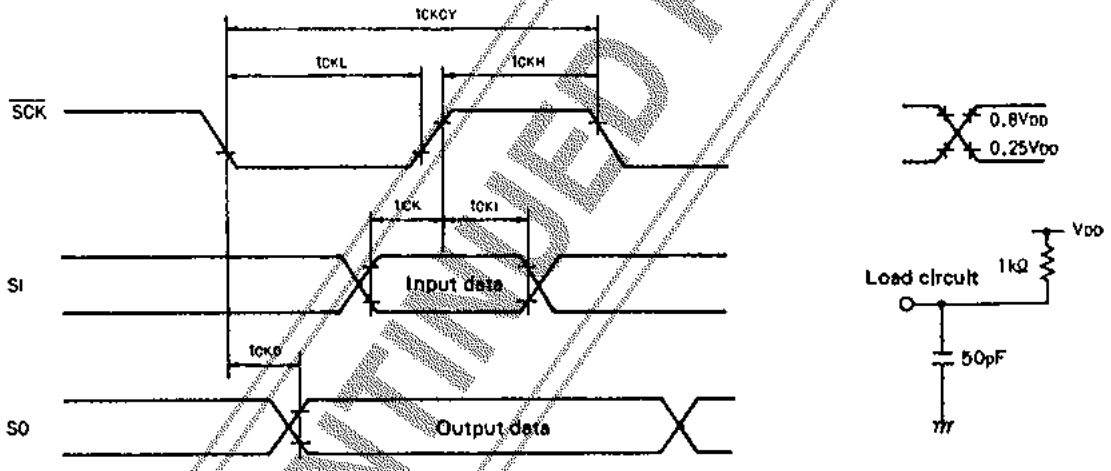
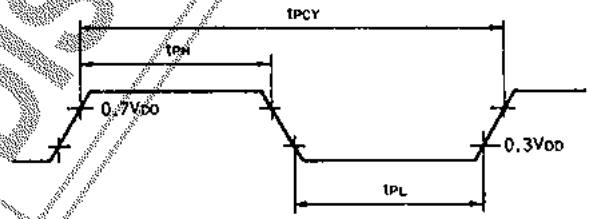


Fig. 5 Serial Input/Output Timing



The load conditions are the same as in Fig. 5.

Fig. 6 Pulse Output Timing at Port PE_0

Notes for Standby Function Application

The LC6543/46 provide the standby function called HALT mode to minimize the current dissipation when the program is in the wait state.

The standby function is controlled by the HALT instruction, PA pin, $\overline{RES}$ pin, and serial transfer completion signal. A peripheral circuit and program must be so designed as to provide precise control of the standby function. In most applications where the standby function is performed, voltage regulation, instantaneous break of power, and external noise are not negligible. When disigning an application circuit and program, whether or not to take some measures must be considered according to the extent to which these factors are allowed. This section mainly describes power failure backup for which the standby function is mostly used. A sample application circuit where the standby function is performed precisely is shown below and notes for circuit design and program design are also given below.

When using the standby function, the application circuit shown below must be used and the notes must be also fully observed.

If any other method than shown in this section is applied, it is necessary to fully check the environmental conditions such as power failure and the actual operation of application equipment.

1. HALT mode release conditions

1-1. Supplementary description of release by serial transfer completion signal.

On completion of serial transfer, the HALT mode is released and the execution of the program starts with an instruction immediately following the HALT instruction. This function can be used to execute the program only when serial transfer occurs, placing the program in the wait state when no serial transfer occurs. This function is effective in reducing the current dissipation or clock noise.

— Notes —

- Release by the serial transfer completion signal is available only when the RC mode is used for system clock generation; and unavailable when the ceramic resonator mode is used.
- On completion of serial transfer, the HALT mode is released unconditionally. In an application, such as capacitor backup application, where the current dissipation must be kept as low as possible during backup and serial transfer by external clock is also used, the HALT mode is released when serial data is transferred externally during backup.

1-2. Summary of HALT release conditions

The HALT mode setting, release conditions are shown in Table 1.

Table 1 HALT mode setting, release conditions

HALT mode setting conditions	HALT mode release conditions
HALT instruction Provided that PA_3 (PA_3 to PA_0 or PA_3 is program-selectable) is at high level.	1 Reset (Low level is applied to $\overline{RES}$.) 2 Low level is applied to PA_3 (PA_3 to PA_0 or PA_3 is program-selectable.) 3 Serial transfer completion.

Note) HALT mode release conditions 2, 3 are available only when the RC mode is used for system clock generation; and unavailable when the ceramic resonator mode is used.

2. Proper cares in using standby function

When using the standby function, an application circuit and program must be designed with the following in mind.

(1) The supply voltage at the standby state must not be less than specified.
(2) Input timing and conditions of each control signal ($\overline{RES}$, port A, serial transfer) must be observed at the standby initiate/release state.
(3) Release operation must not be overlapped at the time of execution of the HALT instruction.

A sample application where the standby function is used for power failure backup is shown below as a concrete method to observe these notes. A sample application circuit, its operation, and notes for program design are given below.

Sample application where the standby function is used for power failure backup

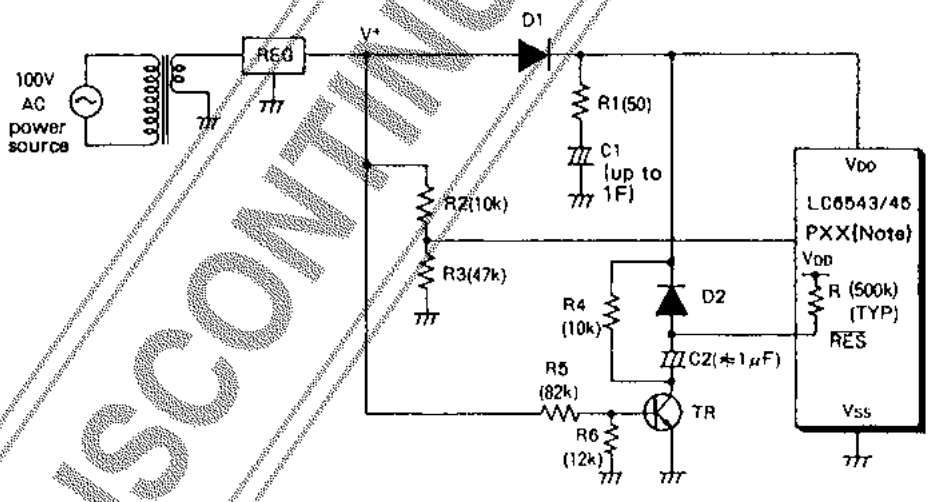
Power failure backup is an application where power failure of the main power source is detected and the HALT instruction is executed to cause the standby state to be entered. The current dissipation is minimized and a backup capacitor is used to retain the contents of the internal registers for a certain period of time. After power is restored, a reset occurs automatically and the execution of the program starts at address 000H of the program counter (PC). Shown below are sample applications where the program selects or not between power-ON reset and reset after power is restored, notes, measures for instantaneous break of AC power, and notes for serial transfer.

2-1. Sampel application 1 where the standby function is used for power failure backup.

Shown below is a sample application where the program does not select between power-ON reset and reset after power is restored.

2-1-1. Sample application circuit — (1)

Fig. 2-1 shows a sample application where the standby function is used for power failure backup.



(Note) Normal input ports other than PA_3

Fig. 2-1. Sample application — (1) where the standby function is used for power failure backup

2-1-2. Operating waveform in sample application circuit – (1)

The operating waveform in the sample application circuit in Fig. 2-1 is shown in Fig. 2-2. The mode is roughly divided as follows:

(a) Power-ON reset
(b) Instantaneous break of main power source
(c) Return from power failure backup

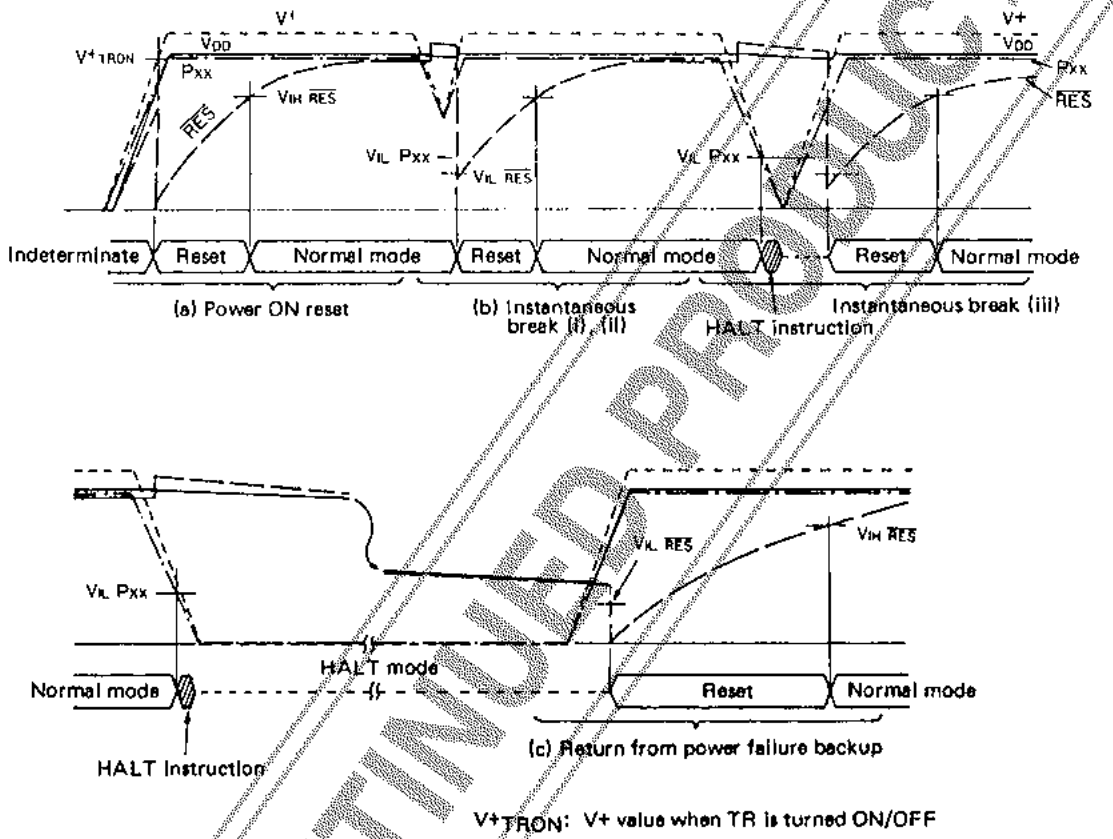


Fig. 2-2 Operating waveform in sample application circuit – (1)

2-1-3. Operation of sample application circuit – (1)

(a) At the time of power-ON reset

After power rises, a reset occurs automatically and the execution of the program starts at address 000H of the program counter (PC).

– Note –

This sample application circuit provides an indeterminate region where no reset occurs before the operating V_{DD} range is entered.

(b) At the time of instantaneous break

(i) When the P_{XX} input voltage does not meet V_{IL} (the P_{XX} input level does not get lower than input threshold level V_{IL}) and the $\overline{RES}$ input voltage only meets V_{IL}:
A reset occurs in the normal mode, providing the same operation as power-ON reset.

(ii) When both of the P_{XX} input voltage and $\overline{RES}$ input voltage do not meet V_{IL}:
The program continues running in the normal mode.

(iii) When both of the P_{XX} input voltage and $\overline{RES}$ input voltage meet V_{IL}:
When two pollings do not regard the P_{XX} input voltage as "L" level, the HALT mode is not entered and a reset occurs.
When two pollings regard the P_{XX} input voltage as "L" level, the HALT mode is entered and after power is restored a reset occurs, releasing the standby mode.

(c) At the time of return from power failure backup
After power is restored, a reset occurs, releasing the standby mode.

2-1-4. Notes for design of sample application circuit — (1)

- V+ rise time and C2
  Make the time constant (C2, R) of the reset circuit 10 times as long as the V^+ rise time. (R: ON-chip resistor, 500kohms typ.)
  Make the V^+ rise time shorter (up to 20ms).
- R1 and C1
  Make the R1 value as small as possible. Make the C1 value as large as possible according to the backup time calculated. (Fix the R1 value so that the C1 charging current does not exceed the power source capacity.)
- R2 and R3
  Make the "H"-level input voltage applied to the P_{XX} pin equal to V_{DD}.
- R4
  Fix the time constant of C2 and R4 so that C2 can discharge during the period of time from when V^+ gets lower than V^+_{TRON} (TR OFF) at the time of instantneous break until the P_{XX} input voltage gets lower than V_{IL} (because release by reset is not available after the HALT mode is entered by instantaneous break).
- R5 and R6
  Make V^+ (V_{BE}*0.6V is obtained by R5 and R6) when the reset circuit works (Tr ON) more than (operating V_{DD} min + V_F of diode D1). Observing this note, make V^+ as low as possible to provide a reset early enough after power-ON.
- Backup time
  The normal operation continues with a relatively high current dissipation from when power failure is detected by the P_{XX} until the HALT instruction is executed. Fix the C1 value so that the standby supply voltage is held during backup time of set + above-mentioned time.

2-1-5. Notes for software design

- Design the program so that port A_0 to A_2 cannot be used for standby release and port A_3 is brought to "H" level at the standby mode.
- Check a standby request by polling the input port twice.

(Example)

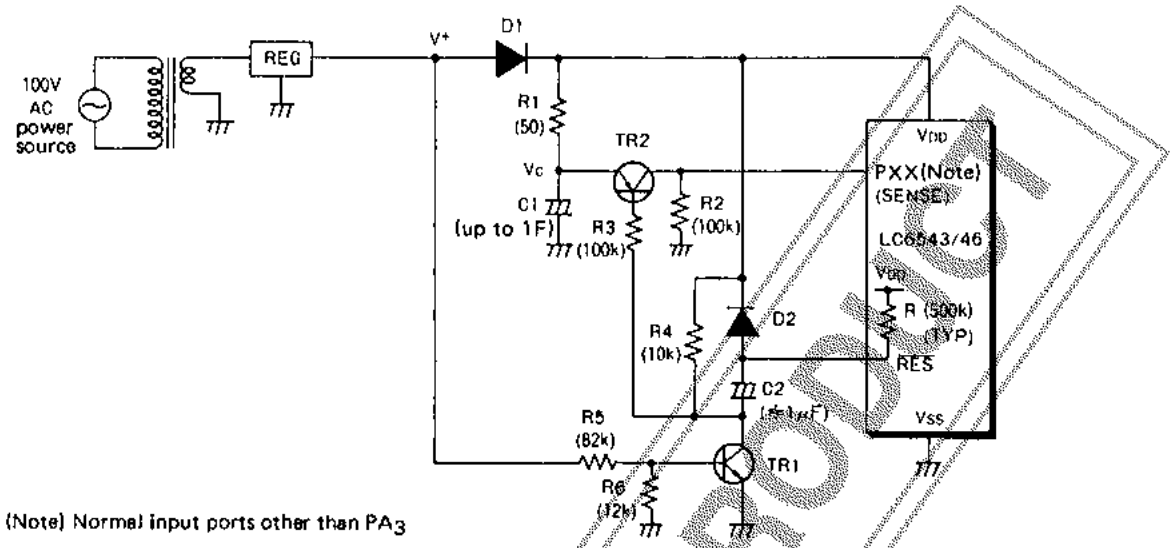
```
        :
        BP1     AAA     ;1st polling
        RCTL    3       ;Interrupt Inhibit
        BP1     AAA     ;2nd polling
        HALT            ;Standby
AAA:    :
```

2-2. Sample application 2 where the standby function is used for power failure backup

Shown below is a sample application where the program selects between power-ON reset and reset after power is restored.

2-2-1. Sample application circuit – (2) (No instantaneous break in power source)

Fig. 2-3 shows a sample application where the standby function is used for power failure backup.



(Note) Normal input ports other than PA_3

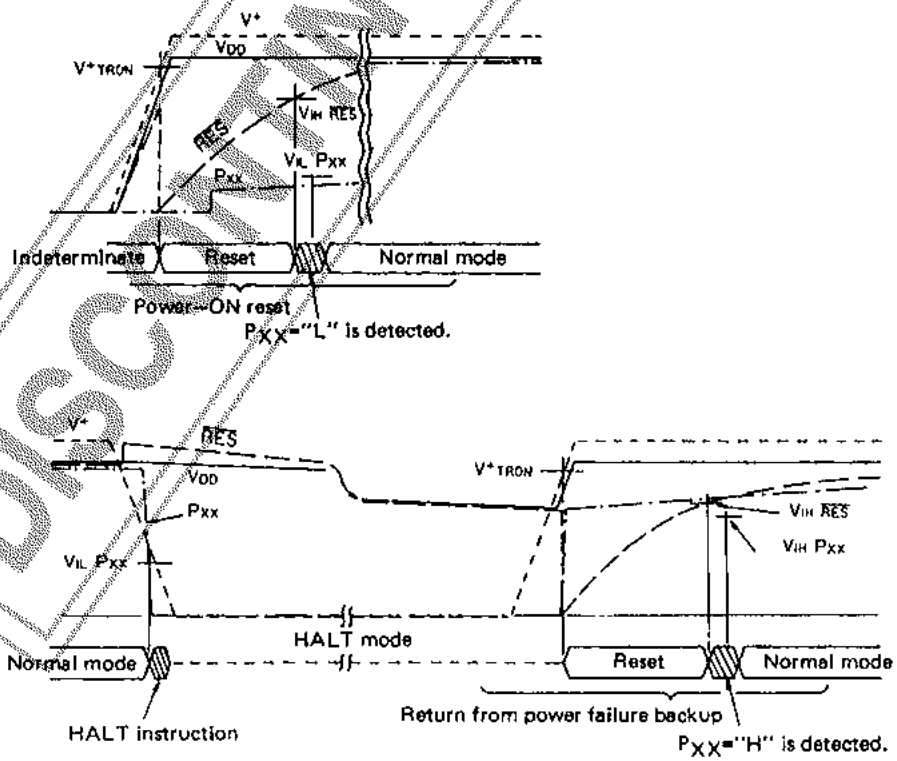
Fig. 2-3. Sample application – (2) where the standby function is used for power failure backup

2-2-2. Operating waveform in sample application circuit – (2)

The operating waveform in the sample application circuit in Fig. 2-3 is shown in Fig. 2-4. The mode is roughly divided as follows:

(1) Power-ON reset

(2) Return from power failure backup



V+TRON: V+ value when TR1 is turned ON/OFF.

Fig. 2-4. Operating waveform in sample application circuit – (2)

2-2-3. Operation of sample application circuit – (2)

(a) At the time of power-ON reset
The operation and notes are the same as for sample application circuit – (1), except that after reset release P_{XX}="L" is program-detected to decide program start after initial reset.

(b) Standby initiation
When one polling regards the P_{XX} input voltage as "L" level, the HALT mode is entered.

(c) At the time of return from power failure backup
After power is restored, a reset occurs, releasing the standby mode. After standby release P_{XX}="H" is program-detected, deciding program start after power is restored.

– Note –
If power is restored after V_{DD} during power failure backup gets lower than V_{IH} on the P_{XX}, P_{XX}="L" may be program-detected, deciding program start after initial reset.

2-2-4. Notes for design of sample application circuit – (2)

- R2 and R3
  Fix the R2 value so that R2≫R1 is yielded and fix the R3 value so that I_B of TR2 is limited.
- R4
  There is no severe restriction on the R4 value, but fix it so that C2 can discharge quickly.
  Other notes are the same as for sample application circuit – (1).

2-2-5. Notes for software design

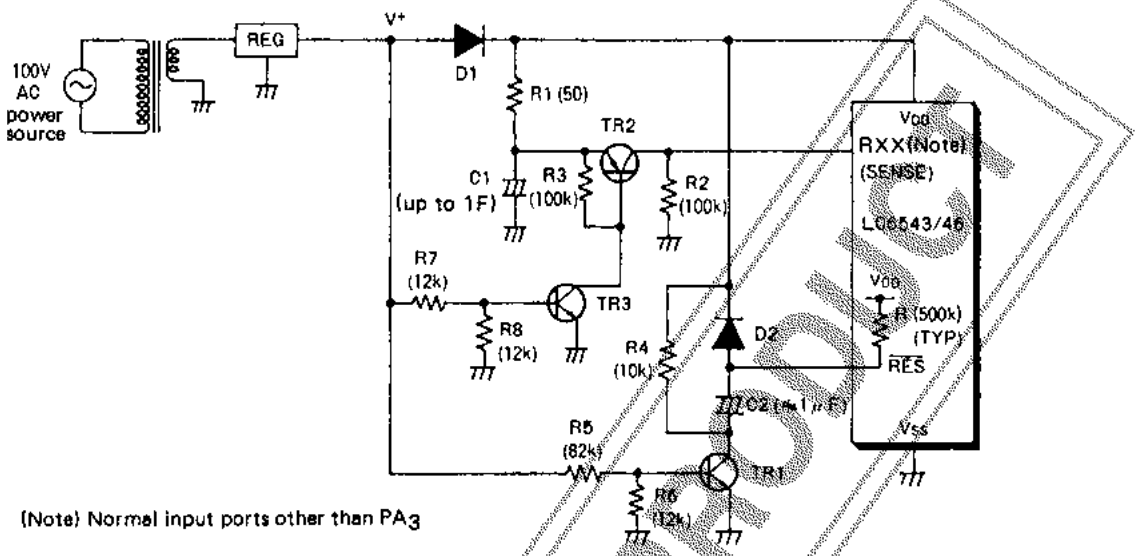
- Design the program so that port A_0 to A_2 cannot be used for standby release and port A_3 is brought to "H" level.
- Check a standby request by polling the input port once.

(Example)

```
        :
        BP1     AAA     ;Polling
        HALT            ;Standby
AAA:    :
```

2-3. Sample application 3 where the standby function is used for power failure backup.

2-3-1. Sample application circuit – (3) (There is an instantaneous break in power source.)
Fig. 2-5 shows a sample application where the standby function is used for power failure backup.

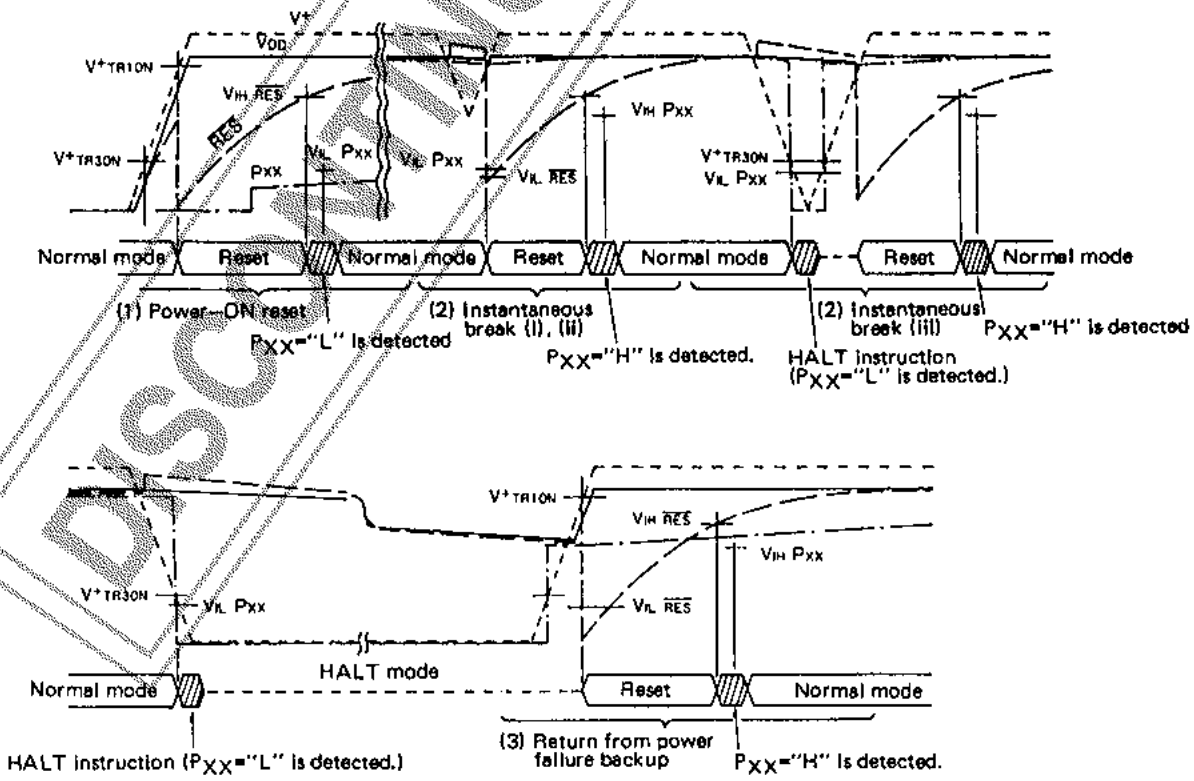


(Note) Normal input ports other than PA_3

Fig. 2-5. Sample application – (3) where the standby function is used for power failure backup

2-3-2. Operating waveform in sample application circuit – (3)
The operating waveform in the sample application circuit in Fig. 2-5 is shown in Fig. 2-6. The mode is roughly divided as follows:

(1) Power-ON reset
(2) Instantaneous break of main power source
(3) Return from power failure backup



V^+_{TR1ON}: V+ value when TR1 is turned ON/OFF
V^+_{TR3ON}: V+ value when TR3 is turned ON/OFF

Fig. 2-6. Operating waveform in sample application circuit – (3)

2-3-3. Operation of sample application circuit – (3)

(a) At the time of power-ON reset
The operation and notes are the same as for sample application circuit – (2)

(b) At the time of instantaneous break

(i) When the P_{XX} input voltage does not meet V_{IL} (the P_{XX} input level does not get lower than input threshold level V_{IL}) and the $\overline{RES}$ input voltage only meets V_{IL}:
A reset occurs in the normal mode. After reset release P_{XX}="H" is program-detected, deciding program start after instantaneous break.

(ii) When both of the P_{XX} input voltage and $\overline{RES}$ input voltage do not meet V_{IL}:
The program continues running in the normal mode.

(iii) When both of the P_{XX} input voltage and $\overline{RES}$ input voltage meet V_{IL}:
When two pollings do not regard the P_{XX} input voltage as "L" level, the HALT mode is not entered and a reset occurs.
When two pollings regard the P_{XX} input voltage as "L" level, the HALT mode is entered and after power is restored a reset occurs, releasing the standby mode. After standby release P_{XX}="H" is program-detected, deciding program start after instantaneous break.

(c) At the time of return from power failure backup
The operation and notes are the same as for sample application circuit – (2)

2-3-4. Notes for design of sample application circuit – (3)

- R3
  Bias resistance of TR2
- R7 and R8
  Fix the R7 and R8 values so that TR3 is turned ON/OFF at approximately 1.5V of V+.

Other notes are the same as for sample application circuit – (1)

2-3-5. Notes for software design
Same as for sample application circuit – (1)

2-4. Notes (1) for providing serial transfer
Notes for providing power failure backup and serial transfer
This application assigns top priority to power failure backup. When power failure backup is provided, serial transfer may not be provided normally.

(1) When the internal clock is used for the serial clock:
Execute the serial transfer start instruction immediately before executing the HALT instruction. If this is done during serial transfer, the power failure backup mode is entered without normal transfer.

(2) When the external clock is used for the serial clock:
When power failure is detected, it is most prioritized that the HALT mode is entered, providing power failure backup. It is necessary to design an application system where no release signal by serial transfer completion is input to the HALT instruction execution cycle and no release signal is input during backup.

2-5. Notes (2) for providing serial transfer
Notes for providing HALT and serial transfer for program standby without power failure backup
This application assigns top priority to serial transfer. The following notes for system design must be observed.

(1) When the internal clock is used for the serial clock:
Transfer starts when it is ready on both sides. When transfer is not ready on the other side, the HALT instruction is executed to reduce the current dissipation. When transfer is ready, the HALT release signal ($\overline{RES}$, PA) causes return from the standby mode, starting serial transfer.

(2) When the external clock is used for the serial clock:
Synchronization must be provided between microcomputers to prevent the HALT instruction and HALT release signal (RSIOEND) from overlapping. When transfer is ready, the serial transfer start instruction is executed and the program is placed in the wait state. The other side adjusts time so that no overlap occurs between the HALT instruction and transfer completion and starts serial transfer. On completion of transfer, the HALT mode is released and the program is executed with an instruction immediately following the HALT instruction.

Notes for Program Evaluation

- When evaluating the LC6543/46 with the evaluation chip (LC6594, LC65PG43-A/46-A, LC65PG43/46), the following must be observed.

Classification	Item	Function		Notes for evaluation
		Mass-production chip	Evaluation chip	
Notes for option	2-pin OSC	PI_0 and OSC2 share one pin (PI_0/OSC2). Either of them is selected exclusively by user option. When 2-pin OSC is selected, PI_0/OSC2 pin provides OSC2 and performs no function of PI_0 port. Data input to PI_0/OSC2 by mistake is always read as "0".	Evaluation chip has PI_0 and OSC2 separately. Pin required for option is selected as required. Even when OSC2 pin is selected by option, PI_0 circuit is present and functions as complete port PI_0.	Since input/output at PI_0 on evaluation chip results in difference between evaluation chip operation and mass-production chip operation, input/output at PI_0 is prohibited.
	1-pin OSC	When 1-pin C OSC is selected, OSC circuit is formed by connecting catalog guranteed C to OSC1 pin.	Since no OSC circuit for 1-pin C OSC is contained, 1-pin C OSC is not available.	2-pin RC provides OSC and frequency is adjusted as desired. OSC characteristic differs, but there is no restriction on program (ES, CS must be used to evaluate OSC characteristic in detail).
	OSC divider	3 selections (1/1, 1/3, 1/4) by option	3 selections (1/1, 1/3, 1/4) available by 2 pins of DIV pin, 3OR4 pin.	DIV pin, 3OR4 pin must be set according to option specified for mass-production chip.
	Ports C, D output level at reset mode	Ports C, D can be brought to "H" or "L" in a group of 4 bits.	Port C and port D can be brought to "H" and "L" by CHL pin and DHL pin respectively.	CHL pin and DHL pin must be set according to option specified for mass-production chip.
	Port output configuration PU/OD	PU or OD can be selected bitwise.	Only OD without PU.	[LC6594-applied evaluation] External resistor (10kohms) on evaluation board must be connected to necessary port. [Piggyback-applied evaluation] Resistor must be connected to necessary port on application boerd.
	PU resistor configuration	PU resistor brought to Hi-Z (Pch Tr to turn OFF) at "L" output mode.	PU resistor, being external resistor, whose impedance remains unchanged at "L" output mode.	For mass-production chip, leakage current only flows in Pch Tr at "L" output mode; for evaluation chip, current continues flowing in PU resistor at "L" output mode.

Classification	Item	Function		Notes for evaluation
		Mass-production chip	Evaluation chip	
Notes for OSC	OSC constants —1	[2-pin RC OSC] Catalog-guaranteed constants provide OSC at frequency specified in catalog.	[2-pin RC OSC] Different from mass-production chip in circuit design and characteristic.	[2-pin RC OSC] Frequency must be adjusted to OSC frequency of mass-production chip by adjusting variable resistor.
		[2-pin ceramic resonator OSC] Catalog-guaranteed constants provide OSC at frequency specified in catalog.	[2-pin ceramic resonator OSC] Different from mass-production chip in circuit design and characteristic. Wiring capacitance may provide unstable OSC.	[2-pin ceramic resonator OSC] External constants must be fine-adjusted according to service conditions.
	OSC constants —2	[2-pin ceramic resonator OSC] Feedback resistor is contained.	[2-pin ceramic resonator OSC] No feedback resistor is contained.	[2-pin ceramic resonator OSC] For evaluation chip, feedback resistor of 1Mohm must be connected externally.
Notes for electrical characteristics	OSC frequency	OSC frequency characteristic as indicated in catalog.	Different from mass-production chip in circuit design, and characteristic.	ES, CS must be used to evaluate characteristic in detail. The standby current cannot be evaluated in detail. However, the standby current can be confirmed roughly in the manner discussed later. Be sure to confirm the standby current.
	Operating current, standby current	Current characteristic as indicated in catalog.	Different from mass-production chip in circuit design, and characteristic.	
Notes for operating conditions	Operating voltage	Supply voltage range as indicated in catalog.	Evaluation chip must be also used at V_{DD}=5V±5% at which EPROM, other LSI are used.	
	Operating temperature	Temperature range as indicated in catalog.	Evaluation chip must be used at 10°C to 40°C.	
	Port A input voltage	Input/output configuration of normal threshold input. Input voltage as indicated in catalog.	Input/output configuration of low threshold input. Different from mass-production chip in input/output configuration.	
	Type No. setting	LC6543/46 differ in ROM, RAM capacity.	RAM capacity is set by RAMC pin according to Type No.	SW3-2 on evaluation board is always placed in PA position. SW3-1 is set according to Type No.

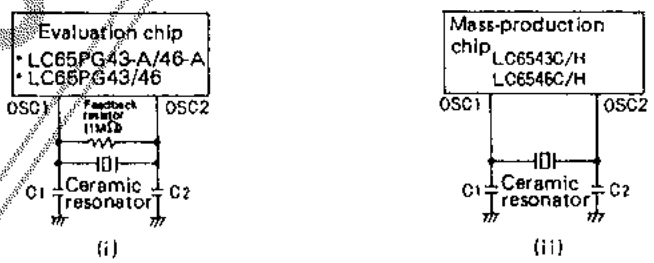
(Confirmation methods for the standby function)
The standby current at the standby mode of the simulation chip can be evaluated not exactly but approximately. Then, do the following steps.

(a) Confirmation of the standby state
Be sure to confirm whether or not the LSI enters the standby mode when the standby conditions are satisfied.
(i) When the OSC1 and OSC2 oscillation option is selected, confirm on an oscilloscope that the oscillation stops in the standby mode.
When the OSC1 terminal C oscillation is used on the LC6543/46 microcomputer, the OSC1 and OSC2 RC (Capacitor-Resistor) oscillation is used for evaluating functions because the simulation chip has no OSC1 terminal C oscillation option. At this time, also confirm on an oscilloscope that the oscillation stops in the standby mode.
(ii) Confirmation by the current dissipation
Remove the EPROM when confirming whether or not the LSI enters the standby mode. The I_{DD} of the LSI can determine whether or not the LSI is now in the standby mode.
When the LSI is in the operating mode, more than some 100μA current is transmitted. When in the standby mode, the current of the I_{DD} is 150μA or less if the DIV, 30R4, CHL, DHL and RAMC are all set to "H" (excluding the load current). If the DIV, 30R4, ———, etc. are all set to "L", the current of the I_{DD} is approximately 20μA.

(b) Confirmation by the load current
Your program must be designed so that the current is not transmitted to the input/output ports prior to the execution of the HALT instruction. This can reduce the useless dissipation of the load current at the standby mode and be confirmed on an oscilloscope.
(i) Design your program so that the current is not transmitted to the output ports prior to the execution of the HALT instruction.
(ii) Design your program and peripherals so that the input ports and input/output ports are not brought to the floating state at the standby mode.
If brought to the floating state, current flows in the microcomputer input circuit section, causing more current dissipation. Therefore, the backup enable time is shortened extremely in applications where the capacitor backup is used.

Ceramic resonator oscillation constants when the EVA-TB6543/46 is used
When developing your program using te target board EVA-TB6543/46, use the constants shown below because the ceramic resonator oscillation constants depend on the conditions for evaluation and the cable length, etc.

Note) When the evaluation chip is used in the 2-pin ceramic resonator oscillation mode, no feedback resistor is contained unlike the mass-production chip.
Connect a feedback resistor of 1Mohm externally as shown below.
Since constants R, C are also differ from those for the mass-production chip, refer to Table shown below and adjust the capacitor value according to the stray capacitance of the circuit.



2-pin Ceramic Resonator Oscillation Circuit for Evaluation Chip and Mass-production Chip

Table of Ceramic Resonator Oscillation Constants when the EVA-TB6543/46 is used

Ceramic resonator			Mas-production chip C1 = C2	Evaluation chip (*)			
				Including capacitance of standard cable		Including no capacitance of standard cable	
				C1 = C2	R	C1 = C2	R
4MHz	CSA4.00MG	(Murata)	33pF	8pF	0 ohm	33pF	0 ohm
	KBR4.0M	(Kyocera)	33pF	10pF	0 ohm	33pF	0 ohm
1MHz	CSB1000K	(Murata)	(CSB1000D used) 220pF	82pF	0 ohm	220pF	0 ohm
	KBR1000H	(Kyocera)	100pF	82pF	0 ohm	220pF	0 ohm
800kHz	CSB800K	(Murata)	(CSB800D used) 220pF	220pF	0 ohm	220pF	0 ohm
	KBR800H	(Kyocera)	220pF	150pF	0 ohm	150pF	0 ohm
400kHz	CSB400P	(Murata)	330pF	470pF	0 ohm	470pF	0 ohm
	KBR400B KBR400H	(Kyocera)	330pF	390pF	0 ohm	330pF	0 ohm

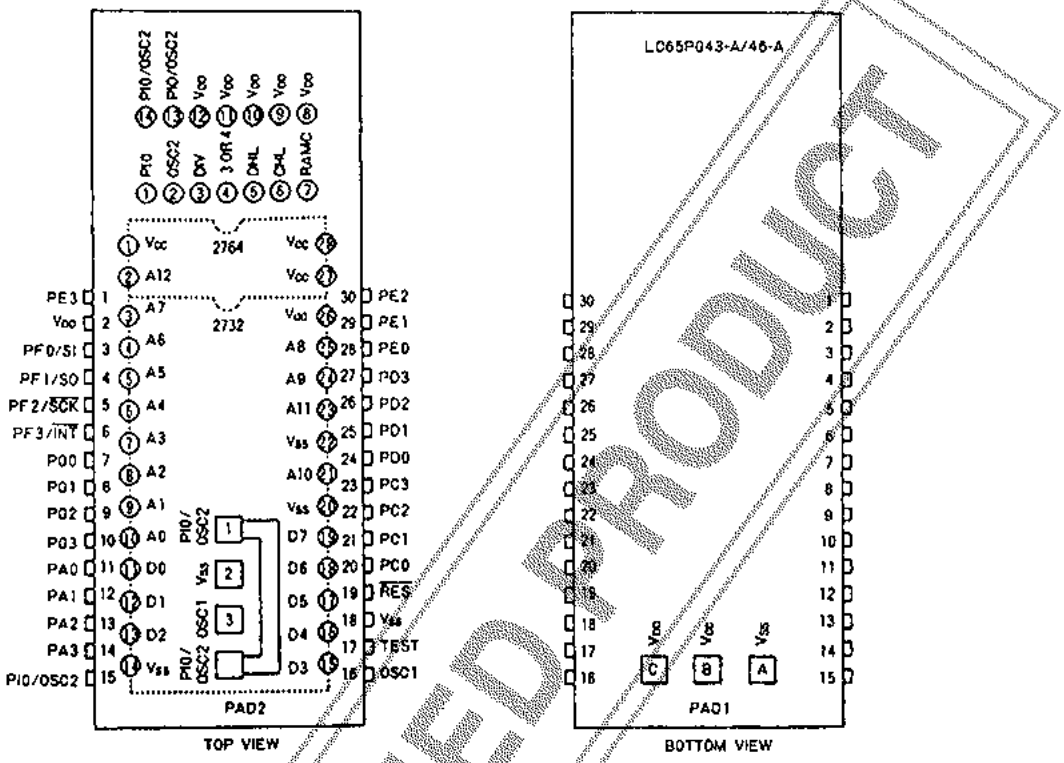
(*) The standard cable is a cable attached to target board EVA-TB6543/46.
The Table shows two cases where the capacitance of the cable is included and no capacitance of the cable is included.

- Example where the capacitance of the cable is included
  The capacitance of the cable is included when the resonator is connected to the user's application board through the cable from the EVA-TB6543/46.
- Example where no capacitance of the cable is included
  No capacitance of the cable is included when the resonator is placed near the evaluation chip (on the EVA-TB6543/46).

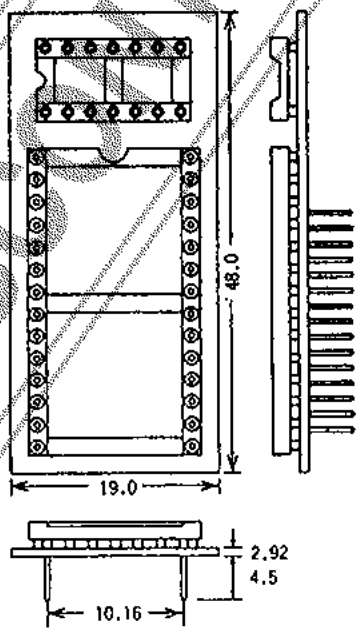
When using any other cable than the attached cable, adjust the capacitor value according to the stray capacitance.

How to use the piggyback chip (LC65PG43/46-A)

(1) Layout of pins and control pads, and External dimensions

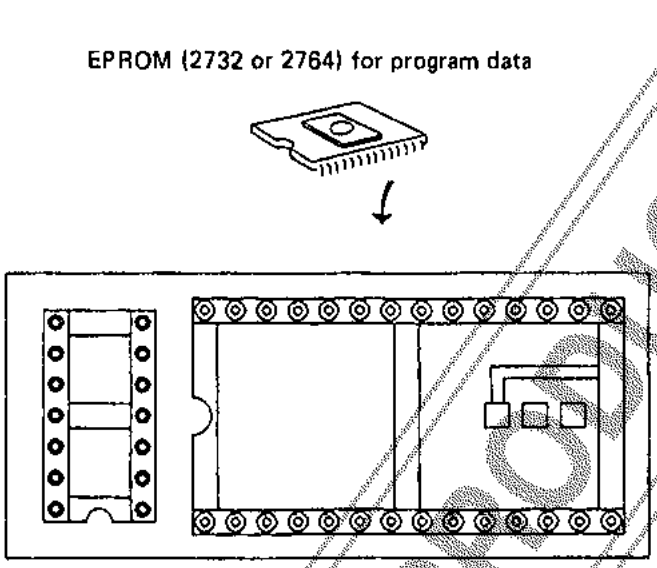


PAD1: Power supply pad
PAD2: Mounting pad for oscillation circuit components



(2) How to mount EPROM

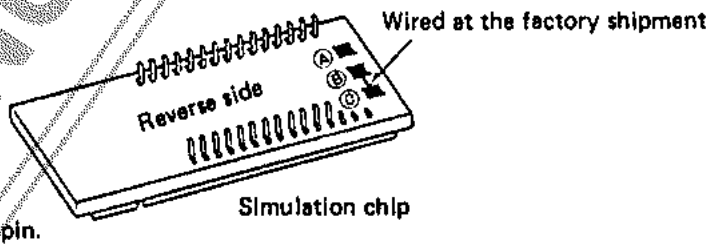
The EPROM to be mounted should contain an already-assembled program data. To write data to the EPROM, use the EPROM writer function on the EVA-800 or EVA-410C board. The mountable EPROM is an Intel 2732, 2764 or their equivalents.



(3) Power supply for EPROM

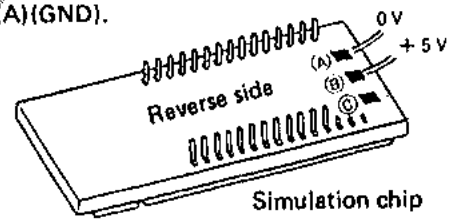
A typical EPROM dissipates the current of 50mA to 100mA. If the power capacity of an application product board is not sufficient, use an independent power supply circuit to provide the EPROM with the current externally.

a) At the factory shipment, the EPROM uses the same power supply circuit as the simulation chip does. To supply external current to the EPROM, the EPROM power supply selection jumpers are provided on the reverse side of the simulation chip. At the factory shipment, the circuit connection is arranged so that current can be supplied to the EPROM through the power supply pin (V_{DD} pin) of the simulation chip.



(A) Connected to the GND (0V) pin.
(B) Connected to the EPROM power supply pin.
(C) Connected to the power supply pin of the simulation chip.
[Note that the circuit connection is arranged at the factory shipment so that the current can be supplied to an EPROM through the simulation chip.]

b) To supply current to an EPROM externally from an independent power source
Disconnect pattern (B) from pattern (C).
Connect the power supply pin (+5V) of an external independent power source circuit to pattern (B) and then the other pin to pattern (A)(GND).



[To supply current to an EPROM from an external power source circuit.]

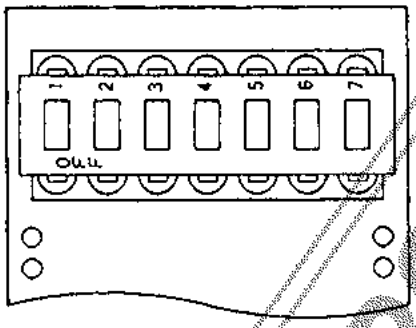
(Note) A simulation chip is an LSI produced in CMOS process technology.
The simulation chip will suffer from a "latch up" which is specific to CMOS LSIs if the voltage below the V_{SS} level is applied to input pins and output pins, or if the voltage above the V_{DD} level is applied such pins. The latch up problem may damage or degrade the device. To prevent it, much care should be taken to the power supply circuit design for the simulation chip and an EPROM.
In turning on a simulation chip and an EPROM, the simulation chip should be the first and the EPROM, the second. To turn off them, the order is reversed.

(4) Switches and pad for option selection

a) Switches for CPU-function settings

On the simulation chip are provided the switches for selecting a RAM capacity, a desired CPU and its.stack level, output logic level at reset for ports C and D, divider circuit's divide ratio, and PI0/OSC2 pin function. These switches are provided on the surface of the simulation chip board.

The figure below shows the outline of the above switches. The switch settings will be described in the item dealing with option specification methods.

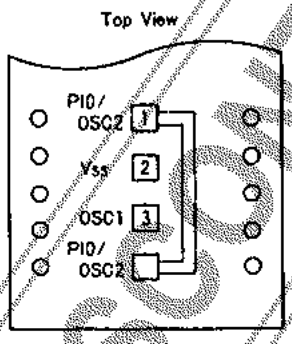


Pin 1 position

Switch 1 (PI0) . . . . . .Sets the PI0/OSC2 pin to the port 10 for input/output.
Switch 2 (OSC2) . . . . .Sets the PI0/OSC2 pin to the OSC2 pin for oscillation.
Switch 3 (DIV) . . . . . } Selects the divide ration for the divider circuit.
Switch 4 (3 or 4) . . . . }
Switch 5 (DHL) . . . . .Select the output logic at the reset for port D.
Switch 6 (CHL) . . . . . .Select the output logic at the reset for port C.
Switch 7 (RAMC) . . . .Select a desired CPU from LC6543 and LC6546.

b) Pad 2

The pad 2 is provided on the piggyback LSI to mount oscillation components. Add an external resistor according to a selected oscillation option. The switch settings will be described in the item dealing with option specification methods.



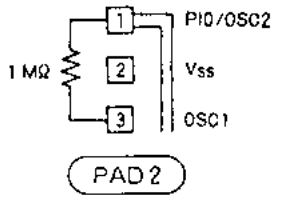
OSC1 : connected to the OSC1 pin of the LSI.
PI0/OSC2 : connected to the PI0/OSC2 pin of the LSI.
V_{SS} : connected to the V_{SS} pin of the LSI.

(5) Option specification methods

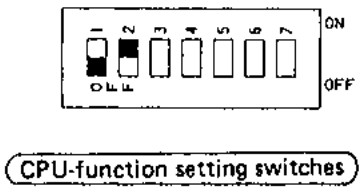
a) Option specification method for oscillation circuits

Oscillation circuits can be selected by using the PAD2 and CPU-function setting switches.

(i) Ceramic oscillation circuit

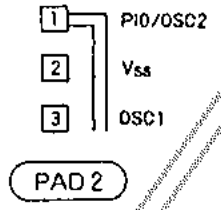


- Connect the PI0/OSC2 pin with the OSC1 pin through an external resistor of 1MΩ.
- For the oscillation constants of an application board, refer to the catalog.
  Fine control may be needed because the ideal RC constant will change due to mounting conditions.

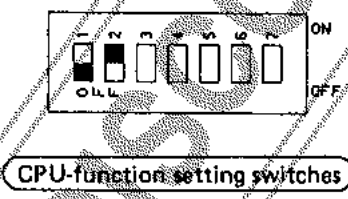


- Switch 1 . . .Set it to the OFF side.
  Switch 2 . . .Set it to the ON side.
- The PI0/OSC2 pin can be used as OSC2 pin for oscillation.

(ii) 2-pins RC oscillation circuit

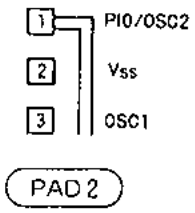


- No external component is required by the PAD2.
- For the oscillation constants of an application board, refer to the catalog.
  Fine control may be needed because the oscillation frequency of a mass-production LSI might differ from that of the application board.

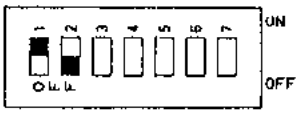


- Switch 1 . . .Set it to the OFF side.
  Switch 2 . . .Set it to the ON side.
- The PI0/OSC2 pin can be used as the OSC2 pin for oscillation.

(iii) External clock circuit

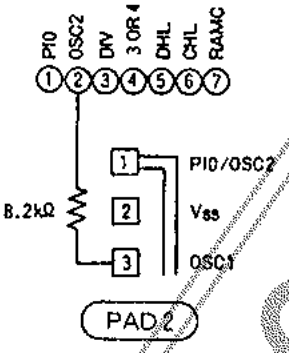


• No external component is required by the PAD2.

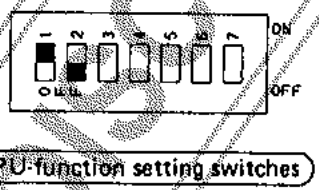


• Switch 1 . . .Set it to the ON side.
Switch 2 . . .Set it to the OFF side.
• The PIO/OSC2 pin can be used as the input/output PIO port.

(iv) 1-pin C oscillation circuit



• Connect the OSC1 pin of the PAD2 to pin 2 (OSC2) of the CPU-function setting switches through an external resistor of 8.2kΩ.
• For the oscillation constants of an application board, refer to the catalog.
Fine control may be needed because the oscillation frequency of a mass-production LSI might be differ from that of the application board.



• Switch 1 . . .Set it to the ON side.
Switch 2 . . .Set it to the OFF side.
• The PIO/OSC2 pin can be used as the input/output PIO port.

b) Option specification method for dividers
Dividers can be selected by using the CPU-function setting switches.
(i) 1/1 divider circuit

• Switch 3 . . .Set it to the OFF side.
Switch 4 . . .Set it to either side.

(ii) 1/3 divider circuit

• Switch 3 . . .Set it to the ON side.
Switch 4 . . .Set it to the ON side.

(iii) 1/4 divider circuit

• Switch 3 . . .Set it to the ON side.
Switch 4 . . .Set it to the OFF side.

c) Option specification method for the output logics of ports C and D at reset
The output logics of ports C and D at the reset can be specified by using the CPU-function setting switches.
Switch 5 (DHL) . . . . .Select the output logic of port D at the reset from H and L.
Switch 6 (CHL). . . . . .Select the output logic of port C at the reset from H and L.
(i) To set the logic level of port D or C at the initial reset to "H" (output OFF in case of open drain output)

• Set switch 5 or switch 6 to the ON side.
• The output logic level of port D or C at the initial reset can be specified independently.

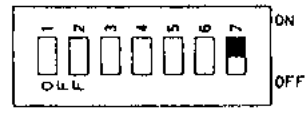
(ii) To set the logic level of port D or C at the initial reset to "L".

• Set switch 5 or switch 6 to the OFF side.
• The output logic level of port D or C at the initial reset can be specified independently.

d) Option specification method for evaluated CPUs
Evaluated microcomputers can be specified by using the CPU-function setting switches.
(i) To develop user application programs for the LC6543 microcomputers.

• Set switch 7 to the OFF side.

(ii) To develop user application programs for the LC6546 microcomputers.



• Set switch 7 to the ON side.

LC6543C, 6543H, 6546C, 6546H SERIES INSTRUCTION SET (BY FUNCTIONS)

Symbol	Description				
AC	: Accumulator	M(DP)	: Memory addressed by DP	( ), [ ]	: Contents
ACi	: Accumulator bit i	$P(DP_L)$	: Input/output port addressed by DP_L	←	: Transfer and direction
CF	: Carry flag	PC	: Program counter	+	: Addition
CTL	: Control register	STACK	: Stack register	−	: Subtraction
DP	: Data pointer	TM	: Timer	∧	: AND
E	: E register	TMF	: Timer (internal) interrupt request flag	∨	: OR
EXTF	: External interrupt request flag	At, Hs, La	: Working register	∀	: Exclusive OR
Fn	: Flag bit n	ZF	: Zero flag		
M	: Memory				

Instruction group	Mnemonic		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	The AC contents are cleared.	ZF	* 1
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	The CF contents are cleared.	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	The CF is set.	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC ← $\overline{(AC)}$	The AC contents are complemented.	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	The AC contents are incremented +1.	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) − 1	The AC contents are decremented −1.	ZF CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC_0 ← (CF), AC_{n+1} ← (AC_n) CF ← (AC_3)	The AC contents are shifted left through the CF.	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)	The AC contents are transferred to the E.		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ⇄ (E)	The AC contents and the E contents are exchanged.		
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← [M(DP)] + 1	The M(DP) contents are incremented +1.	ZF CF	
	DEM	Decrement M	0 0 1 0	1 1 1 1	1	1	M(DP) ← [M(DP)] − 1	The M(DP) contents are decremented −1.	ZF CF	
	SMB bit	Set M data bit	0 0 0 0	1 0 B_1B_0	1	1	M(DP B_1B_0) ← 1	A single bit of the M(DP) specified with B_1B_0 is set.		
	RMB bit	Reset M data bit	0 0 1 0	1 0 B_1B_0	1	1	M(DP B_1B_0) ← 0	A single bit of the M(DP) specified with B_1B_0 is reset.	ZF	
Arithmetic operation/comparison instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC ← (AC) + (M(DP))	Binary addition of the AC contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF	
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC ← [(AC) + (M(DP))] + (CF)	Binary addition of the AC, CF contents and the M(DP) contents is performed and the result is stored in the AC.	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 6	6 is added to the AC contents.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC ← (AC) + 10	10 is added to the AC contents.	ZF	
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) ∀ (M(DP))	The AC contents and the M(DP) contents are exclusive-ORed and the result is stored in the AC.	ZF	
	AND	And M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∧ (M(DP))	The AC contents and the M(DP) contents are ANDed and the result is stored in the AC.	ZF	
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ (M(DP))	The AC contents and the M(DP) contents are ORed and the result is stored in the AC.	ZF	
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	$\overline{(M(DP))}$ + (AC) + 1	The AC contents and the M(DP) contents are compared and the CF and ZF are set/reset.	ZF CF	
	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 $I_3I_2I_1I_0$	2	2	$\overline{I_3I_2I_1I_0}$ + (AC) + 1	The AC contents and the immediate data $I_3I_2I_1I_0$ are compared and the ZF and CF are set/reset.	ZF CF	
	CLI data	Compare DP_L with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 $I_3I_2I_1I_0$	2	2	$(DP_L) \forall I_3I_2I_1I_0$	The DP_L contents and the immediate data $I_3I_2I_1I_0$ are compared.	ZF	
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	$I_3I_2I_1I_0$	1	1	AC ← $I_3I_2I_1I_0$	The immediate data $I_3I_2I_1I_0$ is loaded in the AC.	ZF	* 1
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M(DP) ← (AC)	The AC contents are stored in the M(DP).		
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC ← (M(DP))	The M(DP) contents are loaded in the AC.	ZF	
	XM data	Exchange AC with M then modify DP_H with immediate data	1 0 1 0	0 $M_2M_1M_0$	1	2	(AC) ⇄ (M(DP)) DP_H ← $(DP_H) \forall 0M_2M_1M_0$	The AC contents and the M(DP) contents are exchanged and then the DP_H contents are modified with the contents of $(DP_H) \forall 0M_2M_1M_0$.	ZF	The ZF is set/reset according to the result of $(DP_H) \forall 0M_2M_1M_0$
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	(AC) ⇄ (M(DP))	The AC contents and the M(DP) contents are exchanged.	ZF	The ZF is set/reset according to the DP_H contents at the time of instruction execution.
	XI	Exchange AC with M then increment DP_L	1 1 1 1	1 1 1 0	1	2	(AC) ⇄ (M(DP)) DP_L ← $(DP_L) + 1$	The AC contents and the M(DP) contents are exchanged and then the DP_L contents are incremented +1.	ZF	The ZF is set/reset according to the result of $(DP_L) + 1$
	XD	Exchange AC with M then decrement DP_L	1 1 1 1	1 1 1 1	1	2	(AC) ⇄ (M(DP)) DP_L ← $(DP_L) - 1$	The AC contents and the M(DP) contents are exchanged and then the DP_L contents are decremented −1.	ZF	The ZF is set/reset according to the result of $(DP_L) - 1$
	RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC, E ← ROM (PCh, F, AC)	The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E.		

Comparison result	CF	ZF
[M(DP)] > (AC)	0	0
[M(DP)] = (AC)	1	1
[M(DP)] < (AC)	1	0

Comparison result	CF	ZF
$I_3I_2I_1I_0$ > (AC)	0	0
$I_3I_2I_1I_0$ = (AC)	1	1
$I_3I_2I_1I_0$ < (AC)	1	0

Instruction group	Mnemonic		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Data pointer manipulation instructions	LDZ data	Load DP_H with Zero and DP_L with immediate data respectively	1 0 0 0	$I_3I_2I_1I_0$	1	1	$DP_H \leftarrow 0$ $DP_L \leftarrow I_3I_2I_1I_0$	The DP_H and DP_L are loaded with 0 and the immediate data $I_3I_2I_1I_0$ respectively.		
	LHI data	Load DP_H with immediate data	0 1 0 0	$I_3I_2I_1I_0$	1	1	$DP_H \leftarrow I_3I_2I_1I_0$	The DP_H is loaded with the immediate data $I_3I_2I_1I_0$.		
	IND	Increment DP_L	1 1 1 0	1 1 1 0	1	1	$DP_L \leftarrow (DP_L)+1$	The DP_L contents are incremented +1.	ZF	
	DED	Decrement DP_L	1 1 1 0	1 1 1 1	1	1	$DP_L \leftarrow (DP_L)-1$	The DP_L contents are decremented −1.	ZF	
	TAL	Transfer AC to DP_L	1 1 1 1	0 1 1 1	1	1	$DP_L \leftarrow (AC)$	The AC contents are transferred to the DP_L.		
	TLA	Transfer DP_L to AC	1 1 1 0	1 0 0 1	1	1	$AC \leftarrow (DP_L)$	The DP_L contents are transferred to the AC.	ZF	
	XAH	Exchange AC with DP_H	0 0 1 0	0 0 1 1	1	1	$(AC) \rightleftarrows (DP_H)$	The AC contents and the DP_H contents are exchanged.		
Working register manipulation instructions	XAt XA0 XA1 XA2 XA3	Exchange AC with working register At		1' 10 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 0	1 1 1 1	1 1 1 1	$(AC) \rightleftarrows (A0)$ $(AC) \rightleftarrows (A1)$ $(AC) \rightleftarrows (A2)$ $(AC) \rightleftarrows (A3)$	The AC contents and the contents of working register At are exchanged. At is assigned one of A_0, A_1, A_2, A_3 according to I_1I_0.		
	XHa XH0 XH1	Exchange DP_H with working register Ha		a 1 0 0 0 1 1 0 0	1 1	1 1	$(DP_H) \rightleftarrows (H0)$ $(DP_H) \rightleftarrows (H1)$	The DP_H contents and the contents of working register Ha are exchanged. Ha is assigned either of H0 or H1 according to a.		
	XLa XL0 XL1	Exchange DP_L with working register La		a 0 0 0 0 0 1 0 0	1 1	1 1	$(DP_L) \rightleftarrows (L0)$ $(DP_L) \rightleftarrows (L1)$	The DP_L contents and the contents of working register La are exchanged. La is assigned either of L0 or L1 according to a.		
Flag manipulation instructions	SFB flag	Set flag bit	0 1 0 1	$B_3B_2B_1B_0$	1	1	$Fn \leftarrow 1$	The flag specified with $B_3B_2B_1B_0$ is set.		
	RFB flag	Reset flag bit	0 0 0 1	$B_3B_2B_1B_0$	1	1	$Fn \leftarrow 0$	The flag specified with $B_3B_2B_1B_0$ is reset.	ZF	The flags are divided into 4 groups of F_0 to F_3, F_4 to F_7, F_8 to F_{11}, F_{12} to F_{15}. The ZF is set/reset according to the 4 bits including a single bit specified with the immediate data $B_3B_2B_1B_0$.
Jump/subroutine instructions	JMP addr	Jump in the current bank	0 1 1 0 $P_7P_6P_5P_4$	1 $P_{10}P_9P_8$ $P_3P_2P_1P_0$	2	2	$PC \leftarrow P_{10}P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$	A jump to the address specified with immediate data $P_{10}P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$ occurs.		
	JPEA	Jump in the current page modified by E and AC	1 1 1 1	1 0 1 0	1	1	$PC_{3\sim0} \leftarrow (E, AC)$	A jump to the address specified with the contents of the PC whose low-order 8 bits are replaced by the E and AC contents occurs.		
	CZP addr	Call subroutine in the zero page	1 0 1 1	$P_3P_2P_1P_0$	1	1	STACK $\leftarrow (PC)+1$ $PC_{12\sim6} \leftarrow PC_{5\sim0} \leftarrow 0$ $PC_{5\sim2} \leftarrow P_3P_2P_1P_0$	A subroutine in page 0 of bank 0 is called.		
	CAL addr	Call subroutine in the zero bank	1 0 1 0 $P_7P_6P_5P_4$	1 $P_{10}P_9P_8$ $P_3P_2P_1P_0$	2	2	STACK $\leftarrow (PC)+2$ $PC_{12\sim0} \leftarrow 0P_{10}P_9P_8P_7P_6P_5P_4P_3P_2P_1P_0$	A subroutine in bank 0 is called.		
	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	1	$PC \leftarrow (STACK)$	A return from a subroutine occurs.		
	RTI	Return from interrupt routine	0 0 1 0	0 0 1 0	1	1	$PC \leftarrow (STACK)$ $CF, ZF \leftarrow CSF, ZSF$	A return from an interrupt service routine occurs.	ZF CF	
	BANK	Change bank	1 1 1 1	1 1 0 1	1	1		The bank is changed. A pseudo I/O port is specified.		Effective only when used immediately before an I/O instruction or branch instruction.
Branch instructions	BAt addr	Branch on AC bit	0 1 1 1 $P_7P_6P_5P_4$	0 0 t_1t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ACt = 1	If a single bit of the AC specified with the immediate data t_1t_0 is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BA0 to BA3 according to the value of t.
	BNAt addr	Branch on no AC bit	0 0 1 1 $P_7P_6P_5P_4$	0 0 t_1t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ACt = 0	If a single bit of the AC specified with the immediate data t_1t_0 is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNA0 to BNA3 according to the value of t.
	BMt addr	Branch on M bit	0 1 1 1 $P_7P_6P_5P_4$	0 1 t_1t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if (M(DP.t_1t_0)) = 1	If a single bit of the M(DP) specified with the immediate data t_1t_0 is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BM0 to BM3 according to the value of t.
	BNMt addr	Branch on no M bit	0 0 1 1 $P_7P_6P_5P_4$	0 1 t_1t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if (M(DP.t_1t_0)) = 0	If a single bit of the M(DP) specified with the immediate data t_1t_0 is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNM0 to BNM3 according to the value of t.
	BPt addr	Branch on Port bit	0 1 1 1 $P_7P_6P_5P_4$	1 0 t_1t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if (P(DP$_L$.t_1t_0)) = 1	If a single bit of port P(DP$_L$) specified with the immediate data t_1t_0 is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BP0 to BP3 according to the value of t.
	BNPt addr	Branch on no Port bit	0 0 1 1 $P_7P_6P_5P_4$	1 0 t_1t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if (P(DP$_L$.t_1t_0)) = 0	If a single bit of port P(DP$_L$) specified with the immediate data t_1t_0 is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNP0 to BNP3 according to the value of t.
	BTM addr	Branch on timer	0 1 1 1 $P_7P_6P_5P_4$	1 1 0 0 $P_3P_2P_1P_0$	2	2	$PC_{7\sim0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if TMF = 1 then TMF $\leftarrow$ 0	If the TMF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The TMF is reset.	TMF	

Instruction group	Mnemonic		Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Branch instructions	BNTM addr	Branch on no timer	0 0 1 1 $P_7P_6P_5P_4$	1 1 0 0 $P_3P_2P_1P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if TMF = 0 then TMF ← 0	If the TMF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The TMF is reset.	TMF	
BI addr	Branch on interrupt	0 1 1 1 $P_7P_6P_5P_4$	1 1 0 1 $P_3P_2P_1P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if EXTF = 1 then EXTF ← 0	If the EXTF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The EXTF is reset.	EXTF	
BNI addr	Branch on no interrupt	0 0 1 1 $P_7P_6P_5P_4$	1 1 0 1 $P_3P_2P_1P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if EXTF = 0 then EXTF ← 0	If the EXTF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs. The EXTF is reset.	EXTF	
BC addr	Branch on CF	0 1 1 1 $P_7P_6P_5P_4$	1 1 1 1 $P_3P_2P_1P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if CF = 1	If the CF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
BNC addr	Branch on no CF	0 0 1 1 $P_7P_6P_5P_4$	1 1 1 1 $P_3P_2P_1P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if CF = 0	If the CF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
BZ addr	Branch on ZF	0 1 1 1 $P_7P_6P_5P_4$	1 1 1 0 $P_3P_2P_1P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ZF = 1	If the ZF is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
BNZ addr	Branch on no ZF	0 0 1 1 $P_7P_6P_5P_4$	1 1 1 0 $P_3P_2P_1P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ZF = 0	If the ZF is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		
BFn addr	Branch on flag bit	1 1 0 1 $P_7P_6P_5P_4$	$n_3n_2n_1n_0$ $P_3P_2P_1P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if Fn = 1	If the flag bit of the 16 flags specified with the immediate data $n_3n_2n_1n_0$ is 1, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BF0 to BF15 according to the value of n.
BNFn addr	Branch on no flag bit	1 0 0 1 $P_7P_6P_5P_4$	$n_3n_2n_1n_0$ $P_3P_2P_1P_0$	2	2	$PC_{7-0} \leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if Fn = 0	If the flag bit of the 16 flags specified with the immediate data $n_3n_2n_1n_0$ is 0, a branch to the address specified with the immediate data $P_7P_6P_5P_4P_3P_2P_1P_0$ within the same page occurs.		Mnemonic is BNF0 to BNF15 according to the value of n.
Input/Output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC ← (P(OP$_L$))	Port P(OP$_L$) contents are loaded in the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(OP$_L$) ← (AC)	The AC contents are outputted to port P(OP$_L$).		
	SPB bit	Set port bit	0 0 0 0	0 1 B_1B_0	1	2	P(OP$_L$, B_1B_0) ← 1	A single bit in port P(OP$_L$) specified with the immediate data B_1B_0 is set.		When this instruction is executed, the E contents are destroyed.
	RPB bit	Reset port bit	0 0 1 0	0 1 B_1B_0	1	2	P(OP$_L$, B_1B_0) ← 0	A single bit in port P(OP$_L$) specified with the immediate data B_1B_0 is reset.	ZF	When this instruction is executed, the E contents are destroyed.
Other instructions	SCTL bit	Set control register bit (S)	0 0 1 0 1 0 0 0	1 1 0 0 $B_3B_2B_1B_0$	2	2	CTL ← (CTL) ∨ $B_3B_2B_1B_0$	The bits of the control register specified with the immediate data $B_3B_2B_1B_0$ are set.		
	RCTL bit	Reset control register bit (S)	0 0 1 0 1 0 0 1	1 1 0 0 $B_3B_2B_1B_0$	2	2	CTL ← (CTL) ∧ $\overline{B_3B_2B_1B_0}$	The bits of the control register specified with the immediate data $B_3B_2B_1B_0$ are reset.	ZF	
	WTTM	Write timer	1 1 1 1	1 0 0 1	1	3	TM ← (E), (AC) TMF ← 0	The E and AC contents are loaded in the timer. The TMF is reset.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	All operations stop.		Only when all pins of port PA are set at L, stop
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

*1) If the CLA instruction is used continuously in such a manner as CLA, CLA, ———, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.