Ordering number : ENN*6526

CMOS IC

LC74731W,74732W

On-Screen Display Controller

Preliminary

Overview

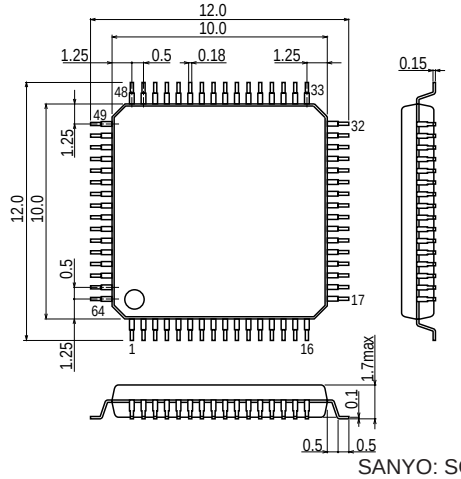
The LC74731W and LC74732W are on-screen display CMOS ICs that display characters and patterns on a TV screen under the control of a microcontroller. These ICs display 16 × 16-dot characters and up to 12 lines of text with 24 characters per line.

Features

- Text structure: 12 lines × 24 characters (Up to 288 characters)
- Character format: 16 × 16 dots
  Character display clock frequency: about 9 MHz
- Character sizes: Four sizes each in the horizontal and vertical directions with the size set in line units.
- Number of characters supported:
  LC74731W:256 (internal)
  LC74732W:512 (internal)
  Up to 8192 using an external ROM (for Japanese)
  [Reference] JIS X0298 (1990): 6877 characters
  JIS level 1 kanji: 2965 characters
  JIS level 2 kanji: 3388 characters
  Special characters: 524 characters
- Display start positions: 128 positions each in the horizontal and vertical directions
- Blinking, reverse video, reversed blinking, and character outlining: May be specified in individual character units.
- Blinking types: Two types with periods of about 1.0 and about 0.5 seconds.
- Blanking: The whole font area (16 ×16 dots) can be blanked in line units
  (Four types: no blanking, character size blanking, character plus outlining size blanking, and whole area up to adjacent character blanking)
- Line spacing control: Zero to seven scan lines, in line units
- Character color: Eight colors in character units (in internal synchronization mode): 2 fsc and 4 fsc
  (Black, red, green, yellow, blue, magenta, cyan, and white)
- Character background color: Eight colors (in internal synchronization mode): 2 fsc and 4 fsc
  (Black, red, green, yellow, blue, magenta, cyan, and transparent)
- Screen background color: Eight colors (in internal synchronization mode): 2 fsc and 4 fsc
  (Black, red, green, yellow, blue, magenta, cyan, and white)
- External control inputs: Serial interface with an 8-bit data size.
- Built-in sync separator circuit
- Video outputs: NTSC, PAL, PALM, PALN, NTSC 4.43, and PAL 60 composite video signal outputs
- Supports Y/C input

Package Dimensions

[LC74731W,74732W]



SANYO: SQFP64

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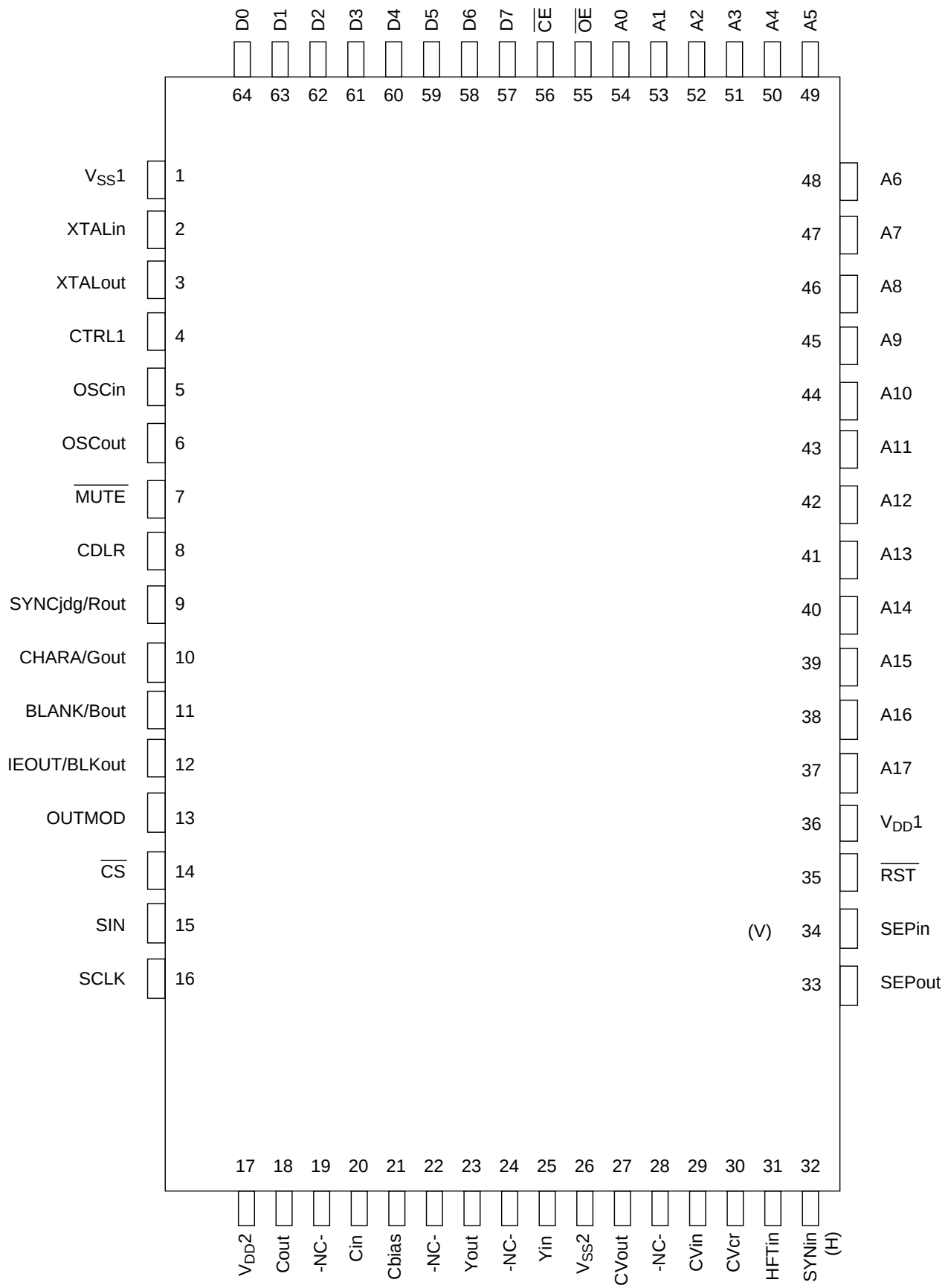
Pin Assignment



Pin Functions

Pin No.	Pin	Function	Description
1	$V_{SS}1$	Ground	Ground connection. (Digital system ground)
2	Xtalin	Crystal oscillator connections	Connections for the crystal element and capacitors that form the internal sync signal generating crystal oscillator. Xtalin can also be used to input an external clock signal. (2fsc or 4fsc)
3	Xtalout		
4	CTRL1	Switches the crystal oscillator input	Selects external clock input mode or crystal oscillator mode. Low: crystal oscillator mode, high: external clock input mode.
5	OSCin	LC oscillator connections	Connections for the coil and capacitor that form the character output dot clock generation oscillator.
6	OSCout		
7	$\overline{\text{MUTE}}$	Muting control input	This is an active-low input with hysteresis characteristics (MORE+). When low, the CVout, Yout, and Cout outputs are set to either, (1) CSYNC, CSYNC, PE, or (2) PE PE, PE. In the initial state, (1) is selected. This setting is switched by commands.
8	CDLR	Background color phase adjustment	Connection for the resistor used to adjust the background color phase
9	SYNCJDG /Rout	External sync signal judgment output (Rout output)	Outputs the result of the judgment as to whether or not the external sync signal is present. A high level is output when a sync signal is present. The dot clock (LC oscillator) is output when $\overline{\text{RST}}$ is low. (The IC can be set up to not output this signal during resets by commands.)
10	CHARA/Gout	Character output (Gout output)	Character signal output
11	BLANK/Bout	Blank output (Bout output)	Blank signal output pin
12	IEout/BLKout	Internal/external output (BLKout output)	Internal synchronization (high)/external synchronization (low) state output pin
13	OUTMOD	Output switching input	Switches between output from pins 9 to 12 and input to pin 32. Low: normal operation, high: RGB output supported
14	$\overline{\text{CS}}$	Enable input	Serial data input enable Serial data input is enabled when low. more+ (Hysteresis input characteristics)
15	SIN	Data input	Serial data input more+ (Hysteresis input characteristics)
16	SCLK	Clock input	Serial data input clock input more+ (Hysteresis input characteristics)
17	$V_{DD}2$	Power supply	Composite video signal level adjustment power supply. (Analog system power supply)
18	COUT	Color signal output	Color (C) signal output
19	NC		This pin must either be left open or connected to ground.
20	CIN	Color signal input	Color (C) signal input
21	CBIAS	Chrominance bias output	Chrominance signal bias level output
22	NC		This pin must be either left open or connected to ground.
23	YOUT	Luminance signal output	Luminance signal (Y) output
24	NC		This pin must be either left open or connected to ground.
25	YIN	Luminance signal input	Luminance signal (Y) input
26	$V_{SS}2$	Ground	Ground
27	CVOUT	Video signal output	Composite video signal output
28	NC		This pin must either be left open or connected to ground.
29	CVIN	Video signal input	Composite video signal input
30	CVCR	Video signal input	SECAM chrominance signal input
31	HFTin	Halftone signal input	Halftone signal input
32	SYNin	Sync separator circuit input	Video signal input to the internal sync separator circuit
33	SEPout	Composite sync signal output	Composite sync signal output from the internal sync separator circuit
34	SEPin	Vertical sync signal input	Vertical sync signal input MORE+ (Hysteresis input characteristics)
35	$\overline{\text{RST}}$	Reset input	System reset input A built-in pull-up resistor can be included in this pin's input circuit. (Hysteresis input characteristics)
36	$V_{DD}1$	Power supply (+5 V)	Power supply (+5 V: digital system power supply)

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Pin No.	Pin	Function	Description
37	A17	Address output 17	ROM address output 17
38	A16	Address output 16	ROM address output 16
39	A15	Address output 15	ROM address output 15
40	A14	Address output 14	ROM address output 14
41	A13	Address output 13	ROM address output 13
42	A12	Address output 12	ROM address output 12
43	A11	Address output 11	ROM address output 11
44	A10	Address output 10	ROM address output 10
45	A9	Address output 9	ROM address output 9
46	A8	Address output 8	ROM address output 8
47	A7	Address output 7	ROM address output 7
48	A6	Address output 6	ROM address output 6
49	A5	Address output 5	ROM address output 5
50	A4	Address output 4	ROM address output 4
51	A3	Address output 3	ROM address output 3
52	A2	Address output 2	ROM address output 2
53	A1	Address output 1	ROM address output 1
54	A0	Address output 0	ROM address output 0
55	$\overline{OE}$	Output enable	ROM output enable output. This is an active-low output.
56	$\overline{CE}$	Chip enable	ROM chip enable output. This is an active-low output.
57	D7	Data input 7	ROM data input 7. MORE+ (Hysteresis input characteristics)
58	D6	Data input 6	ROM data input 6. MORE+ (Hysteresis input characteristics)
59	D5	Data input 5	ROM data input 5. MORE+ (Hysteresis input characteristics)
60	D4	Data input 4	ROM data input 4. MORE+ (Hysteresis input characteristics)
61	D3	Data input 3	ROM data input 3. MORE+ (Hysteresis input characteristics)
62	D2	Data input 2	ROM data input 2. MORE+ (Hysteresis input characteristics)
63	D1	Data input 1	ROM data input 1. MORE+ (Hysteresis input characteristics)
64	D0	Data input 0	ROM data input 0. MORE+ (Hysteresis input characteristics)

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings		Unit
			min	max	
Supply voltage	V_{DD}	$V_{DD}1$ and $V_{DD}2$	V_{SS} – 0.3	V_{SS} + 6.5	V
Input voltage	V_{IN}	All input pins	V_{SS} – 0.3	$V_{DD}1$ + 0.3	V
Output voltage	V_{OUT}	SYNCJDG, BLANK, CHARA, SEPOUT, A0 to A17, CE, and OE	V_{SS} – 0.3	$V_{DD}1$ + 0.3	V
Allowable power dissipation	Pdmax		—	275	mW
Operating temperature	Topr		–30	+70	°C
Storage temperature	Tstg		–40	+125	°C

Recommended Operating Conditions

Parameter	Symbol	Conditions		Ratings			Unit
				min	typ	max	
Supply voltage	$V_{DD}1$	$V_{DD}1$		4.5	5.0	5.5	V
	$V_{DD}2$	$V_{DD}2$		4.5	5.0	6.5	V
Supply voltage [Only for RGB output]	$V_{DD}1$	$V_{DD}1$		2.7	5.0	5.5	V
	$V_{DD}2$	$V_{DD}2$		2.7	5.0	6.5	V
High-level input voltage	$V_{IH}1$	$\overline{CS}$, SIN, SCLK, SEPIN, and MUTE		0.8 $V_{DD}1$	—	5.5	V
	$V_{IH}2$	$\overline{RST}$		0.8 $V_{DD}1$	—	$V_{DD}1$ + 0.3	V
	$V_{IH}3$	CTRL1 and OUTMOD		0.7 $V_{DD}1$	—	$V_{DD}1$ + 0.3	V
	$V_{IH}4$	D0 to D7		0.8 $V_{DD}1$	—	5.5	V
Low-level input voltage	$V_{IL}1$	$\overline{RST}$, $\overline{CS}$, SIN, SCLK, SEPIN, and MUTE		V_{SS} – 0.3	—	0.2 $V_{DD}1$	V
	$V_{IL}2$	CTRL1 and OUTMOD		V_{SS} – 0.3	—	0.3 $V_{DD}1$	V
	$V_{IL}3$	D0 to D7		V_{SS} – 0.3	—	0.2 $V_{DD}1$	V
Pull-up resistor	R_{PU}	$\overline{RST}$, $\overline{CS}$, SIN, SCLK, and MUTE (when the pull-up resistor option is specified)		25	50	90	kΩ
Composite video signal input voltage	$V_{IN}1$	CVIN and CVCR	$V_{DD}1$ = 5 V	—	2.0	—	Vp-p
	$V_{IN}2$	SYNIN	$V_{DD}1$ = 5 V	1.5	2.0	2.5	Vp-p
Input voltage	$V_{IN}3$	XtalIN (when an external clock input is used) fin = 2 fsc, 4 fsc	$V_{DD}1$ = 5 V	—	—	5.0	Vp-p
Oscillator frequency	F_{OSC1}	The XtalIN and XtalOUT oscillator pins (2 fsc: NTSC)			7.159		MHz
		The XtalIN and XtalOUT oscillator pins (4 fsc: NTSC)			14.318		MHz
		The XtalIN and XtalOUT oscillator pins (2 fsc: PAL)		—	8.867	—	MHz
		The XtalIN and XtalOUT oscillator pins (4 fsc: PAL)		—	17.734	—	MHz
	F_{OSC2}	The OSCin and OSCout oscillator pins (LC oscillator)		—	10	—	MHz

Note: If the Xtalin pin is used in clock input mode, applications must take adequate input noise prevention and reduction measures.

Electrical Characteristics at Ta = –30 to +70°C, $V_{DD}1$ = 5 V unless otherwise specified.

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Input off leakage current	Ileak1	CV_{IN}, CV_{CR}, C_{IN}, and Y_{IN}		—	—	1	µA
Output off leakage current	Ileak2	CV_{OUT}, C_{OUT}, and Y_{OUT}		—	—	1	µA
High-level output voltage	$V_{OH}11$	SYNCJDG, SETPOUT, BLANK, CHARA, and IEOUT	$V_{DD}1$ = 5.5 to 4.5 V I_{OH} = –1.0 mA	0.9 $V_{DD}1$	—	—	V
	$V_{OH}12$	SYNCJDG, SETPOUT, BLANK, CHARA, and IEOUT	$V_{DD}1$ = 4.4 to 2.7 V I_{OH} = –0.5 mA	0.9 $V_{DD}1$	—	—	V
	$V_{OH}21$	A0 to A17, OE, and CE	$V_{DD}1$ = 5.5 to 4.5 V I_{OH} = –1.0 mA	0.9 $V_{DD}1$	—	—	V
	$V_{OH}22$	A0 to A17, OE, and CE	$V_{DD}1$ = 4.4 to 2.7 V I_{OH} = –0.5 mA	0.9 $V_{DD}1$	—	—	V
Low-level output voltage	$V_{OL}11$	SYNCJDG, SEPOUT, BLANK, CHARA, and IEOUT	$V_{DD}1$ = 5.5 to 4.5 V I_{OL} = 1.0 mA	—	—	0.1 $V_{DD}1$	V
	$V_{OL}12$	SYNCJDG, SEPOUT, BLANK, CHARA, and IEOUT	$V_{DD}1$ = 4.4 to 2.7 V I_{OL} = 0.5 mA	—	—	0.1 $V_{DD}1$	V
	$V_{OL}21$	A0 to A17, OE, and CE	$V_{DD}1$ = 5.5 to 4.5 V I_{OL} = 1.0 mA	—	—	0.1 $V_{DD}1$	V
	$V_{OL}22$	A0 to A17, OE, and CE	$V_{DD}1$ = 4.4 to 2.7 V I_{OL} = 0.5 mA	—	—	0.1 $V_{DD}1$	V
Input current	I_{IH}	RST, CS, SIN, SCLK, CTRL1, MUTE, and OUTMOD	V_{IN} = $V_{DD}1$	—	—	1	µA
	I_{IL}	CS, SIN, SCLK, CTRL1, and OUTMOD	V_{IN} = $V_{SS}1$	–1	—	—	µA
Operating current drain	$I_{DD}1$	$V_{DD}1$	All outputs: open Xtal: 17.734 MHz LC: 10 MHz	—	—	40	mA
	$I_{DD}2$	$V_{DD}2$	$V_{DD}2$ = 5 V			20	mA

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Parameter	Symbol	Pin	Conditions		Ratings min	Ratings typ	Ratings max	Unit
SYNC level	V_{SN}	CVOUT (1): When SYNC – LEVEL = 0.8 V (2): When SYNC – LEVEL = 1.0 V (3): When SYNC – LEVEL = 1.4 V	$V_{DD}1$ = 5.0 V $V_{DD}2$ = 5.0 V	(1)		0.80		V
				(2)		1.00		
				(3)		1.40		
Pedestal level	V_{PD}			(1)		1.37		V
				(2)		1.57		
				(3)		1.97		
Color burst low level	V_{CBL}			(1)		1.07		V
				(2)		1.27		
				(3)		1.67		
Color burst high level	V_{CBH}			(1)		1.67		V
				(2)		1.87		
				(3)		1.27		
Background color 1 low level	$V_{RSL}1$			(1)		1.23		V
				(2)		1.43		
				(3)		1.83		
Background color 1 high level	$V_{RSH}1$			(1)		2.37		V
				(2)		2.57		
				(3)		2.97		
Background color 2 low level	$V_{RSL}2$			(1)		1.52		V
				(2)		1.72		
				(3)		2.12		
Background color 2 high level	$V_{RSH}2$			(1)		2.01		V
				(2)		2.21		
				(3)		2.61		
Outlining level 1	$V_{BK}1$			(1)		1.50		V
				(2)		1.70		
				(3)		2.10		
Outlining level 2	$V_{BK}2$			(1)		1.80		V
				(2)		2.00		
				(3)		2.40		
Outlining level 3	$V_{BK}3$			(1)		2.08		V
				(2)		2.28		
				(3)		2.68		
Character level 1	$V_{CHA}1$			(1)		2.65		V
				(2)		2.85		
				(3)		3.25		
Character level 3	$V_{CHA}3$			(1)		2.23		V
				(2)		2.43		
				(3)		2.83		

OSD Write (See figure 1.) at Ta = –30 to +70°C, $V_{DD}1$ = 5 ± 0.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	t_w (sclk)	SCLK	200	—	—	ns
	t_w (cs)	$\overline{CS}$ (the period when $\overline{CS}$ is high)	1	—	—	µs
Data setup time	t_{su} (cs)	$\overline{CS}$	200	—	—	ns
	t_{su} (sin)	SIN	200	—	—	ns
Data hold time	t_h (cs)	$\overline{CS}$	2	—	—	µs
	t_h (sin)	SIN	200	—	—	ns
One word write time	t_{word}	The time to write 8 bits of data	4.2	—	—	µs
	t_{wt}	RAM data write time	1	—	—	µs

Supplementary Materials

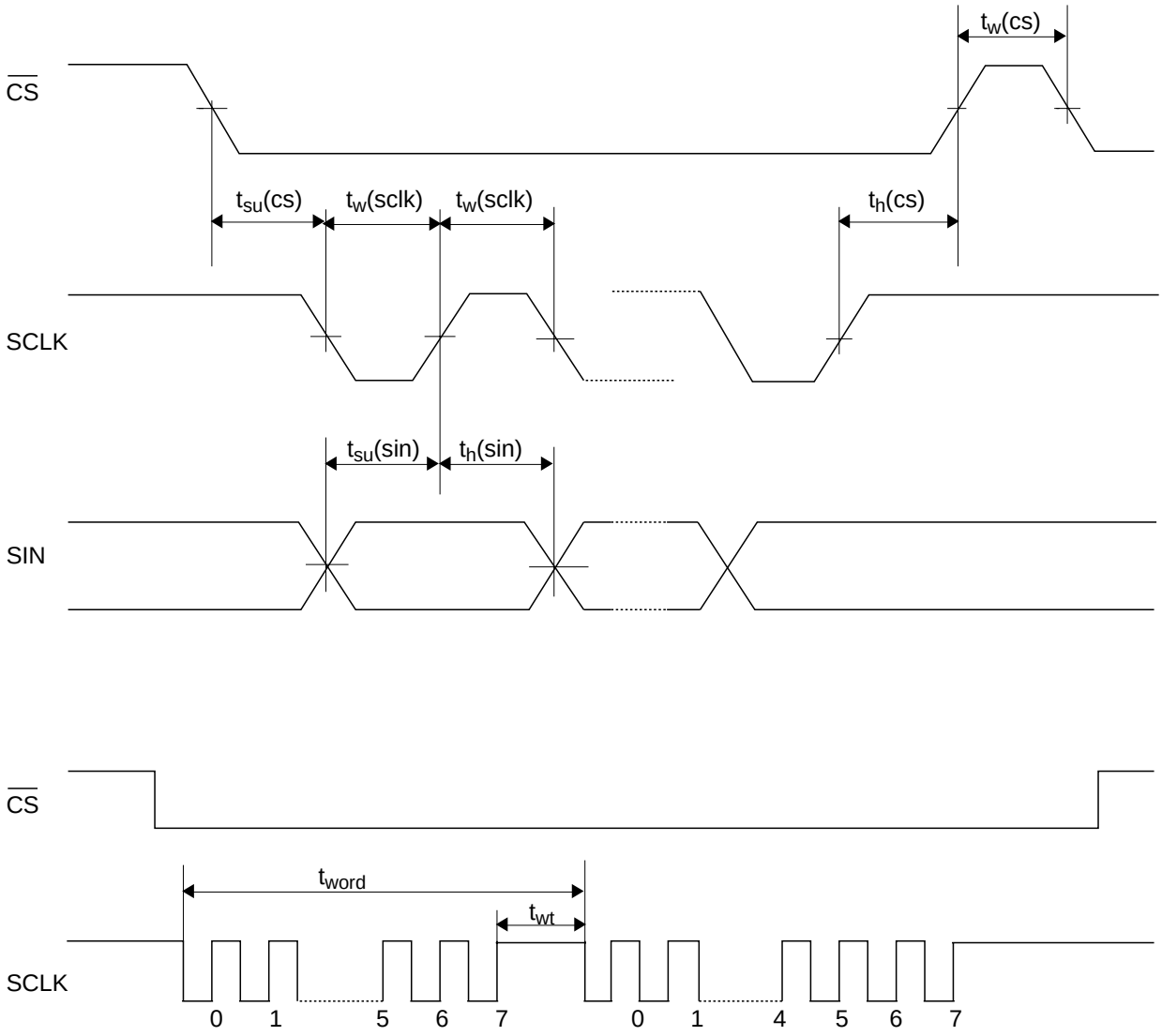
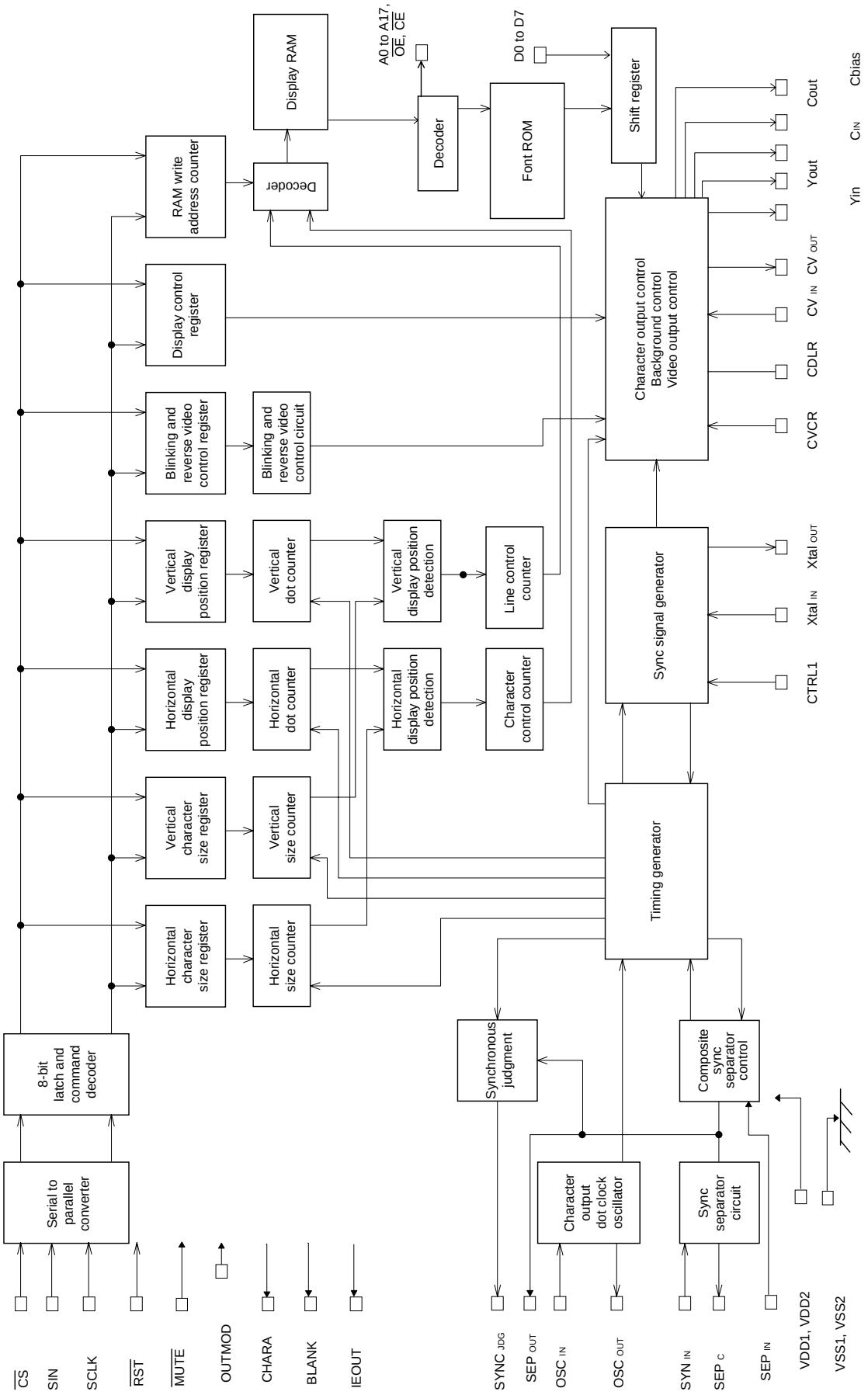


Figure 1 OSD Serial Data Input Timing

System Block Diagram



Display Control Commands

Display control commands have an 8-bit format and are transferred using the serial input function. Commands consist of a command identification code in the first byte and command data in the following bytes.

Display Control Commands

Command	First byte								Second byte							
	Command identification code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 (Write address setup)	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 (Character write)	1	0	0	1	IR	SD2	SD1	SD0	at2	at1	CB2	CB1	CB0	CC2	CC1	CC0
									0	0	0	C12	C11	C10	C9	C8
									C7	C6	C5	C4	C3	C2	C1	C0
COMMAND20 (Vertical display start position)	1	0	1	0	0	0	RRM1	RRM0	0	VP6	VP5	VP4	VP3	VP2	VP1	VP0
COMMAND21 (Horizontal display start position)	1	0	1	0	0	1	0	0	0	HP6	HP5	HP4	HP3	HP2	HP1	HP0
COMMAND22 (Character size)	1	0	1	0	1	0	0	SRM	0	0	0	0	VS1	VS0	HS1	HS0
COMMAND23 (Character size - in line units)	1	0	1	0	1	1	0	LSZUD	0	0	LSZB5	LSZA4	LSZ93	LSZ82	LSZ71	LSZ60
COMMAND3 (Display control)	1	0	1	1	TSTMOD	RAMERS	OSCSTP	SYSRST	0	LCSOFF	XN53S	BLKSEL	LC	FS	BK	DSPON
COMMAND4 (Display control)	1	1	0	0	NP2	NP1	NP0	I/N	0	HLFINT	BCL1	BCL0	CB	PH2	PH1	PH0
COMMAND50 (Sync signal detection 1)	1	1	0	1	0	0	DISLIN	I/E	0	RN2	RN1	RN0	SN3	SN2	SN1	SN0
COMMAND51 (Sync signal detection 2)	1	1	0	1	0	1	MUT1	MUT0	0	O	RNE0	SJN3	SJN2	SJN1	SJC1	SJC0
COMMAND52 (Display control)	1	1	0	1	1	0	EVEBSS	LSPSS	0	CINSEL	CINCTL	VNPSEL	VSPSEL	MSKERS	MSKSEL	EGLSEL
COMMAND53 (Display control)	1	1	0	1	1	1	RSLG1	RSLG0	0	0	CTL3	SPOSEL	PALAL4	IHSEL	VSSEL	HSSEL
COMMAND60 (Outlining setting)	1	1	1	0	0	0	0	BRM	0	BXBLV1	BXBLV0	BXWLV1	BXWLV0	ATSEL	BLK1	BLK0
COOMAND61 (Outlining setting - in line units)	1	1	1	0	0	1	0	LFCUD	0	0	LFCB5	LFCA4	LFC93	LFC82	LFC71	LFC60
COMMAND62 (Line spacing)	1	1	1	0	1	0	0	GRM	0	O	BXC1	GS1	GS0	GY2	GY1	GY0
COMMAND63 (Line spacing - in line units)	1	1	1	0	1	1	0	LGYUD	0	0	LGYB5	LGYA4	LGY93	LGY82	LGY71	LGY60
COMMAND70 (Display level)	1	1	1	1	0	0	0	LRM	0	0	BKLC1	BKLC0	CHLC1	CHLC0	RSLC1	RSLC0
COMMAND71 (Display level - in line units)	1	1	1	1	0	1	0	LCLUD	0	0	LCLB5	LCLA4	LCL93	LCL82	LCL71	LCL60
COMMAND72 (Halftone - in line units)	1	1	1	1	1	0	LHTDAT	LHTUD	0	0	LHTB5	LHTA4	LHT93	LHT82	LHT71	LHT60
COMMAND73 (RGB control)	1	1	1	1	1	1	0	0	0	DASSS	GBSEL	OUTSEL	HSPSW	XONSS	BLK01	BLK00

Note that when the display character data write command (COMMAND1) is written, tthese ICs lock into the display character data write mode, and another first byte cannot be written.
When the $\overline{CS}$ pin is set high, the these ICs are set to the COMMAND0 (display memory write address setup mode) state.

COMMAND0 (Display memory write address setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 0 identification code	
6	—	0	Display memory write address setup	
5	—	0		
4	—	0		
3	V3	0	Display memory line address (0 to B (hexadecimal))	
		1		
2	V2	0		
		1		
1	V1	0		
		1		
0	V0	0		
		1		

• Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0	Second byte identification code	
6	—	0		
5	—	0		
4	H4	0	Display memory line address (0 to 17 (hexadecimal))	
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0	0		
		1		

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

COMMAND1 (Display character data write setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 1 identification code Display character data write settings	Note that when this command is input, the LC74731W/74732W lock into the display character data write mode until the $\overline{CS}$ pin is set high.
6	—	0		
5	—	0		
4	—	1		
3	IR	0	Internal ROM	Switching between internal and external ROM
		1	External ROM	
2	SD2	0	White-on-black (convex) display	Character frame specification
		1	Black-on-white (concave) display	
1	SD1	0	Character frame start: off	
		1	Character frame start: on	
0	SD0	0	Character frame stop: off	
		1	Character frame stop: on	

• Second byte (1)

DA0 to 7	Register	Content					Notes
		State	Function				
7	at2	0	Character attribute 2: off (Character frame upper side: off)				Blinking specification Selected by COM60 second byte and ATSEL.
		1	Character attribute 2: on (Character frame upper side: on)				
6	at1	0	Character attribute 1: off (Character frame lower side: off)				Reverse video specification Selected by COM60 second byte and ATSEL.
		1	Character attribute 1: on (Character frame lower side: on)				
5	cb2	0	cb2	cb1	cb0	Character background color	Character background color specification
		1	(B	G	R)		
4	cb1	0	0	0	0	Black	
		1	0	0	1	Red	
3	cb0	0	0	1	0	Green	
		1	0	1	1	Yellow	
			1	0	0	Blue	
			1	0	1	Magenta	
			1	1	0	Cyan	
			1	1	1	Transparent	
2	cc2	0	cc2	cc1	cc0	Character color	Character color specification
		1	(B	G	R)		
1	cc1	0	0	0	0	Black	
		1	0	0	1	Red	
0	cc0	0	0	1	0	Green	
		1	0	1	1	Yellow	
			1	0	0	Blue	
			1	0	1	Magenta	
			1	1	0	Cyan	
			1	1	1	White	

• Second byte (2)

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0		
6	—	0		
5	—	0		
4	c12	0	Character code (00xx to 1Fxx (hexadecimal))	External ROM upper address
		1		
3	c11	0		
		1		
2	c10	0		
		1		
1	c09	0		
		1		
0	c08	0		
		1		

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

• Second byte (3)

DA0 to 7	Register	Content		Notes
		State	Function	
7	c07	0	Character code (00 to FF (hexadecimal))	External ROM lower address
		1	FE (hexadecimal): Space character	Internal ROM address
6	c06	0	FF (hexadecimal): Transparent space character	
		1		
5	c05	0		
		1		
4	c04	0		
		1		
3	c03	0		
		1		
2	c02	0		
		1		
1	c01	0		
		1		
0	c00	0		
		1		

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

Continuous mode (cleared by setting $\overline{\text{CS}}$ high) operates as follows according to IR.

When internal ROM is specified: 1-1 1-2-1 1-2-2 1-2-3 1-2-3 1-2-3 1-2-3 ⟷

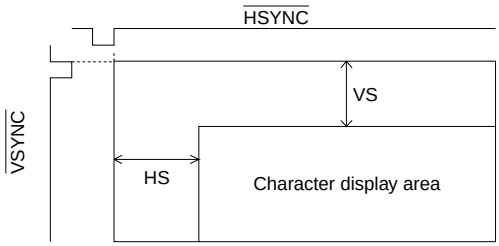
When external ROM is specified: 1-1 1-2-1 1-2-2 1-2-3 1-2-2 1-2-3 1-2-2 1-2-3 ⟷

COMMAND20 (Vertical display start position setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 2 identification code	
6	—	0	Vertical display position and vertical direction character size settings	
5	—	1		
4	—	0		
3	—	0	Extended command 0 identification code	
2	—	0		
1	RRM1	0	RRM1 RRM0	Continuous RAM write mode specification
		1	0 0 Initial value (depends on IR)	
0	RRM0	0	0 1 1-2-1 1-2-2 1-2-3 Fixed	
		1	1 0 1-2-2 1-2-3 Fixed	
			1 1 1-2-3 Fixed	

• Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	VP6 (MSB)	0	If VS is the vertical display start position then:	The vertical display start position is set by the 7 bits VP0 to VP6.
		1		
5	VP5	0	$VS = \alpha + H \times (2\sum_{n=0}^{6} 2^{n} VPn)$	The weight of bit 1 is 2H.
		1		
4	VP4	0	H: the horizontal synchronization pulse period	
		1	α = 20H (525H systems)	
3	VP3	0	= 25H (625H systems)	
		1		
2	VP2	0		
		1		
1	VP1	0		
		1		
0	VP0 (LSB)	0		
		1		

COMMAND21 (Horizontal display start position setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 2 identification code	
6	—	0	Horizontal display position setup and horizontal direction	
5	—	1	character size settings	
4	—	0		
3	—	0	Extended command 1 identification code	
2	—	1		
1	—	0		
0	—	0		

• Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	HP6 (MSB)	0	If HS is the horizontal start position then:	The horizontal display start position is set by the 7 bits HP0 to HP6. The weight of bit 1 is 2Tc.
		1		
5	HP5	0	$HS = Tc \times (2\sum_{n=0}^{6} 2^{n} HPn)$	
		1		
4	HP4	0	Tc: Period of the oscillator connected to OSCIN/OSCOUT in operating mode.	
		1		
3	HP3	0		
		1		
2	HP2	0		
		1		
1	HP1	0		
		1		
0	HP0 (LSB)	0		
		1		

Note that all registers are set to 0 when these ICs are reset by the $\overline{RST}$ pin.

COMMAND22 (Character size setting command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 2 identification code	
6	—	0	Horizontal display position setup and horizontal direction character size settings	
5	—	1		
4	—	0		
3	—	1	Extended command 2 identification code	
2	—	0		
1	—	0		
0	SRM	0	Continuous mode: off	Character size continuous mode specification
		1	Continuous mode: on	

• Second byte

DA0 to 7	Register	Content				Notes
		State	Function			
7	—	0	Second byte identification bit			
6	—	0				
5	—	0				
4	—	0				
3	VS1	0	VS1	VS0	Character size	Vertical direction character size, in line units
		1	0	0	1×	
2	VS0	0	0	1	2×	
		1	1	0	3×	
			1	1	4×	
1	HS1	0	HS1	HS0	Character size	Horizontal direction character size, in line units
		1	0	0	1×	
0	HS0	0	0	1	2×	
		1	1	0	3×	
			1	1	4×	

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

COMMAND23 (Character size and line setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 2 identification code	
6	—	0	Horizontal display position setup and horizontal direction character size settings	
5	—	1		
4	—	0		
3	—	1	Extended command 3 identification code	
2	—	1		
1	—	0		
0	LSZUD	0	Lower lines: 0 to 5 (hexadecimal)	Upper/lower line specification
		1	Upper lines: 6 to B (hexadecimal)	

• Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	LSZB5	0	Line 6 (line 12) specification: off	The line shown in parentheses is specified when LSZUD is 1.
		1	Line 6 (line 12) specification: on	
4	LSZA4	0	Line 5 (line 11) specification: off	
		1	Line 5 (line 11) specification: on	
3	LSZ93	0	Line 4 (line 10) specification: off	
		1	Line 4 (line 10) specification: on	
2	LSZ82	0	Line 3 (line 9) specification: off	
		1	Line 3 (line 9) specification: on	
1	LSZ71	0	Line 2 (line 8) specification: off	
		1	Line 2 (line 8) specification: on	
0	LSZ60	0	Line 1 (line 7) specification: off	
		1	Line 1 (line 7) specification: on	

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

COMMAND3 (Display control setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 3 identification code	
6	—	0	Display character data write settings	
5	—	1		
4	—	1		
3	TSTMOD	0	Normal operating mode	This bit must always be 0.
		1	Test mode	
2	RAMERS	0		The RAM erase operation takes about 500 µs. (It must be executed in the DSPOFF state.)
		1	Erase display RAM (sets the data to FF (hexadecimal))	
1	OSCSTP	0	Do not stop the crystal and LC oscillator circuits.	This setting is valid in external synchronization mode when character display is off.
		1	Stop the crystal and LC oscillator circuits.	
0	SYSRST	0		The reset occurs when the $\overline{CS}$ pin is low, and is cleared when $\overline{CS}$ is set high.
		1	Reset all registers. This turns the display off.	

• Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	LCSOFF	0	Normal operation	Switches the LC oscillator STOP control
		1	LC oscillator STOP: Disabled	
5	XN53S	0	Normal	Switches the crystal oscillator capability
		1	Switching	
4	BLKSEL	0	Character display area	Specifies the character size that fills the whole character area.
		1	Video display area	
3	LC	0	The LC oscillator is used as the dot clock.	Selects the dot clock used for character display in the horizontal direction.
		1	The crystal oscillator is used as the dot clock.	
2	FS	0	Crystal oscillator frequency: 2 fsc	Sets the crystal oscillator frequency.
		1	Crystal oscillator frequency: 4 fsc	
1	BK	0	Blinking period: 0.5 s	Switches the blinking period.
		1	Blinking period: 1 s	
0	DSPON	0	Character display: off	
		1	Character display: on	

Note that all registers are set to 0 when these ICs are reset by the $\overline{RST}$ pin.

COMMAND4 (Display control setup command)

• First byte

DA0 to 7	Register	Content					Notes
		State	Function				
7	—	1	Command 4 identification code				
6	—	1	Display control settings				
5	—	0					
4	—	0					
3	NP2	0	NP2	NP1	NP0	Signal format	Switches the signal format
		1	0	0	0	NTSC	
2	NP1	0	0	0	1	PAL-M	
		1	0	1	0	PAL	
1	NP0	0	0	1	1	PAL-N	
		1	1	0	0	NTSC4.43	
			1	0	1	PAL60	
0	I/N	0	Interlaced				Switches between interlaced and noninterlaced
		1	Noninterlaced				

• Second byte

DA0 to 7	Register	Content					Notes
		State	Function				
7	—	0	Second byte identification bit				
6	HLFINT	0	Normal mode				
		1	Semi-internal synchronization mode				
5	BCL1	0	BCL1	BCL0			Only valid in internal synchronization mode.
		1	0	0	Background color shown		
4	BCL0	0	0	1	No background color (RSL1)		
		1	1	0	No background color (CBH)		
			1	1	No background color (RSH1)		
3	CB	0	The color burst signal is output.				Only valid when BCL is high.
		1	Color burst signal output is stopped.				
2	PH2	0	PH2	PH1	PH0	Background color	Background color specification
		1	B	G	R		
1	PH1	0	0	0	0	Black (RSLx)	
		1	0	0	1	Red	
0	PH0	0	0	1	0	Green	
		1	0	1	1	Yellow	
			1	0	0	Blue	
			1	0	1	Magenta	
			1	1	0	Cyan	
			1	1	1	White (RSHx)	

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

COMMAND50 (Sync signal detection 1 setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 5 identification code	
6	—	1	Sync signal control settings	
5	—	0		
4	—	1		
3	—	0	Extended command 0 identification code	
2	—	0		
1	DISLIN	0	12 lines	Switches the number of lines displayed.
		1	10 lines	
0	I/E	0	External synchronization	Switches between internal and external synchronization
		1	Internal synchronization	

• Second byte

DA0 to 7	Register	Content					Notes
		State	Function				
7	—	0	Second byte identification bit				
6	RN2	0	RN2	RN1	RN0	Number of times HSYNC detected	External sync signal detection control Recognition of the transition from the no signal state to the signal present state. Sets the sampling period in which the sync signal can be detected continuously in the horizontal sync signal period (1H). The values in parentheses apply when RNE0 (COM51) is 1.
		1	0	0	0	0 times (32 times)	
5	RN1	0	0	0	1	4 times (64 times)	
		1	0	1	0	8 times (128 times)	
4	RN0	0	1	0	0	16 times (256 times)	
		1					
3	SN3	0	SN3	SN2	SN1	SN0	Number of times HSYNC detected	External sync signal detection control Recognition of the transition from the signal present state to the no signal state. Sets the sampling period time in which the sync signal cannot be detected continuously in the horizontal sync signal period (1H).
		1	0	0	0	0	Not detected	
2	SN2	0	0	0	0	1	32 times	
		1	0	0	1	0	64 times	
1	SN1	0	0	1	0	0	128 times	
		1	1	0	0	0	256 times	
0	SN0	0						
		1						

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

COMMAND51 (Sync signal detection 2 setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 5 identification code	
6	—	1	Display control settings	
5	—	0		
4	—	1		
3	—	0	Extended command 1 identification code	
2	—	1		
1	MUT1	0	MUT1 MUT0 Output	Video signal output muting function selection
		1	0 0 CSYNC	Valid when the MUTE pin is low.
0	MUT0	0	0 1 PE	
		1	1 0 A0-17 “Z”	

• Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	RNE0	0	Sync signal no signal to signal present discrimination - Normal values	Changes the judgment criterion values for sync signal recognition for the no signal to signal present transition. (COM50)
		1	Sync signal no signal to signal present discrimination - Values shown in parentheses	
4	SJNS3	0	SJNS3 SJNS2 SJNS1 Times	Noise ignoring circuit setting for sync signal recognition for the no signal to signal present transition If more than the number of horizontal signals shown at the left are input during a 1H period, the circuit recognizes a no signal state.
		1	0 0 0 None	
3	SJNS2	0	0 0 1 4	
		1	0 1 0 8	
2	SJNS1	0	0 1 1 16	
		1	1 0 0 32	
			1 0 1 64	
			1 1 0 128	
			1 1 1 256	
1	SJCS1	0	SJCS1 SJCS0 PAL NTSC	Synchronization discrimination Selects the clock used to delimit the HSYNI signal.
		1	0 0 677 ns (1/3) 558 ns (1/2)	
0	SJCS0	0	0 1 903 ns (1/4) 838 ns (1/3)	
		1	1 0 450 ns (1/2) 1117 ns (1/4)	

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

COMMAND52 (Display control setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 5 identification code	
6	—	1	Display control settings	
5	—	0		
4	—	1		
3	—	1	Extended command 2 identification code	
2	—	0		
1	EVEBSS	0	Normal	Switches the ENBVI signal
		1	Always high	
0	LSPSS	0	Normal	LCSTOP control signal
		1	HT12 “on” HT34 “off”	

• Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	CINSEL	0	Blank area (the logical OR of the character and outlining signals)	Switches the CV_{CR} on state signal
		1	Video signal display area	
5	CINCTL	0	CV_{CR}: off	CV_{CR} on/off switching
		1	CV_{CR}: on	
4	VNPSEL	0	V signal falling edges detected	Switches the V signal acquisition polarity when external mode/internal V separation is used
		1	V signal rising edges detected	
3	VSPSEL	0	VSEP: About 8.9 µs (NTSC)	Switches the internal vertical separation time
		1	VSEP: About 17.8 µs (NTSC)	
2	MSKERS	0	Mask enabled	Clears the HSYNC and VSYNC masks
		1	Mask disabled	
1	MSKSEL	0	3H (NTSC)	Switches the VSYNC mask
		1	20H (NTSC)	
0	EGL	0	Outlining level 0 only (VBK0)	Switches the outlining level (Only valid when BLK0 is 0 and BLK1 is 1.)
		1	Two-stage outlining level (VBK0, VBK1)	

Note that all registers are set to 0 when these ICs are reset by the $\overline{RST}$ pin.

COMMAND53 (Display control setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 5 identification code	
6	—	1	Display control settings	
5	—	0		
4	—	1		
3	—	1	Extended command 3 identification code	
2	—	1		
1	RSLG1	0	RSLG1 RSLG0	Switches the screen background color level
		1	0 0 NO1 RS1	
0	RDLG0	0	0 1 NO2 RS2	
		1	1 0 NO3 RS3	

• Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	CTL3	0	Internal vertical separation circuit	Switches the VSYNC signal input
		1	External input	
4	SP0SEL	0	CSYNC (sync separator output)	Switches the SEPout pin output
		1	Halftone output	
3	PALAL4	0	Normal	
		1	Always use 4 fsc timing (PAL)	
2	IHSEL	0	SYNin pin input signal	Switches the internal vertical separation input signal
		1	SEPin pin input signal	
1	VSSEL	0	Negative polarity	Switches the SEPin input polarity
		1	Positive polarity	
0	HSSEL	0	Negative polarity	Switches the SYNin input polarity (Invalid for CVIDEO input)
		1	Positive polarity	

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

SYnin: CVIDEO (Built-in sync separator circuit)
SEPin: None (internal vertical separation)
or
:VSYNC
SYNin: HD
SEPin: CSYNC (internal vertical separation)

SYNin: HSYNC
SEPin: VSYNC

SYNin: CSYNC (internal vertical separation)
SEPin: None

COMMAND60 (Outlining control setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 6 identification code	
6	—	1	Display control settings	
5	—	1		
4	—	0		
3	—	0	Extended command 0 identification code	
2	—	0		
1	—	0		
0	BRM	0	Normal mode	Specifies continuous mode
		1	Continuous mode	

• Second byte

DA0 to 7	Register	Content					Notes
		State	Function				
7	—	0	Second byte identification bit				
6	BXBLV1	0	BXBLV1	BXBLV0			Character frame - black level specification
		1	0	0	NO1	BK1	In line units
5	BXBLV0	0	0	1	NO2	BK2	
		1	1	0	NO3	BK3	
4	BXWLV1	0	BXWLV1	BXWLV0			Character frame - white level specification
		1	0	0	NO1	CHA1	In line units
3	BXWLV0	0	0	1	NO2	CHA2	
		1	1	0	NO3	CHA3	
2	ATSEL	0	Reverse video, blinking				Setup for the at1 and at2 function
		1	Character frame specified				In line units
1	BLK1	0	BLK1	BLK0	Mode		Outlining mode specification
		1	0	0	Normal		In line units
0	BLK0	0	0	1	Character size		
		1	1	0	Outlining size		
			1	1	Full area size		

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

COMMAND61 (Outlining control and line specification setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 6 identification code	
6	—	1	Display control settings	
5	—	1		
4	—	0		
3	—	0	Extended command 1 identification code	
2	—	1		
1	—	0		
0	LFCUD	0	Lower lines (0 to 5 (hexadecimal))	Outlining control line specification
		1	Upper lines (6 to B (hexadecimal))	

• Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	LFCB5	0	Line 6 (line 12) setting: off	Outlining line setting The values in parentheses apply when LFCUD is 1.
		1	Line 6 (line 12) setting: on	
4	LFCA4	0	Line 5 (line 11) setting: off	
		1	Line 5 (line 11) setting: on	
3	LFC93	0	Line 4 (line 10) setting: off	
		1	Line 4 (line 10) setting: on	
2	LFC82	0	Line 3 (line 9) setting: off	
		1	Line 3 (line 9) setting: on	
1	LFC71	0	Line 2 (line 8) setting: off	
		1	Line 2 (line 8) setting: on	
0	LFC60	0	Line 1 (line 7) setting: off	
		1	Line 1 (line 7) setting: on	

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

COMMAND62 (Line spacing control setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 6 identification code	
6	—	1	Display control settings	
5	—	1		
4	—	0		
3	—	1	Extended command 2 identification code	
2	—	0		
1	—	0		
0	GRM	0	Normal mode	Continuous mode specification
		1	Continuous mode	

• Second byte

DA0 to 7	Register	Content					Notes
		State	Function				
7	—	0	Second byte identification bit				
6	—	0					
5	BXC1	0	Display outside the character area				Box left/right display specification
		1	Forces display within the character area				In line units
4	GS1	0	GS1	GS0	Mode		In line units
		1	0	0	Normal (character background color)		
3	GS0	0	0	1	Full area and reverse invalid (other than ±1)		
		1	1	0	Transparent 1 (all)		
			1	1	Transparent 2 (other than ±1)		
2	GY2	0	GY2	GY1	GY0	Line spacing	In line units
		1	0	0	0	0	
1	GY1	0	0	0	1	±1	
		1	0	1	0	2	
0	GY0	0	0	1	1	3	
		1	1	0	0	4	
			1	0	1	5	
			1	1	0	6	
			1	1	1	7	

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

COMMAND63 (Line spacing control - line specification setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 6 identification code	
6	—	1	Display control settings	
5	—	1		
4	—	0		
3	—	1	Extended command 3 identification code	
2	—	1		
1	—	0		
0	LGYUD	0	Lower lines (0 to 5 (hexadecimal))	Line spacing control - line specification
		1	Upper lines (6 to B (hexadecimal))	

• Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	LGYB5	0	Line 6 (line 12) setting: off	Line setting for line spacing control The values in parentheses apply when LGYUD is 1.
		1	Line 6 (line 12) setting: on	
4	LGYA4	0	Line 5 (line 11) setting: off	
		1	Line 5 (line 11) setting: on	
3	LGY93	0	Line 4 (line 10) setting: off	
		1	Line 4 (line 10) setting: on	
2	LGY82	0	Line 3 (line 9) setting: off	
		1	Line 3 (line 9) setting: on	
1	LGY71	0	Line 2 (line 8) setting: off	
		1	Line 2 (line 8) setting: on	
0	LGY60	0	Line 1 (line 7) setting: off	
		1	Line 1 (line 7) setting: on	

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

COMMAND70 (Display control setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 7 identification code	
6	—	1	Display control settings	
5	—	1		
4	—	1		
3	—	0	Extended command 0 identification code	
2	—	0		
1	—	0		
0	LRM	0	Normal mode	Continuous mode specification
		1	Continuous mode	

• Second byte

DA0 to 7	Register	Content					Notes
		State	Function				
7	—	0	Second byte identification bit				
6	—	0					
5	BKLC1	0	BKLC1	BKLC0			Character color and character background color: black level specification In line units
		1	0	0	NO1	BK1	
4	BKLC0	0	0	1	NO2	BK2	
		1	1	0	NO3	BK3	
3	CHLC1	0	CHLC1	CHLC0			Character color and character background color: white level specification In line units
		1	0	0	NO1	CHA1	
2	CHLC0	0	0	1	NO2	CHA2	
		1	1	0	NO3	CHA3	
1	RSLC2	0	RSLC1	RSLC0			Character color and character background color: color level specification In line units
		1	0	0	NO1	RS1	
0	RSLC1	0	0	1	NO2	RS2	
		1	1	0	NO3	RS3	

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

COMMAND71 (Display levels - line specification setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 7 identification code	
6	—	1	Display control settings	
5	—	1		
4	—	1		
3	—	0	Extended command 1 identification code	
2	—	1		
1	—	0		
0	LCLUD	0	Lower lines (0 to 5 (hexadecimal))	Display levels - line specification
		1	Upper lines (6 to B (hexadecimal))	

• Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	LCLB5	0	Line 6 (line 12) setting: off	Display level line setting The values in parentheses apply when LCLUD is 1.
		1	Line 6 (line 12) setting: on	
4	LCLA4	0	Line 5 (line 11) setting: off	
		1	Line 5 (line 11) setting: on	
3	LCL93	0	Line 4 (line 10) setting: off	
		1	Line 4 (line 10) setting: on	
2	LCL82	0	Line 3 (line 9) setting: off	
		1	Line 3 (line 9) setting: on	
1	LCL71	0	Line 2 (line 8) setting: off	
		1	Line 2 (line 8) setting: on	
0	LCL60	0	Line 1 (line 7) setting: off	
		1	Line 1 (line 7) setting: on	

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

COMMAND72 (Halftone - line specification setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 7 identification code	
6	—	1	Display control setup	
5	—	1		
4	—	1		
3	—	1	Extended command 2 identification code	
2	—	0		
1	LHTDAT	0	Halftone: off	Halftone control
		1	Halftone: on	
0	LHTUD	0	Lower lines (0 to 5 (hexadecimal))	Halftone line specification
		1	Upper lines (6 to B (hexadecimal))	

• Second byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	LHTB5	0	Line 6 (line 12) setting: off	Halftone line setting The values in parentheses apply when LHTUD is 1.
		1	Line 6 (line 12) setting: on	
4	LHTA4	0	Line 5 (line 11) setting: off	
		1	Line 5 (line 11) setting: on	
3	LHT93	0	Line 4 (line 10) setting: off	
		1	Line 4 (line 10) setting: on	
2	LHT82	0	Line 3 (line 9) setting: off	
		1	Line 3 (line 9) setting: on	
1	LHT71	0	Line 2 (line 8) setting: off	
		1	Line 2 (line 8) setting: on	
0	LHT60	0	Line 1 (line 7) setting: off	
		1	Line 1 (line 7) setting: on	

Note that all registers are set to 0 when these ICs are reset by the $\overline{\text{RST}}$ pin.

COMMAND73 (RGB control setup command)

• First byte

DA0 to 7	Register	Content		Notes
		State	Function	
7	—	1	Command 7 identification code	
6	—	1	Display control setup	
5	—	1		
4	—	1		
3	—	1	Extended command 3 identification code	
2	—	1		
1	—	0		
0	—	0		

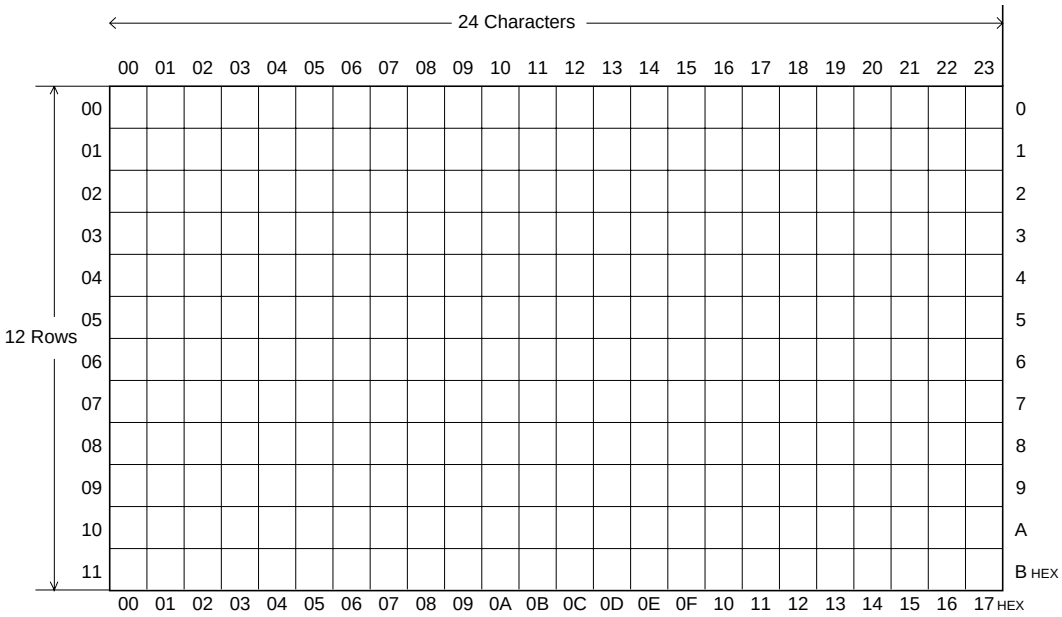
• Second byte

DA0 to 7	Register	Content				Notes
		State	Function			
7	—	0	Second byte identification bit			
6	DASSS	0	Normal			Switches the XTALIN amplifier input
		1	CLKD = CLKX			Only valid when RGB output is specified.
5	GBSEL	0	Background color: off			Switches the background color in RGB output mode
		1	Background color: on			The background color is specified by COM4 second byte.
4	OUTSEL	0				Switches the P9 to P12 outputs
		1	RGB output switching			The logical OR with the OUTMOD input.
3	HSPSW	0	Internal Sync separator used			Switches the SYNin input
		1	Internal Sync separator not used			The logical OR with the OUTMOD input.
2	XONSS	0	Operation depends on the CTRL1 pin			Enables or disables the feedback resistor for the XTALIN clock.
		1	Feedback resistor disconnected			
1	BLK02	0	BLK01	BLK00		Switches the BLKout output
		1	0	0	CHA + BK + CHAB	Box is always on.
0	BLK01	0	0	1	CHA +BK only	Always on when GBSEL = 1.
		1	1	0	CHA only	
			1	1	BK only	

Display Screen Structure

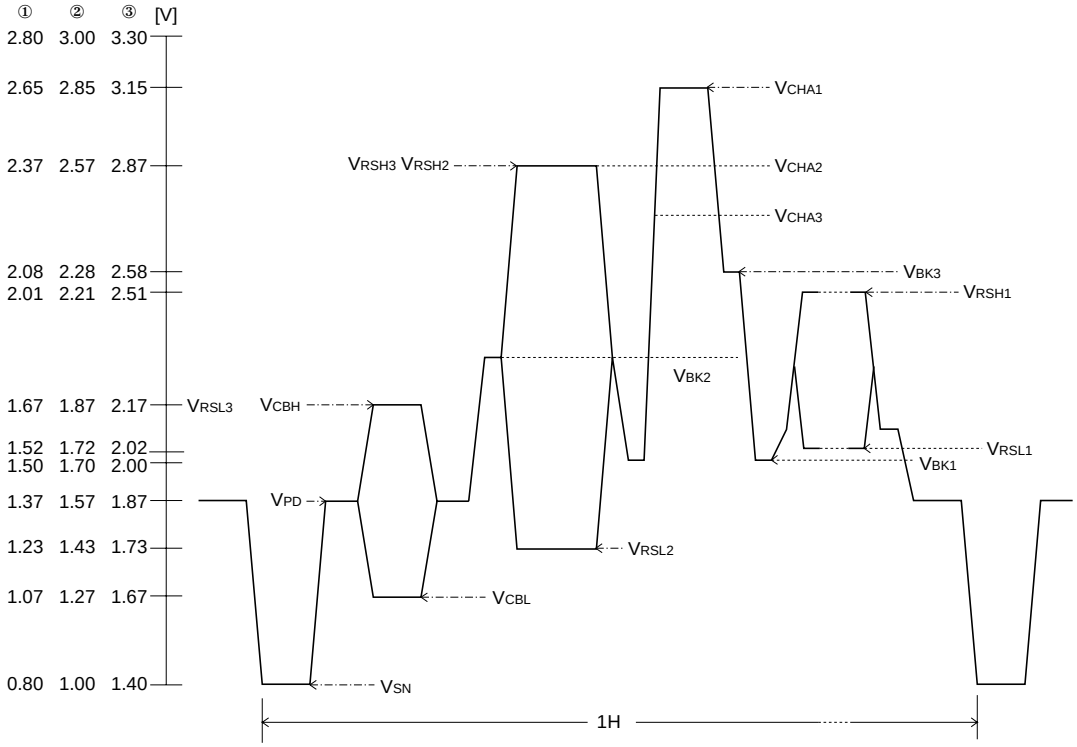
The display consists of 12 lines of 24 characters.
Up to 288 characters can be displayed.
The number of characters that can be displayed is less than the 288 maximum when enlarged characters are displayed.
Display memory addresses are specified as row (0 to 11 decimal) and column (0 to 23 decimal) addresses.

Display Screen Structure (display memory addresses)



Composite Video Signal Output Levels (internally generated levels)

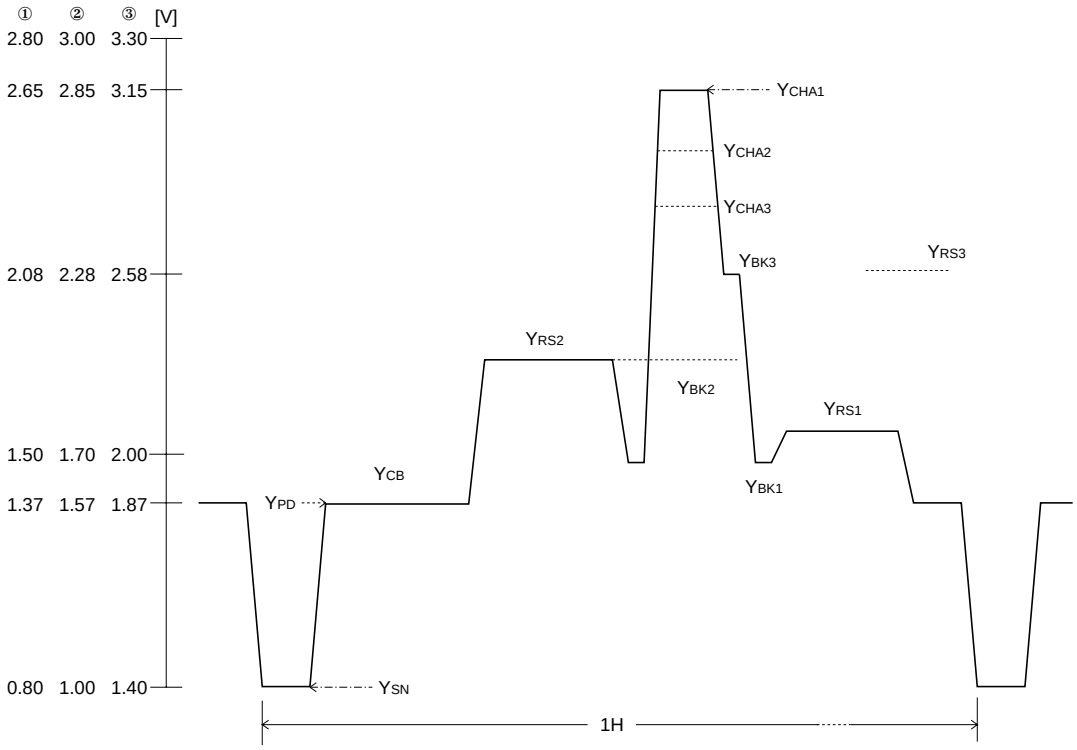
• CVOUT Output Level Waveform ($V_{DD}2$ = 5.00 V)



Output level	Output voltage (1) [V]	Output voltage (2) [V]	Output voltage (3) [V]
V_{CHA1}: Character 1	2.65	2.85	3.25
V_{RSH2}: Background color 2: high	2.37	2.57	2.97
V_{CHA3}: Character 3	2.23	2.43	2.83
V_{BK3}: Outlining: 3	2.08	2.28	2.68
V_{RSH1}: Background color 1: high	2.01	2.21	2.61
V_{BK2}: Outlining: 2	1.80	2.00	2.40
V_{CBH}: Color burst: high	1.67	1.87	2.27
V_{RSL1}: Background color 1: low	1.52	1.72	2.12
V_{BK1}: Outlining: 1	1.50	1.70	2.10
V_{PD}: Pedestal	1.37	1.57	1.97
V_{RSL2}: Background color 2: low	1.23	1.43	1.83
V_{CBL}: Color burst: low	1.07	1.27	1.67
V_{SN}: Sync	0.80	1.00	1.40

BCOL01: RSL1
BCOL0: CBH
BCOL11:RSH1

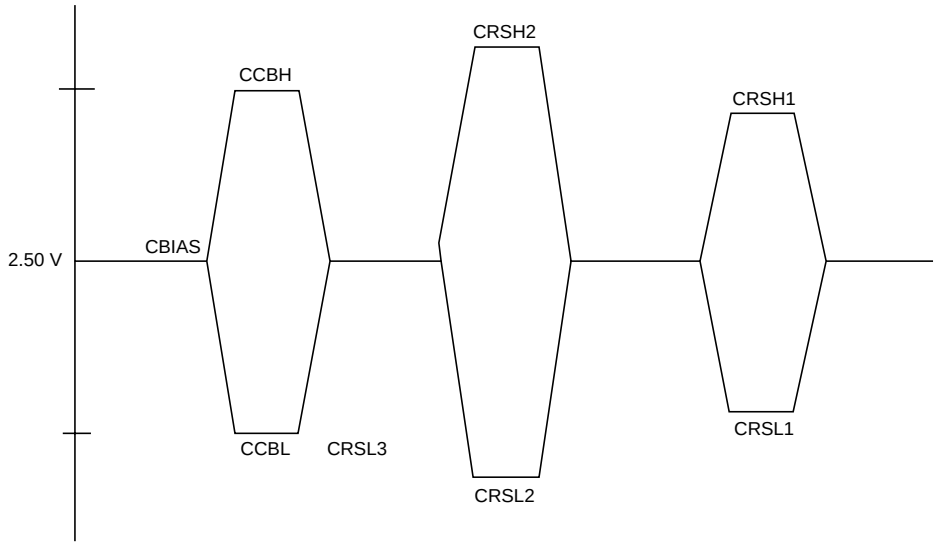
YOUT Output Level Waveform ($V_{DD}2$ = 5.00 V)



Output level	Output voltage (1) [V]	Output voltage (2) [V]	Output voltage (3) [V]
Y_{CHA1}: Character 1	2.65	2.85	3.25
Y_{CHA2}: Character 2	2.37	2.57	2.97
Y_{CHA3}: Character 3	2.23	2.43	2.83
Y_{BK3}: Outlining: 3	2.08	2.28	2.68
Y_{RS3}: Background color 3	2.02	2.22	2.62
Y_{RS2}: Background color 2	1.80	2.00	2.40
Y_{RS1}: Background color 1	1.76	1.96	2.36
Y_{BK1}: Outlining: 1	1.50	1.70	2.10
Y_{CB}: Color burst	1.37	1.57	1.97
Y_{PD}: Pedestal	1.37	1.57	1.97
Y_{SN}: Sync	0.80	1.00	1.40

BCOL01: YBK1
BCOL10: YRS1
BCOL11: YRS3

• COUT Output Level Waveform ($V_{DD}2$ = 5.00 V)

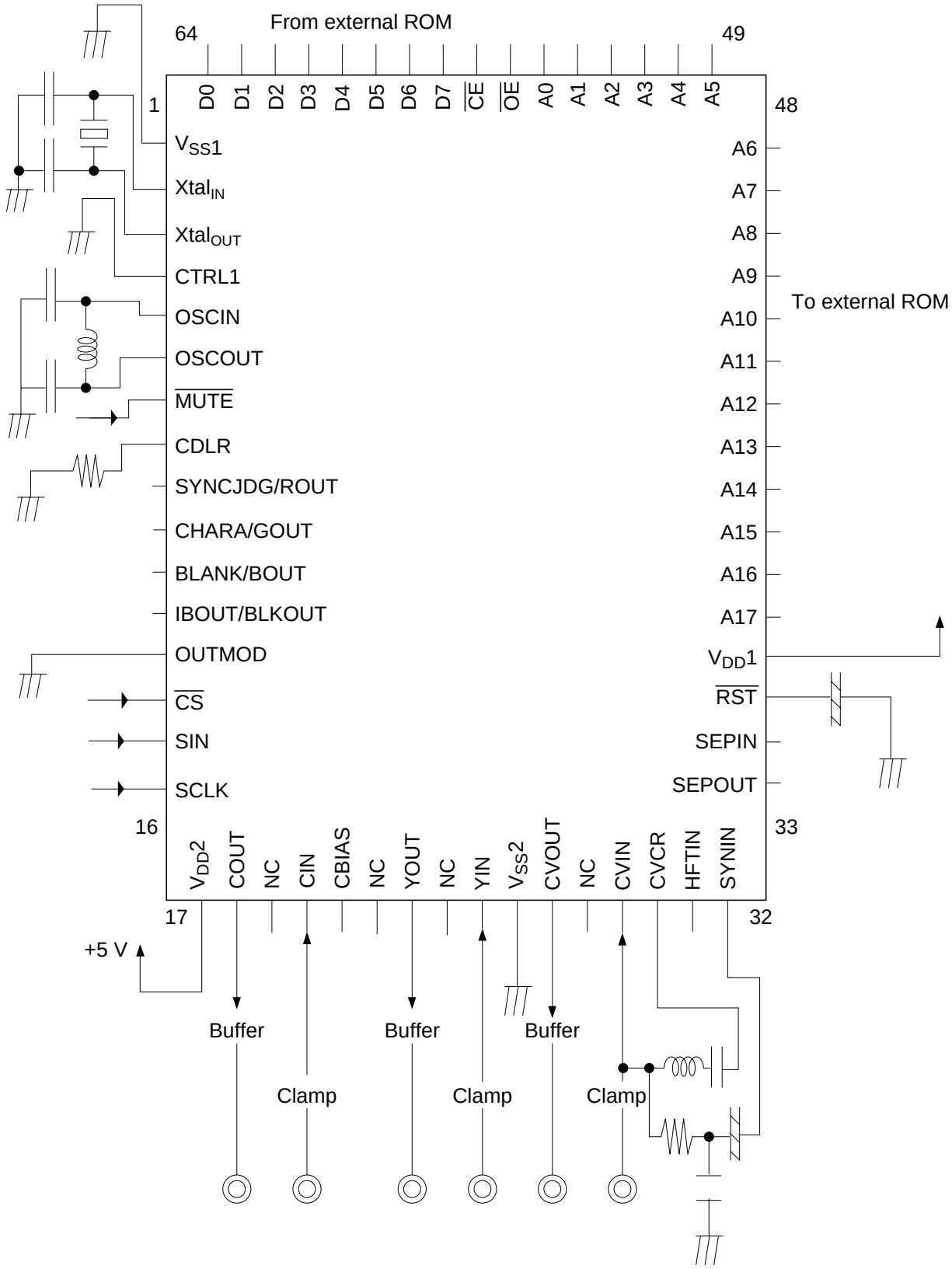


Output level	Output voltage (1) [V]	Output voltage (2) [V]	Output voltage (3) [V]
C_{RSH2}: Background color 2: high	3.07	3.07	3.07
C_{CBH}: Color burst: high	2.80	2.80	2.80
C_{RSH1}: Background color 1: low	2.74	2.74	2.74
C_{BIAS}: Bias	2.50	2.50	2.50
C_{RSL1}: Background color 2: low	2.25	2.25	2.25
C_{CBL}: Color burst: low	2.20	2.20	2.20
C_{RSL2}: Background color 2: low	1.93	1.93	1.93

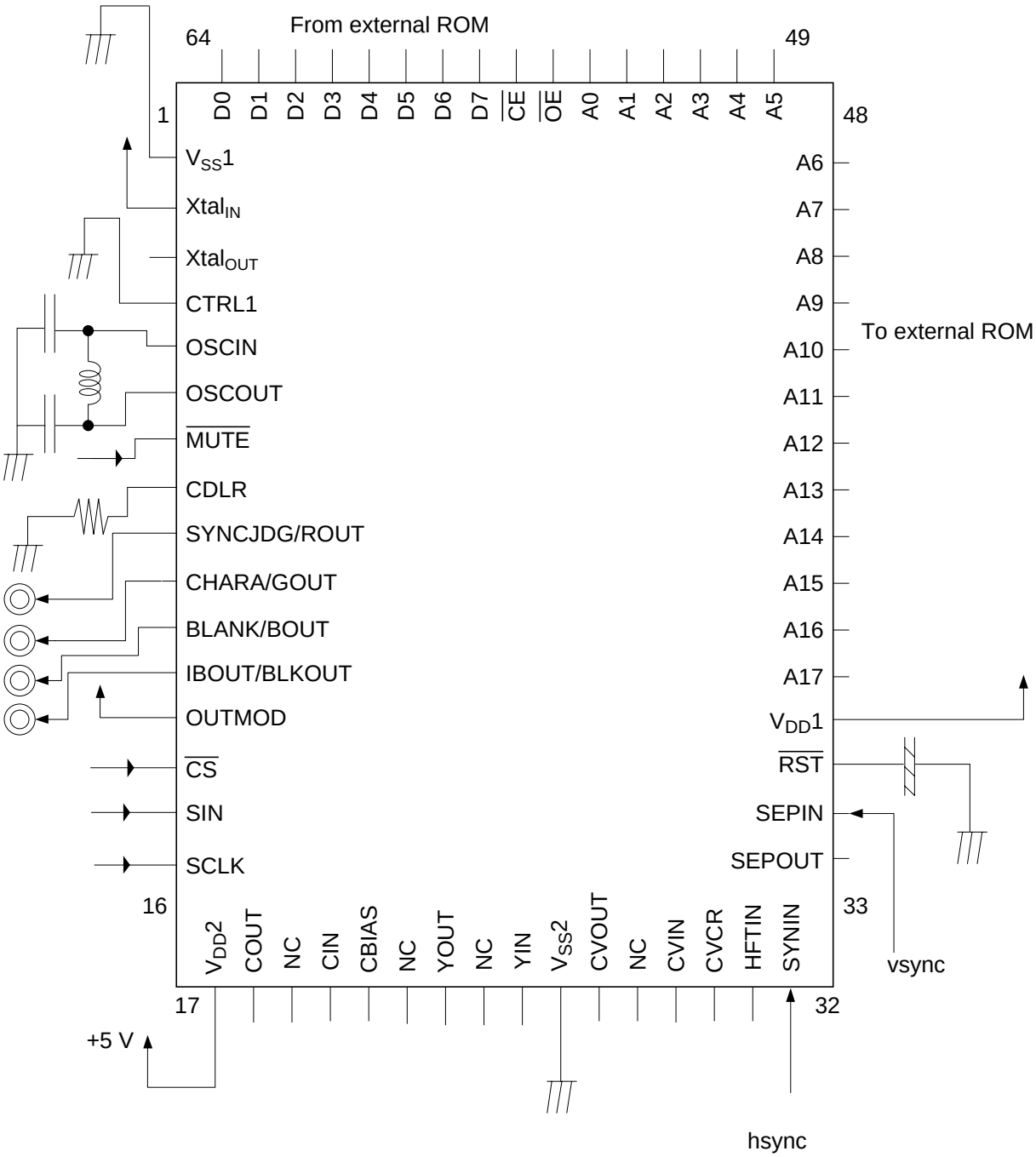
BCOL01, 10, 11: CBIAS

Sample Application Circuit

• Cvideo, Y/C



• RGB


From external ROM
64
49
1
48
D0
D1
D2
D3
D4
D5
D6
D7
CE
OE
A0
A1
A2
A3
A4
A5
VSS1
XtalIN
XtalOUT
CTRL1
OSCIN
OSCOUT
MUTE
CDLR
SYNCJDG/ROUT
CHARA/GOUT
BLANK/BOUT
IBOUT/BLKOUT
OUTMOD
CS
SIN
SCLK
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
VDD1
RST
SEPIN
SEPOUT
To external ROM
16
33
17
32
VDD2
COUT
NC
CIN
CBIAS
NC
YOUT
NC
YIN
VSS2
CVOUT
NC
CVIN
CVCR
HFTIN
SYNIN
+5 V
vsync
hsync