Ordering number : EN*5919

CMOS IC

LC74775, 74775M

On-Screen Display Controller IC

Preliminary

Overview

The LC74775/M is an on-screen display controller CMOS IC that displays characters and patterns on the TV screen under microprocessor control. This IC includes a built-in PDC/VPS/UDT interface circuit.

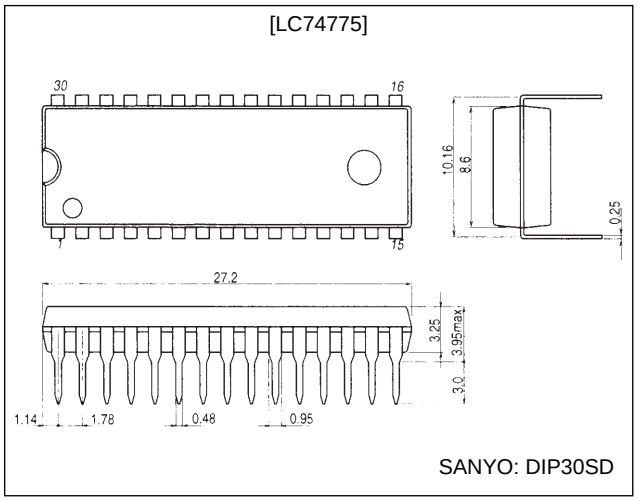
Functions

- Display format: 24 characters by 12 rows (Up to 288 characters)
- Character format: 12 (horizontal) × 18 (vertical) dots
- Character sizes: Three sizes each in the horizontal and vertical directions
- Characters in font: 128 (Of the 128 characters, one is a space character (7E hexadecimal) and one is a transparent space character (7F hexadecimal))
- Initial display positions: 64 horizontal positions and 64 vertical positions
- Blinking: Specifiable in character units
- Blinking types: Two periods supported: 1.0 second and 0.5 second
- Blanking: Over the whole font (12 × 18 dots)
- Background color: 8 colors (internal synchronization mode): $4f_{SC}$ and $2f_{SC}$
  Blue background only: NTSC
- Line background color: Three lines can be set up.
  8 line background colors (in internal synchronization mode): $4f_{SC}$ and $2f_{SC}$
- External control input: 8-bit serial input format
- On-chip sync separator circuit
- Video outputs: PAL and NTSC format composite video outputs
- On-chip PDC/VPS/UDT interface circuit supporting I^2C
- Package: DIP30SD
  MFP30S

Package Dimensions

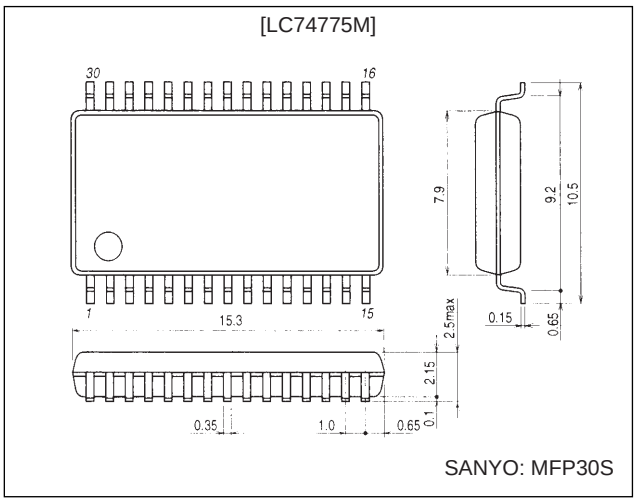
unit: mm

3196-DIP30SD



unit: mm

3216A-MFP30S

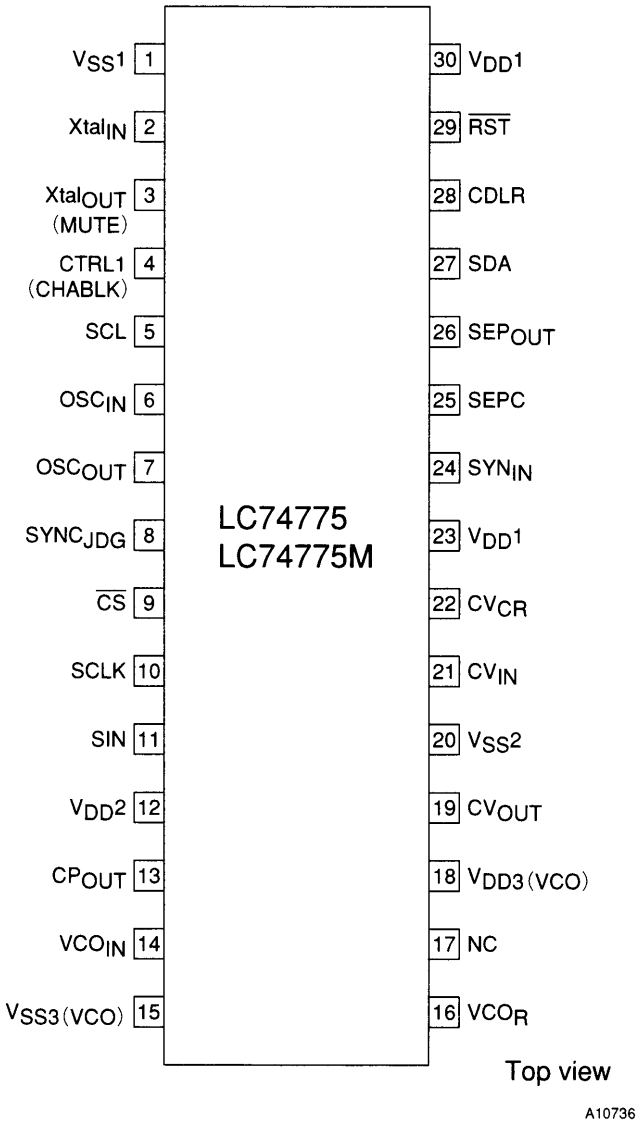


■ Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

■ SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Pin Assignment



Pin Functions

Pin no.	Pin	Function	Notes
1	$V_{SS}1$	Ground	Ground connection (digital system ground)
2	$Xtal_{IN}$	Crystal oscillator (MUTE input)	These pins are used either to connect the crystal and capacitors used to form an external crystal oscillator circuit to generate the internal synchronizing signals, or to input an external clock signal (2fsc or 4fsc). As a mask option, the $Xtal_{OUT}$ pin can be set to function as the MUTE input pin. When this pin is set low, the video output is held at the pedestal level. (A pull-up resistor is built in and the input has hysteresis characteristics.)
3	$Xtal_{OUT}$ (MUTE)		
4	CTRL1 (CHABLK)	Crystal oscillator input switching (CHABLK)	Switches the mode between external clock input and crystal oscillator operation. A low level selects crystal oscillator operation and a high level selects external clock input. As a mask option, the CTRL1 input pin can be set to function as the CHABLK (character . frame) output. This is a 3-value output.
5	SCL	I^2C clock input	Clock input for the PDC/VPS data output. I^2C bus.
6	OSC_{IN}	LC oscillator connections	Connection for the external coil and capacitor for the oscillator used to generate the character output dot clock
7	OSC_{OUT}		
8	$SYNC_{JDC}$	External synchronizing signal judgment output	Outputs the state of the external synchronizing signal presence/absence judgment. Outputs a high level when synchronizing signals are present. Outputs either the crystal oscillator clock if $\overline{CS}$ and $\overline{RST}$ are low, or the VCO clock if $\overline{CS}$ and $\overline{RST}$ are high. (This signal is not output after a command reset.)
9	$\overline{CS}$	Enable input	Enable input for the OSD serial data input. Serial data input is enabled when this pin is low. A pull-up resistor is built in and the input has hysteresis characteristics.
10	SCLK	Clock input	Serial data input enable pin. A pull-up resistor is built in and the input has hysteresis characteristics.
11	SIN	Data input	Serial data input. A pull-up resistor is built in and the input has hysteresis characteristics.
12	$V_{DD}2$	Power supply	Composite video signal level adjustment power supply (analog system power supply)
13	CP_{OUT}	Charge pump output	Charge pump output. Connect a low-pass filter to this pin.
14	VCO_{IN}	Oscillator control voltage input	VCO oscillator control voltage input. (For data slicing)
15	$V_{SS}3$	Ground	Ground (VCO ground)
16	VCO_R	Oscillator range adjustment	VCO oscillator range adjustment resistor connection
17	NC		This pin must either be connected to ground or left open
18	$V_{DD}3$	Power supply (+5 V)	Power supply (+5 V: VCO power supply)
19	CV_{OUT}	Video signal output	Composite video signal output
20	$V_{SS}2$	Ground	Ground (analog system ground)
21	CV_{IN}	Video signal input	Composite video signal input
22	CV_{CR}	Video signal input	SECAM chrominance signal input
23	$V_{DD}1$	Power supply (+5 V)	Power supply (+5 V: digital system power supply)
24	SYN_{IN}	Sync separator circuit input	Video signal input to the internal sync separator circuit
25	SEPC	Slice level output	Slice level verification pin
26	SEP_{OUT}	Composite synchronizing signal output	Internal sync separator circuit composite synchronizing signal output. The signal actually output can be switched by MOD0 and SEL0. The DAV signal is output in the initial state.
27	SDA	I^2C bus data I/O	PDC/VPS data I/O. The I^2C bus write address is [0111 1100]. The I^2C bus read address is [0111 1101].
28	CDLR	Background color phase adjustment	Background color phase adjustment resistor connection
29	$\overline{RST}$	Reset input	System reset input. A pull-up resistor is built in and the input has hysteresis characteristics.
30	$V_{DD}1$	Power supply (+5 V)	Power supply (+5 V: digital system power supply)

Note: *Both $V_{DD}1$ pins must be connected to power.

Absolute Maximum Ratings

Paremeter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD}max	$V_{DD}1$, $V_{DD}2$, and $V_{DD}3$	V_{SS} – 0.3 to V_{SS} + 6.5	V
Maximum input voltage	V_{IN}max	All input pins	V_{SS} – 0.3 to $V_{DD}1$ + 0.3	V
Maximum output voltage	V_{OUT}max	SDA, $SYNC_{JDG}$, and SEP_{OUT}	V_{SS} – 0.3 to $V_{DD}1$ + 0.3	V
Allowable power dissipation	Pd max	Ta = 25°C	350	mW
Operating temperature	Topr		–30 to + 70	°C
Storage temperature	Tstg		–40 to + 125	°C

Allowable Operating Ranges

Paremeter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	$V_{DD}1$, $V_{DD}3$	4.5	5.0	5.5	V
	$V_{DD}2$	$V_{DD}2$	4.5	5.0	6.5	V
Input high-level voltage	$V_{IH}1$	$\overline{CS}$, SIN, SCLK, SDA, SCL,	$0.8V_{DD}1$		5.5	V
	$V_{IH}2$	$\overline{RST}$, MUTE	$0.8V_{DD}1$		$V_{DD}1 + 0.3$	V
	$V_{IH}3$	CTRL1	$0.7V_{DD}1$		$V_{DD}1 + 0.3$	V
Input low-level voltage	$V_{IL}1$	$\overline{RST}$, $\overline{CS}$, SIN, SCLK, SDA, SCL, MUTE	V_{SS} – 0.3		$0.2V_{DD}1$	V
	$V_{IL}2$	CTRL1	V_{SS} – 0.3		$0.3V_{DD}1$	V
Pull-up resistance	R_{PU}	$\overline{RST}$, $\overline{CS}$, SIN, SCLK, MUTE Applies to pins set up by options.	25	50	90	kΩ
Composite video signal input voltage	$V_{IN}1$	CV_{IN}, CV_{CR}: $V_{DD}1$ = 5V		2.0		Vp-p
	$V_{IN}2$	SYN_{IN}: $V_{DD}1$ = 5V	1.5	2.0	2.5	Vp-p
Input voltage	$V_{IN}3$	$Xtal_{IN}$ (when used for external clock input) f_{IN} = 2fsc or 4fsc: $V_{DD}1$= 5V	0.10		5.0	Vp-p
Oscillator frequencies	$f_{OSC}1$	$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (2fsc: PAL)		8.867		MHz
	$f_{OSC}2$	$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (4fsc: PAL)		17.734		MHz
	$f_{OSC}3$	OSC_{IN} and OSC_{OUT} oscillator pins (LC oscillator)	5		10	MHz

Note: Applications must be especially cautious about noise when using the $Xtal_{IN}$ input pin in clock input mode.

Electrical Characteristics at Ta = –30 to +70°C, $V_{DD}1$ = 5 V unless otherwise specified

Paremeter	Symbol	Conditions		Ratings			Unit
				min	typ	max	
Input off leakage current	$I_{leak}1$	CV_{IN}, CV_{CR}				1	µA
Output off leakage current	$I_{leak}2$	CV_{OUT}, SDA				1	µA
Output high-level voltage	$V_{OH}1$	SEP_{OUT}, CP_{OUT}, $SYNC_{JDG}$ $V_{DD}1$ = 4.5V, I_{OH} = –1.0 mA		3.5			V
Output low-level voltage	$V_{OL}1$	SEP_{OUT}, CP_{OUT}, $SYNC_{JDG}$ $V_{DD}1$ = 4.5 V, I_{OL} = 1.0 mA				1.0	V
	$V_{OL}2$	SDA: $V_{DD}1$ = 5.0V, I_{OL} = 3.0 mA				0.4	V
Three-value output voltage	V_O	CHABLK: $V_{DD}1$ = 5.0 V	H	3.3		5.0	V
			M	1.8		2.3	V
			L	0		0.8	V
Input current	I_{IH}	$\overline{RST}$, $\overline{CS}$, SIN, SCLK, SDA, SCL, CTRL1, MUTE, VCOIN: V_{IN} = $V_{DD}1$				1	µA
	I_{IL}	CTRL1, SDA, SCL, VCOIN V_{IN} = $V_{SS}1$		–1			µA
Operating mode current drain	$I_{DD}1$	$V_{DD}1$ and $V_{DD}3$: With all outputs open Xtal: 17.734 MHz, LC: 8 MHz				40	mA
	$I_{DD}2$	$V_{DD}2$: $V_{DD}2$ = 5 V				20	mA
SYNC level	V_{SN}	CV_{OUT}: $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	(1)		0.80		V
			(2)		1.00		V
			(3)		1.40		V
Pedestal level	V_{PD}	CV_{OUT}: $V_{DD}1$ = 5.0 V, $V_{DD}2$ = 5.0 V	(1)		1.37		V
			(2)		1.57		V
			(3)		1.97		V

Continued on next page.

Continued from preceding page.

Paremeter	Symbol	Conditions		Ratings min	Ratings typ	Ratings max	Unit
Color burst low level	V_{CBL}	CV_{OUT}: $V_{DD}1$ = 5.0V, $V_{DD}2$ = 5.0V	(1)		1.07		V
			(2)		1.27		V
			(3)		1.67		V
Color burst high level	V_{CBH}	CV_{OUT}: $V_{DD}1$ = 5.0V, $V_{DD}2$ = 5.0V	(1)		1.67		V
			(2)		1.87		V
			(3)		2.27		V
Background color (other than blue) low level	$V_{RSL}0$	CV_{OUT}: $V_{DD}1$ = 5.0V, $V_{DD}2$ = 5.0V	(1)		1.23		V
			(2)		1.43		V
			(3)		1.83		V
Background color (other than blue) high level	$V_{RSH}0$	CV_{OUT}: $V_{DD}1$ = 5.0V, $V_{DD}2$ = 5.0V	(1)		2.37		V
			(2)		2.57		V
			(3)		2.97		V
Blue background color 1 low level	$V_{RSL}1$	CV_{OUT}: $V_{DD}1$ = 5.0V, $V_{DD}2$ = 5.0V	(1)		1.16		V
			(2)		1.36		V
			(3)		1.76		V
Blue background color 2 low level	$V_{RSL}2$	CV_{OUT}: $V_{DD}1$ = 5.0V, $V_{DD}2$ = 5.0V	(1)		1.52		V
			(2)		1.72		V
			(3)		2.12		V
Blue background color 1 and 2 high level	V_{RSH}	CV_{OUT}: $V_{DD}1$ = 5.0V, $V_{DD}2$ = 5.0V	(1)		2.01		V
			(2)		2.21		V
			(3)		2.61		V
Frame level 0	$V_{BK}0$	CV_{OUT}: $V_{DD}1$ = 5.0V, $V_{DD}2$ = 5.0V	(1)		1.50		V
			(2)		1.70		V
			(3)		2.10		V
Frame level 1	$V_{BK}1$	CV_{OUT}: $V_{DD}1$ = 5.0V, $V_{DD}2$ = 5.0V	(1)		2.08		V
			(2)		2.28		V
			(3)		2.68		V
Character level	V_{CHA}	CV_{OUT}: $V_{DD}1$ = 5.0V, $V_{DD}2$ = 5.0V	(1)		2.65		V
			(2)		2.85		V
			(3)		3.25		V

Notes: (1): When the sync level = 0.8 V
(2): When the sync level = 1.0 V
(3): When the sync level = 1.4 V
The blue background color (1 or 2) is set as an option.

Timing Characteristics at Ta = –30 to +70°C, $V_{DD}1$ = 5 ±0.5 V

• OSD Write (See figure 1.)

Paremeter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	t_W (SCLK)	SCLK	200			ns
	t_W (CS)	$\overline{CS}$ (The period when $\overline{CS}$ is high)	1			µs
Data setup time	t_{SU} (CS)	$\overline{CS}$	200			ns
	t_{SU} (SIN)	SIN	200			ns
Data hold time	t_h (CS)	$\overline{CS}$	2			µs
	t_h (SIN)	SIN	200			ns
One word write time	t_{word}	The 8-bit data write time	4.2			µs
	t_{wt}	The RAM data write time	1			µs

• PDC/VPS Write and Read (I^2C timing)

Paremeter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SCL frequency	f_{SCL}				100	kHz
Bus release time	t_{BUF}		4.7			µs
Start/hold	t_{HD}: STA		4.0			µs
SCL low-level period	t_{LOW}		4.7			µs
SCL high-level period	t_{HIGH}		4.0			µs
Data hold	t_{HD}: DAT		0			µs
Data setup	t_{SU}: DAT		250			ns
Rise time	t_R				1000	ns
Fall time	t_F				300	ns
Stop/setup	t_{SU}: S_{TO}		4.0			µs

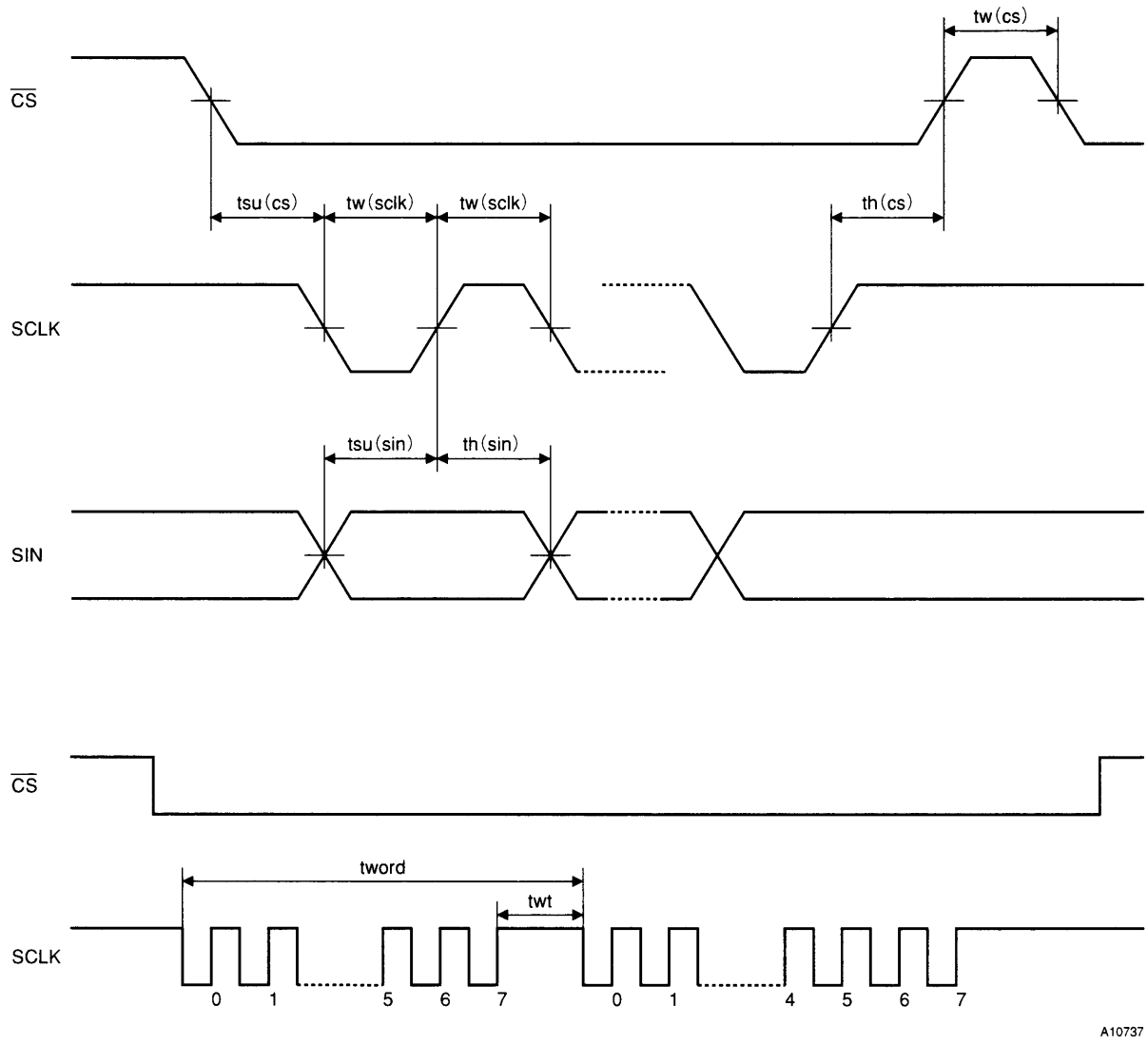


Figure 1 OSD Serial Data Input Timing

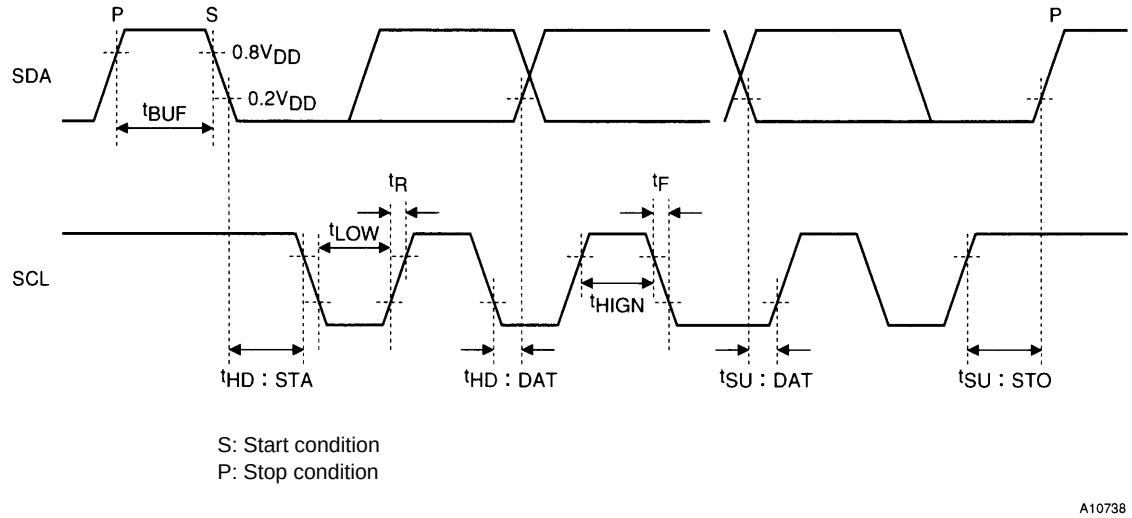
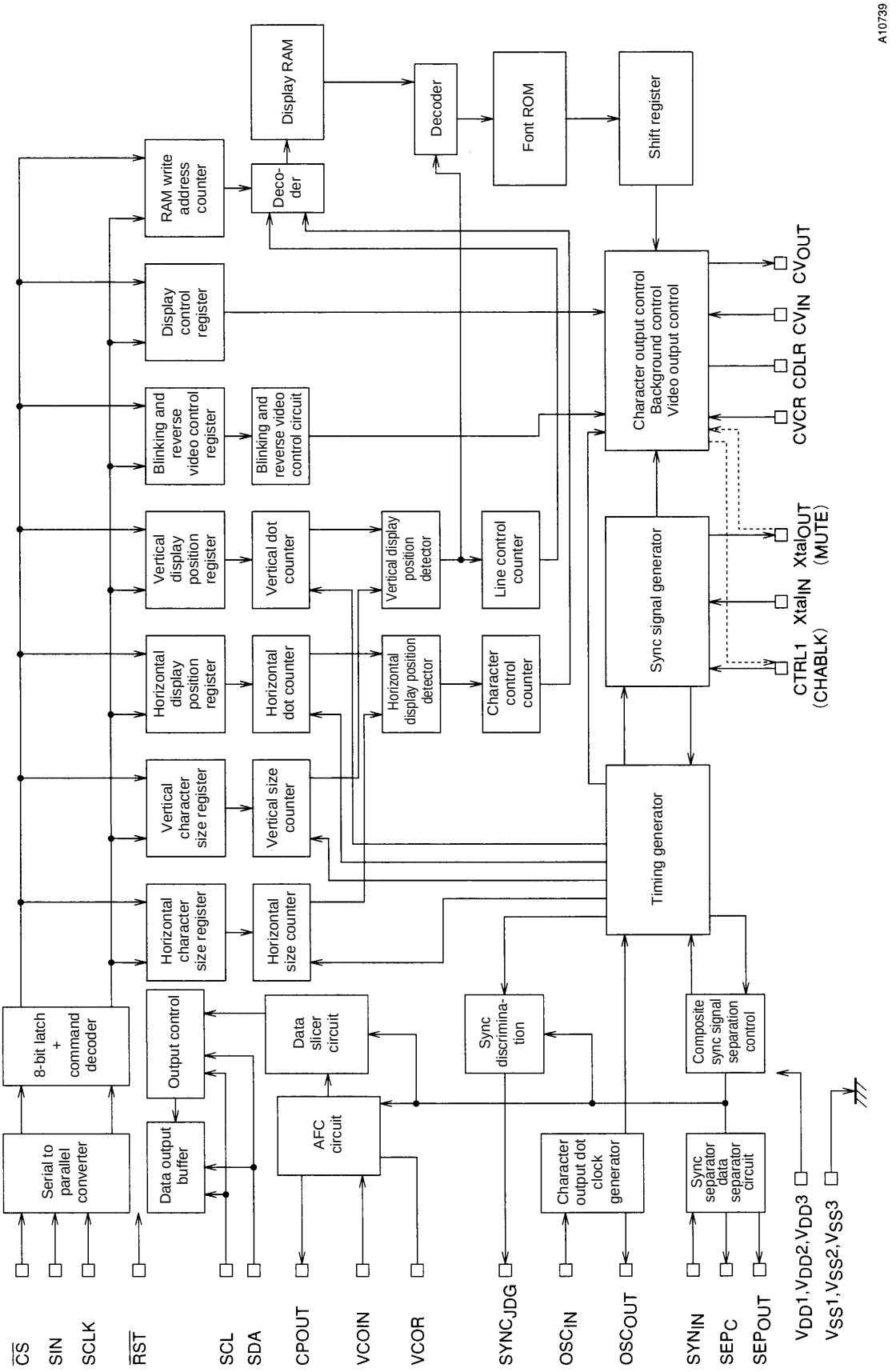


Figure 2 PDC/VPS Serial Timing (I²C bus)

System Block Diagram



Display Control Commands

Display control commands have an 8-bit format and are transferred using the serial input function. Commands consist of a command identification code in the first byte and command data in the following bytes. The following commands are supported.

COMMAND0: Display memory (VRAM) write address setup command
COMMAND1: Display character data write command
COMMAND2: Vertical display start position and vertical character size setup command
COMMAND3: Horizontal display start position and horizontal character size setup command
COMMAND4: Display control setup command
COMMAND5: Display control setup command
COMMAND6: Synchronizing signal detection setup command
COMMAND7 to COMMAND12 and COMMAND18: Display control setup commands
COMMAND13 to COMMAND17: VPS/PDC control commands. These commands can only be written with the I²C bus (the SCL and SDA pins).

Display Control Command Table

Command	First byte								Second byte							
	Command identification code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 (Write address setup)	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 (Character write)	1	0	0	1	0	0	0	0	at	c6	c5	c4	c3	c2	c1	c0
COMMAND2 (Vertical character size and vertical display start position)	1	0	1	0	VS 21	VS 20	VS 11	VS 10	0	FS	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND3 (Horizontal character size and horizontal display start position)	1	0	1	1	HS 21	HS 20	HS 11	HS 10	0	LC	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND4 (Display control)	1	1	0	0	TST MOD	RAM ERS	OSC STP	SYS RST	0	BLK 2	BLK 1	BLK 0	BK 1	BK 0	RV	DSP ON
COMMAND5 (Display control)	1	1	0	1	NP 1	NP 0	NON	INT	0	RSH LV2	HLF INT	BCL	CB	PH 2	PH 1	PH 0
COMMAND6 (Synchronizing signal detection)	1	1	1	0	SEL 0	MOD 0	DIS LIN	MUT	0	RN 2	RN 1	RN 0	SN 3	SN 2	SN 1	SN 0
COMMAND7 (Display control)	1	1	1	1	0	0	0	0	0	CIN SEL	CIN CTL	VNP SEL	VSP SEL	MSK ERS	MSK SEL	EGL
COMMAND8 (Display control)	1	1	1	1	0	0	0	1	0	LNA 3	LNA 2	LNA 1	LNA 0	LPA 2	LPA 1	LPA 0
COMMAND9 (Display control)	1	1	1	1	0	0	1	0	0	LNB 3	LNB 2	LNB 1	LNB 0	LPB 2	LPB 1	LPB 0
COMMAND10 (Display control)	1	1	1	1	0	0	1	1	0	LNC 3	LNC 2	LNC 1	LNC 0	LPC 2	LPC 1	LPC 0
COMMAND11 (Display control)	1	1	1	1	0	1	0	0	0	0	VSP DCK	VSP SLC	LNC SEL	MOD 3	LNB SEL	MOD 2
COMMAND12 (Display control)	1	1	1	1	0	1	0	1	0	0	OTD S1	OTD S0	HLF INT	SEL 2	OTH	IND
COMMAND18 (Display control)	1	1	1	1	1	0	1	1	0	0	RNE 0	SJN 3	SJN 2	SJN 1	SJC 1	SJC 0
COMMAND13 (VPS/PDC control)	1	1	1	1	0	1	0	1	0	CPA 2	CPA 1	CPA 0	VPM 3	VPM 2	VPM 1	VPM 0
COMMAND14 (VPS/PDC control)	1	1	1	1	0	1	1	0	0	VMW SE2	VMW SEL	HBS 2	HBS 1	BMS	EMS	DCE
COMMAND15 (VPS/PDC control)	1	1	1	1	0	1	1	1	0	0	ECV 15	ECV 14	ECV 13	ECV 12	ECV 11	ECV 5
COMMAND16 (VPS/PDC control)	1	1	1	1	1	0	0	0	0	ECP 19	ECP 18	ECP 17	ECP 16	ECP 15	ECP 14	ECP 13
COMMAND17 (VPS/PDC control)	1	1	1	1	1	0	0	1	0	0	ECP 25	ECP 24	ECP 23	ECP 22	ECP 21	ECP 20

Once written, a first byte command identification code is stored until the next first byte is written. However, when the display character data write command (COMMAND1) is written, the LC74775/M locks into the display character data write mode, and another first byte cannot be written.
When the $\overline{CS}$ pin is set high, the LC74775/M is set to the COMMAND0 (display memory write address setup mode) state.

COMMAND0 (Display memory write address setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 0 identification code. Display memory write address setup.	
6	–	0		
5	–	0		
4	–	0		
3	V3	0	Display memory line address (0 to B hexadecimal)	
		1		
2	V2	0		
		1		
1	V1	0		
		1		
0	V0	0		
		1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	–	0		
5	–	0		
4	H4	0	Display memory column address (0 to 17 hexadecimal)	
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0	0		
		1		

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND1 (Display character data write setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 1 identification code. Display character data write mode setup.	When this command is input, the LC74775/M locks in the display character data write mode until the $\overline{\text{CS}}$ pin goes high.
6	–	0		
5	–	0		
4	–	1		
3	–	0		
2	–	0		
1	–	0		
0	–	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	at	0	Character attribute off	
		1	Character attribute on	
6	c6	0	Character code (00 to 7F hexadecimal) ($7E_{HEX}$: Space character) ($7F_{HEX}$: Transparent space character)	
		1		
5	c5	0		
		1		
4	c4	0		
		1		
3	c3	0		
		1		
2	c2	0		
		1		
1	c1	0		
		1		
0	c0	0		
		1		

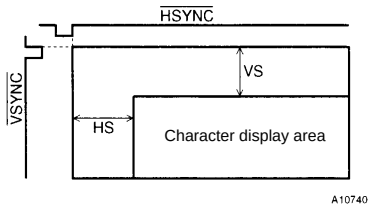
Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{RST}$ pin.

COMMAND2: Vertical display start position and vertical character size setup command

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 2 identification code. Vertical display start position and the vertical character size setup.	
6	–	0		
5	–	1		
4	–	0		
3	VS21	0	VS21 \ VS20: 0 / 1 0: 1H/dot / 2H/dot 1: 3H/dot / 1H/dot	Second line vertical character size
		1		
2	VS20	0		
		1		
1	VS11	0	VS11 \ VS10: 0 / 1 0: 1H/dot / 2H/dot 1: 3H/dot / 1H/dot	First line vertical character size
		1		
0	VS10	0		
		1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	FS	0	Crystal oscillator frequency: 2fsc	
		1	Crystal oscillator frequency: 4fsc	
5	VP5 (MSB)	0	If VS is the vertical display start position then: $VS = \alpha + H \times \left(2 \sum_{n=0}^{5} 2^n VP_n \right)$ H: The horizontal synchronization pulse period α = 20H (525H systems) α = 25H (625H systems)  	The vertical display start position is set by the 6 bits VP0 to VP5. The weight of bit 1 is 2H.
		1		
4	VP4	0		
		1		
3	VP3	0		
		1		
2	VP2	0		
		1		
1	VP1	0		
		1		
0	VP0 (LSB)	0		
		1		

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{RST}$ pin.

COMMAND3 (Horizontal display start position and horizontal size setup command)

• First byte

<table>
<tr><th rowspan="2">DA 0 to 7</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>–</td><td>1</td><td rowspan="4">Command 3 identification code.
Horizontal display start position and the horizontal character size setup.</td><td rowspan="4"></td></tr>
<tr><td>6</td><td>–</td><td>0</td></tr>
<tr><td>5</td><td>–</td><td>1</td></tr>
<tr><td>4</td><td>–</td><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">HS21</td><td>0</td><td rowspan="4"><table><tr><td>VS21 \ VS20</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1Tc/dot</td><td>2Tc/dot</td></tr><tr><td>1</td><td>3Tc/dot</td><td>1Tc/dot</td></tr></table></td><td rowspan="4">Second line horizontal character size</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">HS20</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">HS11</td><td>0</td><td rowspan="4"><table><tr><td>VS11 \ VS10</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1Tc/dot</td><td>2Tc/dot</td></tr><tr><td>1</td><td>3Tc/dot</td><td>1Tc/dot</td></tr></table></td><td rowspan="4">First line horizontal character size</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">HS10</td><td>0</td></tr>
<tr><td>1</td></tr>
</table>

• Second byte

<table>
<tr><th rowspan="2">DA 0 to 7</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>–</td><td>0</td><td>Second byte identification bit</td><td></td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">LC</td><td>0</td><td>Use the LC oscillator as the dot clock</td><td rowspan="2">Selects the dot clock used for character display in the horizontal direction.</td></tr>
<tr><td>1</td><td>Use the crystal oscillator as the dot clock</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">HP5
(MSB)</td><td>0</td><td rowspan="10">If HS is the horizontal start position then:
$HS = Tc \times \left(2 \sum_{n=0}^{5} 2^n HPn\right)$
Tc: Period of the oscillator connected to OSCIN/OSCOUT in operating mode.</td><td rowspan="10">The horizontal display start position is set by the 6 bits HP0 to HP5.
The weight of bit 1 is 2Tc.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">HP4</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">HP3</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">HP2</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">HP1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">HP0
(LSB)</td><td>0</td></tr>
<tr><td>1</td></tr>
</table>

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{RST}$ pin.

COMMAND4 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 4 identification code. Display character data write setup.	
6	–	1		
5	–	0		
4	–	0		
3	TSTMOD	0	Normal operating mode	This bit must be set to 0
		1	Test mode	
2	RAMERS	0		Erasing RAM takes about 500 µs. (This operation must be executed in the DSPOFF state.)
		1	Erase display RAM.(The RAM data is set to 7F hexadecimal.)	
1	OSCSTP	0	Do not stop the crystal and VCO oscillators	Valid in external synchronization mode when character display is off
		1	Stop the crystal and VCO oscillators	
0	SYSRST	0		The registers are reset when the $\overline{CS}$ pin is low, and the reset state is cleared when $\overline{CS}$ is set high.
		1	Reset all registers and turn display off	

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	BLK2	0	Character display area	Specifies the size for complete fill in
		1	Video display area	
5	BLK1	0	BLK1 \ BLK0: 0 = Blanking off; 1 = Character size; 1 = Frame size; 1 = Complete fill in size	Changes the blanking size
		1		
4	BLK0	0		
		1		
3	BK1	0	Blinking period: About 0.5 s	Switches the blinking period
		1	Blinking period: About 1.0 s	
2	BK0	0	Blinking off	Blinking in character reverse video mode switches the display between normal character display and reverse video display
		1	Blinking on	
1	RV	0	Reverse video off	
		1	Reverse video on	
0	DSPON	0	Character display off	
		1	Character display on	

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{RST}$ pin.

COMMAND5 (Display control setup command)

- First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 5 identification code. Display control setup.	
6	–	1		
5	–	0		
4	–	1		
3	NP1	0	NTSC	Switches between NTSC and PAL
		1	PAL	
2	NP0	0	525 lines	Modified by the external input signal V
		1	625 lines	
1	NON	0	Interlaced	Switches between interlaced and noninterlaced video
		1	Noninterlaced	
0	INT	0	External synchronization	Switches between external and internal synchronization
		1	Internal synchronization	

- Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	RSHLV2	0	Background color level 1. (Level that is different from blue.)	Switches the background color signal level
		1	Background color level 2. (Level that is identical to the blue level.)	
5	HLFINT	0	Normal mode	
		1	Partial internal synchronization mode	
4	BCL	0	Background color on	Only valid in internal synchronization mode
		1	No background color. (Only the background level is set.)	
3	CB	0	Color burst signal output	Only valid when BCL is high
		1	Color burst signal output stopped	
2	PH2	0	See table below	Background color specification
		1		
1	PH1	0		
		1		
0	PH0	0		
		1		

PH2	PH1	PH0 (phase)	Background color
0	0	0	Cyan
0	0	1	Yellow
0	1	0	Red
0	1	1	Blue
1	0	0	Cyan - blue
1	0	1	Green
1	1	0	Orange
1	1	1	Magenta

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND6 (Synchronizing signal detection setup command)

• First byte

<table>
<tr><th rowspan="2">DA 0 to 7</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>–</td><td>1</td><td rowspan="4">Command 6 identification code.
Synchronizing signal control setup.</td><td rowspan="4"></td></tr>
<tr><td>6</td><td>–</td><td>1</td></tr>
<tr><td>5</td><td>–</td><td>1</td></tr>
<tr><td>4</td><td>–</td><td>0</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">SEL0</td><td>0</td><td rowspan="5"><table><tr><th>SEL0</th><th>MOD0</th><th>SEPOUT</th></tr><tr><td>0</td><td>0</td><td>DAV</td></tr><tr><td>0</td><td>1</td><td>Sliced data width</td></tr><tr><td>1</td><td>0</td><td>CSYNC</td></tr><tr><td>1</td><td>1</td><td>ST pulse signal</td></tr></table></td><td rowspan="3">Switches the SEP_{OUT} (pin 19) output</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">MOD0</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">DISLIN</td><td>0</td><td>12 lines</td><td rowspan="2">Switches the number of lines displayed</td></tr>
<tr><td>1</td><td>10 lines</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">MUT</td><td>0</td><td>Normal output</td><td rowspan="2">CV_{OUT} switching</td></tr>
<tr><td>1</td><td>CV_{IN} is cut and CV_{OUT} is held at the pedestal level</td></tr>
</table>

• Second byte

<table>
<tr><th rowspan="2">DA 0 to 7</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>–</td><td>0</td><td>Second byte identification bit</td><td></td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">RN2</td><td>0</td><td rowspan="4"><table><tr><th>RN2</th><th>RN1</th><th>RN0</th><th>Number of times HSYNC detected</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0 (32)</td></tr><tr><td>0</td><td>0</td><td>1</td><td>4 (64)</td></tr><tr><td>0</td><td>1</td><td>0</td><td>8 (128)</td></tr><tr><td>1</td><td>0</td><td>0</td><td>16 (256)</td></tr></table></td><td rowspan="4">External synchronizing signal detection control.
Signal absent → signal present transition detection.
Sets the sampling period in which SYNC can be detected continuously in the horizontal synchronizing signal period (1H).
Values in parentheses apply when RNE0 (COM18) is 1.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">RN1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">RN0</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">SN3</td><td>0</td><td rowspan="5"><table><tr><th>SN3</th><th>SN2</th><th>SN1</th><th>SN0</th><th>Number of times HSYNC detected</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Not output</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>32</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>64</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>128</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>256</td></tr></table></td><td rowspan="5">External synchronizing signal detection control.
Signal present → signal absent transition detection.
Sets the sampling period in which SYNC cannot be detected continuously in the horizontal synchronizing signal period (1H).</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">SN2</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">SN1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">SN0</td><td>0</td></tr>
<tr><td>1</td></tr>
</table>

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{RST}$ pin.

COMMAND7 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 7 identification code. Display control setup.	
6	–	1		
5	–	1		
4	–	1		
3	–	0	Extended command 0 identification code	
2	–	0		
1	–	0		
0	–	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7		0	Second byte identification bit	
6	CINSEL	0	Blank area (The logical OR of the character and frame signals)	CV_{CR} on signal switching
		1	Video signal display area	
5	CINCTL	0	CV_{CR}: off	CV_{CR} on/off switching
		1	CV_{CR}: on	
4	VNPSEL	0	V falling edge detection	Switches the V acquisition polarity in external mode when internal V separation is used.
		1	V rising edge detection	
3	VSPSEL	0	VSEP: about 8.9 µs (NTSC)	Switches the internal V separation period
		1	VSEP: about 17.8 µs (NTSC)	
2	MSKERS	0	Mask valid	Clears the HSYNC and VSYNK masks
		1	Mask invalid	
1	MSKSEL	0	3H (NTSC)	Switches the VSYNC mask
		1	20H (NTSC)	
0	EGL	0	Frame level 0 only (VBK0)	Switches the frame level. (Only valid when BLK0 is 0 and BLK1 is 1.)
		1	Two-stage frame level (VBK0 and VBK1)	

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{RST}$ pin.

COMMAND8 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 7 identification code. Display control setup.	
6	–	1		
5	–	1		
4	–	1		
3	–	0	Extended command 1 identification code	
2	–	0		
1	–	0		
0	–	1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	LNA3	0	See table below	Specifies the line whose background is to be changed. (When the background color is specified for the same line with LNA*, LNB*, and LNC*, the command specified last becomes valid. The previously specified registers (LN* and LP*) are all cleared to 0.)
		1		
5	LNA2	0		
		1		
4	LNA1	0		
		1		
3	LNA0	0		
		1		
2	LPA2	0	See table below	Specifies the background color
		1		
1	LPA1	0		
		1		
0	LPA0	0		
		1		

LNA3	LNA2	LNA1	LNA0	Specified line
0	0	0	0	Do not change the line background
0	0	0	1	Line 1
0	0	1	0	Line 2
0	0	1	1	Line 3
0	1	0	0	Line 4
0	1	0	1	Line 5
0	1	1	0	Line 6
0	1	1	1	Line 7
1	0	0	0	Line 8
1	0	0	1	Line 9
1	0	1	0	Line 10
1	0	1	1	Line 11
1	1	–	–	Line 12

LPA2	LPA1	LPA0	Line background color (phase)
0	0	0	Cyan
0	0	1	Yellow
0	1	0	Red
0	1	1	Blue
1	0	0	Cyan - blue
1	0	1	Green
1	1	0	Orange
1	1	1	Magenta

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND9 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 7 identification code. Display control setup.	
6	–	1		
5	–	1		
4	–	1		
3	–	0	Extended command 2 identification code	
2	–	0		
1	–	1		
0	–	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	LNB3	0	See table below	Specifies the line whose background is to be changed. (When the background color is specified for the same line with LNA*, LNB*, and LNC*, the command specified last becomes valid. The previously specified registers (LN* and LP*) are all cleared to 0.)
		1		
5	LNB2	0		
		1		
4	LNB1	0		
		1		
3	LNB0	0		
		1		
2	LPB2	0	See table below	Specifies the background color
		1		
1	LPB1	0		
		1		
0	LPB0	0		
		1		

LNB3	LNB2	LNB1	LNB0	Specified line
0	0	0	0	Do not change the line background
0	0	0	1	Line 1
0	0	1	0	Line 2
0	0	1	1	Line 3
0	1	0	0	Line 4
0	1	0	1	Line 5
0	1	1	0	Line 6
0	1	1	1	Line 7
1	0	0	0	Line 8
1	0	0	1	Line 9
1	0	1	0	Line 10
1	0	1	1	Line 11
1	1	–	–	Line 12

LPC2	LPC1	LPC0	Line background color (phase)
0	0	0	Cyan
0	0	1	Yellow
0	1	0	Red
0	1	1	Blue
1	0	0	Cyan - blue
1	0	1	Green
1	1	0	Orange
1	1	1	Magenta

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND10 (Display control setup command)

- First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 7 identification code. Display control setup.	
6	–	1		
5	–	1		
4	–	1		
3	–	0	Extended command 3 identification code	
2	–	0		
1	–	1		
0	–	1		

- Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	LNC3	0	See table below	Specifies the line whose background is to be changed. (When the background color is specified for the same line with LNA*, LNB*, and LNC*, the command specified last becomes valid. The previously specified registers (LN* and LP*) are all cleared to 0.)
		1		
5	LNC2	0		
		1		
4	LNC1	0		
		1		
3	LNC0	0		
		1		
2	LPC2	0	See table below	Specifies the background color
		1		
1	LPC1	0		
		1		
0	LPC0	0		
		1		

LNB3	LNB2	LNB1	LNB0	Specified line
0	0	0	0	Do not change the line background
0	0	0	1	Line 1
0	0	1	0	Line 2
0	0	1	1	Line 3
0	1	0	0	Line 4
0	1	0	1	Line 5
0	1	1	0	Line 6
0	1	1	1	Line 7
1	0	0	0	Line 8
1	0	0	1	Line 9
1	0	1	0	Line 10
1	0	1	1	Line 11
1	1	–	–	Line 12

LPB2	LPB1	LPB0	Line background color (phase)
0	0	0	Cyan
0	0	1	Yellow
0	1	0	Red
0	1	1	Blue
1	0	0	Cyan - blue
1	0	1	Green
1	1	0	Orange
1	1	1	Magenta

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND11 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 7 identification code. Display control setup.	
6	–	1		
5	–	1		
4	–	1		
3	–	0	Extended command 4 identification code	
2	–	1		
1	–	0		
0	–	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	–	0		
5	VSPDCK	0	LC oscillator: operating	LC oscillator control
		1	LC oscillator: stopped	
4	VSPSLC	0	VCO: operating	VCO control
		1	VCO: stopped	
3	LNCSEL	0	Normal line background color operation	Switches the RV mode background color for RV specified characters in LNC* specified lines
		1	RV characters have the background color specified by PH* and the RV character background color is white	
2	MOD3	0	The LNCSEL = 1 setting specifications	Valid when LNCSEL is high
		1	RV characters have the background color specified by PH* and characters are white	
1	LNBSEL	0	Normal line background color operation	Switches the RV mode background color for RV specified characters in LNB* specified lines
		1	RV characters have the background color specified by PH* and the RV character background color is white	
0	MOD2	0	The LNBSEL = 1 setting specifications	Valid when LNBSEL is high
		1	RV characters have the background color specified by PH* and characters are white	

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND12 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 7 identification code. Display control setup.	
6	–	1		
5	–	1		
4	–	1		
3	–	0	Extended command 5 identification code	
2	–	1		
1	–	0		
0	–	1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	–	0		
5	OTDCS1	0	OTDS1 = 0, OTDS0 = 0: LC oscillator OTDS1 = 0, OTDS0 = 1: Crystal oscillator OTDS1 = 1, OTDS0 = 0: VCO	External synchronization mode dot clock setting
		1		
4	OTDCS0	0		
		1		
3	HLFTON	0	SEL2 = 0, HLFTON = 0: $SYNC_{JDG}$ SEL2 = 0, HLFTON = 1: Halftone SEL2 = 1, HLFTON = 0: LOCK SEL2 = 1, HLFTON = 1: SYNCDET	$SYNC_{JDG}$ pin (pin 8) output switching. The halftone output line specification depends on background color specification (the logical OR of the 3-line specification).
		1		
2	SEL2	0		
		1		
1	OTHS	0	CSYNCB (sync separator)	External synchronization mode H input switching
		1	HDB (slicer AFC)	
0	IND3	0	LC oscillator	Internal synchronization mode dot clock setup
		1	Crystal oscillator	

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{RST}$ pin.

COMMAND18 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 7 identification code. Display control setup.	
6	–	1		
5	–	1		
4	–	1		
3	–	1	Extended command B identification code	
2	–	0		
1	–	1		
0	–	1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	–	0		
5	RNE0	0	Sync discrimination signal absent → present: normal value	Changes the discrimination value for the sync discrimination signal absent → present transition
		1	Sync discrimination signal absent → present: value shown in parentheses	
4	SJNS3	0	SJNS3 / SJNS2 / SJNS1 / Number of times 0 / 0 / 0 / None 0 / 0 / 1 / 4 0 / 1 / 0 / 8 0 / 1 / 1 / 16 1 / 0 / 0 / 32 1 / 0 / 1 / 64 1 / 1 / 0 / 128 1 / 1 / 1 / 256	Setting for the noise rejection circuit used for sync discrimination signal absent → present transition. The sync signal absent state is recognized when the number of high-level signals shown in the table is input during a 1H period.
		1		
3	SJNS2	0		
		1		
2	SJNS1	0		
		1		
1	SJCS1	0	SJCS1 / SJCS0 / PAL / NTSC 0 / 0 / 677 ns (1/3) / 558 ns (1/2) 0 / 1 / 903 ns (1/4) / 838 ns (1/3) 1 / 0 / 450 ns (1/2) / 1117 ns (1/4)	Sync discrimination. HSYNI signal extraction clock selection.
		1		
0	SJCS0	0		
		1		

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND13 (VPS/PDC control setup command) I^2C bus only

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 7 identification code. Display control setup.	
6	–	1		
5	–	1		
4	–	1		
3	–	0	Extended command 5 identification code	
2	–	1		
1	–	0		
0	–	1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	CPA2	0	CPA2 CPA1 CPA0 Clock 0 0 0 No. 1 0 0 1 No. 2 0 1 0 No. 3 0 1 1 No. 4 1 0 0 No. 5 1 0 1 No. 6 1 1 0 No. 7 1 1 1 No. 8	Data acquisition clock selection. Shifts in multiples of 8 clock units with respect to the data.
		1		
5	CPA1	0		
		1		
4	CPA0	0		
		1		
3	VPM3	0	M3 M2 M1 M0 Operating mode 0 0 0 0 VPS 0 0 0 1 8/30/2 (PDC) 0 0 1 0 Automatic PDC/VPS discrimination 1 0 0 1 1 8/30/1 (UDT) 0 1 0 0 Header time 1 0 1 0 1 Header time 2 0 1 1 0 Header time 3 0 1 1 1 Header time 4 1 0 0 0 Status display 1 1 0 0 1 Status display 2 1 0 1 0 Status display 3 1 0 1 1 Status display 4 1 1 0 0 PAL Pulse 1 1 0 1 Automatic PDC/VPS discrimination 2 1 1 1 0 Automatic PDC/VPS discrimination 3 1 1 1 1 Automatic PDC/VPS discrimination 4	Slicer mode selection
		1		
2	VPM2	0		
		1		
1	VPM1	0		
		1		
0	VPM0	0		
		1		

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{RST}$ pin.

COMMAND14 (VPS/PDC control setup command) I²C bus only

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 7 identification code. Display control setup.	
6	–	1		
5	–	1		
4	–	1		
3	–	0	Extended command 6 identification code	
2	–	1		
1	–	1		
0	–	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	VMWSE2	0	V mask period start - From the retrace period	CPOUT pin (pin 13) V mask period switching 2
		1	V mask period start - From 10H before the retrace period	
5	VMWSEL	0	The V mask period is the retrace period	CPOUT pin (pin 13) V mask period switching
		1	The V mask period is 9H	
4	HBS2	0	Clock running discrimination 1 (2 times)	Clock running discrimination count setting
		1	Clock running discrimination 2 (4 times)	
3	HBS1	0	Framing code discrimination 1	Framing code discrimination selection
		1	Framing code discrimination 2 (Single bad bits are ignored)	
2	BMS	0	Error check valid (Error checking can be turned on or off on a per-byte basis.)	When set to 0, if there are no errors in bytes for which error checking is turned on, those bytes are written to P-S. When set to 1, all bytes are written to P-S regardless of the error status.
		1	Error check invalid (Applications can select whether data for which an error is detected is held or writing on a per-byte basis.)	
1	EMS	0	Data hold	Specifies handling of bytes for which error checking is set to off but in which an error occurred when error checking is turned on
		1	Data write (When the error bit is 0 in VPS mode.)	
0	DCE	0	Error checking enabled for unused data bytes. VPS: bytes 3, 4, and 6 to 10, PDC: bytes 7 to 12, header 1: bytes 14 to 37, header 2: bytes 14 to 29, header 3: bytes 14 to 21, status 1 (3): bytes 7 to 25, status 2 (4): bytes 7 to 35	Error checking setting for unused data bytes. Biphase (VPS), Hamming (PDC), and odd parity (header)
		1	Error checking disabled for unused data bytes. VPS: bytes 3, 4, and 6 to 10, PDC: bytes 7 to 12, header 1: bytes 14 to 37, header 2: bytes 14 to 29, header 3: bytes 14 to 21, status 1 (3): bytes 7 to 25, status 2 (4): bytes 7 to 35	

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND15 (VPS/PDC control setup command) I²C bus only

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 7 identification code. Display control setup.	
6	–	1		
5	–	1		
4	–	1		
3	–	0	Extended command 7 identification code	
2	–	1		
1	–	1		
0	–	1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	–	0		
5	ECV15	0	Byte 15 biphase error check on (Data hold)	Specification when the VPS data BMS bit is 0. The item in parentheses is the specification when the VPS data BMS bit is 1.
		1	Byte 15 biphase error check off (Data write)	
4	ECV14	0	Byte 14 biphase error check on (Data hold)	
		1	Byte 14 biphase error check off (Data write)	
3	ECV13	0	Byte 13 biphase error check on (Data hold)	
		1	Byte 13 biphase error check off (Data write)	
2	ECV12	0	Byte 12 biphase error check on (Data hold)	
		1	Byte 12 biphase error check off (Data write)	
1	ECV11	0	Byte 11 biphase error check on (Data hold)	
		1	Byte 11 biphase error check off (Data write)	
0	ECV5	0	Byte 5 biphase error check on (Data hold)	
		1	Byte 5 biphase error check off (Data write)	

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND16 (VPS/PDC control setup command) I²C bus only

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 7 identification code. Display control setup.	
6	–	1		
5	–	1		
4	–	1		
3	–	1	Extended command 8 identification code	
2	–	0		
1	–	0		
0	–	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	ECP19	0	Byte 19 Hamming error check on (Data hold) {Bytes 44, 28, 36, 20, 32, 42, 32, and 42}	Specification when the PDC data BMS bit is 0. The item in parentheses is the specification when the BMS bit is 1. The item in curly braces lists the odd parity check on/off bytes for header modes 1, 2, 3, and 4 and status mode 1, 2, 3, and 4.
		1	Byte 19 Hamming error check off (Data write) {Bytes 44, 28, 36, 20, 32, 42, 32, and 42}	
5	ECP18	0	Byte 18 Hamming error check on (Data hold) {Bytes 43, 27, 35, 19, 31, 41, 31, and 41}	
		1	Byte 18 Hamming error check off (Data write) {Bytes 43, 27, 35, 19, 31, 41, 31, and 41}	
4	ECP17	0	Byte 17 Hamming error check on (Data hold) {Bytes 42, 26, 34, 18, 30, 40, 30, and 40}	
		1	Byte 17 Hamming error check off (Data write) {Bytes 42, 26, 34, 18, 30, 40, 30, and 40}	
3	ECP16	0	Byte 16 Hamming error check on (Data hold) {Bytes 41, 25, 33, 17, 29, 39, 29, and 39}	
		1	Byte 16 Hamming error check off (Data write) {Bytes 41, 25, 33, 17, 29, 39, 29, and 39}	
2	ECP15	0	Byte 15 Hamming error check on (Data hold) {Bytes 40, 24, 32, 16, 28, 38, 28, and 38}	
		1	Byte 15 Hamming error check off (Data write) {Bytes 40, 24, 32, 16, 28, 38, 28, and 38}	
1	ECP14	0	Byte 14 Hamming error check on (Data hold) {Bytes 39, 23, 31, 15, 27, 37, 27, and 37}	
		1	Byte 14 Hamming error check off (Data write) {Bytes 39, 23, 31, 15, 27, 37, 27, and 37}	
0	ECP13	0	Byte 13 Hamming error check on (Data hold) {Bytes 38, 22, 30, 14, 26, 36, 26, and 36}	
		1	Byte 13 Hamming error check off (Data write) {Bytes 38, 22, 30, 14, 26, 36, 26, and 36}	

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{\text{RST}}$ pin.

COMMAND17 (VPS/PDC control setup command) I²C bus only

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	1	Command 7 identification code. Display control setup.	
6	–	1		
5	–	1		
4	–	1		
3	–	1	Extended command 9 identification code	
2	–	0		
1	–	0		
0	–	1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	–	0	Second byte identification bit	
6	–	0		
5	ECP25	0	Byte 25 Hamming error check on (Data hold)	Specification when the PDC data BMS bit is 0. The item in parentheses is the specification when the BMS bit is 1. The item in curly braces lists the odd parity check on/off bytes for header modes 1, 2, 3, and 4 and status mode 1, 2, 3, and 4.
		1	Byte 25 Hamming error check off (Data write)	
4	ECP24	0	Byte 24 Hamming error check on (Data hold)	
		1	Byte 24 Hamming error check off (Data write)	
3	ECP23	0	Byte 23 Hamming error check on (Data hold)	
		1	Byte 23 Hamming error check off (Data write)	
2	ECP22	0	Byte 22 Hamming error check on (Data hold) {Bytes , , , , 35, 45, 35, and 45}	
		1	Byte 22 Hamming error check off (Data write) {Bytes , , , , 35, 45, 35, and 45}	
1	ECP21	0	Byte 21 Hamming error check on (Data hold) {Bytes , , , , 34, 44, 34, and 44}	
		1	Byte 21 Hamming error check off (Data write) {Bytes , , , , 34, 44, 34, and 44}	
0	ECP20	0	Byte 20 Hamming error check on (Data hold) {Bytes 45, 29, 37, 21, 33, 43, 33, and 43}	
		1	Byte 20 Hamming error check off (Data write) {Bytes 45, 29, 37, 21, 33, 43, 33, and 43}	

Note: All registers are set to 0 when the LC74775/M is reset by the $\overline{\text{RST}}$ pin.

PDC/VPS Output Data Format

Data is output in order starting with bit 7 of byte 1.

Output data		PDC 8/30 mode				VPS mode		Header time mode 1 (3)		Header time mode 2 (4)	
		Format 1		Format 2							
Byte 1	Bit 7	byte 15	bit 0	byte 16	bit 0	byte 11	bit 0	byte 38	bit 0	byte 22	bit 0
	6		1		1		1	(30)	1	(14)	1
	5		2		2		2		2		2
	4		3		3		3		3		3
	3		4	byte17	bit 0		4		4		4
	2		5		1		5		5		5
	1		6		2		6		6		6
	0		7		3		7		7		7
Byte 2	Bit 7	byte 16	bit 0	byte 18	bit 0	byte 12	bit 0	byte 39	bit 0	byte 23	bit 0
	6		1		1		1	(31)	1	(15)	1
	5		2		2		2		2		2
	4		3		3		3		3		3
	3		4	byte19	bit 0		4		4		4
	2		5		1		5		5		5
	1		6		2		6		6		6
	0		7		3		7		7		7
Byte 3	Bit 7	byte 17	bit 0	byte 20	bit 0	byte 13	bit 0	byte 40	bit 0	byte 24	bit 0
	6		1		1		1	(32)	1	(16)	1
	5		2		2		2		2		2
	4		3		3		3		3		3
	3		4	byte 21	bit 0		4		4		4
	2		5		1		5		5		5
	1		6		2		6		6		6
	0		7		3		7		7		7
Byte 4	Bit 7	byte 18	bit 0	byte 22	bit 0	byte 14	bit 0	byte 41	bit 0	byte 25	bit 0
	6		1		1		1	(33)	1	(17)	1
	5		2		2		2		2		2
	4		3		3		3		3		3
	3		4	byte 23	bit 0		4		4		4
	2		5		1		5		5		5
	1		6		2		6		6		6
	0		7		3		7		7		7
Byte 5	Bit 7	byte 19	bit 0	byte 14	bit 0	byte 5	bit 0	byte 42	bit 0	byte 26	bit 0
	6		1		1		1	(34)	1	(18)	1
	5		2		2		2		2		2
	4		3		3		3		3		3
	3		4	byte 15	bit 0		4		4		4
	2		5		1		5		5		5
	1		6		2		6		6		6
	0		7		3		7		7		7
Byte 6	Bit 7	byte 20	bit 0	byte 24	bit 0	byte 15	bit 0	byte 43	bit 0	byte 27	bit 0
	6		1		1		1	(35)	1	(19)	1
	5		2		2		2		2		2
	4		3		3		3		3		3
	3		4	byte 25	bit 0		4		4		4
	2		5		1		5		5		5
	1		6		2		6		6		6
	0		7		3		7		7		7

Continued on next page.

Continued from preceding page.

Output data		PDC 8/30 mode				VPS mode		Header time mode 1 (3)		Header time mode 2 (4)	
		Format 1		Format 2							
Byte 7	Bit 7	byte 21	bit 0	byte 13	bit 0	1		byte 44	bit 0	byte 28	bit 0
	6		1		1	1		(36)	1	(20)	1
	5		2		2	1			2		2
	4		3		3	1			3		3
	3		4	1		1			4		4
	2		5	1		1			5		5
	1		6	1		1			6		6
	0		7	1		0			7		7
Byte 8	Bit 7	byte 13	bit 0	Error information 1	byte 16	Error information	byte 11	byte 45	bit 0	byte 29	bit 0
	6		1		17		12	(37)	1	(21)	1
	5		2		18		13		2		2
	4		3		19		14		3		3
	3		4		20		5		4		4
	2		5		21		15		5		5
	1		6		22	0			6		6
	0		7		23	0			7		7
Byte 9	Bit 7	byte 14	bit 0	Error information 2	14			Error information	byte 38 (30)	Error information	byte 22 (14)
	6		1		15				39 (31)		23 (15)
	5		2		24				40 (32)		24 (16)
	4		3		25				41 (33)		25 (17)
	3		4		13				42 (34)		26 (18)
	2		5	0					43 (35)		27 (19)
	1		6	0					44 (36)		28 (20)
	0		7	0					45 (37)		29 (21)
Byte 10	Bit 7	byte 22	bit 0								
	6		1								
	5		2								
	4		3								
	3		4								
	2		5								
	1		6								
	0		7								
Byte 11	Bit 7	byte 23	bit 0								
	6		1								
	5		2								
	4		3								
	3		4								
	2		5								
	1		6								
	0		7								
Byte 12	Bit 7	byte 24	bit 0								
	6		1								
	5		2								
	4		3								
	3		4								
	2		5								
	1		6								
	0		7								
Byte 13	Bit 7	byte 25	bit 0								
	6		1								
	5		2								
	4		3								
	3		4								
	2		5								
	1		6								
	0		7								

Note: A value of 1 is output for section with no output data setting.

Data is output in order starting with bit 7 of byte 1.

Status display 1 and 2: 8/30/2 - Status display 1 and 2: 8/30/1

Output data		Status display mode 1 (3)		Status display mode 2 (4)		PAL Puls
Byte 1	Bit 7	byte 26	bit 0	byte 36	bit 0	bit 0
	6	(26)	1	(36)	1	1
	5		2		2	2
	4		3		3	3
	3		4		4	4
	2		5		5	5
	1		6		6	6
	0		7		7	7
Byte 2	Bit 7	byte 27	bit 0	byte 37	bit 0	bit 8
	6	(27)	1	(37)	1	9
	5		2		2	10
	4		3		3	11
	3		4		4	12
	2		5		5	13
	1		6		6	0
	0		7		7	0
Byte 3	Bit 7	byte 28	bit 0	byte 38	bit 0	
	6	(28)	1	(38)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 4	Bit 7	byte 29	bit 0	byte 39	bit 0	
	6	(29)	1	(39)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 5	Bit 7	byte 30	bit 0	byte 39	bit 0	
	6	(30)	1	(40)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 6	Bit 7	byte 31	bit 0	byte 41	bit 0	
	6	(31)	1	(41)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 7	Bit 7	byte 32	bit 0	byte 42	bit 0	
	6	(32)	1	(42)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	

Continued on next page.

Continued from preceding page.

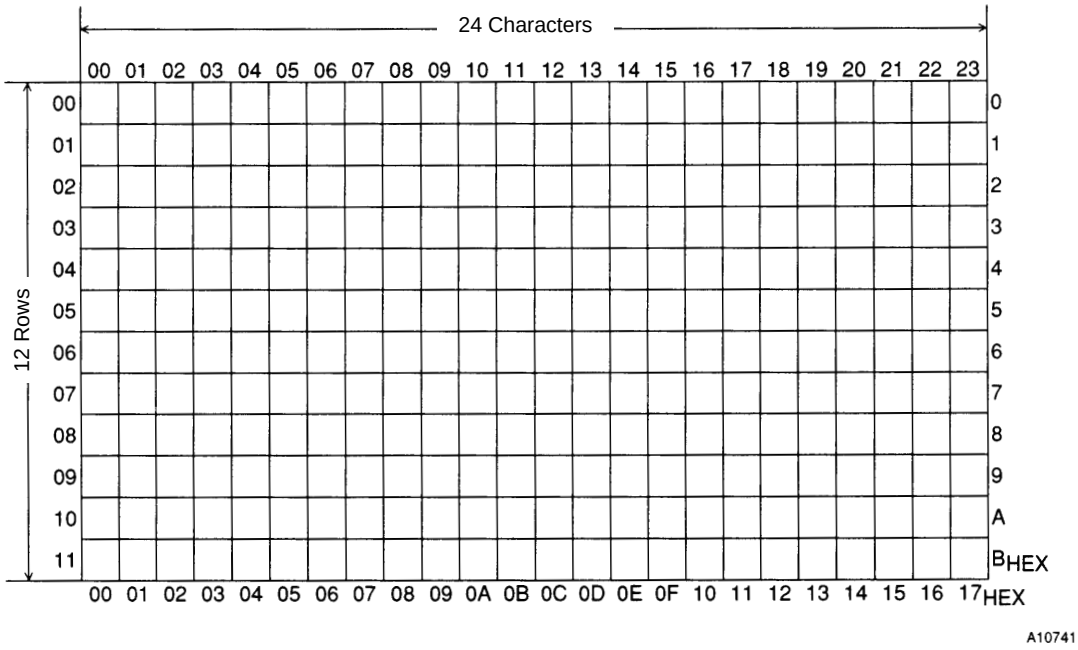
Output data		Status display mode 1 (3)		Status display mode 2 (4)		PAL Puls
Byte 8	Bit 7	byte 33	bit 0	byte 43	bit 0	
	6	(33)	1	(43)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 9	Bit 7	byte 34	bit 0	byte 44	bit 0	
	6	(34)	1	(44)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 10	Bit 7	byte 35	bit 0	byte 45	bit 0	
	6	(35)	1	(45)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte 11	Bit 7	Error information 1	byte 26 (26)	Error information 1	byte 36 (36)	
	6		27 (27)		37 (37)	
	5		28 (28)		38 (38)	
	4		29 (29)		39 (39)	
	3		30 (30)		40 (40)	
	2		31 (31)		41 (41)	
	1		32 (32)		42 (42)	
	0		33 (33)		43 (43)	
Byte 12	Bit 7	Error information 2	byte 34 (34)	Error information 1	byte 44 (44)	
	6		35 (35)		45 (45)	
	5		0		0	
	4		0		0	
	3		0		0	
	2		0		0	
	1		0		0	
	0		0		0	
Byte 13	Bit 7					
	6					
	5					
	4					
	3					
	2					
	1					
	0					

Note: A value of 1 is output for section with no output data setting.

Display Screen Structure

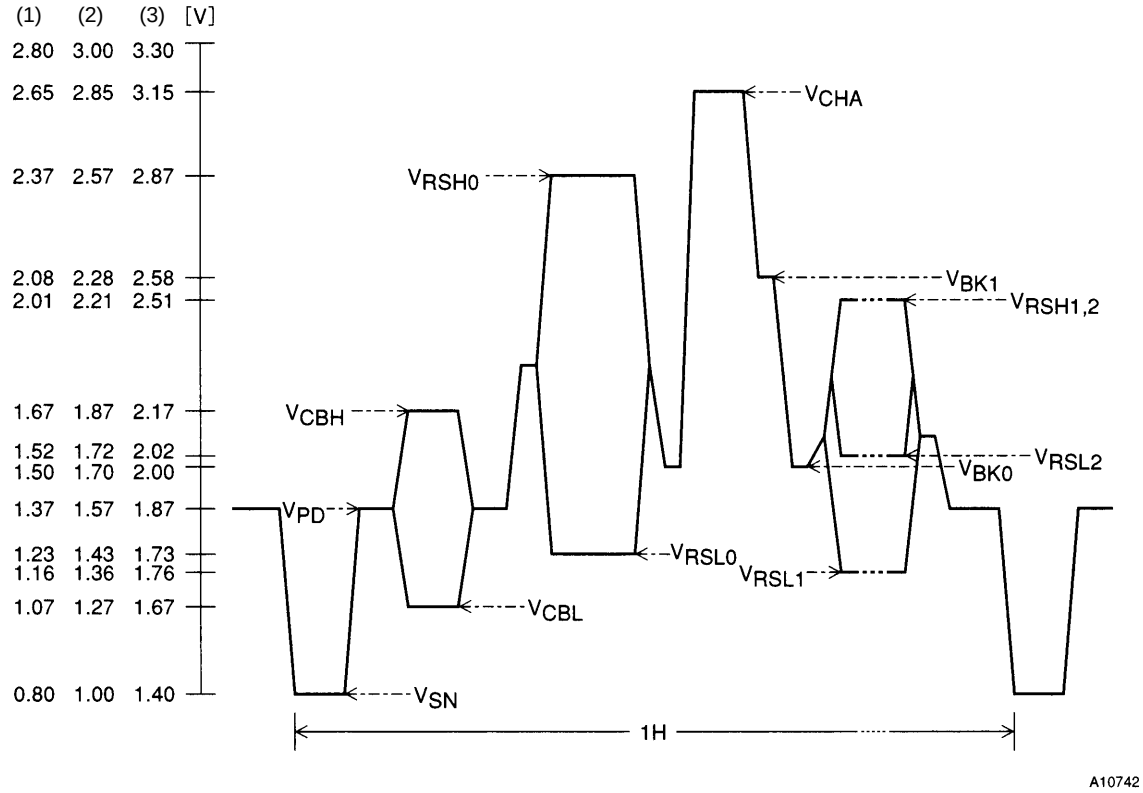
The display consists of 12 lines of 24 characters.
Up to 288 characters can be displayed.
The number of characters that can be displayed is reduced from the 288 maximum when enlarged characters are displayed.
Display memory addresses are specified as row (0 to 11 decimal) and column (0 to 23 decimal) addresses.

Display Screen Structure (display memory addresses)



Composite Video Signal Output Levels (internally generated levels)

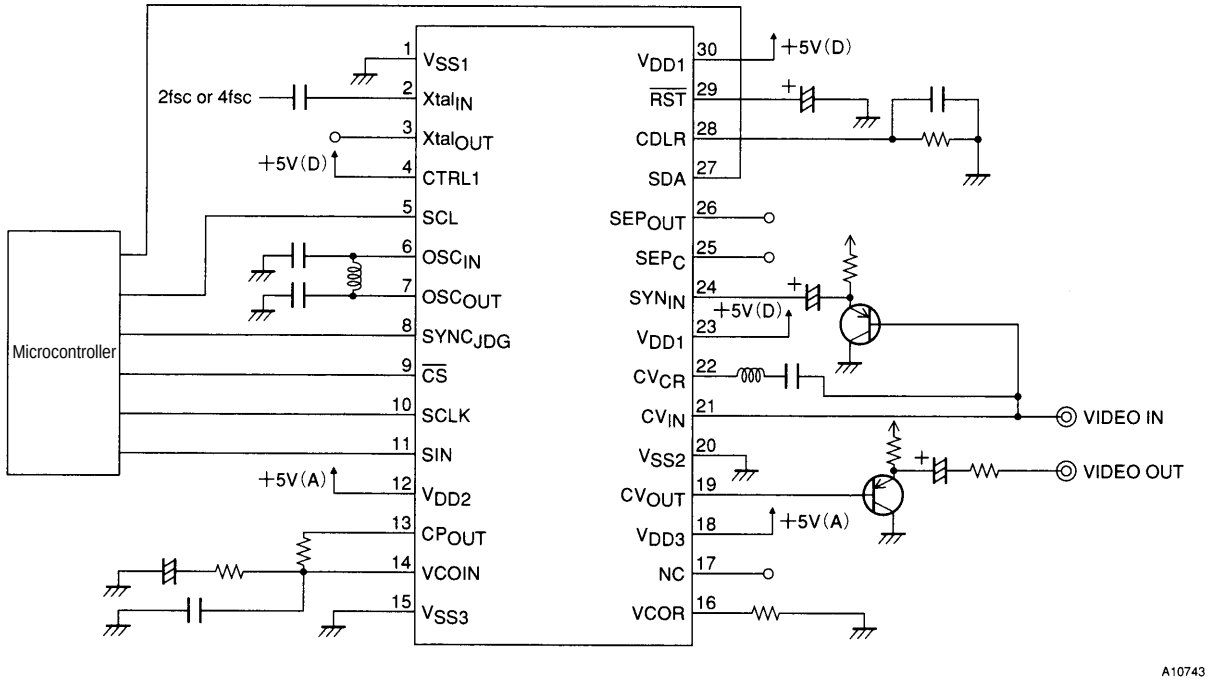
CV_{OUT} output level waveform ($V_{DD}2$ = 5.00 V)



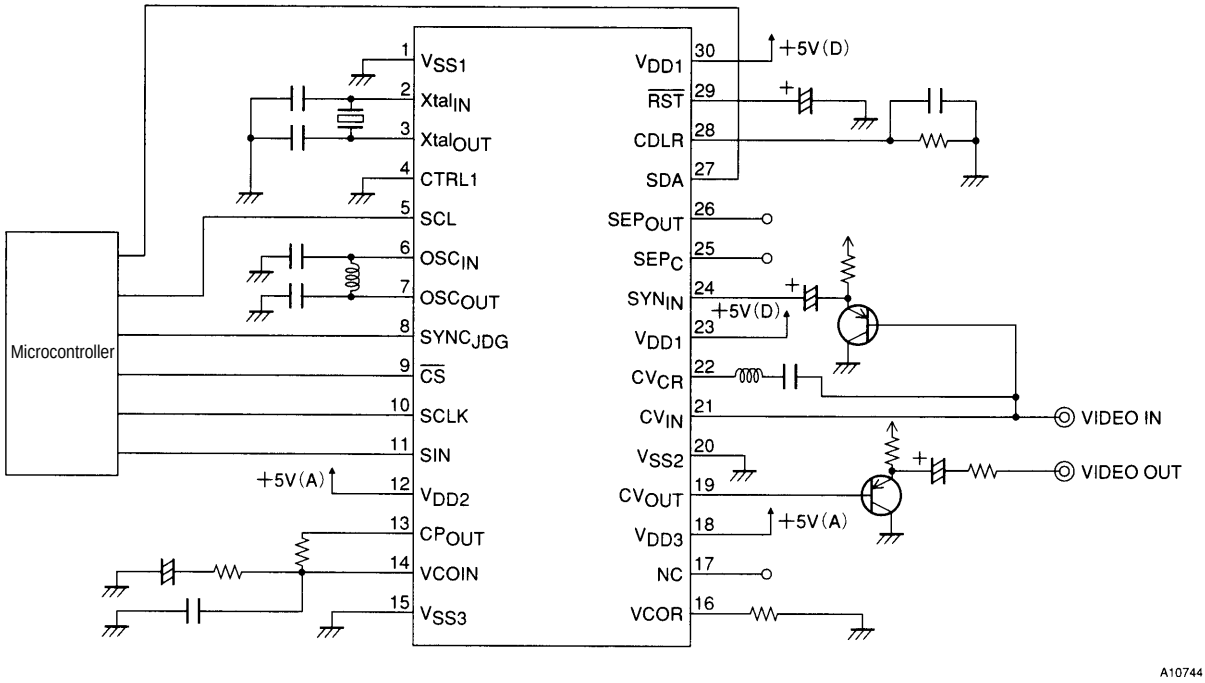
Output level		Output voltage (1) [V]	Output voltage (2) [V]	Output voltage (3) [V]
V_{CHA}	: Character	2.65	2.85	3.25
V_{RSH0}	: Background colors other than blue: high	2.37	2.57	2.97
$V_{RSH1, 2}$	: Blue background colors 1 and 2: high	2.01	2.21	2.61
V_{CBH}	: Color burst high	1.67	1.87	2.27
V_{RSL0}	: Background colors other than blue: low	1.23	1.43	1.83
V_{RSL1}	: Blue background color 1: low	1.16	1.36	1.76
V_{RSL2}	: Blue background color 2: low	1.52	1.72	2.12
V_{BK1}	: Frame 1	2.08	2.28	2.68
V_{BK0}	: Frame 2	1.50	1.70	2.10
V_{PD}	: Pedestal	1.37	1.57	1.97
V_{CBL}	: Color burst low	1.07	1.27	1.67
V_{SN}	: Sync	0.80	1.00	1.40

Application Circuit Examples (When used connected to a single-chip Y/C circuit)

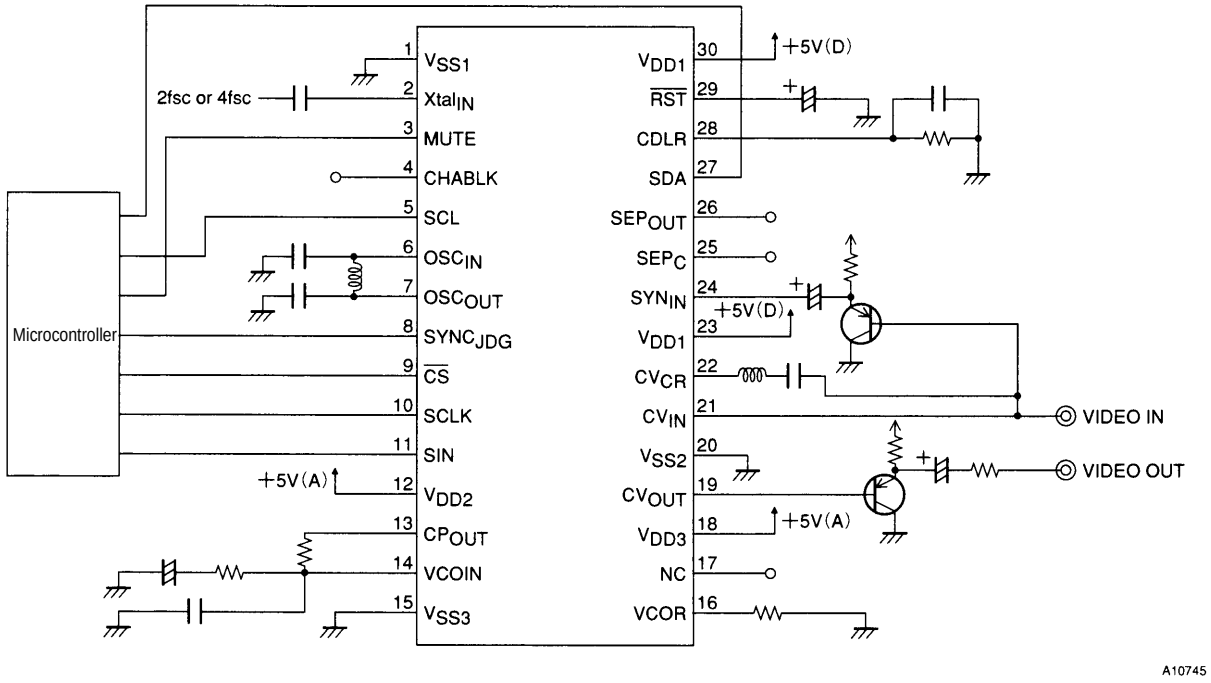
• External system clock input



• Crystal oscillator



• External system clock input (with pins 3 and 4 modified in the mask options)



The electrolytic capacitor connected to SYNIN must be connected with the correct polarity when a sync tip level of 1.4 VDC (CVIN input signal: sync tip = 1.4 V) is selected in the options for video signals generated with internal synchronization.

When $V_{DD}1$ is 5.0 V, the SYNIN input video signal pedestal level will be clamped to about 2.5 V.

■ Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

■ SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

■ In the event that any and all SANYO products described or contained herein fall under strategic products (including services) controlled under the Foreign Exchange and Foreign Trade Control Law of Japan, such products must not be exported without obtaining export license from the Ministry of International Trade and Industry in accordance with the above law.

■ No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.

■ Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.

■ Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of Nobemver, 1998. Specifications and information herein are subject to change without notice.