No.1890

LC7520

C MOS IC

GRAPHIC EQUALIZER VOLUME CONTROLLER FOR HOME STEREO, MUSIC CENTER USE

The 3-chip configuration consisting of the LC7520, a controller (LC7060 or general-purpose microcomputer LC6502), and a display LSI (LC7560 LCD, LC7565 FLT, LED) provides an electronic graphic equalizer system having the following features.

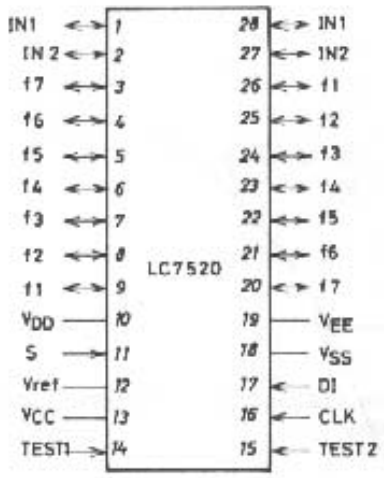
Functions

- On-chip electronic volume control for graphic equalizer with 7 bands each of right/left.
- 2dB/step variable in each band.
- Maximum boost of +10dB, maximum cut of -10dB, and 11 positions in each band.
- Setting can be made separately for right/left band.
- Band setting is made by serial data input. There are 2 control lines.
- Wide dynamic range.
- CMOS LSI of 40V breakdown voltage.

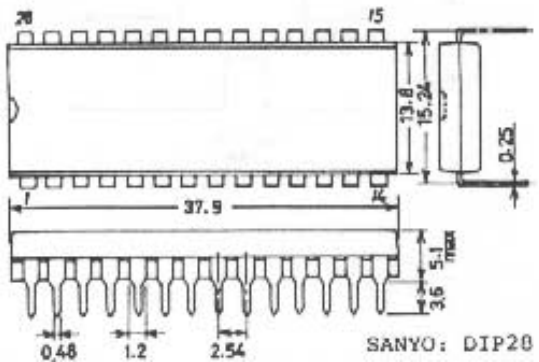
Features

- The gain in each band can be increased/decreased with one touch.
- Since the preset memory contents can be called with one touch, your desired frequency characteristic to the music can be selected.
  (Example) User option 2 modes + Maker option 3 modes + Last channel memory
- '0dB in each band (flat function)', 'The frequency characteristic in each band is reversed with respect to 0dB (reverse function).' - These functions can be software-controlled with one touch.
- Spectrum analyzing display facilitates recording equalization.
- Since 2 control lines can be also used for a display LSI, wiring between microcomputer and LSI is facilitated.

Pin Assignment



Case Outline 3012A-D28IC
(unit:mm)



SANYO: DIP28

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

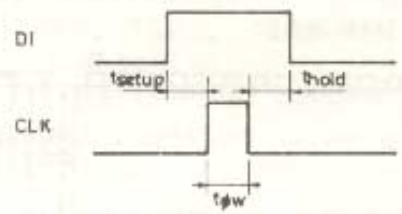
					unit
Maximum Supply Voltage	V_{DD}max	V_{DD}	$V_{EE} \leqq V_{SS}$	$V_{DD}-V_{EE} \leqq 40$	V
	V_{EE}max	V_{EE}			
	V_{ref}	V_{ref}	$V_{SS} \leqq Vref$	$V_{DD}-Vref \leqq 11$	V
	V_{CC}max	V_{CC}		V_{SS} to $V_{SS}+7$	V
Maximum Input Voltage	V_{I1}max	CLK,DI		$V_{SS}-0.3$ to $V_{CC}+0.3$	V
	V_{I2}max	f1 to f7,IN1,2		$V_{EE}-0.3$ to $V_{DD}+0.3$	V
	V_{I3}max	S,TEST1,2		Vref-0.3 to $V_{DD}+0.3$	V
Allowable Power Dissipation	Pdmax		Ta≦75°C	150	mW
Operating Temperature	Topg			-30 to +75	°C
Storage Temperature	Tstg			-40 to +125	°C

Allowable Operating Conditions at Ta=25°C, V_{SS}=0V

					unit
Supply Voltage	V_{DD}	V_{DD}	$V_{EE} \leqq V_{SS}$	$8 \leqq V_{DD}-V_{EE} \leqq 37$	V
	V_{EE}	V_{EE}	$V_{CC} \geqq V_{DD}$		
	V_{ref}	V_{ref}	$V_{DD}-Vref \geqq 10$	0 to $V_{DD}-4.5$	V
	V_{CC}	V_{CC}		4.5 to (5.0typ) to 5.5	V
Input "H"-Level Voltage	V_{IH1}	CLK,DI		$0.8V_{CC}$ to V_{CC}	V
	V_{IH2}	S		Vref+0.9(V_{DD}-Vref) to V_{DD}	V
Input "L"-Level Voltage	V_{IL1}	CLK,DI		V_{SS} to $0.2V_{CC}$	V
	V_{IL2}	S		Vref to Vref+0.1(V_{DD}-Vref)	V
Input Pulse Width	tøw	CLK		1 min.	us
Setup Time	t_{setup}	DI		1 min.	us
Hold Time	t_{hold}	DI		1 min.	us

Electrical Characteristics at Ta=25°C, V_{SS}=0V

				min	typ	max	unit
Total Harmonic Disortion	THD1	IN1,2:All bands flat, f=20kHz,output 1V				0.005	%
	THD2	IN1,2:Boost,f=20kHz,Output 1V				0.05	%
Closstalk	CT	:f=1kHz		60			dB
Setting Error	ΔB	Other band flat, Test Circuit 1 (No reversion occurs.)	±10dB	±9	±10	±11.5	dB
			±8dB	±6.6	±7.6	±9.0	dB
			±6dB	±4.9	±5.9	±7.2	dB
			±4dB	±3.0	±3.8	±4.9	dB
			±2dB	±1.0	±1.9	±3.0	dB
Analog SW OFF Leak	I_{OFF}	IN1,IN2,f1~f7				10	uA
Pull-down Resistance	R_{PD}	S :V_{DD}=13V,S		100			kohm
Current Dissipation	I_{DD}					1	mA
	I_{CC}					0.5	mA



Test Circuit 1