Ordering number : EN5506

Bi-CMOS LSI

LV1100

Digital Surround Audio Signal-Processing IC

Overview

The LV1100 is an audio signal-processing Bi-CMOS LSI that integrates input and output filters, a delay line (built-in memory), and a delay/reverb function with a maximum delay of 120 ms on a single chip. It also provides built-in fixed matrix (L+R, L–R) and front mixing (with level and phase switching) functions. A full complement of surround modes can be easily implemented by combining these functions.

Functions and Features

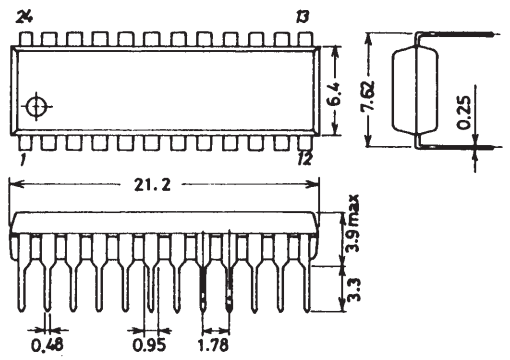
- Input switching (L+R, L–R, IN–A)
- On-chip memory (12K SRAM)
- Front adder (+3 dB, 0 dB, –3 dB, -∞)
- Input and output filters
- Input filter –7 kHz low-pass filter
- Output filter –5 kHz low-pass filter: switchable with a 3 kHz low-pass filter
- On-chip V_{DD} circuit
- Input and output muting function
- A simulated surround system can be easily implemented with only one chip.
- ADM A/D and D/A converters
- Variable delay times
  - – Short mode; Maximum delay: 60 ms. Delay time selectable from six delay times in 10-ms steps.
  - – Long mode; Maximum delay: 120 ms. Delay time selectable from six delay times in 20-ms steps.

Package Dimensions

unit: mm

3067-DIP24S

[LV1100]



SANYO: DIP24S

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		12	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	420	mW
Operating temperature	Topr		–25 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		9	V
Operating supply voltage range	V_{CC} opg		8 to 10	V

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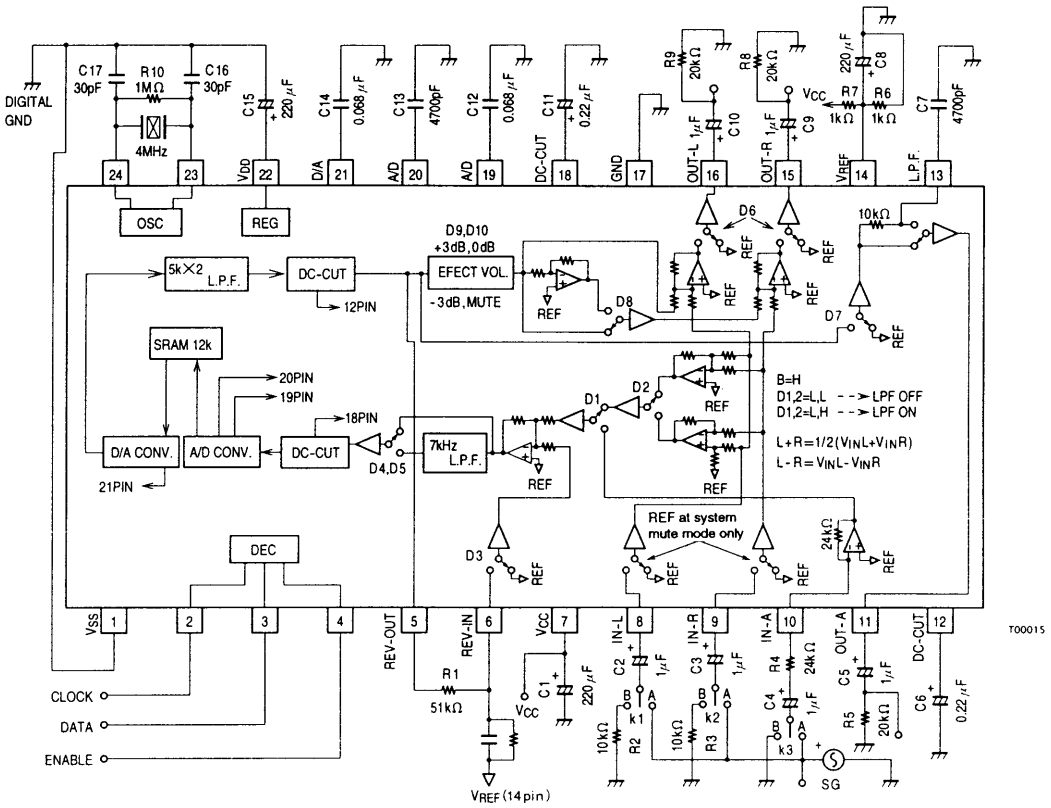
Electrical Characteristics at Ta = 25°C, V_{CC} = 9 V, R_L = 20 kΩ, V_{IN} = 300 mV and f = 1 kHz unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}		15	28	42	mA
Maximum output voltage	V_O maxA	OUT-A, CLOCK FAST, THD = 10% V_{CC} = 8 V	0.7	1.0		V
	V_O maxL	OUT-L, THD = 1% (effect off), V_{CC} = 8 V	1.6			V
	V_O maxR	OUT-R, THD = 1% (effect off), V_{CC} = 8 V	1.6			V
Output noise voltage	V_{NO}AF	OUT-A, CLOCK FAST (5 kHz L.P.F) JIS A, Rg = 10 kΩ		–89	–80	dBV
	V_{NO}AS	OUT-A, CLOCK SLOW (3 kHz L.P.F) JIS A, Rg = 10 kΩ		–84	–75	dBV
	V_{NO}L	OUT-L (effect off), JIS A, Rg = 10 kΩ		–103	–95	dBV
	V_{NO}R	OUT-R (effect off), JIS A, Rg = 10 kΩ		–103	–95	dBV
	V_{NO}LE	OUT-L (effect –3 dB), JIS A, Rg = 10 kΩ		–88	–80	dBV
	V_{NO}RE	OUT-R (effect –3 dB), JIS A, Rg = 10 kΩ		–88	–80	dBV
Output level deviation	VGA	OUT-A, CLOCK FAST	–4	0	4	dB
	VGL	OUT-L (effect off)	–2	0	2	dB
	VGR	OUT-R (effect off)	–2	0	2	dB
Total harmonic distortion	THDAF	OUT-A, CLOCK FAST (5 kHz L.P.F): 400 to 30 kHz BPF		0.3	1.0	%
	THDAS	OUT-A, CLOCK SLOW (3 kHz L.P.F): 400 to 30 kHz BPF		0.6	1.5	%
	THDL	OUT-L (effect off): 400 to 30 kHz B.P.F		0.01	0.03	%
	THDR	OUT-R (effect off): 400 to 30 kHz B.P.F		0.01	0.03	%

Control Data

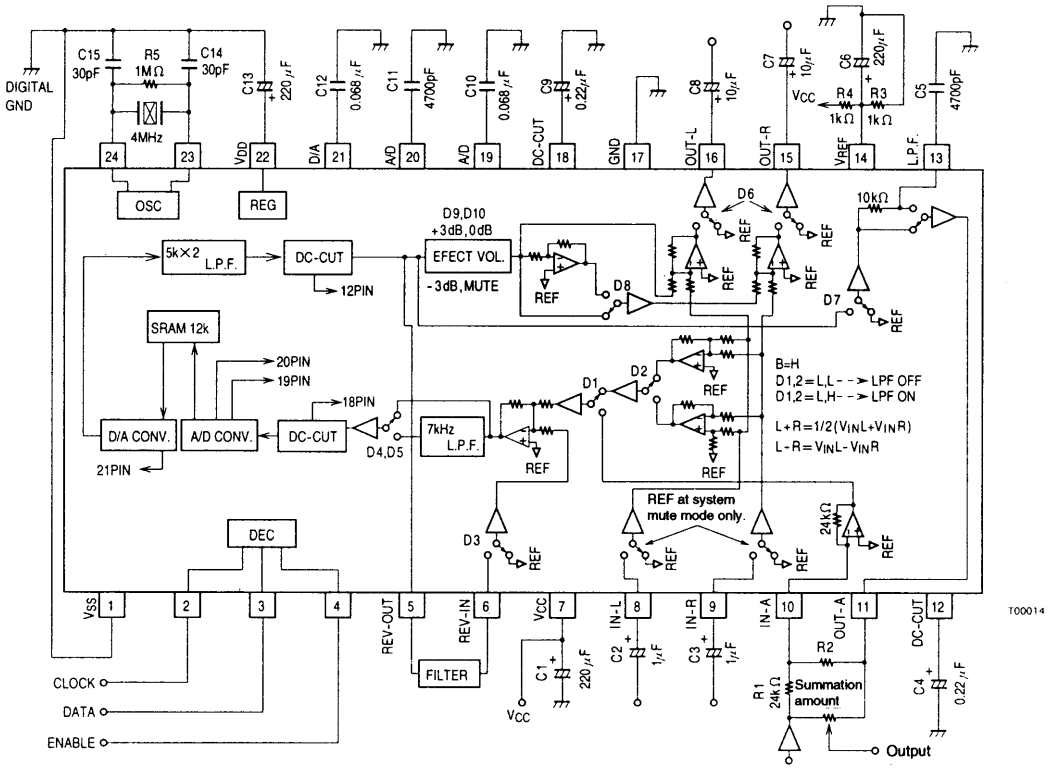
Parameter	Symbol	Conditions	Ratings	Unit
Control data Input low-level voltage	V_{IL}		0 to 1.5	V
Control data Input high-level voltage	V_{IH}		3.5 to 5.5	V

Test Circuit



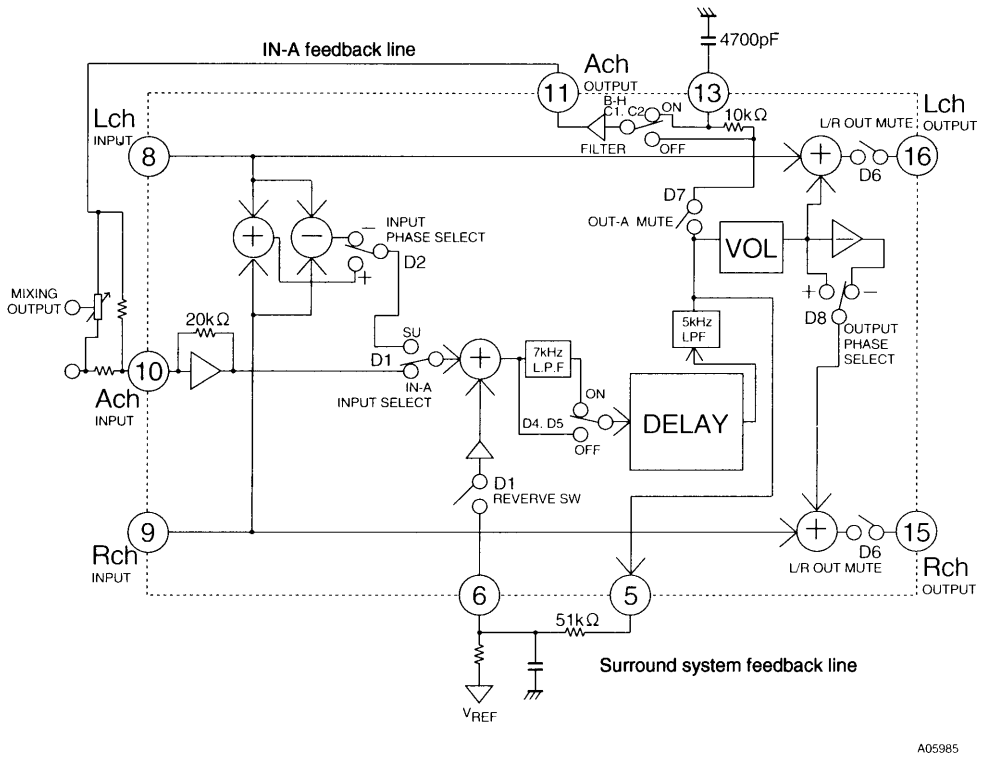
Notes: 1. The items D1 through D10 in the figure indicate points that are switched by the serial data.
2. Use capacitors with good high-frequency characteristics for the capacitors on pins 7, 14, and 22. Also, connect 0.1-μF ceramic capacitors in parallel.

Application Circuit Example



Note: The items D1 through D10 in the figure indicate points that are switched by the serial data.

Block Diagram



Functional Description

1.INPUT PHASE SELECT

Selects either the input summation signal (L+R) or the input difference signal (L-R). When set to low, L+R is selected, and when set to high, L-R is selected.

2.INPUT SELECT

Selects either the IN-L and IN-R input signals, or the IN-A input signal.

3.INPUT FILTER

Selects whether the signal input from either IN-L and IN-R or IN-A is passed through a 7-kHz low-pass filter, or whether it is directly input to the delay block.

4.DELAY

In clock fast mode, creates one of six delayed signals with delays of 10 to 60 ms in 10-ms steps.
In clock slow mode, creates one of six delayed signals with delays of 20 to 120 ms in 20-ms steps.

5.VOL (effect volume)

Selects the amount of the front L and R signals added to the delayed signal. Possible settings are +3 dB, 0 dB, –3 dB, and –∞.

6.OUTPUT PHASE SELECT

Selects in-phase (+ setting) or out-of-phase (– setting) with respect to the left channel for the right channel of the VOL output signal.

7.REVERVE SW

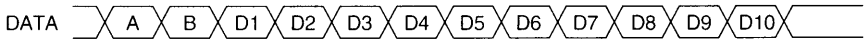
Set this switch to the on position to specify that the surround system output signal be fed back.

8.IN-A OUTPUT FILTER

Allows the signal to be output after passing through a 3-kHz low-pass filter.

Command List

LV1100 Control Format



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A = L ... Selects the LV1100.

B = L ... When B is low, the mode settings listed below can be made.

	L	H
D1	IN-A DELAY	L+R, L–R DELAY
D2	L+R	L–R
D3	DELAY OUT ON; Turns on surround system feedback	DELAY OUT OFF; Turns off surround system feedback
7 kHz L.P.F ON/OFF		
D4, D5		
LL	THROUGH	
LH	NOT USE	
HL	FILTER	
HH	A/D INPUT MUTE	
	L	H
D6	OUT-L, –R MUTE ON	OUT-L, –R MUTE OFF
D7	OUT-A MUTE ON	OUT-A MUTE OFF
D8	FRONT ADD INPHASE (In-phase addition)	FRONT ADD INVERTED PHASE (Out-of-phase addition)
FRONT ADD EFFECT VOL (Addition to the front left and right channels)		
D9, D10		
LL	+3 dB	
LH	0 dB	
HL	–3 dB	
HH	MUTE	

B = H ... When B is high, the mode settings listed below can be made.

D1	D2	IN-A output filter
L	L	3 kHz L.P.F-OFF
L	H	3 kHz L.P.F-ON

D3	D4	D5
*	*	*

* = don’t care

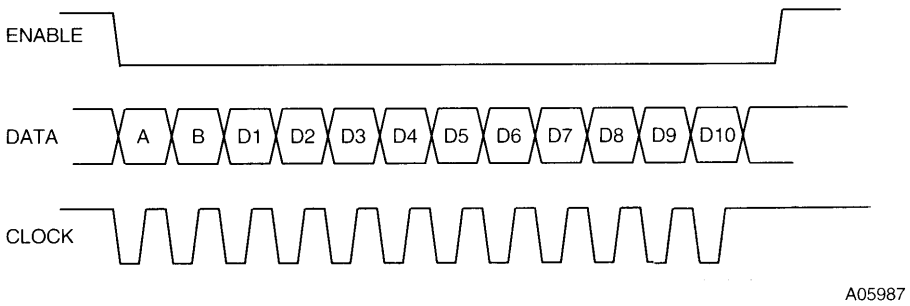
Delay Time Data (D6 to D8)

D6	D7	D8	CLK FAST	CLK SLOW
L	L	L	10 ms	20 ms
L	L	H	20 ms	40 ms
L	H	L	30 ms	60 ms
L	H	H	40 ms	80 ms
H	L	L	50 ms	100 ms
H	L	H	60 ms	120 ms

Note: D6, D7, and D8 must not be used for any purposes other than the above commands.

	L	H
D9	SYSTEM MUTE ON	SYSTEM MUTE OFF
D10	CLK FAST	CLK SLOW

Control Data Format



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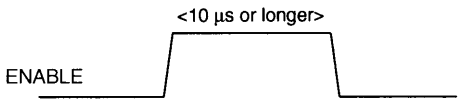
- Data is read in on the rising edge of the clock.
- The control data consists of 12 bits.
- The input data is latched on the rising edge of the enable signal.
- The clock and enable signals must be held high when not being used to control the LV1100.
- Command interval time
  The timing of intervals between enable signals must meet the conditions shown in the figure.



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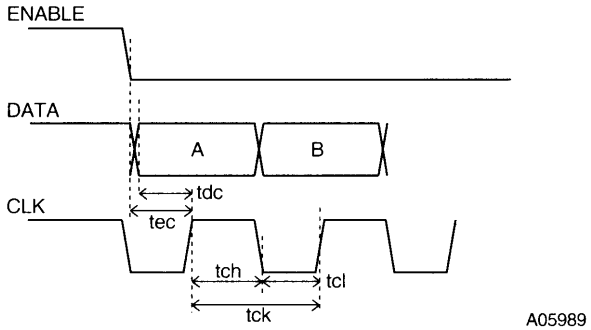
Notes on Mode Control (System Mute Usage)

1 When power is first applied, after the IC is fully operating (about 2 seconds after power is applied) applications must send commands that turn the system muting off and then on again.

2 Applications must perform system muting on/off operations when switching the delay time or clock fast/slow settings. After sending a system muting on command along with the new data, send the new data again, this time with a system muting off command.

Note: By performing the operations described in items 1 and 2 here, the memory contents are initialized, thus preventing incorrect operation.

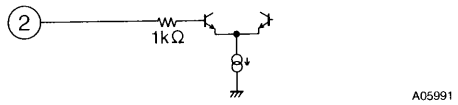
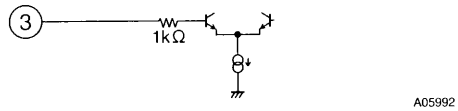
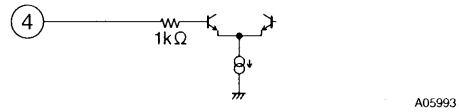
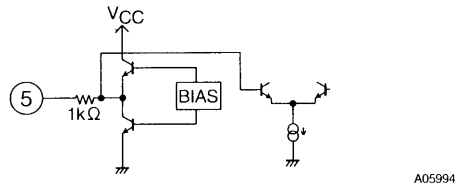
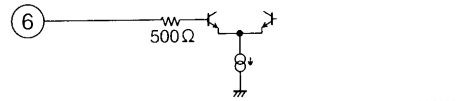
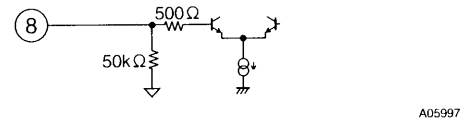
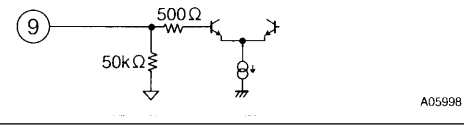
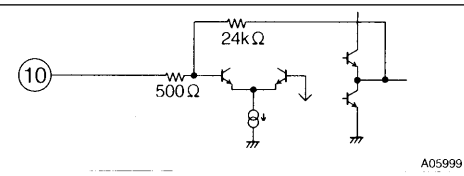
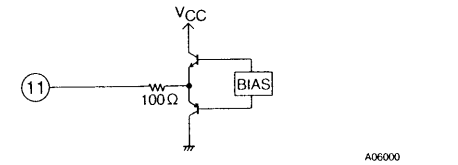
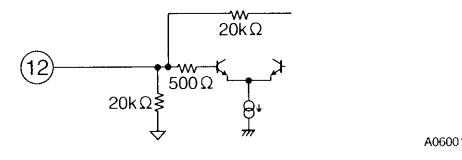
Data Timing



Timing Characteristics

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Enable clock delay time	tec		5			µs
Data clock delay time	tdc		5			µs
Clock high-level hold time	tch		5			µs
Clock low-level hold time	tcl		5			µs
Clock cycle time	tck		10			µs

Pin Functions

Pin no.	Pin	Pin voltage	Internal equivalent circuit
1	DIGITAL–GND	0 V	
2	CLK	Control voltage Apply a voltage of 0 or 5 V.	
3	DATA	Control voltage Apply a voltage of 0 or 5 V.	
4	ENABLE	Control voltage Apply a voltage of 0 or 5 V.	
5	REV-OUT	1/2 V_{CC}	
6	REV-IN	1/2 V_{CC} Apply the voltage output by pin 5 through an external resistor.	
7	V_{CC}	V_{CC} (Power-supply voltage)	
8	IN-L	1/2 V_{CC}	
9	IN-R	1/2 V_{CC}	
10	IN-AUX	1/2 V_{CC}	
11	OUT-AUX	1/2 V_{CC}	
12	DC-CUT	1/2 V_{CC}	

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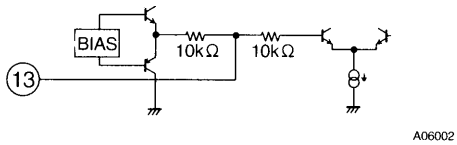
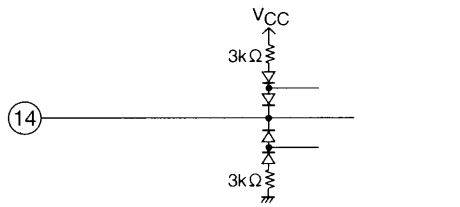
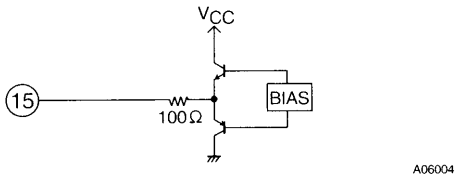
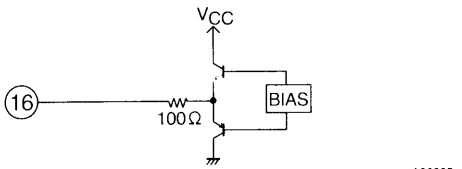
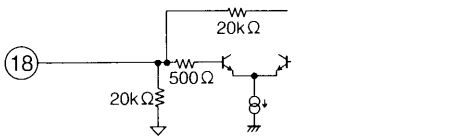
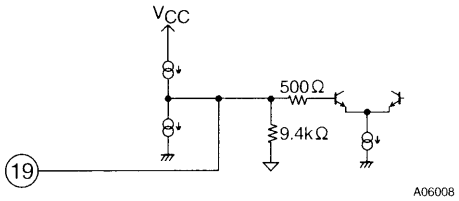
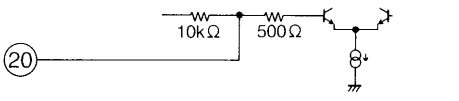
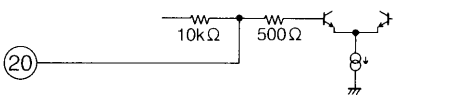
Pin no.	Pin	Pin voltage	Internal equivalent circuit
13	L.P.F	1/2 V_{CC}	
14	V_{REF}	1/2 V_{CC}	
15	OUT-R	1/2 V_{CC}	
16	OUT-L	1/2 V_{CC}	
17	ANALOG-GND	0 V	
18	DC-CUT	1/2 V_{CC}	
19	A/D integrator	1/2 V_{CC}	
20	A/D noise shaper	1/2 V_{CC}	
21	D/A integrator	1/2 V_{CC}	
22	V_{DD}	5 V	
23 24	OSC	Charged by 0 or 5 V.