LH28F160BVHE-BTL90

Flash Memory

16M (2M ×8/1M x 16)

(Model No.: LHF16V11)

Spec No.: EL10Y079A
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LH28F160BVHE-BTL90
16M-BIT (2Mbit × 8 / 1Mbit × 16)
Boot Block FLASH MEMORY

- Single Voltage Operation
  - 2.7V-3.6V V_{CC} and V_{PP} Read/Write/Erase Operation
- High-Block Erase and Word/Byte Write Performance
  - Usable 12V±0.6V V_{PP}
- User-Configurable ×8 or ×16 Operation
- High-Performance Access Time
  - 90ns(V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C)
- Optimized Array Blocking Architecture
  - Two 4K-word Boot Blocks
  - Six 4K-word Parameter Blocks
  - Thirty-one 32K-word Main Blocks
  - Bottom Boot Location
- Extended Cycling Capability
  - 100,000 Block Erase Cycles
- Low Power Management
  - Deep Power-Down Mode
  - Automatic Power Savings Mode Decreases I_{CC} in Static Mode
- Enhanced Data Protection Features
  - Absolute Protection with V_{PP}=GND
  - Block Erase and Word/Byte Write Lockout during Power Transitions
  - Boot Blocks Protection with WP#=V_{IL}
- Enhanced Automated Suspend Options
  - Word/Byte Write Suspend to Read
  - Block Erase Suspend to Word/Byte Write
  - Block Erase Suspend to Read
- Automated Word/Byte Write and Block Erase
  - Command User Interface
  - Status Register
- SRAM-Compatible Write Interface
- Industry-Standard Packaging
  - 48-Lead TSOP
- ETOX^{TM*} Nonvolatile Flash Technology
- CMOS Process (P-type silicon substrate)
- Not designed or rated as radiation hardened

SHARP's LH28F160BVHE-BTL90 Flash memory is a high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications. LH28F160BVHE-BTL90 can operate at V_{CC}=2.7V-3.6V and V_{PP}=2.7V-3.6V. Its low voltage operation capability realize battery life and suits for cellular phone application.

Its Boot, Parameter and Main-blocked architecture, flexible voltage and extended cycling provide for highly flexible component suitable for portable terminals and personal computers. Its enhanced suspend capabilities provide for an ideal solution for code + data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F160BVHE-BTL90 offers two levels of protection: absolute protection with V_{PP} at GND, selective hardware boot block locking. These alternatives give designers ultimate control of their code security needs.

The LH28F160BVHE-BTL90 is manufactured on SHARP's 0.35μm ETOX^{TM*} process technology. It come in industry-standard package: the 48-lead TSOP ideal for board constrained applications.

*ETOX is a trademark of Intel Corporation.

1 INTRODUCTION

This datasheet contains LH28F160BVHE-BTL90 specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4 and 5 describe the memory organization and functionality. Section 6 covers electrical specifications.

1.1 Features

Key enhancements of LH28F160BVHE-BTL90 Flash memory are:

- 2.7V-3.6V V_{CC} and V_{PP} Read/Write/Erase Operations
- Enhanced Suspend Capabilities
- Boot Block Architecture

Please note following contents:

- V_{PPLK} has been lowered to 1.5V to support 2.7V-3.6V block erase and word/byte write operations. The V_{PP} voltage transitions to GND is recommended for designs that switch V_{PP} off during read operation.

1.2 Product Overview

The LH28F160BVHE-BTL90 is a high-performance 16M-bit Flash memory organized as 2M-byte of 8 bits or 1M-word of 16 bits. The 2M-byte/1M-word of data is arranged in two 8K-byte/4K-word boot blocks, six 8K-byte/4K-word parameter blocks and thirty-one 64K-byte/32K-word main blocks which are individually erasable in-system. The memory map is shown in Figure 3.

A choice of V_{CC} and V_{PP} combinations, as shown in Table 1, to meet system performance and power expectations. V_{PP} at 2.7V-3.6V eliminates the need for a separate 12V converter, while V_{PP}=12V maximizes block erase and word/byte write performance. In addition to flexible erase and program voltages, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

Table 1. V_{CC} and V_{PP} Voltage Combinations

V_{CC} Voltage	V_{PP} Voltage
2.7V-3.6V	2.7V-3.6V, 11.4V-12.6V

Internal V_{CC} and V_{PP} detection Circuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase and word/byte write operations.

A block erase operation erases one of the device's 32K-word blocks typically within 1.2s (3.0V V_{CC}, 3.0V V_{PP}), 4K-word blocks typically within 0.5s (3.0V V_{CC}, 3.0V V_{PP}) independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in word/byte increments of the device's 32K-word blocks typically within 55μs (3.0V V_{CC}, 3.0V V_{PP}), 4K-word blocks typically within 60μs (3.0V V_{CC}, 3.0V V_{PP}). Word/byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

The boot blocks can be locked for the WP# pin. Block erase or word/byte write for boot block must not be carried out by WP# to Low and RP# to V_{IH}.

The status register indicates when the WSM's block erase or word/byte write operation is finished.

The RY/BY# output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/BY# minimizes both CPU overhead and system power consumption. When low, RY/BY# indicates that the WSM is performing a block erase or word/byte write. RY/BY#-high Z indicates that the WSM is ready for a new command, block erase is suspended (and word/byte write is inactive), word/byte write is suspended, or the device is in deep power-down mode.

The access time is 90ns (t_{AVQV}) over the operating temperature range (-40°C to +85°C) and V_{CC} supply voltage range of 2.7V-3.6V.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 3mA at 2.7V-3.6V V_{CC}.

When CE# and RP# pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the RP# pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (t_{PHQV}) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from RP#-high until writes to the CUI are recognized. With RP# at GND, the WSM is reset and the status register is cleared.

The device is available in 48-lead TSOP (Thin Small Outline Package, 1.2 mm thick). Pinout is shown in Figure 2.

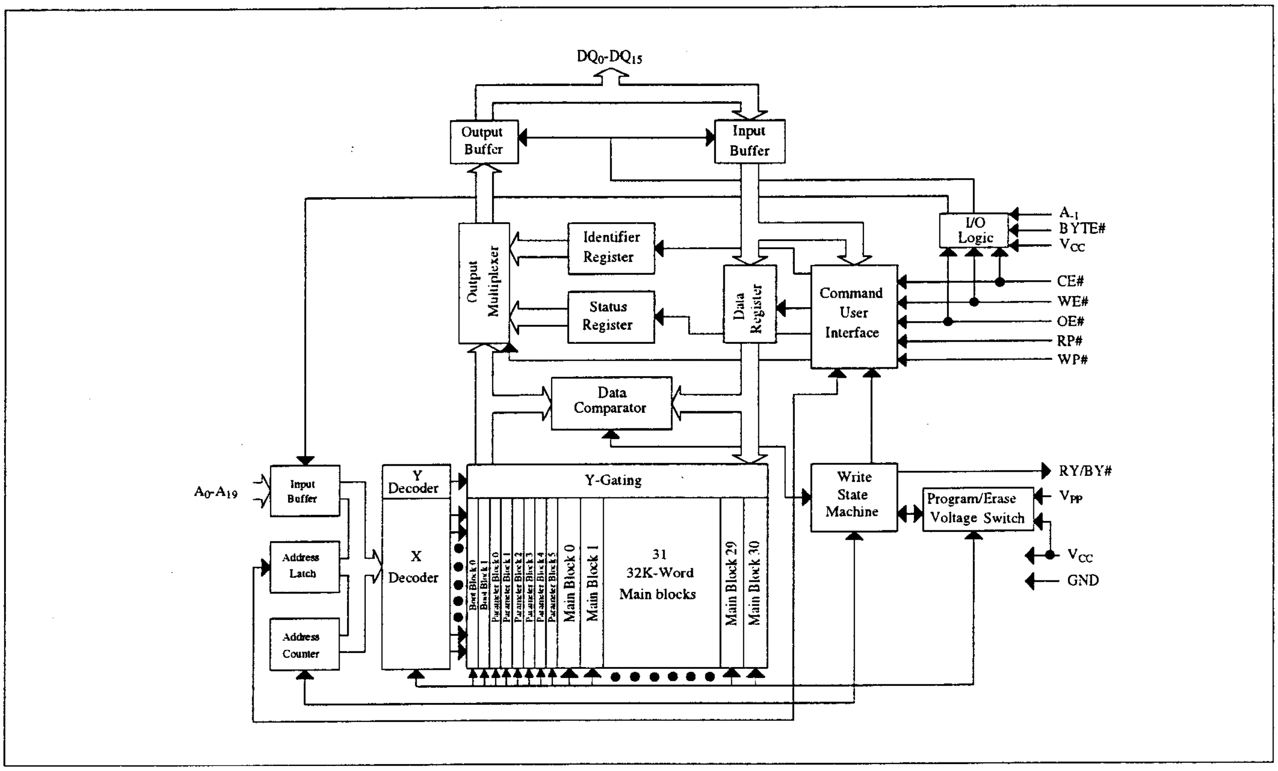

DQ0-DQ15
Output Buffer
Input Buffer
I/O Logic
A-1
BYTE#
VCC
Identifier Register
Status Register
Output Multiplexer
Data Register
Command User Interface
CE#
WE#
OE#
RP#
WP#
Data Comparator
A0-A19
Input Buffer
Address Latch
Address Counter
Y Decoder
X Decoder
Y-Gating
Boot Block 0
Boot Block 1
Parameter Block 0
Parameter Block 1
Parameter Block 2
Parameter Block 3
Parameter Block 4
Parameter Block 5
Main Block 0
Main Block 1
31 32K-Word Main blocks
Main Block 29
Main Block 30
Write State Machine
Program/Erase Voltage Switch
RY/BY#
VPP
VCC
GND

Figure 1. Block Diagram

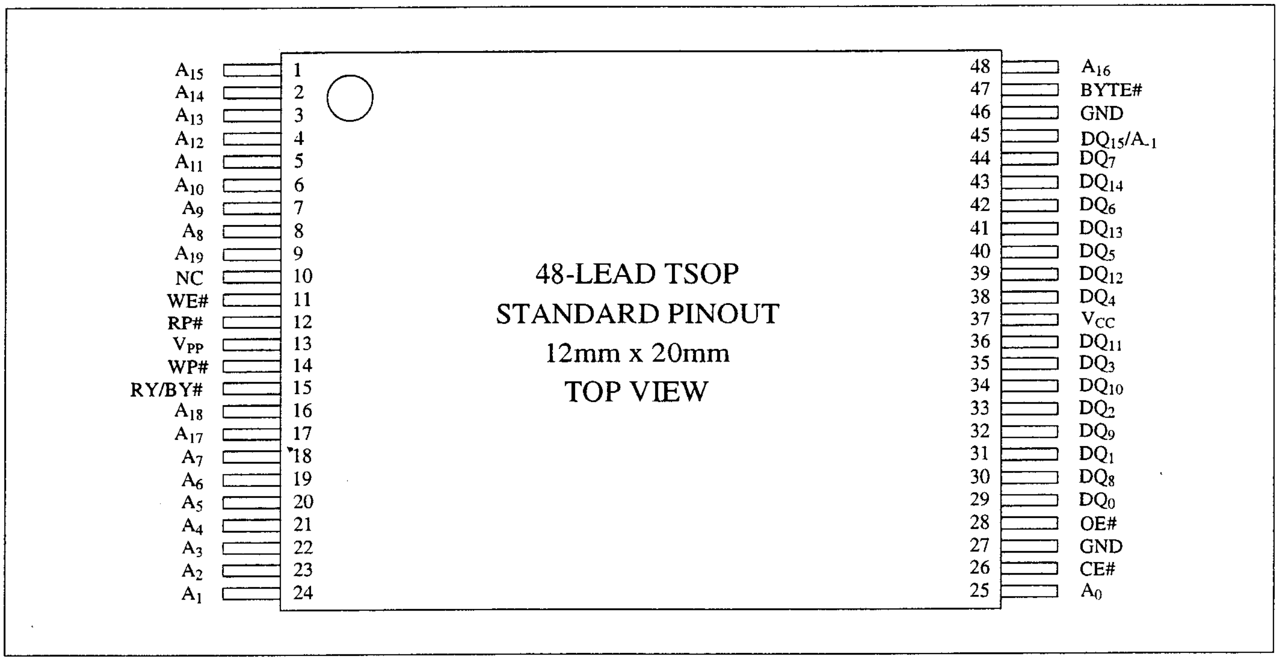

A15 1
A14 2
A13 3
A12 4
A11 5
A10 6
A9 7
A8 8
A19 9
NC 10
WE# 11
RP# 12
VPP 13
WP# 14
RY/BY# 15
A18 16
A17 17
A7 18
A6 19
A5 20
A4 21
A3 22
A2 23
A1 24
48 A16
47 BYTE#
46 GND
45 DQ15/A-1
44 DQ7
43 DQ14
42 DQ6
41 DQ13
40 DQ5
39 DQ12
38 DQ4
37 VCC
36 DQ11
35 DQ3
34 DQ10
33 DQ2
32 DQ9
31 DQ1
30 DQ8
29 DQ0
28 OE#
27 GND
26 CE#
25 A0
48-LEAD TSOP
STANDARD PINOUT
12mm x 20mm
TOP VIEW

Figure 2. TSOP 48-Lead Pinout

Table 2. Pin Descriptions

Symbol	Type	Name and Function
A_{-1} A_0-A_{19}	INPUT	ADDRESS INPUTS: Addresses are internally latched during a write cycle. A_{-1} : Byte Select Address. Not used in ×16 mode. A_0-A_{10} : Row Address. Selects 1 of 2048 word lines. A_{11}-A_{14} : Column Address. Selects 1 of 16 bit lines. A_{15}-A_{19} : Main Block Address. (Boot and Parameter block Addresses are A_{12}-A_{19}.)
DQ_0-DQ_{15}	INPUT/ OUTPUT	DATA INPUT/OUTPUTS: DQ_0-DQ_7:Inputs data and commands during CUI write cycles; outputs data during memory array, status register and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle. DQ_8-DQ_{15}:Inputs data during CUI write cycles in ×16 mode; outputs data during memory array read cycles in ×16 mode; not used for status register and identifier code read mode. Data pins float to high-impedance when the chip is deselected, outputs are disabled, or in ×8 mode(Byte#=V_{IL}). Data is internally latched during a write cycle.
CE#	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high deselects the device and reduces power consumption to standby levels.
RP#	INPUT	RESET/DEEP POWER-DOWN: Puts the device in deep power-down mode and resets internal automation. RP#-high enables normal operation. When driven low, RP# inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode. With RP#=V_{HH}, block erase or word/byte write can operate to all blocks without WP# state. Block erase or word/byte write with V_{IH}<RP#<V_{HH} produce spurious results and should not be attempted.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
WP#	INPUT	WRITE PROTECT: Master control for boot blocks locking. When V_{IL}, locked boot blocks cannot be erased and programmed.
BYTE#	INPUT	BYTE ENABLE: BYTE# V_{IL} places device in ×8 mode. All data is then input or output on DQ_{0-7}, and DQ_{8-15} float. BYTE# V_{IH} places the device in ×16 mode , and turns off the A_{-1} input buffer.
RY/BY#	OPEN DRAIN OUTPUT	READY/BUSY#: Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase or word/byte write). RY/BY#-high Z indicates that the WSM is ready for new commands, block erase is suspended, and word/byte write is inactive, word/byte write is suspended, or the device is in deep power-down mode.
V_{PP}	SUPPLY	BLOCK ERASE AND WORD/BYTE WRITE POWER SUPPLY: For erasing array blocks or writing words/bytes. With $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. Block erase and word/byte write with an invalid V_{PP} (see DC Characteristics) produce spurious results and should not be attempted.
V_{CC}	SUPPLY	DEVICE POWER SUPPLY: Do not float any power pins. With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internal connected; it may be driven or floated.

2 PRINCIPLES OF OPERATION

The LH28F160BVHE-BTL90 Flash memory includes an on-chip WSM to manage block erase and word/byte write functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erasure and word/byte write, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erasure and word/byte writing. All functions associated with altering memory contents–block erase, word/byte write, status and identifier codes–are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase and word/byte write. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Addresses and data are internally latch during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes or outputs status register data.

Interface software that initiates and polls progress of block erase and word/byte write can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read/write data from/to blocks other than that which is suspend. Word/byte write suspend allows system software to suspend a word/byte write to read data from any other flash memory array location.

[A_{19}-A_0]	Bottom Boot	
FFFFF F8000	32K-word Main Block	30
F7FFF F0000	32K-word Main Block	29
EFFFF E8000	32K-word Main Block	28
E7FFF E0000	32K-word Main Block	27
DFFFF D8000	32K-word Main Block	26
D7FFF D0000	32K-word Main Block	25
CFFFF C8000	32K-word Main Block	24
C7FFF C0000	32K-word Main Block	23
BFFFF B8000	32K-word Main Block	22
B7FFF B0000	32K-word Main Block	21
AFFFF A8000	32K-word Main Block	20
A7FFF A0000	32K-word Main Block	19
9FFFF 98000	32K-word Main Block	18
97FFF 90000	32K-word Main Block	17
8FFFF 88000	32K-word Main Block	16
87FFF 80000	32K-word Main Block	15
7FFFF 78000	32K-word Main Block	14
77FFF 70000	32K-word Main Block	13
6FFFF 68000	32K-word Main Block	12
67FFF 60000	32K-word Main Block	11
5FFFF 58000	32K-word Main Block	10
57FFF 50000	32K-word Main Block	9
4FFFF 48000	32K-word Main Block	8
47FFF 40000	32K-word Main Block	7
3FFFF 38000	32K-word Main Block	6
37FFF 30000	32K-word Main Block	5
2FFFF 28000	32K-word Main Block	4
27FFF 20000	32K-word Main Block	3
1FFFF 18000	32K-word Main Block	2
17FFF 10000	32K-word Main Block	1
0FFFF 08000	32K-word Main Block	0
07FFF 07000	4K-word Parameter Block	5
06FFF 06000	4K-word Parameter Block	4
05FFF 05000	4K-word Parameter Block	3
04FFF 04000	4K-word Parameter Block	2
03FFF 03000	4K-word Parameter Block	1
02FFF 02000	4K-word Parameter Block	0
01FFF 01000	4K-word Boot Block	1
00FFF 00000	4K-word Boot Block	0

Figure 3. Memory Map

2.1 Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory block erases or word/byte writes are required) or hardwired to $V_{PPH1/2}$. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. The CUI, with two-step block erase or word/byte write command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP}. All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when RP# is at V_{IL}. The device's boot blocks locking capability for WP# provides additional protection from inadvertent code or data alteration by block erase and word/byte write operations. Refer to Table 6 for write protection alternatives.

3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any block, identifier codes or status register independent of the V_{PP} voltage. RP# can be at either V_{IH} or V_{HH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Six control pins dictate the data flow in and out of the component: CE#, OE#, WE#, RP#, WP# and BYTE#. CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control, and when active enables the selected memory device. OE# is the data output (DQ_0-DQ_{15}) control and when active drives the selected memory data onto the I/O bus. WE# must be at V_{IH} and RP# must be at V_{IH} or V_{HH}. Figure 11, 12 illustrates read cycle.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (DQ_0-DQ_{15}) are placed in a high-impedance state.

3.3 Standby

CE# at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ_0-DQ_{15} outputs are placed in a high-impedance state independent of OE#. If deselected during block erase or word/byte write, the device continues functioning, and consuming active power until the operation completes.

3.4 Deep Power-Down

RP# at V_{IL} initiates the deep power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100 ns. Time t_{PHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase or word/byte write modes, RP#-low will abort the operation. RY/BY# remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase or word/byte write modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code and device code (see Figure 4). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms.

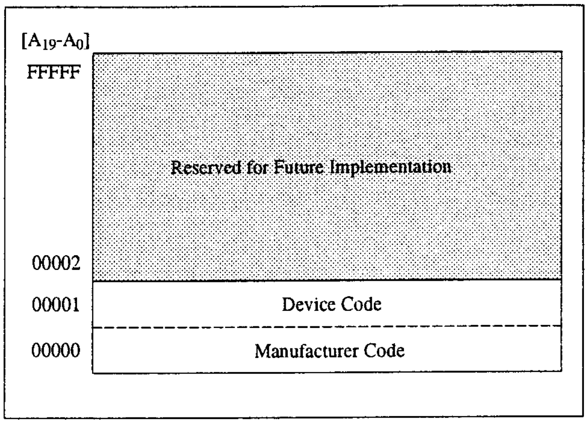


Figure 4. Device Identifier Code Memory Map

3.6 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When V_{CC}=2.7V-3.6V and V_{PP}=$V_{PPH1/2}$, the CUI additionally controls block erasure and word/byte write.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word/Byte Write command requires the command and address of the location to be written.

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. Figures 13 and 14 illustrate WE# and CE# controlled write operations.

4 COMMAND DEFINITIONS

When the V_{PP} voltage $\leq V_{PPLK}$, Read operations from the status register, identifier codes, or blocks are enabled. Placing $V_{PPH1/2}$ on V_{PP} enables successful block erase and word/byte write operations.

Device operations are selected by writing specific commands into the CUI. Table 4 defines these commands.

Table 3.1. Bus Operations(BYTE#=V_{IH})$^{(1,2)}$

Mode	Notes	RP#	CE#	OE#	WE#	Address	V_{PP}	DQ_{0-15}	RY/BY#$^{(3)}$
Read	8	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable		V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby	10	V_{IH} or V_{HH}	V_{IH}	X	X	X	X	High Z	X
Deep Power-Down	4,10	V_{IL}	X	X	X	X	X	High Z	High Z
Read Identifier Codes	8	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	See Figure 4	X	Note 5	High Z
Write	6,7,8	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

Table 3.2. Bus Operations(BYTE#=V_{IL})$^{(1,2)}$

Mode	Notes	RP#	CE#	OE#	WE#	Address	V_{PP}	DQ_{0-7}	DQ_{8-15}	RY/BY#$^{(3)}$
Read	8	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	High Z	X
Output Disable		V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	High Z	X
Standby	10	V_{IH} or V_{HH}	V_{IH}	X	X	X	X	High Z	High Z	X
Deep Power-Down	4,10	V_{IL}	X	X	X	X	X	High Z	High Z	High Z
Read Identifier Codes	8,9	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	See Figure 4	X	Note 5	High Z	High Z
Write	6,7,8	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X	X

NOTES:

1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/2}$ for V_{PP}. See DC Characteristics for V_{PPLK} and $V_{PPH1/2}$ voltages.
3. RY/BY# is V_{OL} when the WSM is executing internal block erase or word/byte write algorithms. It is High Z during when the WSM is not busy, in block erase suspend mode (with word/byte write inactive), word/byte write suspend mode or deep power-down mode.
4. RP# at GND±0.2V ensures the lowest deep power-down current.
5. See Section 4.2 for read identifier code data.
6. Command writes involving block erase or word/byte write are reliably executed when $V_{PP}=V_{PPH1/2}$ and V_{CC}=2.7V-3.6V. Block erase or word/byte write with $V_{IH}<RP\#<V_{HH}$ produce spurious results and should not be attempted.
7. Refer to Table 4 for valid D_{IN} during a write operation.
8. Never hold OE# low and WE# low at the same timing.
9. A_{-1} set to V_{IL} or V_{IH} in byte mode (BYTE#=V_{IL}).
10. WP# set to V_{IL} or V_{IH}.

Table 4. Command Definitions[(7)]

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper[(1)]	Addr[(2)]	Data[(3)]	Oper[(1)]	Addr[(2)]	Data[(3)]
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥2	4	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Word/Byte Write	2	5,6	Write	WA	40H or 10H	Write	WA	WD
Block Erase and Word/Byte Write Suspend	1	5	Write	X	B0H			
Block Erase and Word/Byte Write Resume	1	5	Write	X	D0H			

NOTES:

1. BUS operations are defined in Table 3.1 and Table 3.2.
2. X=Any valid address within the device.
   IA=Identifier Code Address: see Figure 4. A_{-1} set to V_{IL} or V_{IH} in Byte Mode (BYTE#=V_{IL}).
   BA=Address within the block being erased. The each block can select by the address pin A_{19} through A_{12} combination.
   WA=Address of memory location to be written.
3. SRD=Data read from status register. See Table 7 for a description of the status register bits.
   WD=Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   ID=Data read from identifier codes.
4. Following the Read Identifier Codes command, read operations access manufacturer and device codes. See Section 4.2 for read identifier code data.
5. If the block is boot block, WP# must be at V_{IH} or RP# must be at V_{HH} to enable block erase or word/byte write operations. Attempts to issue a block erase or word/byte write to a boot block while WP# is V_{IH} or RP# is V_{IH}.
6. Either 40H or 10H are recognized by the WSM as the word/byte write setup.
7. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase or word/byte write, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Word/Byte Write Suspend command. The Read Array command functions independently of the V_{PP} voltage and RP# can be V_{IH} or V_{HH}.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 4 retrieve the manufacturer and device codes (see Table 5 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage and RP# can be V_{IH} or V_{HH}. Following the Read Identifier Codes command, the following information can be read:

Table 5. Identifier Codes

Code	Address [A_{19}-A_0]	Data [DQ_7-DQ_0]
Manufacture Code	00000H	B0H
Device Code	00001H	49H

4.3 Read Status Register Command

The status register may be read to determine when a block erase or word/byte write is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#, whichever occurs. OE# or CE# must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. RP# can be V_{IH} or V_{HH}.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 or SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 7). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple blocks or writing several words/bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} Voltage. RP# can be V_{IH} or V_{HH}. This command is not functional during block erase or word/byte write suspend modes.

4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFFFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 5). The CPU can detect block erase completion by analyzing the output data of the RY/BY# pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when V_{CC}=2.7V-3.6V and $V_{PP}=V_{PPH1/2}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". Successful block erase for boot blocks requires that the corresponding if set, that WP#=V_{IH} or RP#=V_{HH}. If block erase is attempted to boot block when the corresponding WP#=V_{IL} or RP#=V_{IH}, SR.1 and SR.5 will be set to "1". Block erase operations with V_{IH}<RP#<V_{HH} produce spurious results and should not be attempted.

4.6 Word/Byte Write Command

Word/byte write is executed by a two-cycle command sequence. Word/byte write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word/byte write and write verify algorithms internally. After the word/byte write sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect the completion of the word/byte write event by analyzing the RY/BY# pin or status register bit SR.7.

When word/byte write is complete, status register bit SR.4 should be checked. If word/byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word/byte writes can only occur when V_{CC}=2.7V-3.6V and $V_{PP}=V_{PPH1/2}$. In the absence of this high voltage, memory contents are protected against word/byte writes. If word/byte write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful word/byte write for boot blocks requires that the corresponding if set, that WP#=V_{IH} or RP#=V_{HH}. If word/byte write is attempted to boot block when the corresponding WP#=V_{IL} or RP#=V_{IH}, SR.1 and SR.4 will be set to "1". Word/byte write operations with V_{IH}<RP#<V_{HH} produce spurious results and should not be attempted.

4.7 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or word/byte write data in another block of memory. Once the block-erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/BY# will also transition to High Z. Specification t_{WHRZ2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Word/Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Word/Byte Write Suspend command (see Section 4.8), a word/byte write operation can also be suspended. During a word/byte write operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/BY# output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 7). V_{PP} must remain at $V_{PPH1/2}$ (the same V_{PP} level used for block erase) while block erase is suspended. RP# must also remain at V_{IH} or V_{HH} (the same RP# level used for block erase). WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for block erase). Block erase cannot resume until word/byte write operations initiated during block erase suspend have completed.

4.8 Word/Byte Write Suspend Command

The Word/Byte Write Suspend command allows word/byte write interruption to read data in other flash memory locations. Once the word/byte write process starts, writing the Word/Byte Write Suspend command requests that the WSM suspend the word/byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word/Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word/byte write operation has been suspended (both will be set to "1"). RY/BY# will also transition to High Z. Specification t_{WHRZ1} defines the word/byte write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word/byte write is suspended are Read Status Register and Word/Byte Write Resume. After Word/Byte Write Resume command is written to the flash memory, the WSM will continue the word/byte write process. Status register bits SR.2 and SR.7 will automatically clear and RY/BY# will return to V_{OL}. After the Word/Byte Write Resume command is written, the device automatically outputs status register data when read (see Figure 8). V_{PP} must remain at $V_{PPH1/2}$ (the same V_{PP} level used for word/byte write) while in word/byte write suspend mode. RP# must also remain at V_{IH} or V_{HH} (the same RP# level used for word/byte write). WP# must also remain at V_{IL} or V_{IH} (the same WP# level used for word/byte write).

4.9 Considerations of Suspend

After the suspend command write to the CUI, read status register command has to write to CUI, then status register bit SR.6 or SR.2 should be checked for places the device in suspend mode.

4.10 Block Locking

This Boot Block Flash memory architecture features two hardware-lockable boot blocks so that the kernel code for the system can be kept secure while other blocks are programmed or erased as necessary.

4.10.1 $V_{PP}=V_{IL}$ for Complete Protection

The V_{PP} programming voltage can be held low for complete write protection of all blocks in the flash device.

4.10.2 $WP\#=V_{IL}$ for Block Locking

The lockable blocks are locked when $WP\#=V_{IL}$; any program or erase operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two boot blocks are lockable. For the bottom configuration, the bottom tow boot blocks are lockable. Unlocked blocks can be programmed or erased normally (Unless V_{PP} is below V_{PPLK}).

4.10.3 $WP\#=V_{IH}$ for Block Unlocking

$WP\#=V_{IH}$ unlocks all lockable blocks.

These blocks can now be programmed or erased.

WP# controls 2 boot blocks locking and V_{PP} provides protection against spurious writes. Table 6 defines the write protection methods.

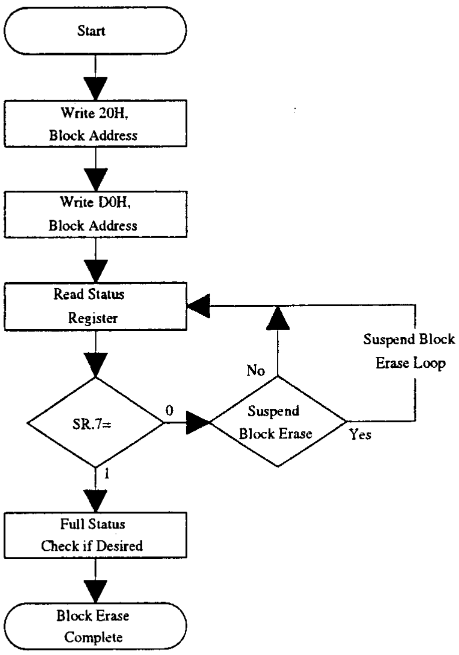
Table 6. Write Protection Alternatives

Operation	V_{PP}	RP#	WP#	Effect
Block Erase or Word/Byte Write	V_{IL}	X	X	All Blocks Locked.
	$>V_{PPLK}$	V_{IL}	X	All Blocks Locked.
		V_{HH}	X	All Blocks Unlocked.
		V_{IH}	V_{IL}	2 Boot Blocks Locked.
			V_{IH}	All Blocks Unlocked.

Table 7. Status Register Definition

WSMS	ESS	ES	WBWS	VPPS	WBWSS	DPS	R
7	6	5	4	3	2	1	0

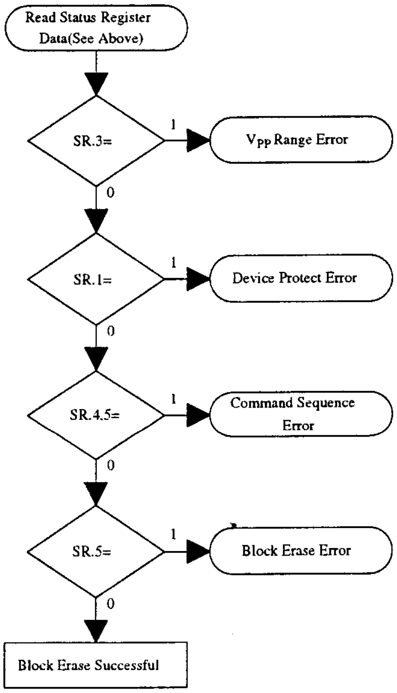
	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check RY/BY# or SR.7 to determine block erase or word/byte write completion. SR.6-0 are invalid while SR.7="0".
SR.6 = ERASE SUSPEND STATUS (ESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5 = ERASE STATUS (ES) 1 = Error in Block Erasure 0 = Successful Block Erase	If both SR.5 and SR.4 are "1"s after a block erase attempt, an improper command sequence was entered.
SR.4 = WORD/BYTE WRITE STATUS (WBWS) 1 = Error in Word/Byte Write 0 = Successful Word/Byte Write	
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase or Word/Byte Write command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP} \neq V_{PPH1/2}$.
SR.2 = WORD/BYTE WRITE SUSPEND STATUS (WBWSS) 1 = Word/Byte Write Suspended 0 = Word/Byte Write in Progress/Completed	
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = WP# or RP# Lock Detected, Operation Abort 0 = Unlock	The WSM interrogates the WP# and RP# only after Block Erase or Word/Byte Write command sequences. It informs the system, depending on the attempted operation, if the WP# is not V_{IH}, RP# is not V_{HH}.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.0 is reserved for future use and should be masked out when polling the status register.


Start
Write 20H,
Block Address
Write D0H,
Block Address
Read Status
Register
SR.7=
0
1
Suspend
Block Erase
No
Yes
Suspend Block
Erase Loop
Full Status
Check if Desired
Block Erase
Complete

Bus Operation	Command	Comments
Write	Erase Setup	Data=20H Addr=Within Block to be Erased
Write	Erase Confirm	Data=D0H Addr=Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent block erasures.
Full status check can be done after each block erase or after a sequence of block erasures.
Write FFH after the last operation to place device in read array mode.

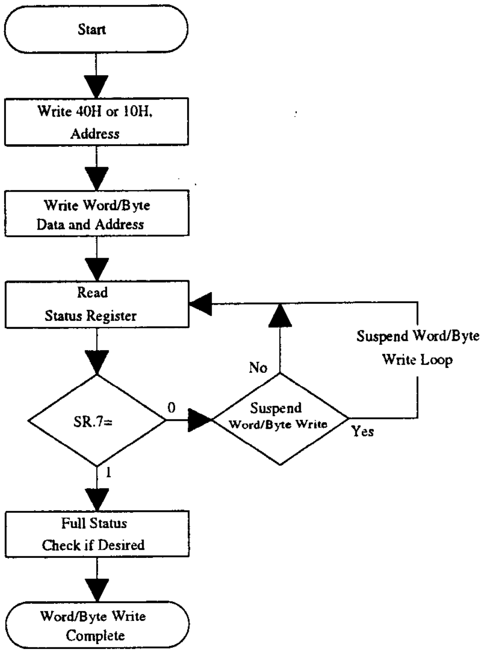
FULL STATUS CHECK PROCEDURE


Read Status Register
Data(See Above)
SR.3=
1
Vpp Range Error
0
SR.1=
1
Device Protect Error
0
SR.4,5=
1
Command Sequence
Error
0
SR.5=
1
Block Erase Error
0
Block Erase Successful

Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Block Erase Error

SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

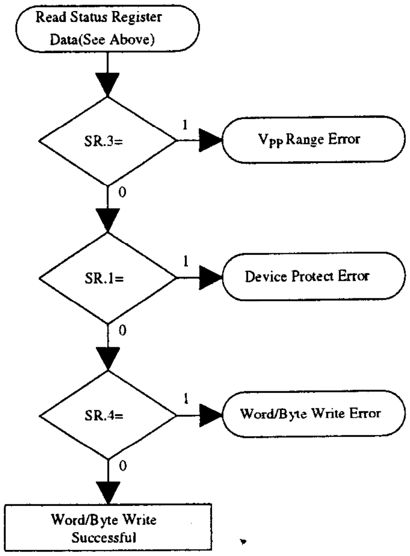
Figure 5. Automated Block Erase Flowchart


Start
Write 40H or 10H, Address
Write Word/Byte Data and Address
Read Status Register
SR.7=
0
1
Suspend Word/Byte Write
No
Yes
Suspend Word/Byte Write Loop
Full Status Check if Desired
Word/Byte Write Complete

Bus Operation	Command	Comments
Write	Setup Word/Byte Write	Data=40H or 10H Addr=Location to Be Written
Write	Word/Byte Write	Data=Data to Be Written Addr=Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent byte writes.
SR full status check can be done after each Word/Byte write, or after a sequence of Word/Byte writes.
Write FFH after the last Word/Byte write operation to place device in read array mode.

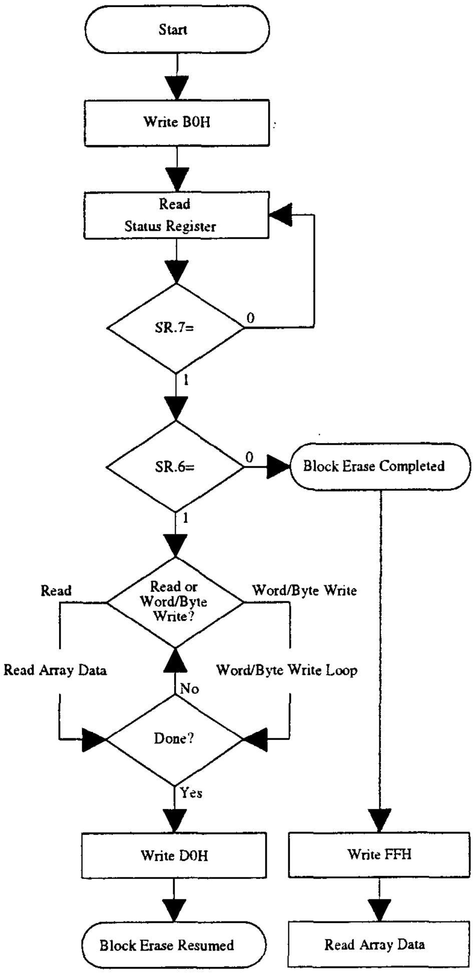
FULL STATUS CHECK PROCEDURE


Read Status Register Data(See Above)
SR.3=
1
Vpp Range Error
0
SR.1=
1
Device Protect Error
0
SR.4=
1
Word/Byte Write Error
0
Word/Byte Write Successful

Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4 1=Data Write Error

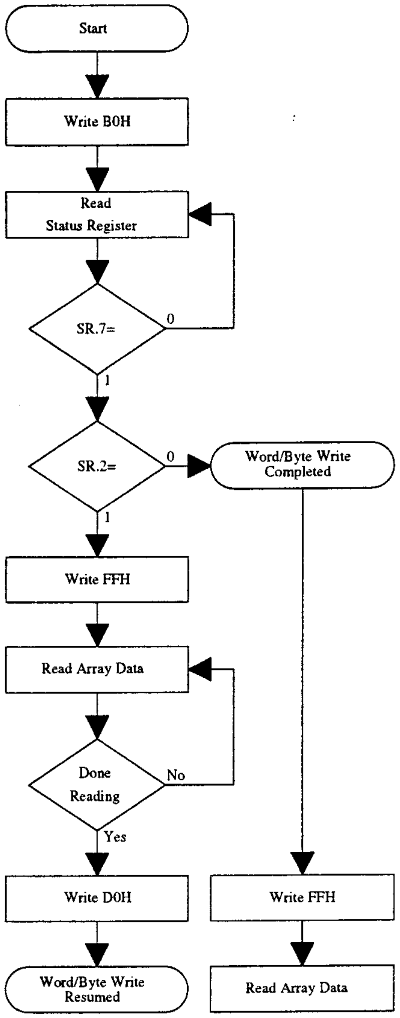
SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 6. Automated Word/Byte Write Flowchart


Start
Write B0H
Read
Status Register
SR.7=
0
1
SR.6=
0
1
Block Erase Completed
Read or
Word/Byte
Write?
Read
Word/Byte Write
Read Array Data
Word/Byte Write Loop
No
Done?
Yes
Write D0H
Write FFH
Block Erase Resumed
Read Array Data

Bus Operation	Command	Comments
Write	Erase Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Write	Erase Resume	Data=D0H Addr=X

Figure 7. Block Erase Suspend/Resume Flowchart


Start
Write B0H
Read
Status Register
SR.7=
0
1
SR.2=
0
1
Word/Byte Write
Completed
Write FFH
Read Array Data
Done
Reading
No
Yes
Write D0H
Word/Byte Write
Resumed
Write FFH
Read Array Data

Bus Operation	Command	Comments
Write	Word/Byte Write Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=Word/Byte Write Suspended 0=Word/Byte Write Completed
Write	Read Array	Data=FFH Addr=X
Read		Read Array locations other than that being written.
Write	Word/Byte Write Resume	Data=D0H Addr=X

Figure 8. Word/Byte Write Suspend/Resume Flowchart

5 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

a. Lowest possible memory power dissipation.
b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 RY/BY#, Block Erase and Word/Byte Write Polling

RY/BY# is an open drain output that should be connected to V_{CC} by a pulllup resistor to provide a hardware method of detecting block erase and word/byte write completion. It transitions low after block erase or word/byte write commands and returns to High Z when the WSM has finished executing the internal algorithm.

RY/BY# can be connected to an interrupt input of the system CPU or controller. It is active at all times. RY/BY# is also High Z when the device is in block erase suspend (with word/byte write inactive), word/byte write suspend or deep power-down modes.

5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1µF ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.4 V_{PP} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} Power supply trace. The V_{PP} pin supplies the memory cell current for word/byte writing and block erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

5.5 V_{CC}, V_{PP}, RP# Transitions

Block erase and word/byte write are not guaranteed if V_{PP} falls outside of a valid $V_{PPH1/2}$ range, V_{CC} falls outside of a valid 2.7V-3.6V range, or RP#≠V_{IH} or V_{HH}. If V_{PP} error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If RP# transitions to V_{IL} during block erase or word/byte write, RY/BY# will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or RP# transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}.

After block erase or word/byte write, even after V_{PP} transitions down to V_{PPLK}, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block erasure or word/byte writing during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{CC}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

WP# provide additional protection from inadvertent code or data alteration. The device is disabled while RP#=V_{IL} regardless of its control inputs state.

5.7 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering RP# to V_{IL} standby or sleep modes. If access is again needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after RP# is first raised to V_{IH}. See AC Characteristics– Read Only and Write Operations and Figures 11, 12, 13 and 14 for more information.

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

Operating Temperature
  During Read, Block Erase and
  Word/Byte Write .... -40°C to +85°C[1]
  Temperature under Bias .... -40°C to +85°C

Storage Temperature .... -65°C to +125°C

Voltage On Any Pin
  (except V_{CC}, V_{PP}, and RP#) ..... -0.5V to V_{CC}+0.5V[2]

V_{CC} Supply Voltage .... -0.2V to +3.9V[2]

V_{PP} Update Voltage during Block
  Erase and Word/Byte Write .... -0.2V to +14.0V[2,3]

RP# Voltage .... -0.5V to +14.0V[2,3]

Output Short Circuit Current .... 100mA[4]

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
3. Maximum DC voltage on V_{PP} and RP# may overshoot to +14.0V for periods <20ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Test Condition
T_A	Operating Temperature	-40	+85	°C	Ambient Temperature
V_{CC}	V_{CC} Supply Voltage (2.7V-3.6V)	2.7	3.6	V	

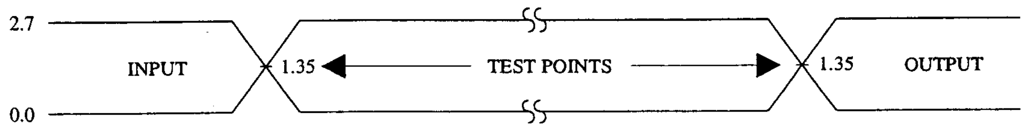
6.2.1 CAPACITANCE(1)

T_A=+25°C, f=1MHz

Symbol	Parameter	Typ.	Max.	Unit	Condition
C_{IN}	Input Capacitance	7	10	pF	V_{IN}=0.0V
C_{OUT}	Output Capacitance	9	12	pF	V_{OUT}=0.0V

NOTE:
1. Sampled, not 100% tested.

6.2.2 AC INPUT/OUTPUT TEST CONDITIONS


2.7
0.0
INPUT
1.35
TEST POINTS
1.35
OUTPUT

AC test inputs are driven at 2.7V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.35V. Input rise and fall times (10% to 90%) <10 ns.

Figure 9. Transient Input/Output Reference Waveform for V_{CC}=2.7V-3.6V

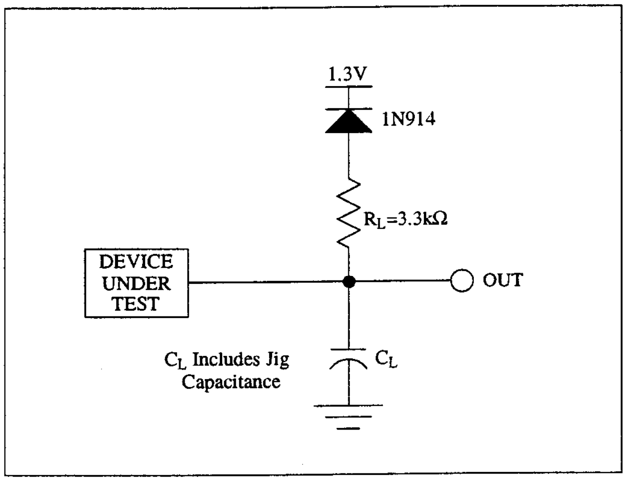

1.3V
1N914
R_L=3.3kΩ
DEVICE UNDER TEST
OUT
C_L Includes Jig Capacitance
C_L

Figure 10. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

Test Configuration	C_L(pF)
V_{CC}=2.7V-3.6V	30

6.2.3 DC CHARACTERISTICS

DC Characteristics

Sym.	Parameter	Notes	V_{CC}=2.7V-3.6V		Unit	Test Conditions
			Typ.	Max.		
I_{LI}	Input Load Current	1		±0.5	µA	V_{CC}=V_{CC}Max. V_{IN}=V_{CC} or GND
I_{LO}	Output Leakage Current	1		±0.5	µA	V_{CC}=V_{CC}Max. V_{OUT}=V_{CC} or GND
I_{CCS}	V_{CC} Standby Current	1,3,6, 10	25	50	µA	CMOS Inputs V_{CC}=V_{CC}Max. CE#=RP#=V_{CC}±0.2V
		1,3,6	0.2	2	mA	TTL Inputs V_{CC}=V_{CC}Max. CE#=RP#=V_{IH}
I_{CCD}	V_{CC} Deep Power-Down Current	1,10	5	10	µA	RP#=GND±0.2V I_{OUT}(RY/BY#)=0mA
I_{CCR}	V_{CC} Read Current	1,5,6		25	mA	CMOS Inputs V_{CC}=V_{CC}Max., CE#=GND f=5MHz, I_{OUT}=0mA
				30	mA	TTL Inputs V_{CC}=V_{CC}Max., CE#=GND f=5MHz, I_{OUT}=0mA
I_{CCW}	V_{CC} Word/Byte Write Current	1,7		17	mA	V_{PP}=2.7V-3.6V
				12	mA	V_{PP}=11.4V-12.6V
I_{CCE}	V_{CC} Block Erase Current	1,7		17	mA	V_{PP}=2.7V-3.6V
				12	mA	V_{PP}=11.4V-12.6V
I_{CCWS} I_{CCES}	V_{CC} Word/Byte Write or Block Erase Suspend Current	1,2		6	mA	CE#=V_{IH}
I_{PPS}	V_{PP} Standby or Read Current	1	±2	±15	µA	V_{PP}≤V_{CC}
I_{PPR}			10	200	µA	V_{PP}>V_{CC}
I_{PPD}	V_{PP} Deep Power-Down Current	1	0.1	5	µA	RP#=GND±0.2V, V_{PP}≤V_{CC}
			10	150	µA	RP#=GND±0.2V, V_{PP}>V_{CC}
I_{PPW}	V_{PP} Word/Byte Write Current	1,7	12	40	mA	V_{PP}=2.7V-3.6V
				30	mA	V_{PP}=11.4V-12.6V
I_{PPE}	V_{PP} Block Erase Current	1,7	8	25	mA	V_{PP}=2.7V-3.6V
				20	mA	V_{PP}=11.4V-12.6V
I_{PPWS} I_{PPES}	V_{PP} Word/Byte Write or Block Erase Suspend Current	1	10	200	µA	V_{PP}=$V_{PPH1/2}$

DC Characteristics (Continued)

Sym.	Parameter	Notes	V_{CC}=2.7V-3.6V Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	7	-0.5	0.8	V	
V_{IH}	Input High Voltage	7	0.7 V_{CC}	V_{CC}+0.3	V	
V_{OL}	Output Low Voltage	3,7		0.4	V	$V_{CC}=V_{CC}$ Min. I_{OL}=2.0mA
V_{OH1}	Output High Voltage	3,7	0.85 V_{CC}		V	$V_{CC}=V_{CC}$ Min. I_{OH}=-2.0mA
			V_{CC}-0.2		V	$V_{CC}=V_{CC}$ Min. I_{OH}=-100μA
V_{PPLK}	V_{PP} Lockout Voltage during Normal Operations	4,7		1.5	V	
V_{PPH1}	V_{PP} Voltage during Word/Byte Write or Block Erase Operations		2.7	3.6	V	
V_{PPH2}	V_{PP} Voltage during Word/Byte Write or Block Erase Operations		11.4	12.6	V	
V_{LKO}	V_{CC} Lockout Voltage		1.5		V	
V_{HH}	RP# Unlock Voltage	8,9	11.4	12.6	V	Unavailable WP#

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and T_A=+25°C.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or word/byte written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Includes RY/BY#.
4. Block erases and word/byte writes are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed in the range between V_{PPLK}(max.) and V_{PPH1}(min.), between V_{PPH1}(max.) and V_{PPH2}(min.) and above V_{PPH2}(max.).
5. Automatic Power Savings (APS) reduces typical I_{CCR} to 3mA in static operation.
6. CMOS inputs are either V_{CC}±0.2V or GND±0.2V. TTL inputs are either V_{IL} or V_{IH}.
7. Sampled, not 100% tested.
8. Boot block erases and word/byte writes are inhibited when the corresponding RP#=V_{IH} and WP#=V_{IL}. Block erase and word/byte write operations are not guaranteed with V_{IH}<RP#<V_{HH} and should not be attempted.
9. RP# connection to a V_{HH} supply is allowed for a maximum cumulative period of 80 hours.
10. BYTE# input level is V_{CC}±0.2V in word mode or GND±0.2V in byte mode. WP# input level is V_{CC}±0.2V or GND±0.2V.

6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS(1)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		90		ns
t_{AVQV}	Address to Output Delay			90	ns
t_{ELQV}	CE# to Output Delay	2		90	ns
t_{PHQV}	RP# High to Output Delay			10	µs
t_{GLQV}	OE# to Output Delay	2		45	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# High to Output in High Z	3		45	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# High to Output in High Z	3		20	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns
t_{FVQV}	BYTE# to Output Delay	3		90	ns
t_{FLQZ}	BYTE# Low to Output in High Z	3		30	ns
t_{ELFV}	CE# to BYTE# High or Low	3,4		5	ns

NOTES:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. If BYTE# transfer during reading cycle, exist the regulations separately.

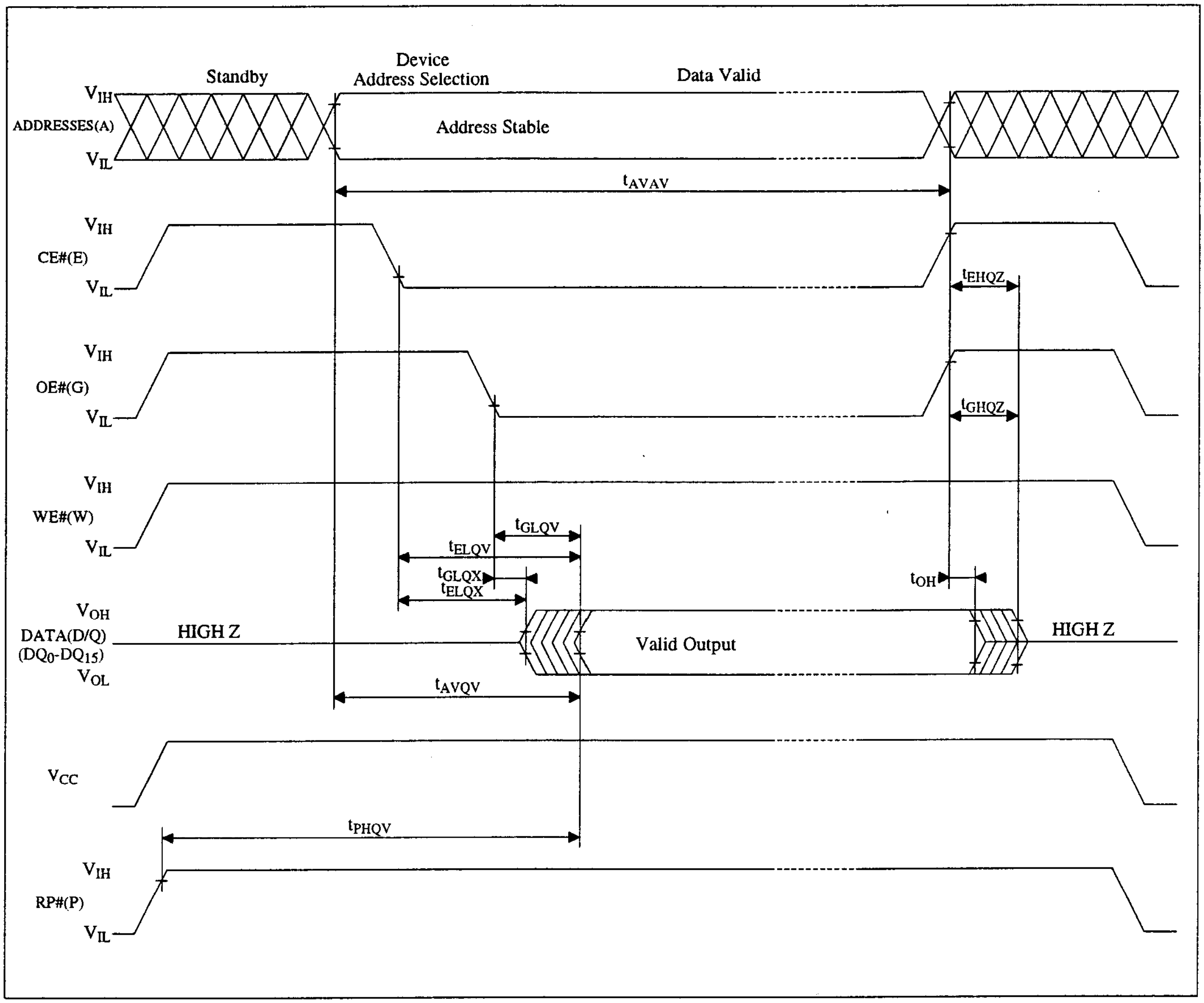

Standby
Device Address Selection
Data Valid
V_IH
ADDRESSES(A)
V_IL
Address Stable
t_AVAV
CE#(E)
t_EHQZ
OE#(G)
t_GHQZ
WE#(W)
t_GLQV
t_ELQV
t_GLQX
t_ELQX
t_OH
V_OH
DATA(D/Q)
(DQ0-DQ15)
V_OL
HIGH Z
Valid Output
HIGH Z
t_AVQV
V_CC
t_PHQV
RP#(P)

Figure 11. AC Waveform for Read Operations

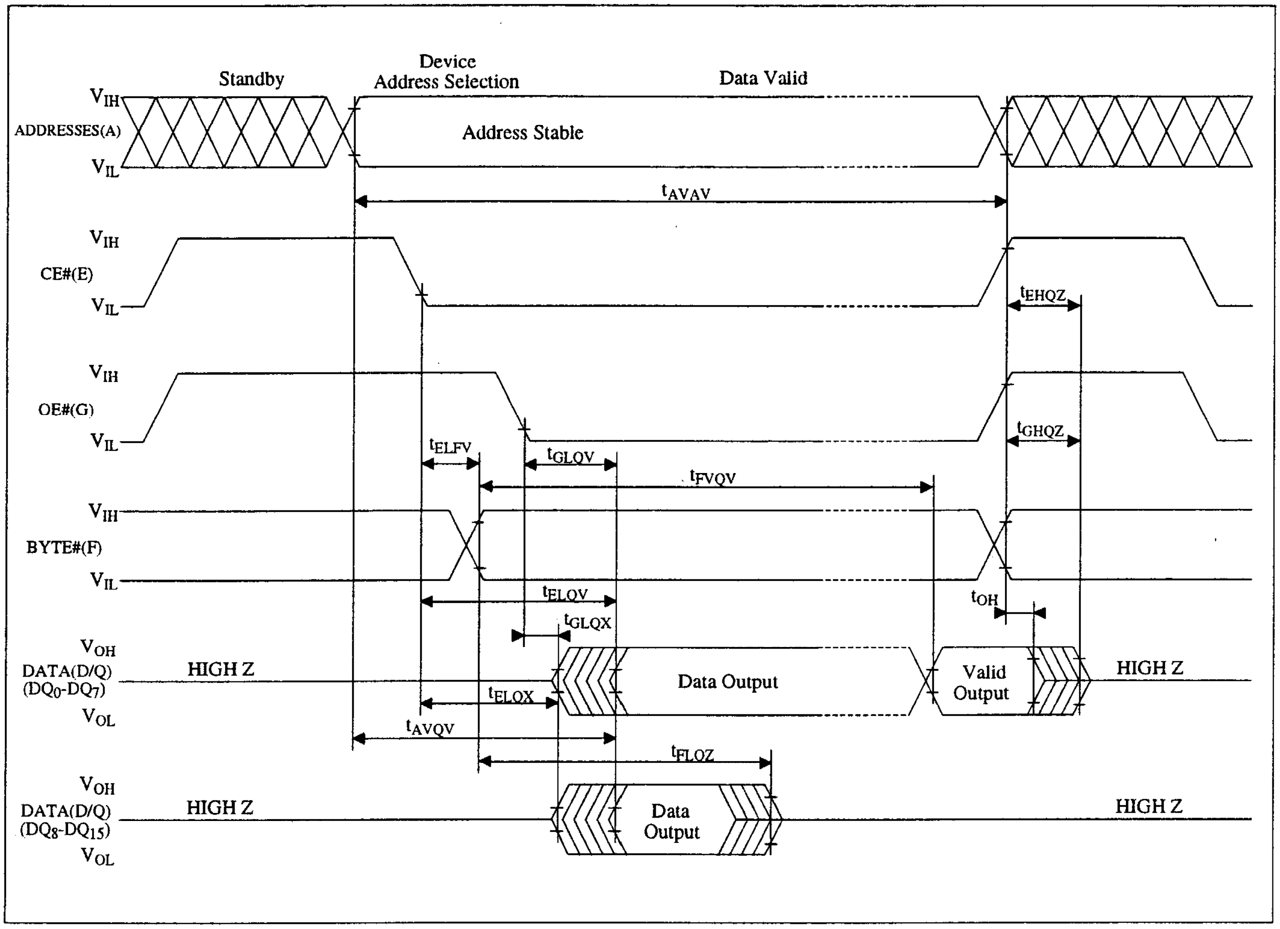

Standby
Device Address Selection
Data Valid
ADDRESSES(A)
Address Stable
V_{IH}
V_{IL}
t_{AVAV}
CE#(E)
t_{EHQZ}
OE#(G)
t_{GHQZ}
t_{ELFV}
t_{GLQV}
t_{FVQV}
BYTE#(F)
t_{ELQV}
t_{GLQX}
t_{OH}
V_{OH}
DATA(D/Q) (DQ_0-DQ_7)
V_{OL}
HIGH Z
Data Output
Valid Output
HIGH Z
t_{ELQX}
t_{AVQV}
t_{FLQZ}
DATA(D/Q) (DQ_8-DQ_{15})
HIGH Z
Data Output
HIGH Z

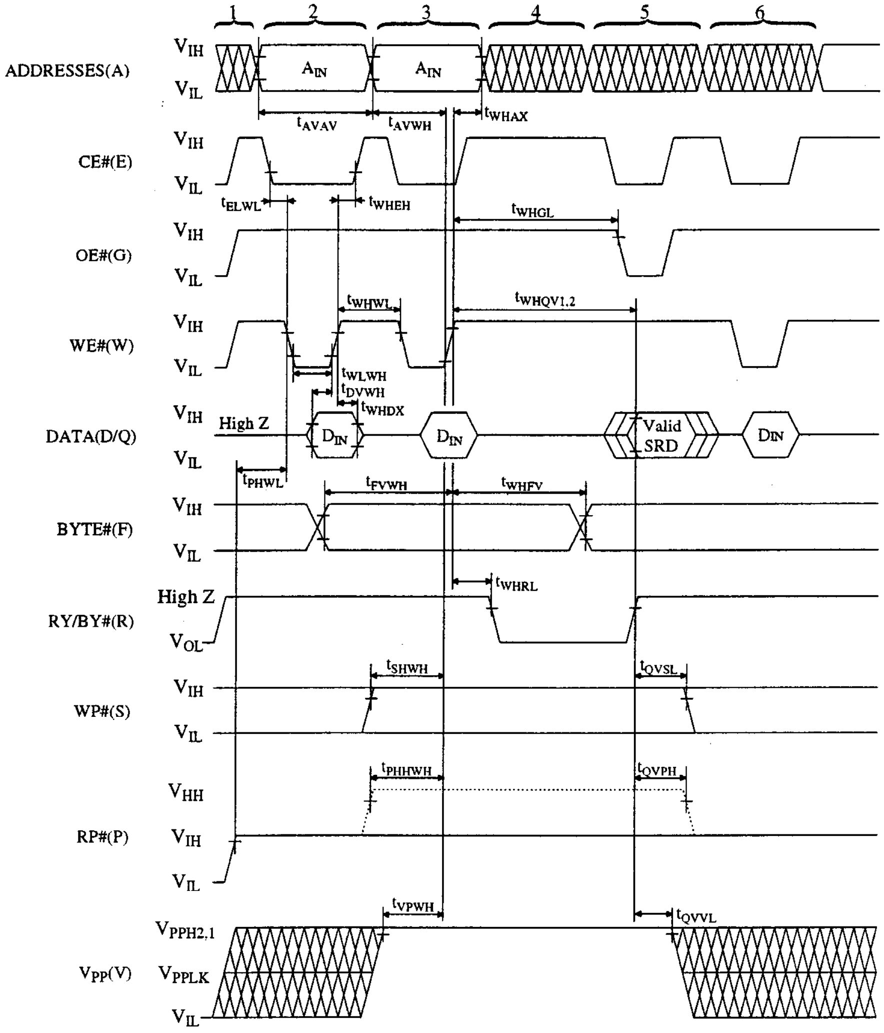
Figure 12. BYTE# timing Waveform

6.2.5 AC CHARACTERISTICS - WRITE OPERATIONS(1)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		90		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	10		µs
t_{ELWL}	CE# Setup to WE# Going Low		0		ns
t_{WLWH}	WE# Pulse Width		50		ns
t_{PHHWH}	RP# V_{HH} Setup to WE# Going High	2	100		ns
t_{SHWH}	WP# V_{IH} Setup to WE# Going High	2	100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	2	100		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		ns
t_{DVWH}	Data Setup to WE# Going High	3	50		ns
t_{WHDX}	Data Hold from WE# High		0		ns
t_{WHAX}	Address Hold from WE# High		0		ns
t_{WHEH}	CE# Hold from WE# High		0		ns
t_{WHWL}	WE# Pulse Width High		30		ns
t_{WHRL}	WE# High to RY/BY# Going Low			100	ns
t_{WHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High Z	2,4	0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High Z	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, RY/BY# High Z	2,4	0		ns
t_{FVWH}	BYTE# Setup to WE# Going High	5	50		ns
t_{WHFV}	BYTE# Hold from WE# High	5	90		ns

NOTES:
1. Read timing characteristics during block erase and word/byte write operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase or word/byte write.
4. V_{PP} should be held at $V_{PPH1/2}$ (and if necessary RP# should be held at V_{HH}) until determination of block erase or word/byte write success (SR.1/3/4/5=0).
5. If BYTE# switch during reading cycle, exist the regulations separately.


1
2
3
4
5
6
ADDRESSES(A)
VIH
VIL
AIN
AIN
tAVAV
tAVWH
tWHAX
CE#(E)
tELWL
tWHEH
tWHGL
OE#(G)
tWHWL
tWHQV1,2
WE#(W)
tWLWH
tDVWH
tWHDX
DATA(D/Q)
High Z
DIN
DIN
Valid SRD
DIN
tPHWL
tFVWH
tWHFV
BYTE#(F)
High Z
VOL
tWHRL
RY/BY#(R)
tSHWH
tQVSL
WP#(S)
VHH
tPHHWH
tQVPH
RP#(P)
tVPWH
tQVVL
VPPH2,1
VPPLK
VPP(V)

NOTES:

1. V_{CC} power-up and standby.
2. Write block erase or word/byte write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Figure 13. AC Waveform for WE#-Controlled Write Operations

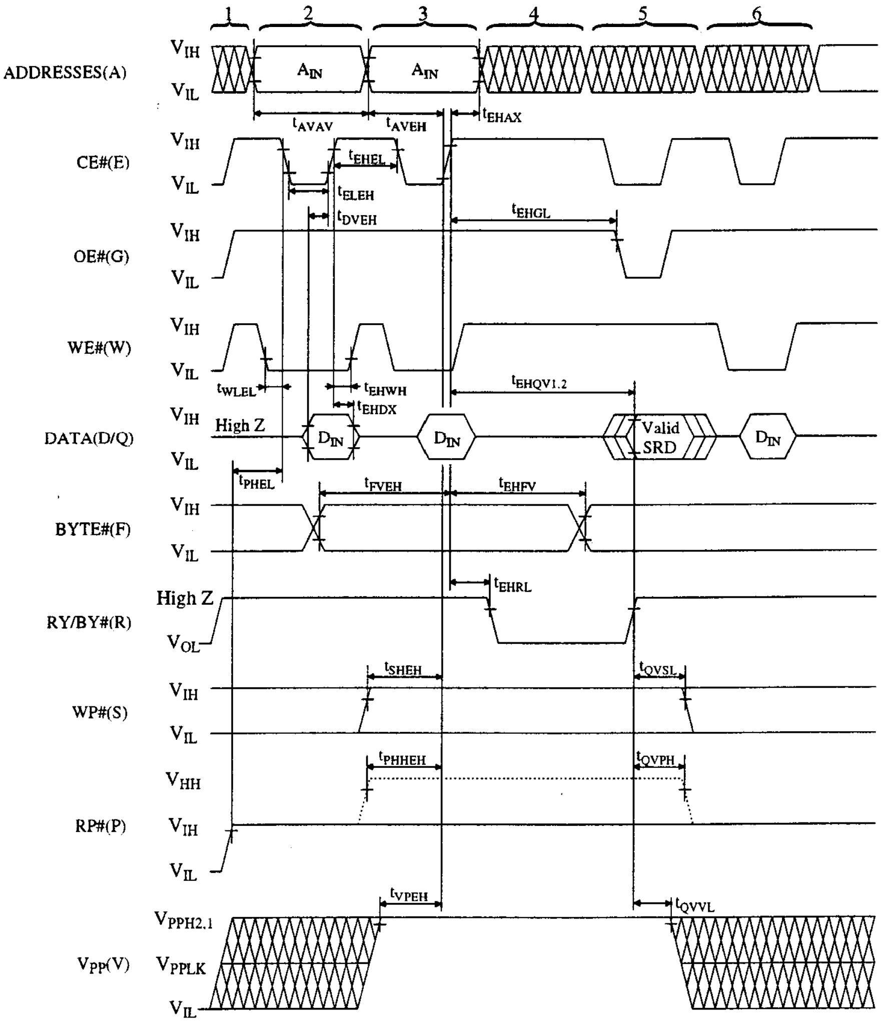
6.2.6 ALTERNATIVE CE#-CONTROLLED WRITES(1)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		90		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	10		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		ns
t_{ELEH}	CE# Pulse Width		70		ns
t_{PHHEH}	RP# V_{HH} Setup to CE# Going High	2	100		ns
t_{SHEH}	WP# V_{IH} Setup to CE# Going High	2	100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	2	100		ns
t_{AVEH}	Address Setup to CE# Going High	3	50		ns
t_{DVEH}	Data Setup to CE# Going High	3	50		ns
t_{EHDX}	Data Hold from CE# High		0		ns
t_{EHAX}	Address Hold from CE# High		0		ns
t_{EHWH}	WE# Hold from CE# High		0		ns
t_{EHEL}	CE# Pulse Width High		25		ns
t_{EHRL}	CE# High to RY/BY# Going Low			100	ns
t_{EHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/BY# High Z	2,4	0		ns
t_{QVPH}	RP# V_{HH} Hold from Valid SRD, RY/BY# High Z	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, RY/BY# High Z	2,4	0		ns
t_{FVEH}	BYTE# Setup to CE# Going High	5	50		ns
t_{EHFV}	BYTE# Hold from CE# High	5	90		ns

NOTES:

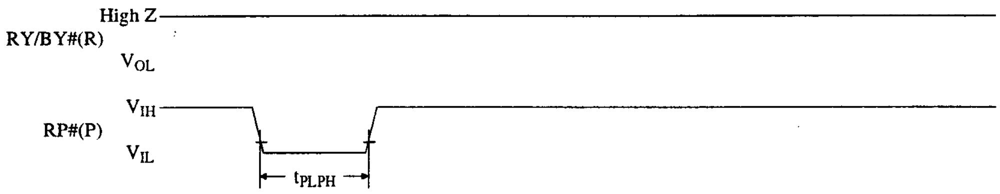
1. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold, and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase or word/byte write.
4. V_{PP} should be held at $V_{PPH1/2}$ (and if necessary RP# should be held at V_{HH}) until determination of block erase or word/byte write success (SR.1/3/4/5=0).
5. If BYTE# switch during reading cycle, exist the regulations separately.


1
2
3
4
5
6
ADDRESSES(A)
V_{IH}
V_{IL}
A_{IN}
A_{IN}
t_{AVAV}
t_{AVEH}
t_{EHAX}
CE#(E)
V_{IH}
V_{IL}
t_{EHEL}
t_{ELEH}
t_{DVEH}
t_{EHGL}
OE#(G)
V_{IH}
V_{IL}
WE#(W)
V_{IH}
V_{IL}
t_{WLEL}
t_{EHWH}
t_{EHDX}
$t_{EHQV1,2}$
DATA(D/Q)
V_{IH}
V_{IL}
High Z
D_{IN}
D_{IN}
Valid SRD
D_{IN}
t_{PHEL}
t_{FVEH}
t_{EHFV}
BYTE#(F)
V_{IH}
V_{IL}
t_{EHRL}
RY/BY#(R)
High Z
V_{OL}
t_{SHEH}
t_{QVSL}
WP#(S)
V_{IH}
V_{IL}
t_{PHHEH}
t_{QVPH}
RP#(P)
V_{HH}
V_{IH}
V_{IL}
t_{VPEH}
t_{QVVL}
$V_{PP}(V)$
$V_{PPH2,1}$
V_{PPLK}
V_{IL}

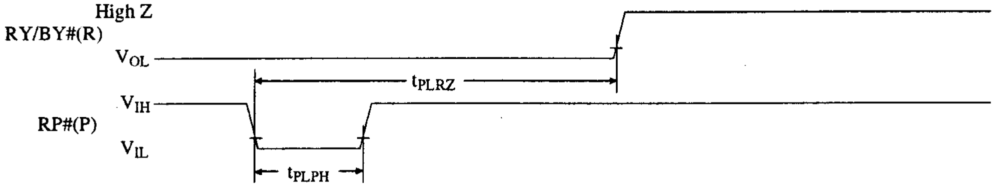
NOTES:
1. V_{CC} power-up and standby.
2. Write block erase or word/byte write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Figure 14. AC Waveform for CE#-Controlled Write Operations

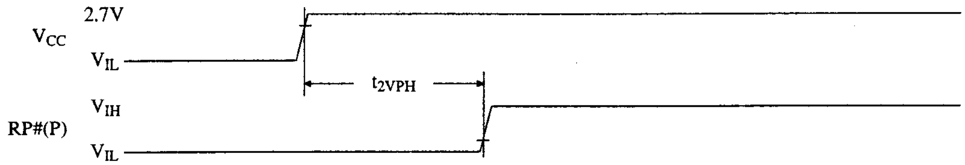
6.2.7 RESET OPERATIONS


High Z
RY/BY#(R)
V_{OL}
V_{IH}
RP#(P)
V_{IL}
t_{PLPH}

(A)Reset During Read Array Mode


High Z
RY/BY#(R)
V_{OL}
t_{PLRZ}
V_{IH}
RP#(P)
V_{IL}
t_{PLPH}

(B)Reset During Block Erase or Word/Byte Write


2.7V
V_{CC}
V_{IL}
t_{2VPH}
V_{IH}
RP#(P)
V_{IL}

(C)RP# rising Timing

Figure 15. AC Waveform for Reset Operation

Reset AC Specifications

Sym.	Parameter	Notes	V_{CC}=2.7V-3.6V		Unit
			Min.	Max.	
t_{PLPH}	RP# Pulse Low Time (If RP# is tied to V_{CC}, this specification is not applicable)		100		ns
t_{PLRZ}	RP# Low to Reset during Block Erase or Word/Byte Write	1,2		23.6	µs
t_{2VPH}	V_{CC} 2.7V to RP# High	3	100		ns

NOTES:

1. If RP# is asserted while a block erase or word/byte write operation is not executing, the reset will complete within 100ns.
2. A reset time, t_{PHQV}, is required from the later of RY/BY# going High Z or RP# going high until outputs are valid.
3. When the device power-up, holding RP# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

6.2.8 BLOCK ERASE AND WORD/BYTE WRITE PERFORMANCE(3)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Sym.	Parameter		Notes	V_{PP}=2.7V-3.6V		V_{PP}=11.4V-12.6V		Unit
				Typ.(1)	Max.	Typ.(1)	Max.	
t_{WHQV1} t_{EHQV1}	Word/Byte Write Time	32K word Block	2	55		15		µs
		4K word Block	2	60		30		µs
	Block Write Time	32K word Block	2,4	1.8		0.6		s
		4K word Block	2,4	0.3		0.2		s
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K word Block	2	1.2		0.7		s
		4K word Block	2	0.5		0.5		s
t_{WHRZ1} t_{EHRZ1}	Word/Byte Write Suspend Latency Time to Read			7.5	8.6	6.5	7.5	µs
t_{WHRZ2} t_{EHRZ2}	Erase Suspend Latency Time to Read			19.3	23.6	11.8	15	µs

NOTES:

1. Typical values measured at T_A=+25°C and V_{CC}=3.0V, V_{PP}=3.0V or V_{CC}=3.0V, V_{PP}=12.0V. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled but not 100% tested.
4. All values are in word mode (BYTE#=V_{IH}). At byte mode (BYTE#=V_{IL}), those values are double.

7 Package and packing specification

1. Package Outline Specification
   Refer to drawing No.AA1142
2. Markings
   2－1. Marking contents
   (1) Product name : LH28F160BVHE－BTL90
   (2) Company name : SHARP
   (3) Date code
   (Example) Z YY WW ××× Indicates the product was manufactured in the WWth week of 19YY.
   ××× → Denotes the production ref.code (1~3)
   WW → Denotes the production week. (01,02,03,・・・・・52,53)
   YY → Denotes the production year. (Lower two digit of the year.)
   Z → Denotes the production ref.code (No marking , A , B , C)
   (4) "JAPAN" is marked on the package when both wafer and assembly processes are done in Japan ,indicating the country of origin.
   2－2. Marking layout
   Refer drawing No.AA1142
   (This layout does not define the dimensions of marking character and marking position.)
3. Packing Specification (Dry packing for surface mount packages)

Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).
When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package.
This dry packing is designed to prevent the above problem from occurring in surface mount packages.

3－1. Packing Materials

Material Name	Material Specificaiton	Purpose
Tray	Conductive plastic (50devices/tray)	Fixing of device
Upper cover tray	Conductive plastic (1tray/case)	Fixing of device
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
P P band	Polypropylene (3pcs/case)	Fixing of tray
Inner case	Card board (500device/case)	Packaging of device
Label	Paper	Indicates part number, quantity and date of manufacture
Outer case	Card board	Outer packing of tray

(Devices shall be placed into a tray in the same direction.)

3－2. Outline dimension of tray
Refer to attached drawing

4. Storage and Opening of Dry Packing

4－1. Store under conditions shown below before opening the dry packing
(1) Temperature range : 5～40℃
(2) Humidity : 80% RH or less

4－2. Notes on opening the dry packing
(1) Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.
(2) The tray has been treated to be conductive or anti-static. If the device is transferred to another tray, use a equivalent tray.

4－3. Storage after opening the dry packing
Perform the following to prevent absorption of moisture after opening.
(1) After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less and mount ICs within 72 hours after opening dry packing.

4－4. Baking (drying) before mounting
(1) Baking is necessary
(A) If the humidity indicator in the desiccant becomes pink
(B) If the procedure in section 4－3 could not be performed
(2) Recommended baking conditions
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16~24 hours at 120℃.
Heat resistance tray is used for shipping tray.

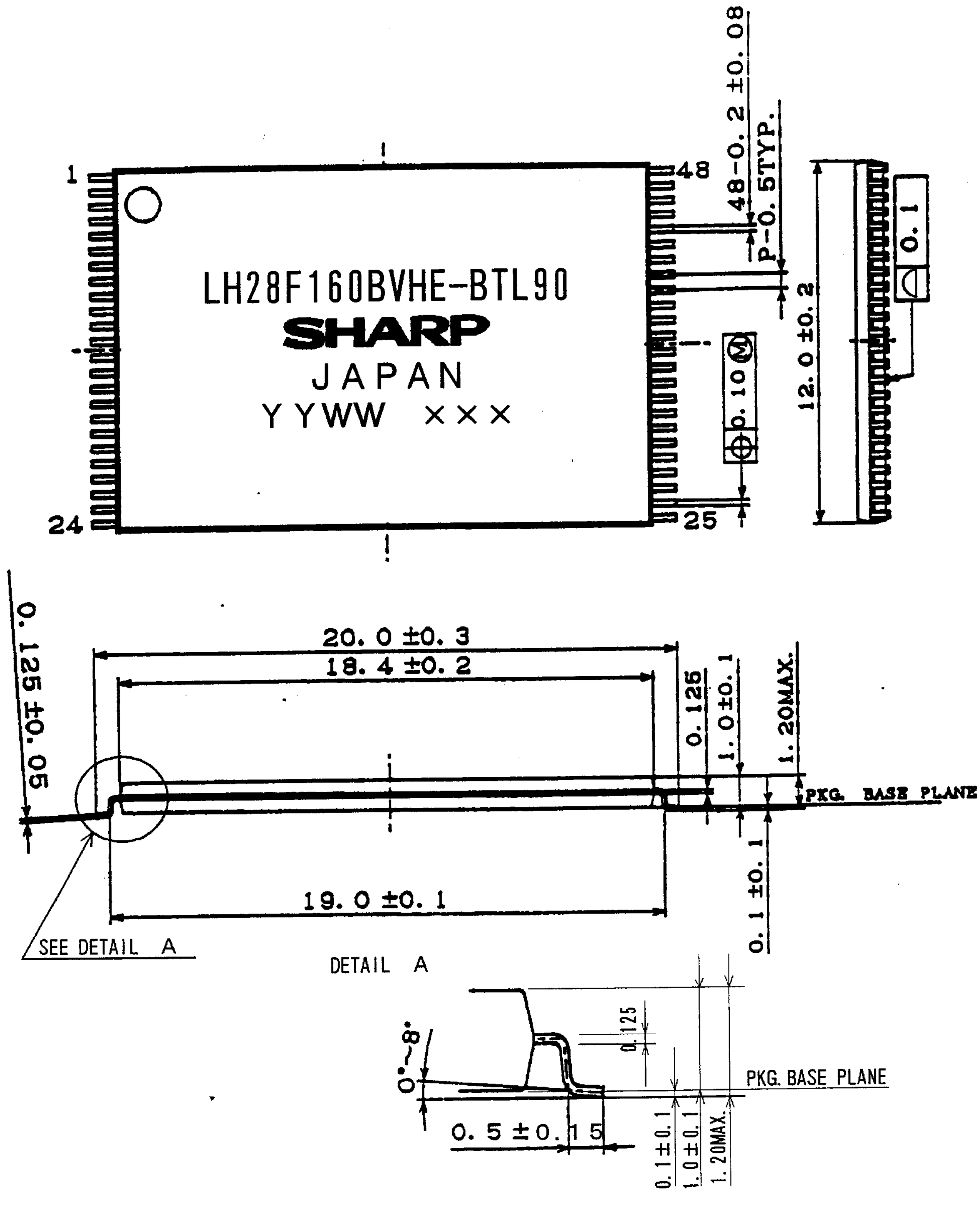
5. Surface Mount Conditions

Please perform the following conditions when mounting ICs not to deteriorate IC quality.

5－1.Soldering conditions(The following conditions are valid only for one time soldering.)

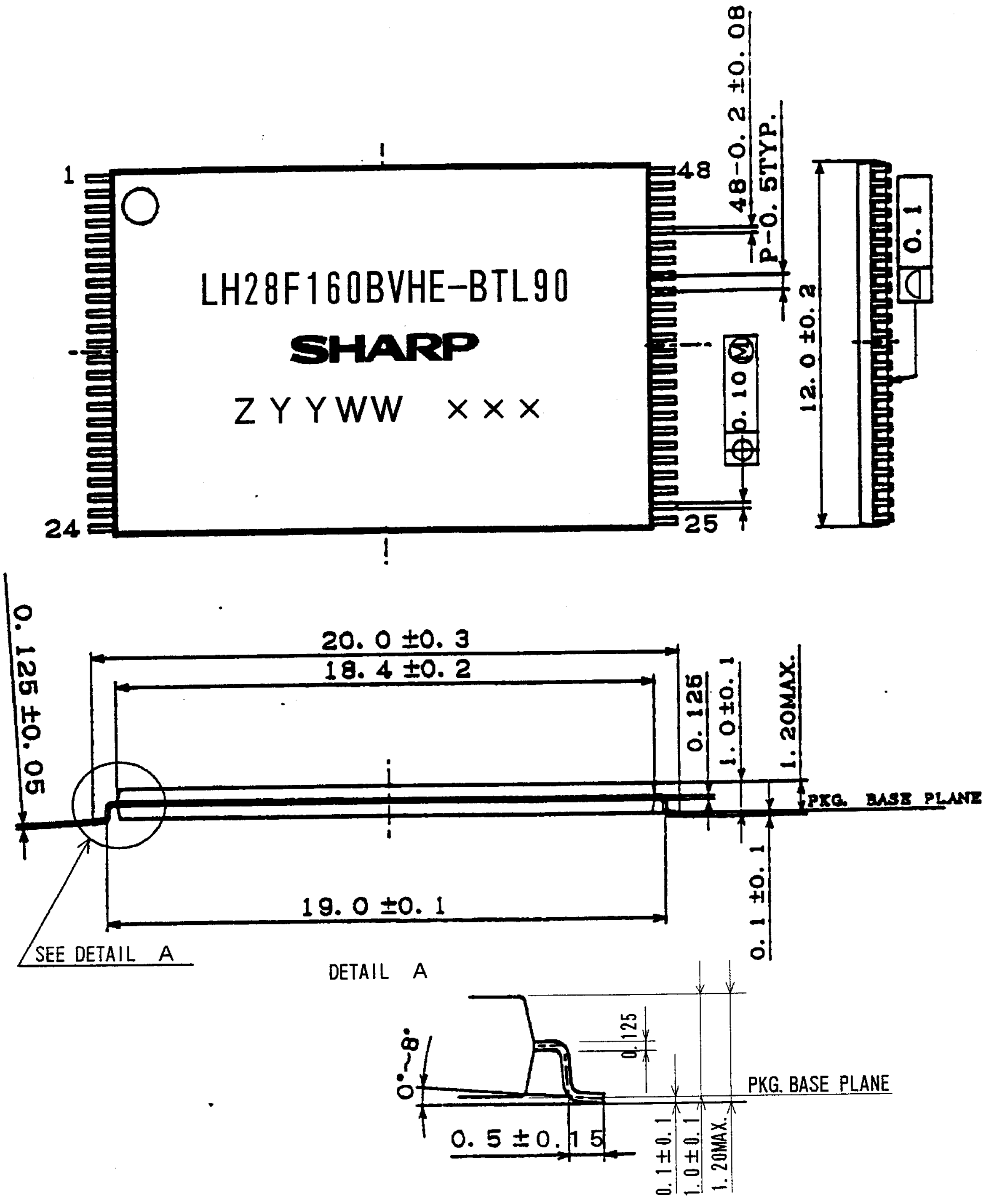
Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 230℃ or less, duration of less than 15 seconds. 200℃ or over,duration of less than 40 seconds. Temperature increase rate of 1～4℃/second	IC package surface
Manual soldering (soldering iron)	260℃ or less, duration of less than 10 seconds.	IC outer lead surface

5－2. Conditions for removal of residual flux
(1) Ultrasonic washing power : 25 Watts/liter or less
(2) Washing time : Total 1 minute maximum
(3) Solvent temperature : 15～40℃


1
48
24
25
LH28F160BVHE-BTL90
SHARP
JAPAN
YYWW ×××
48−0.2 ±0.08
P−0.5TYP.
0.1
⊕ 0.10 Ⓜ
12.0 ±0.2
0.125 ±0.05
20.0 ±0.3
18.4 ±0.2
0.125
1.0±0.1
1.20MAX.
PKG. BASE PLANE
0.1 ±0.1
19.0 ±0.1
SEE DETAIL A
DETAIL A
0°~8°
0.125
PKG. BASE PLANE
0.5 ±0.15
0.1±0.1
1.0±0.1
1.20MAX.

注記 ：『JAPAN』表記がある場合のマーク仕様
NOTES : Marking specification when “JAPAN” is marked.

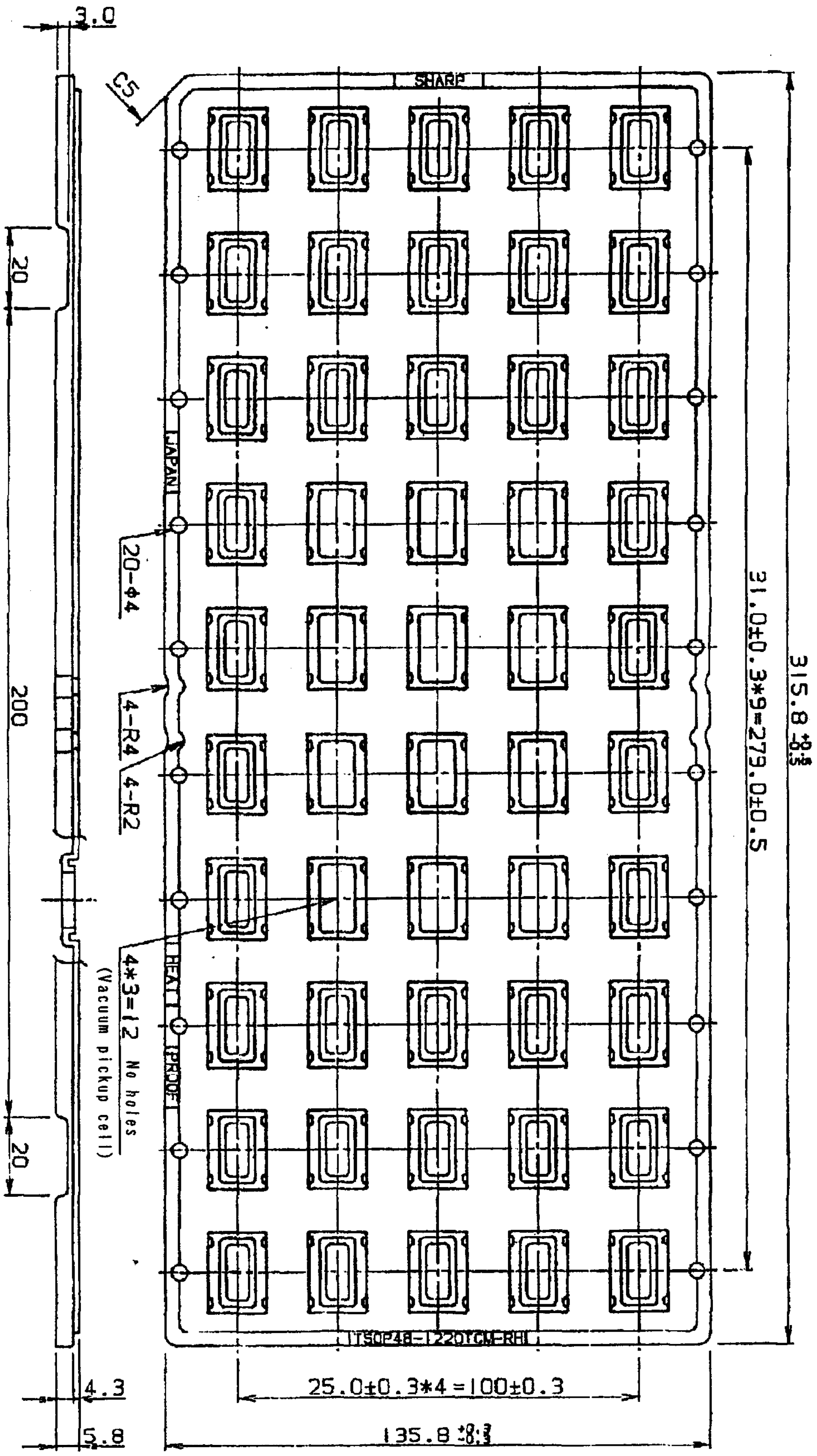
名称 NAME	TSOP48-P-1220	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 NOTE	プラスチックパッケージ外形寸法は、バリを含まないものとする。 Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1142	単位 UNIT	mm		


1
48
24
25
LH28F160BVHE-BTL90
SHARP
ZYYWW ×××
48-0.2 ±0.08
P-0.5TYP.
0.10 Ⓜ
12.0 ±0.2
0.1
0.125 ±0.05
20.0 ±0.3
18.4 ±0.2
0.125
1.0±0.1
1.20MAX.
PKG. BASE PLANE
19.0 ±0.1
0.1 ±0.1
SEE DETAIL A
DETAIL A
0°~8°
0.125
PKG. BASE PLANE
0.5 ±0.15
0.1±0.1
1.0±0.1
1.20MAX.

注記 ：『JAPAN』表記がない場合のマーク仕様

NOTES : Marking specification when "JAPAN" is not marked.

名称 NAME	TSOP48-P-1220	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。 NOTE Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA1142	単位 UNIT	mm	

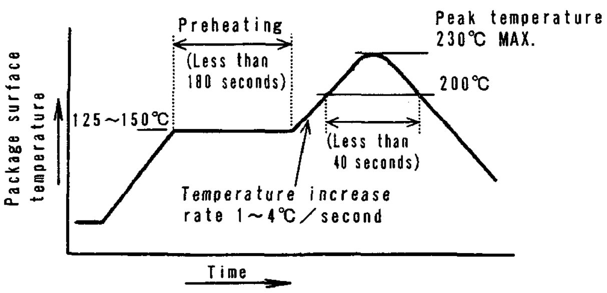

3.0
C5
SHARP
20
200
20
JAPAN
20-Φ4
4-R4
4-R2
4*3=12 No holes
(Vacuum pickup cell)
HEAT PROOF
31.0±0.3*9=279.0±0.5
315.8 +0.5 -0.5
TSOP48-1220TCM-RH
4.3
5.8
25.0±0.3*4=100±0.3
135.8 +0.3 -0.3

名称 NAME	TSOP48−1220TCM−RH			備考 NOTE
DRAWING NO.	CV756	単位 UNIT	mm	

《Supplementary data》

LHF16V11 Recommended mounting conditions for two time reflow soldering .	
Product name(Package)	LH28F160BVHE-BTL90 (TSOP48-P-1220)
Packing specification	Tray (Dry packing)
Mounting method	Reflow soldering (Air)
Reflow soldering conditions	Peak temperature of 230℃ or less. 200℃ or over, duration of less than 40 seconds. Preheat temperature of 125～150℃,duration of less than 180 seconds. Temperature increase rate of 1～4℃/second.
Measurement point	IC package surface
Storage conditions	After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less. If doing reflow soldering twice,do the first reflow soldering within 72 hours after opening dry packing and do the second reflow soldering within 72 hours after the first reflow soldering.
Note	If the above storage conditions are not applicable, bake it before reflow soldering. The recommended conditions are 16~24 hours at 120℃. (Heat resistance tray is used for shipping tray.)

Recommended Reflow Soldering(Air) Temperature Profile


Preheating
(Less than 180 seconds)
Peak temperature 230℃ MAX.
200℃
125～150℃
(Less than 40 seconds)
Temperature increase rate 1～4℃／second
Package surface temperature
Time

Flash memory LHF16BXX/16VXX family Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems.

Such noises, when induced onto WE# signal or power supply, may be interpreted as false commands, causing undesired memory updating.

To protect the data stored in the flash memory against unwanted overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

1) Protecting data in specific block

By setting a WP# to low, only the boot block can be protected against overwriting.

Parameter and main blocks cannot be locked.

System program, etc., can be locked by storing them in the boot block.

When a high voltage is applied to RP#, overwrite operation is enabled for all blocks.

For further information on controlling of WP# and RP#, refer to the specification. (See chapter 4.10)

2) Data protection through Vpp

When the level of Vpp is lower than VPPLK (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected. (See chapter 4.10.)

For the lockout voltage, refer to the specification. (See chapter 6.2.3.)

3) Data protection through RP#

When the RP# is kept low during power up and power down sequence such as voltage transition, write operation on the flash memory is disabled, write protecting all blocks.

For the details of RP# control, refer to the specification. (See chapter 5.6 and 6.2.7.)

4) Noise rejection of WE#

Consider noise rejection of WE# in order to prevent false write command input.

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

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