

# LZ2336

Two-power supply (+5 V and +12 V) operation  
1/3 type B/W CCD Area Sensor for EIA

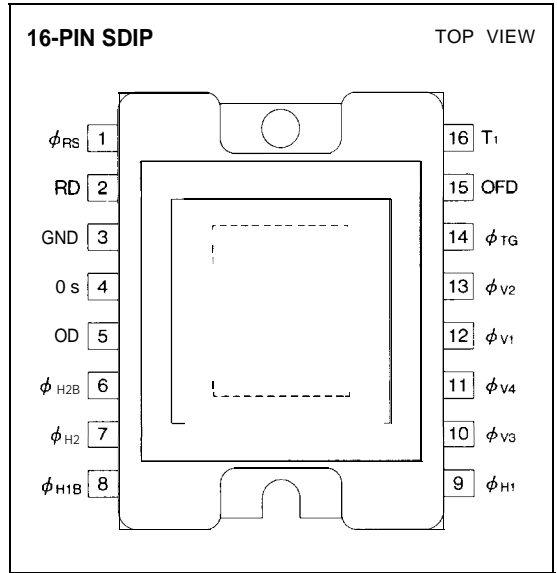
## DESCRIPTION

LZ2336 is a 1/3-type (6.0 mm) solid-state image sensor that consists of PN photo-diodes and CCDs (charge-coupled devices) driven by only positive voltages. Having approximately 190000 pixels (horizontal 384 × vertical 492), the sensor provides a stable B/W image.

## FEATURES

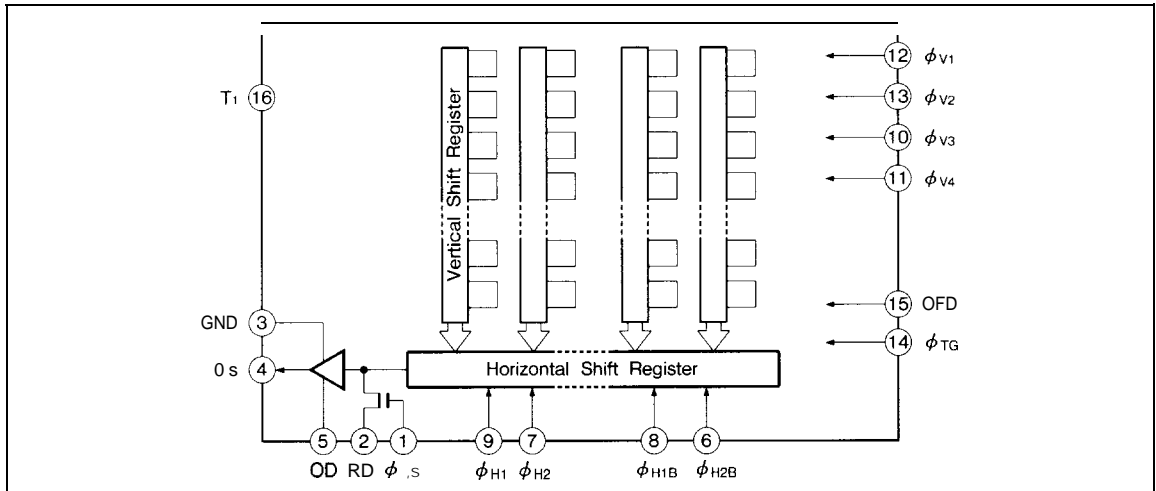
- Number of pixels : 362 (H) × 492 (V)  
Pixel pitch : 13.6 μm (H) × 7.5 μm (V)  
Number of optical black pixels : Horizontal; front 2 and rear 20
- Low fixed pattern noise and lag
- No sticking and no image distortion
- Blooming suppression structure
- Built-in output amplifier
- Variable electronic shutter (1/60 to 1/1 000s)
- Compatible with EIA standard
- Package : 16-pin SDIP [CERDIP] (WDIP016-N-0500B)

## PIN CONNECTIONS



2 CCD AREA SENSORS

## BLOCK DIAGRAM



## PIN DESCRIPTION

| SYMBOL   | PIN NAME                             |
|--|--------------------------------------|
| RD   | Reset transistor drain               |
| OD   | Output transistor drain              |
| Os   | Video output                         |
| $\phi_{RS}$                                    | Reset transistor gate clock          |
| $\phi_{V1}, \phi_{V2}, \phi_{V3}, \phi_{V4}$   | Vertical shift register gate clock   |
| $\phi_{H1}, \phi_{H2}, \phi_{H1B}, \phi_{H2B}$ | Horizontal shift register gate clock |
| $\phi_{TG}$                                    | Transfer gate clock                  |
| OFD  | Overflow drain                       |
| T <sub>1</sub>                                 | Test terminal                        |
| GND  | Ground                               |

## ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

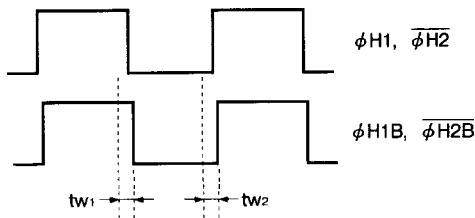
| PARAMETER                               | SYMBOL           | RATING      | UNIT |
|---|------------------|-------------|------|
| Output transistor drain voltage         | V <sub>OD</sub>  | 0 to +15    | v    |
| Reset transistor drain voltage          | V <sub>RD</sub>  | 0 to +15    | v    |
| Test terminal, T <sub>1</sub>           | V <sub>T1</sub>  | 0 to +15    | v    |
| Reset gate clock voltage                | V $\phi_{RS}$    | -0.3 to +15 | v    |
| Vertical shift register clock voltage   | V $\phi_V$       | -0.3 to +15 | v    |
| Horizontal shift register clock voltage | V $\phi_H$       | -0.3 to +15 | v    |
| Transfer gate clock voltage             | V $\phi_{TG}$    | -0.3 to +15 | v    |
| Overflow drain voltage                  | V <sub>OFD</sub> | 0 to +27    | v    |
| Storage temperature                     | T <sub>stg</sub> | -40 to +85  | °C   |
| Operating ambient temperature           | T <sub>opr</sub> | -20 to +70  | °C   |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER                                 |                                 | SYMBOL                             | MIN.           | TYP.     | MAX.            | UNIT | NOTE |
|---|---------------------------------|------------------------------------|----------------|----------|-----------------|------|------|
| Operating ambient temperature             |                                 | $T_{opr}$                          |                | 25.0     |                 | °C   |      |
| Output transistor drain voltage           |                                 | $V_{OD}$                           | 12.0           | 12.5     | 14.0            | v    |      |
| Reset transistor drain voltage            |                                 | $V_{RD}$                           |                | $V_{OO}$ |                 | v    |      |
| Overflow drain voltage                    | When DC is applied              | $V_{om}$                           | 3.0            |          | 12.0            | v    | 1    |
|   | When pulse is applied p-p level | $V_{\phi OFD}$                     | 12.0           | 12.5     | 14.0            | v    | 2    |
| Test terminal, $T_1$                      |                                 | $V_{T1}$                           |                | $V_{OD}$ |                 | v    |      |
| Ground voltage                            |                                 | <b>GND</b>                         |                | 0.0      |                 | V    |      |
| Transfer gate clock                       | LOW level                       | $V_{\phi TGL}$                     | -0.05          | 0.0      | 0.05            | v    |      |
|   | HIGH level                      | $V_{\phi TGH}$                     | 12.0           | 12.5     | 14.0            | v    |      |
| Vertical shift register clock             | LOW level                       | $V_{\phi V1-4L}$                   | -0.05          | 0.0      | 0.05            | v    |      |
|   | HIGH level                      | $V_{\phi V1-4H}$                   | 4.7            | 5.0      | 6.0             | v    |      |
| Horizontal shift register clock           | LOW level                       | $V_{\phi H1-2L}, V_{\phi H1B-2BL}$ | -0.05          | 0.0      | 0.05            | v    |      |
|   | HIGH level                      | $V_{\phi H1-2H}, V_{\phi H1B-2BH}$ | 4.7            | 5.0      | 6.0             | v    |      |
| Reset gate clock                          | LOW level                       | $V_{\phi RSL}$                     | 0.0            |          | $V_{RD} - 10.5$ | v    |      |
|   | HIGH level                      | $V_{\phi RSH}$                     | $V_{RD} - 6.0$ |          | 9.5             | v    |      |
| Vertical shift register clock frequency   |                                 | $f_{\phi V1-4}$                    |                | 15.73    |                 | kHz  |      |
| Horizontal shift register clock frequency |                                 | $f_{\phi H1-2}, f_{\phi H1B-2B}$   |                | 6.75     |                 | MHz  |      |
| Reset gate clock frequency                |                                 | $f_{\phi RS}$                      |                | 6.75     |                 | MHz  |      |
| Horizontal shift register clock phase     |                                 | $tw_1, tw_2$                       | 0.0            | 5.0      | 10.0            | ns   | 3    |

## NOTES :

- When DC voltage is applied, shutter speed is 1/@ seconds.
- When pulse is applied, shutter speed is less than 1/60 seconds.
- 



## ELECTRICAL CHARACTERISTICS (Drive method : Field Accumulation)

( $T_a = 25^\circ\text{C}$ , Operating conditions : typical values for the recommended operating conditions, Color temperature of light source : 3200 K / IR cut-off filter (CM-500, 1 mm))

| PARAMETER                       | SYMBOL          | MIN. | TYP. | MAX. | UNIT     | NOTE |
|---------------------------------|-----------------|------|------|------|----------|------|
| Photo response non-uniformity   | PRNU            |      |      | 15   | %        | 2    |
| Saturation signal               | Vsat            | 500  |      |      | mV       | 3    |
| Dark output voltage             | Vdark           |      | 5.0  | 15.0 | mV       | 1, 4 |
| Dark signal non-uniformity      | DSNU            |      | 1.5  | 5.0  | mV       | 1, 5 |
| Sensitivity                     | R               | 160  | 220  |      | mV       | 6    |
| Smear ratio                     | SMR             |      | - 85 | - 76 | dB       | 7    |
| Image lag                       | AI              |      |      | 1.0  | %        | 8    |
| Blooming suppression ratio      | ABL             | 1000 |      |      |          | 9    |
| Output transistor drain current | I <sub>OD</sub> |      | 2.5  | 5.0  | mA       |      |
| Output impedance                | R <sub>O</sub>  |      | 400  |      | $\Omega$ |      |

. The standard output voltage is defined as 150 mV by the average output voltage under uniform illumination.

- The standard exposure level is defined when the average output voltage is 150 mV under uniform illumination.

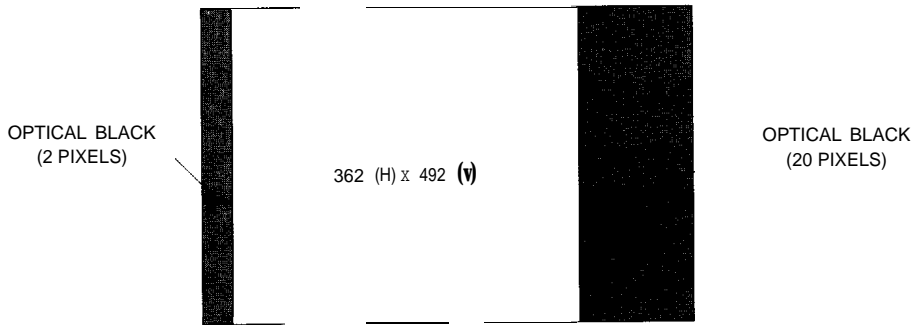
## NOTES :

1.  $T_a : +60^\circ\text{C}$
2. The image area is divided into 10x 10 segments. The segment's voltage is the average output voltage of all the pixels within the segment. PRNU is defined by  $(V_{\text{max}} - V_{\text{min}})/V_o$ , where  $V_{\text{max}}$  and  $V_{\text{min}}$  are the maximum and the minimum values of each segment's voltage respectively, when the average output voltage  $V_o$  is 150mV.
3. The image area is divided into 10x 10 segments.  
The saturation signal is defined as the minimum of each segment's voltage which is the average output voltage of all the pixels within the segment, when the exposure level is set as 10 times, compared to standard level,
4. The average output voltage under a non-exposure condition.
5. The image area is divided into 10x 10 segments. DSNU is defined by  $(V_{\text{dmax}} - V_{\text{dmin}})$  under the non-exposure con-

dition where  $V_{\text{dmax}}$  and  $V_{\text{dmin}}$  are the maximum and the minimum values of each segment's voltage, respectively, that is the average output voltage over all pixels in the segment.

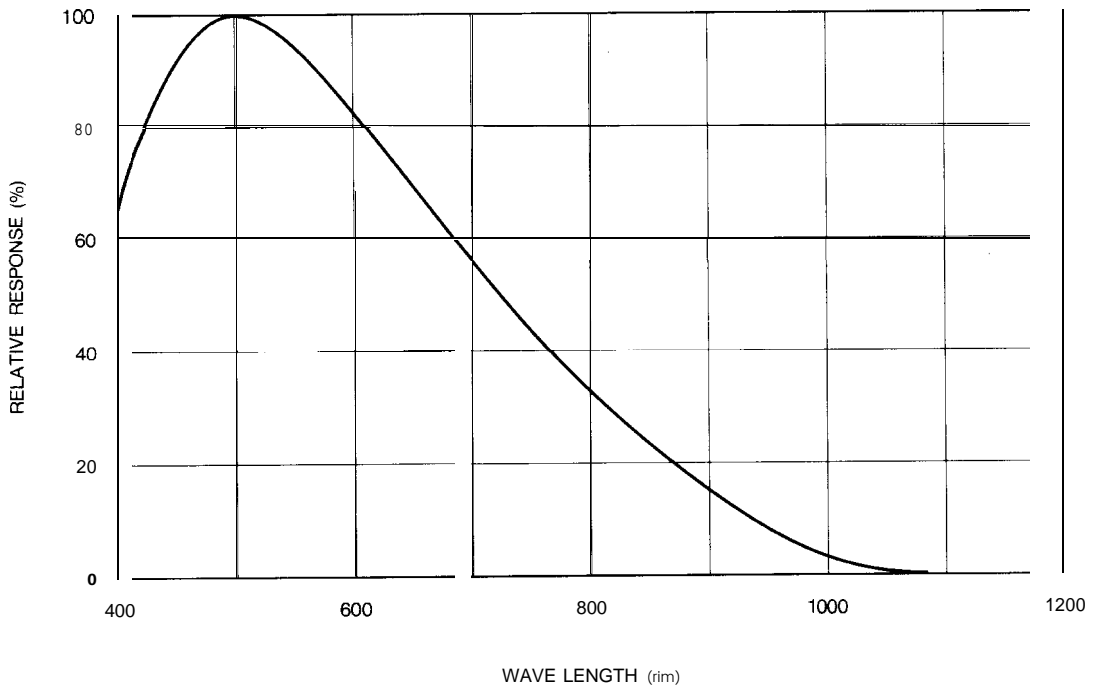
- 6 The average output voltage when a 1000lux light source attached with a 90% reflector is imaged by a lens of F4, f50 mm.
- 7 The sensor is adjusted to position a V/I O square at the center of image area where V is the vertical length of the image area, SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the pixel voltage in the V/I O square.
- 8 The sensor is exposed at the exposure level corresponding to the standard condition preceding non-exposure condition. AI is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.
- 9 The sensor is adjusted to position a V/I O square at the center of image area. ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.

PIXEL STRUCTURE



CCD AREA SENSORS  
2

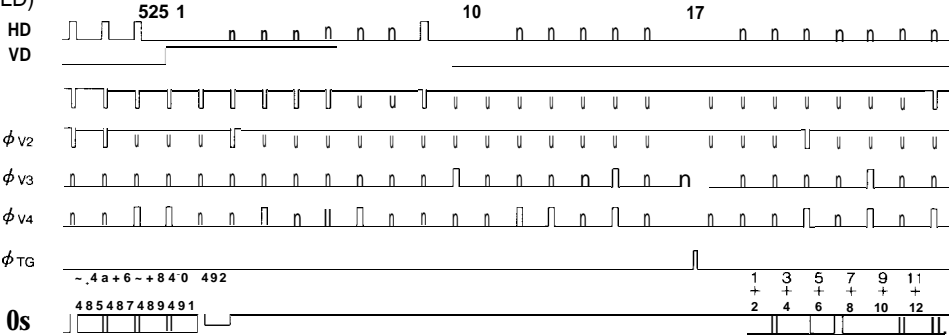
SPECTRAL RESPONSE EXAMPLE



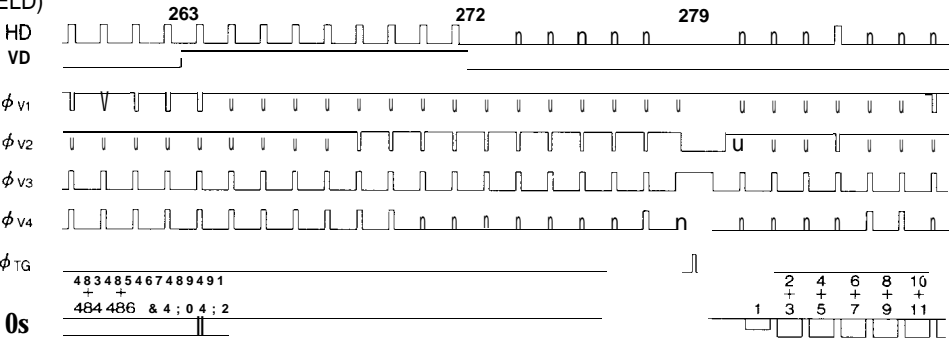
TIMING DIAGRAM EXAMPLE

VERTICAL TRANSFER TIMING

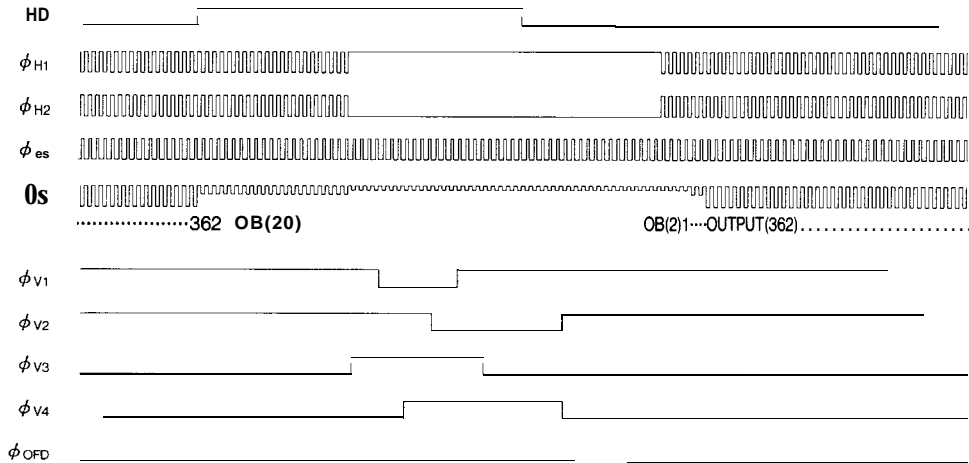
(ODD FIELD)



(EVEN FIELD)

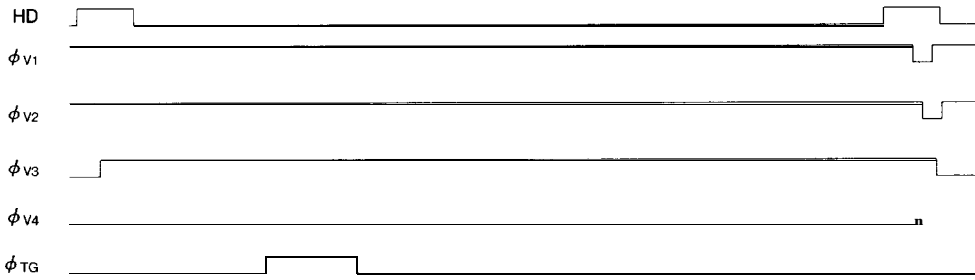


HORIZONTAL TRANSFER TIMING

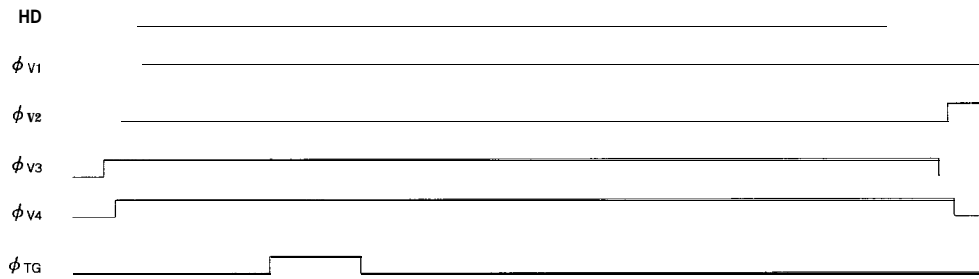


## READOUT TIMING

(ODD FIELD)



(EVEN FIELD)



## SYSTEM CONFIGURA ON EXAMP E

