LOW DROPOUT CMOS VOLTAGE REGULATOR S-818 Series

The S-818 Series is a positive voltage regulator developed utilizing CMOS technology featured by low dropout voltage, high output voltage accuracy and low current consumption. Built-in low on-resistance transistor provides low dropout voltage and large output current. A ceramic capacitor of 2 µF or more can be used as an output capacitor. A power-OFF circuit ensures long battery life.

The SOT-23-5 miniaturized package and the SOT-89-5 package are recommended for configuring portable devices and large output current applications, respectively.

■ Features

- Low current consumption
  During operation: Typ. 30 µA, Max. 40 µA
  During power off: Typ. 100 nA, Max. 500 nA
- Output voltage: 0.1 V steps between 2.0 and 6.0 V
- High accuracy output voltage: ±2.0%
- Peak output current;
  200 mA capable (3.0 V output product, V_{IN}=4 V) [Note]
  300 mA capable (5.0 V output product, V_{IN}=6 V) [Note]
- Low dropout voltage
  Typ. 170 mV (5.0 V output product, I_{OUT} = 60 mA)
  A ceramic capacitor (2 µF or more) can be used as an output capacitor.
- Built-in power-off circuit
- Compact package: SOT-23-5, SOT-89-5

■ Applications

- Power source for battery-powered devices
- Power source for personal communication devices
- Power source for home electric/electronic appliances

Note : Please consider power dissipation of the package when the output current is large.

■ Package

- 5-pin SOT-23-5 (Package drawing code: MP005-A)
- 5-pin SOT-89-5 (Package drawing code: UP005-A)

■ Block Diagram

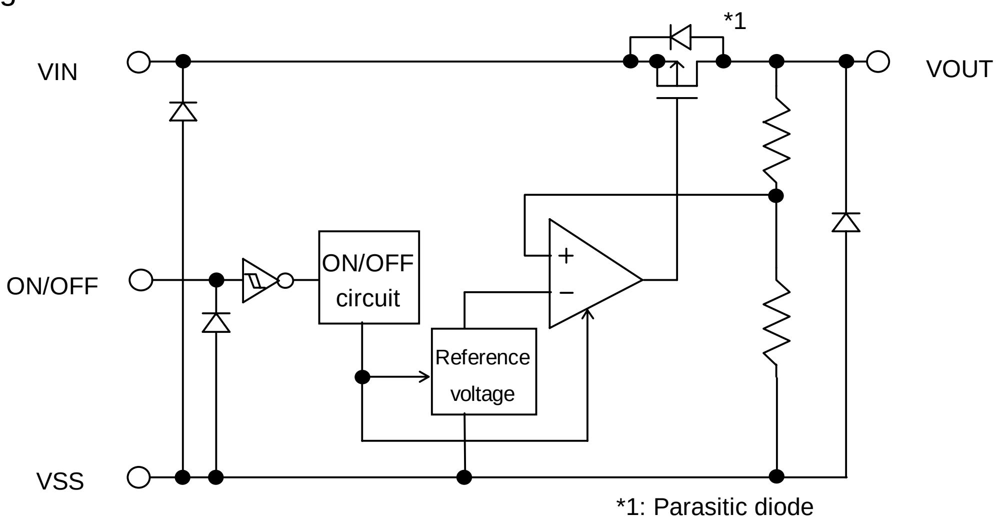


Figure 1 Block Diagram

■ Selection Guide

1. Product Name

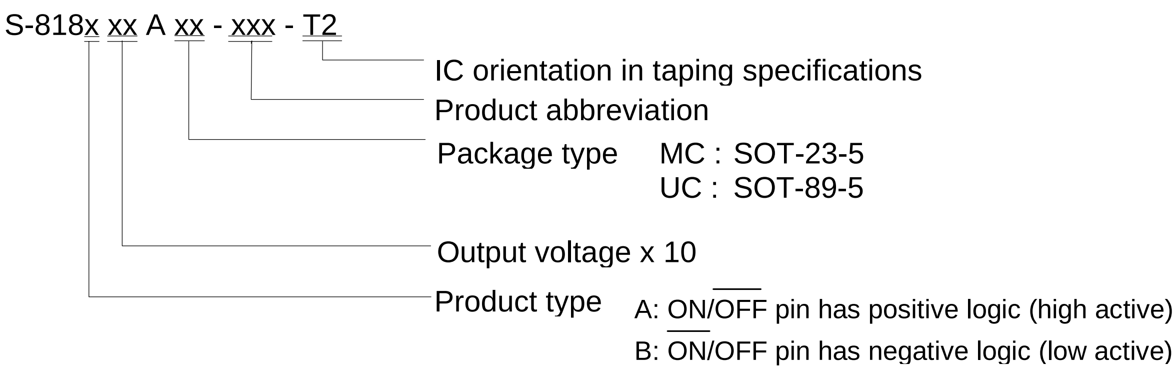


Table 1 Selection Guide

Output Voltage	SOT-23-5	SOT-89-5
2.0 V ± 2.0%	S-818A20AMC-BGA-T2	S-818A20AUC-BGA-T2
2.5 V ± 2.0%	S-818A25AMC-BGF-T2	S-818A25AUC-BGF-T2
2.8 V ± 2.0%	S-818A28AMC-BGI-T2	S-818A28AUC-BGI-T2
3.0 V ± 2.0%	S-818A30AMC-BGK-T2	S-818A30AUC-BGK-T2
3.3 V ± 2.0%	S-818A33AMC-BGN-T2	S-818A33AUC-BGN-T2
3.8 V ± 2.0%	S-818A38AMC-BGS-T2	S-818A38AUC-BGS-T2
4.0 V ± 2.0%	S-818A40AMC-BGU-T2	S-818A40AUC-BGU-T2
5.0 V ± 2.0%	S-818A50AMC-BHE-T2	S-818A50AUC-BHE-T2

Note:
Contact SII sales division for product with an output voltage other than those specified above or product type B, low active product.

■ Pin Configuration

Please refer to the package drawings at the end of this document for details.

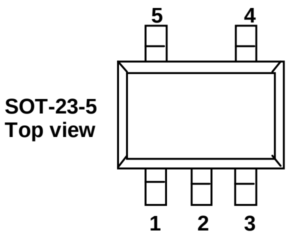


Figure 2 SOT-23-5

Table 2 Pin Assignment

Pin No.	Symbol	Description
1	VIN	Voltage input pin
2	VSS	GND pin
3	ON/OFF	Power off pin
4	NC Note	No connection
5	VOUT	Voltage output pin

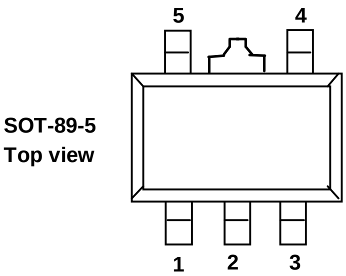


Figure 3 SOT-89-5

Table 3 Pin Assignment

Pin No.	Symbol	Description
1	VOUT	Voltage output pin
2	VSS	GND pin
3	NC Note	No connection
4	ON/OFF	Power off pin
5	VIN	Voltage input pin

Note: NC means electrical open. Connecting NC pin to VIN or VSS is allowed.

■ Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Absolute Maximum Rating	Unit
Input voltage	V_{IN}	12	V
	$V_{ON / OFF}$	V_{SS}-0.3 to 12	V
Output voltage	V_{OUT}	V_{SS}-0.3 to V_{IN}+0.3	V
Power dissipation	P_D	250 (SOT-23-5) 500 (SOT-89-5)	mW
Operating temperature range	Tope	-40 to +85	°C
Storage temperature range	Tstg	-40 to +125	°C

The IC has a protection circuit against static electricity. DO NOT apply high static electricity or high voltage that exceeds the performance of the protection circuit to the IC.

■ Electrical Characteristics

S-818AXXAMC/UC, S-818BXXAMC/UC

Table 5 Electrical Characteristics (Ta=25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units	Test circuits
Output voltage *1)	$V_{OUT}(E)$	$V_{IN}=V_{OUT}(S)+1V, I_{OUT}=30mA$		$V_{OUT}(S)\times0.98$	$V_{OUT}(S)$	$V_{OUT}(S)\times1.02$	V	1
Output current *2)	I_{OUT}	$V_{OUT}(S)+1V \le V_{IN} \le 10V$	$2.0V \le V_{OUT}(S) \le 2.4V$	100 *5)	–	–	mA	3
			$2.5V \le V_{OUT}(S) \le 2.9V$	150 *5)	–	–	mA	3
			$3.0V \le V_{OUT}(S) \le 3.9V$	200 *5)	–	–	mA	3
			$4.0V \le V_{OUT}(S) \le 4.9V$	250 *5)	–	–	mA	3
			$5.0V \le V_{OUT}(S) \le 6.0V$	300 *5)	–	–	mA	3
Dropout voltage *3)	Vdrop	I_{OUT} = 60mA	$2.0V \le V_{OUT}(S) \le 2.4V$	–	0.51	0.87	V	1
			$2.5V \le V_{OUT}(S) \le 2.9V$	–	0.38	0.61	V	1
			$3.0V \le V_{OUT}(S) \le 3.4V$	–	0.30	0.44	V	1
			$3.5V \le V_{OUT}(S) \le 3.9V$	–	0.24	0.33	V	1
			$4.0V \le V_{OUT}(S) \le 4.4V$	–	0.20	0.26	V	1
			$4.5V \le V_{OUT}(S) \le 4.9V$	–	0.18	0.22	V	1
			$5.0V \le V_{OUT}(S) \le 5.4V$	–	0.17	0.21	V	1
			$5.5V \le V_{OUT}(S) \le 6.0V$	–	0.17	0.20	V	1
Line regulation 1	$\frac{\Delta V_{OUT}1}{\Delta V_{IN} \bullet V_{OUT}}$	$V_{OUT}(S) + 0.5\ V \le V_{IN} \le 10\ V$, I_{OUT} = 30mA		—	0.05	0.2	%/V	1
Line regulation 2	$\frac{\Delta V_{OUT}2}{\Delta V_{IN} \bullet V_{OUT}}$	$V_{OUT}(S) + 0.5\ V \le V_{IN} \le 10\ V$, I_{OUT} = 10µA		—	0.05	0.2	%/V	1
Load regulation	$\Delta V_{OUT}3$	$V_{IN} = V_{OUT}(S) + 1\ V$, $10µA \le I_{OUT} \le 80mA$		—	30	50	mV	1
Output voltage temperature coefficient *4)	$\frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}$	$V_{IN} = V_{OUT}(S) + 1\ V$, I_{OUT} = 30mA, -40°C ≤ Ta ≤ 85°C			±100	—	ppm/°C	1
Current consumption during operation	$I_{SS}1$	$V_{IN} = V_{OUT}(S) + 1\ V$, ON/OFF pin = ON, no load		—	30	40	µA	2
Current consumption when power off	$I_{SS}2$	$V_{IN} = V_{OUT}(S) + 1\ V$, ON/OFF pin = OFF, no load		—	0.1	0.5	µA	2
Input voltage	V_{IN}			—	—	10	V	1
Power-off pin input voltage "H"	V_{SH}	$V_{IN} = V_{OUT}(S) + 1\ V$, R_L = 1kΩ, Judged by V_{OUT} output level.		1.5	—	—	V	4
Power-off pin input voltage "L"	V_{SL}	$V_{IN} = V_{OUT}(S) + 1\ V$, R_L = 1kΩ, Judged by V_{OUT} output level.		—	—	0.3	V	4
Power-off pin input current "H"	I_{SH}	$V_{IN} = V_{OUT}(S) + 1\ V$, ON/OFF = 7 V		—	—	0.1	µA	4
Power-off pin input current "L"	I_{SL}	$V_{IN} = V_{OUT}(S) + 1\ V$, ON/OFF = 0 V		—	—	-0.1	µA	4
Ripple rejection	|RR|	$V_{IN} = V_{OUT}(S) + 1\ V$, f = 100Hz, ΔVrip = 0.5 V p-p, I_{OUT}=30mA		—	45	—	dB	5

*1) $V_{OUT}(S)$=Specified output voltage
$V_{OUT}(E)$=Effective output voltage, i.e., the output voltage at fixet I_{OUT}(=30 mA) and input $V_{OUT}(S)$+1.0 V.

*2) Output current when the output voltage goes below 95% of $V_{OUT}(E)$ after gradually increasing output current.

*3) Vdrop = $V_{IN}1-(V_{OUT}(E) \times 0.98)$
$V_{IN}1$ = Input voltage when output voltage falls 98% of $V_{OUT}(E)$ after gradually decreasing input voltage.

*4) Output voltage shift by temperature [mV/°C] is calculated using the following equation.

$$\frac{\Delta V_{OUT}}{\Delta Ta}[mV/°C] = V_{OUT}(S)[V] \times \frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}[ppm/°C] \div 1000$$

↑ Output voltage shift by temperature
↑ Specified output voltage
↑ Output voltage temperature coefficient

*5) Peak output current can exceed the minimum value.

■ Test Circuits

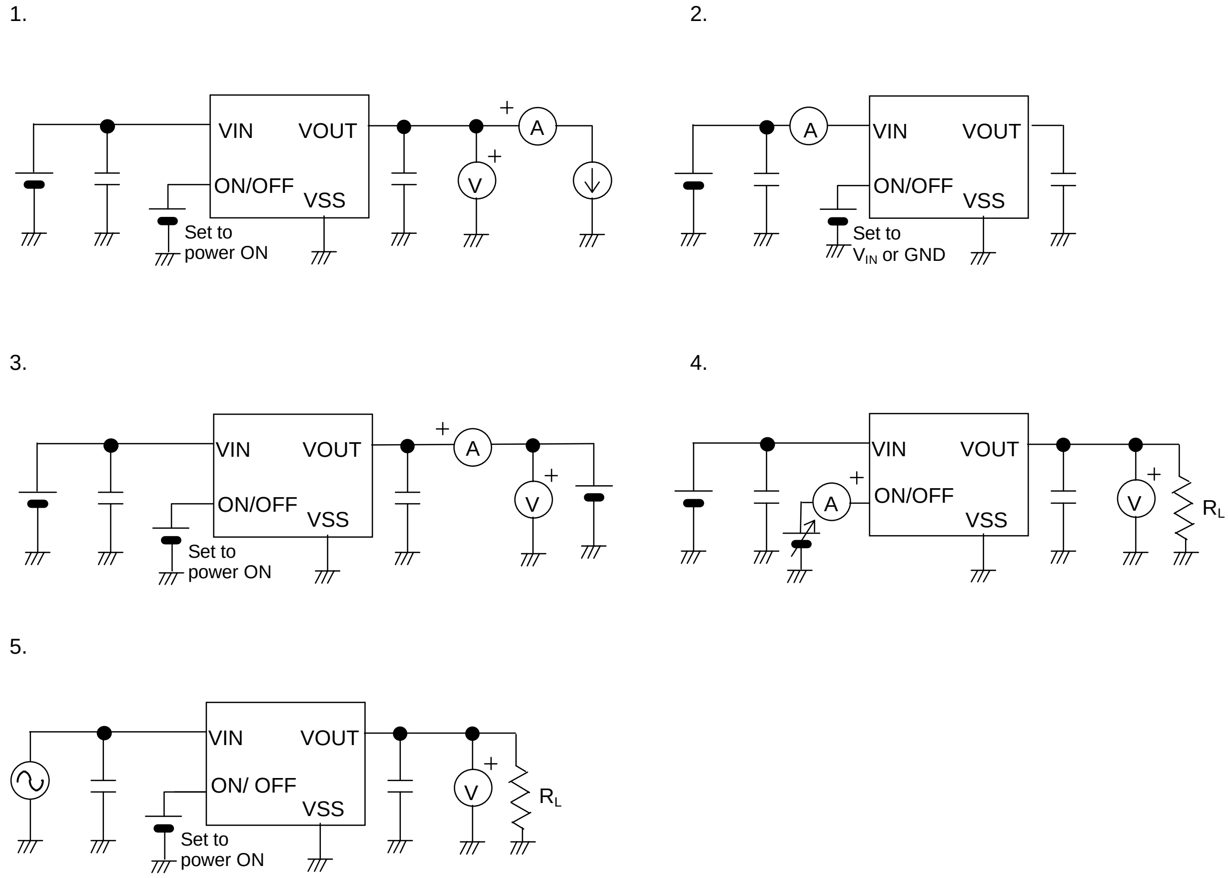
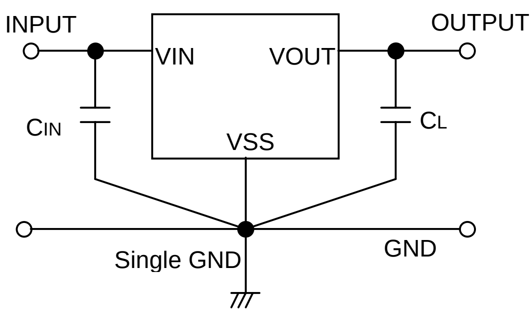


Figure 4 Test Circuits

■ Standard Circuit



In addition to a tantalum capacitor, a ceramic capacitor of 2 μF or more can be used in CL.
CIN is a capacitor used to stabilize input. Use a capacitor of 0.47 μF or more.

Figure 5 Standard Circuit

■ Operating Conditions

Input capacitor (C_{IN})	: 0.47 μF or more
Output capacitor (C_L)	: 2 μF or more
Equivalent Series Resistor (ESR)	: 10 Ω or less
Input Series Resistor (R_{IN})	: 10 Ω or less

■ Technical Terms

1. Low dropout voltage regulator
   The low dropout voltage regulator is a voltage regulator having a low dropout voltage characteristic due to the internal low on-resistance transistor.

2. Output voltage (V_{OUT})
   The accuracy of the output voltage is ensured at ± 2.0% under the specified conditions of input voltage, output current, and temperature, which differ product by product.

   Note:
   When the above conditions are changed, the output voltage may vary and go out of the accuracy range of the output voltage. See the electrical characteristics and characteristic data for details.

3. Line regulations 1 and 2 ($\Delta V_{OUT}1$, $\Delta V_{OUT}2$)
   Line regulation indicates the input voltage dependence of the output voltage. The value shows how much the output voltage changes due to the change of the input voltage when the output current is kept constant.

4. Load regulation ($\Delta V_{OUT}3$)
   Load regulation indicates the output current dependence of output voltage. The value shows how much the output voltage changes due to the change of the output current when the input voltage is kept constant.

5. Dropout voltage (Vdrop)
   Let $V_{IN}1$ be an input voltage where the output voltage falls to the 98% of the actual output voltage $V_{OUT}(E)$ when gradually decreasing input voltage. The dropout voltage is the difference between the $V_{IN}1$ and the resultant output voltage defined as following equation.
   $Vdrop = V_{IN}1-[V_{OUT}(E) \times 0.98]$

6. Temperature coefficient of output voltage [$\Delta V_{OUT}/(\Delta Ta \bullet V_{OUT})$]
   The shadowed area in Figure 6 is the range where V_{OUT} varies in the operating temperature range when the temperature coefficient of the output voltage is ±100 ppm/°C.

Typical Example of the S-818A28A

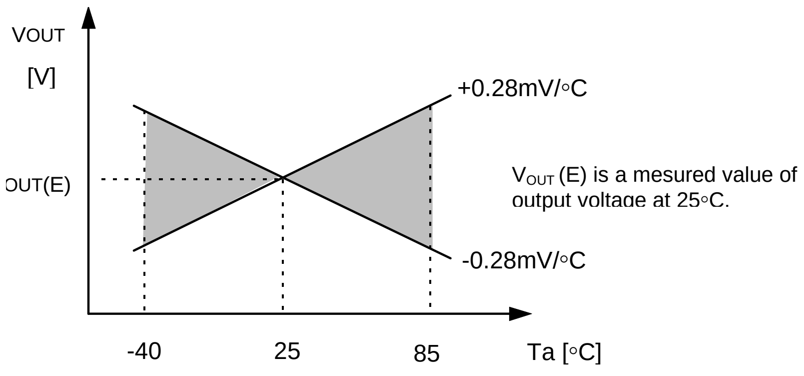


Figure 6 Temperature coefficient range of output voltage

A change of output voltage in temperature [mV/°C] is calculated using the following equation.

$$\frac{\Delta V_{OUT}}{\Delta Ta}[mV/°C] = V_{OUT}(S)[V] \times \frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}[ppm/°C] \div 1000$$

↑ Change of output voltage in temperatures

↑ Specified output voltage

↑ Output voltage temperature coefficient

■ Operation

1. Basic operation
   Figure 7 shows the block diagram of the S-818 Series.
   The error amplifier compares a reference voltage V_{REF} with the part of the output voltage divided by the feedback resistors Rs and Rf. It supplies the output transistor with the gate voltage, necessary to ensure certain output voltage free of any fluctuations of input voltage and temperature.

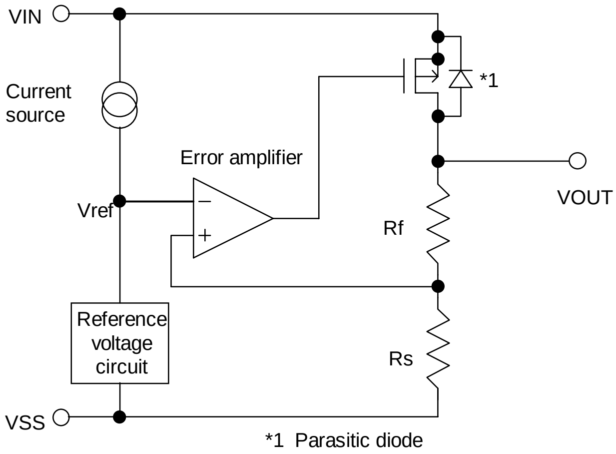


Figure 7 Typical Circuit Block Diagram

2. Output transistor
   The S-818 Series uses a low on-resistance Pch MOS FET as the output transistor.
   Be sure that VOUT does not exceed VIN+0.3 V to prevent the voltage regulator from being broken due to inverse current flowing from VOUT pin to VIN pin through the parasitic diode.

3. Power Off Pin (ON/OFF Pin)
   This pin activates and inactivates the regulator.
   When the ON/OFF pin is switched to the power off level, the operation of all internal circuit stops, the built-in Pch MOSFET output transistor between VIN and VOUT pin is switched off, suppressing current consumption. The VOUT pin goes to the Vss level due to internal divided resistance of several MΩ between VOUT pin and VSS pin.
   The structure of the ON/OFF pin is shown in Figure 8. Since the ON/OFF pin is neither pulled down nor pulled up internally, do not keep it in the floating state. Current consumption increases if a voltage of 0.3 V to VIN-0.3 V is applied to the ON/OFF pin. When the power off pin is not used, connect it to the VIN pin for product type "A" and to the VSS pin for product type "B".

Table 6 Power off pin function by product type

Product type	ON/OFF pin	Internal circuit	VOUT pin voltage	Current consumption
A	“H” : Power on	Operating	Set value	Iss1
A	“L” : Power off	Stop	Vss level	Iss2
B	“H” : Power off	Stop	Vss level	Iss2
B	“L” : Power on	Operating	Set value	Iss1

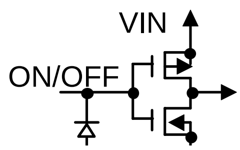


Figure 8 ON/OFF Pin

■ Selection of Output Capacitor (CL)

The S-818 series needs an output capacitor between VOUT pin and VSS pin for phase compensation. A small ceramic or an OS electrolytic capacitor of 2 μF or more can be used. If a tantalum or an aluminum electrolytic capacitor is used, its capacitance must be 2 μF or more and the ESR must be 10 Ω or less.
Attention should be paid not to cause an oscillation due to increase of ESR at low temperatures when using an aluminum electrolytic capacitor.
Evaluate the performance including temperature characteristics before prototyping the circuit.
Overshoot and undershoot characteristics differ depending upon the type of the output capacitor. Refer to output capacitor dependence data in transient response characteristics .

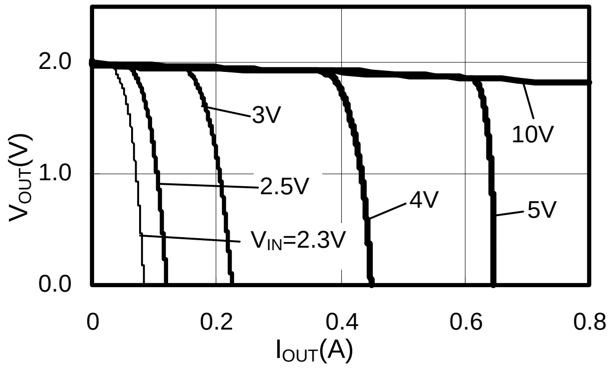
■ Design Considerations

- Design wiring patterns for VIN, VOUT and GND pins to decrease impedance.
  When mounting an output capacitor, connection from the capacitor to the VOUT pin and to the VSS pin should be as close as possible.
- Note that output voltage may increase when the voltage regulator is used at low load current (less than 10 μA).
- To prevent oscillation, it is recommended to use the external components under the following conditions:
  * Input capacitor (C_{IN}): 0.47 μF or more
  * Output capacitor (C_L): 2 μF or more
  * Equivalent Series Resistance (ESR): 10 Ω or less
  * Input series resistance (R_{IN}): 10 Ω or less
- The voltage regulator may oscillate when the impedance of the power supply is high and the input capacitor is small or not connected.
- Be sure that input voltage and load current do not exceed the power dissipation level of the package.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.
- In determining necessary output current, consider the value of output current of Table 4 “Electrical Characteristics” and Note *5) (page 4).

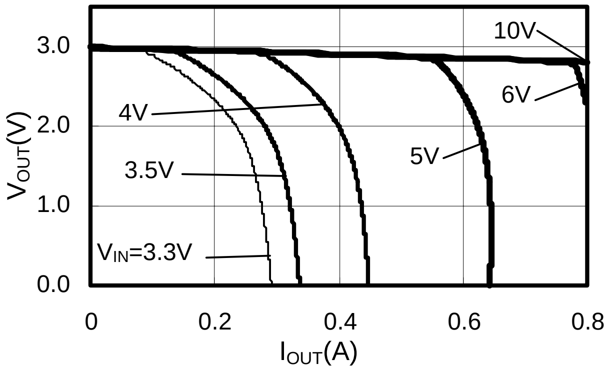
■ Typical Characteristics (Typical Data)

(1) OUTPUT VOLTAGE vs. OUTPUT CURRENT (When load current increases)

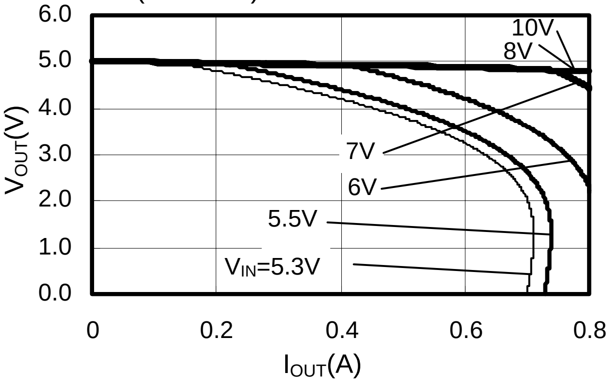
S-818A20A(Ta=25°C)



S-818A30A(Ta=25°C)



S-818A50A(Ta=25°C)

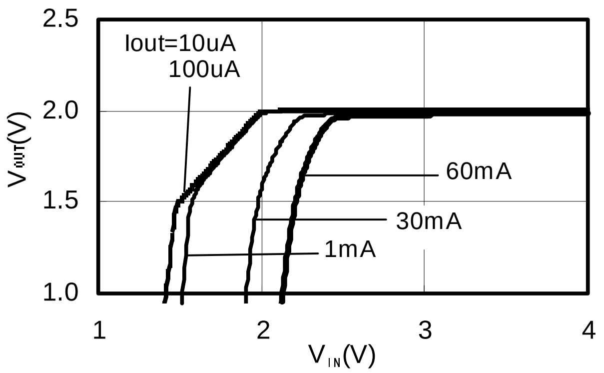


* In determining necessary output current, consider the following parameters:

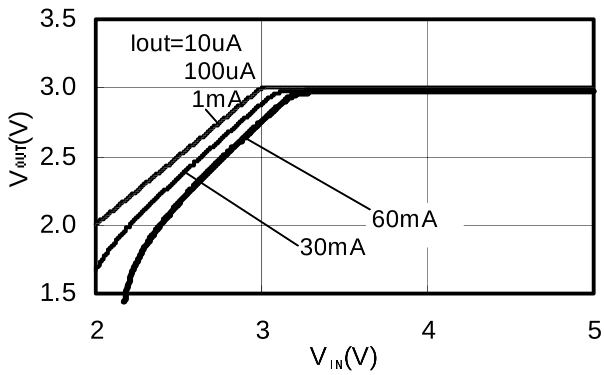
- Minimum value of output current in Table 4 “Electrical Characteristics” and Note *5) (page 4);
- Power dissipation of the package

(2) OUTPUT VOLTAGE vs. INPUT VOLTAGE

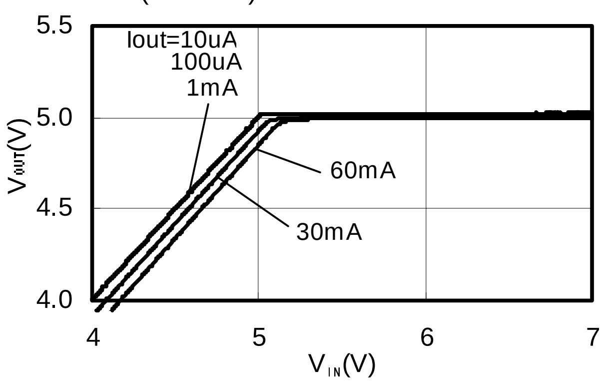
S-818A20A (Ta=25°C)



S-818A30A (Ta=25°C)

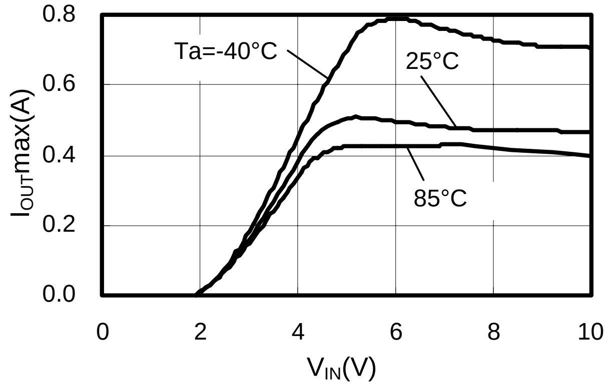


S-818A50A (Ta=25°C)

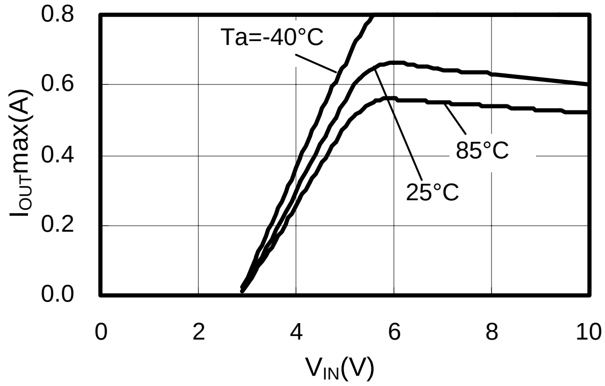


(3) MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE

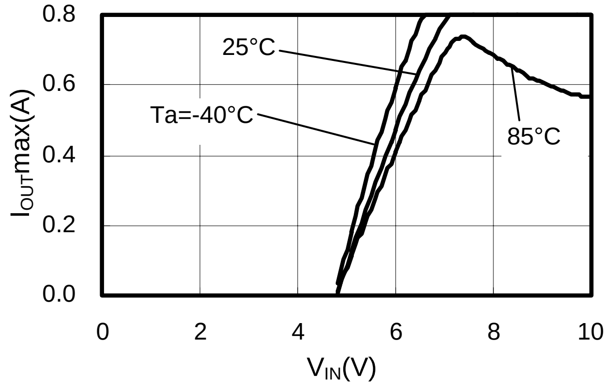
S-818A20A



S-818A30A



S-818A50A

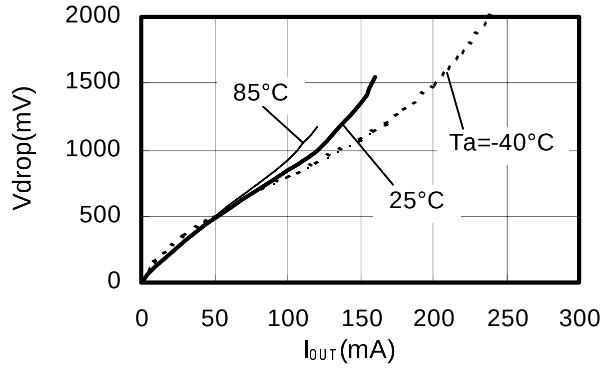


* In determining necessary output current, consider the following parameters:

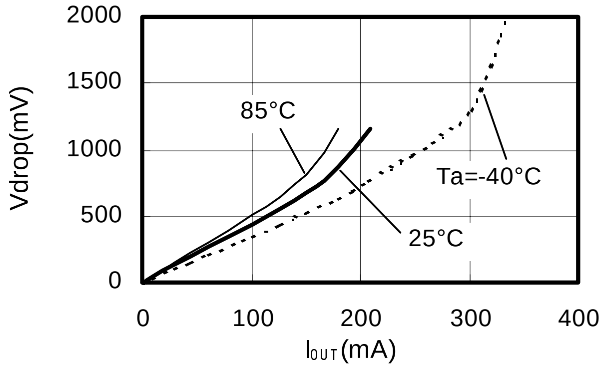
- Minimum value of output current in Table 4 “Electrical Characteristics” and Note *5) (page 4);
- Power dissipation of the package

(4) DROPOUT VOLTAGE vs. OUTPUT CURRENT

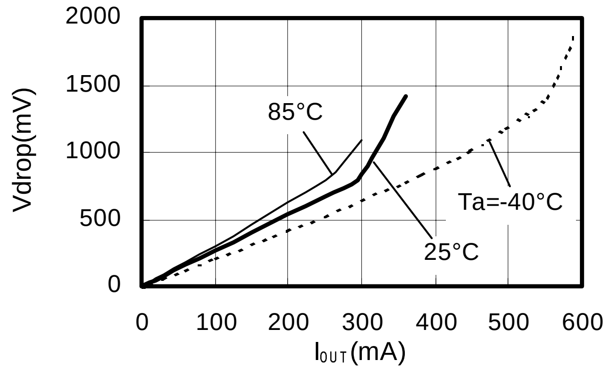
S-818A20A



S-818A30A

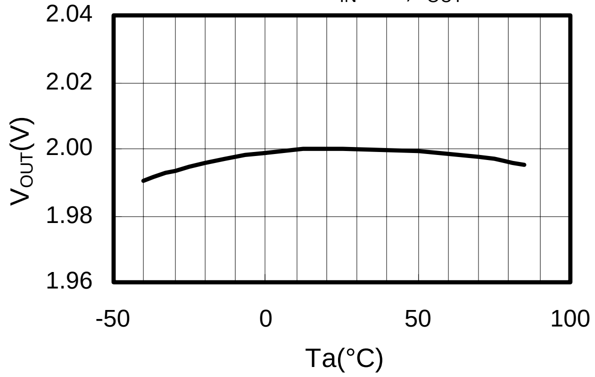


S-818A50A

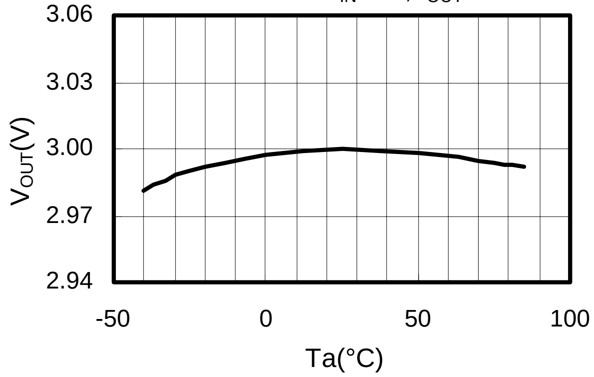


(5) OUTPUT VOLTAGE TEMPERATURE DEPENDENCE

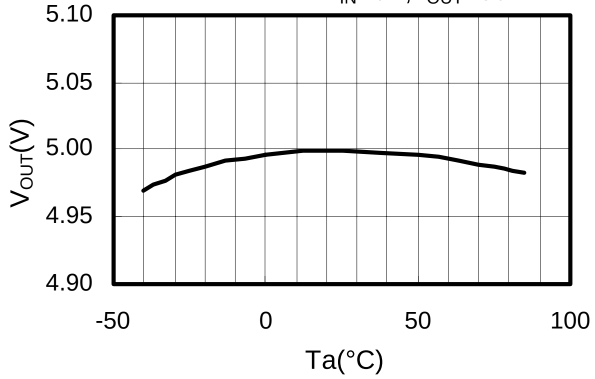
S-818A20A V_{IN}=3V, I_{OUT}=30mA



S-818A30A V_{IN}=4V, I_{OUT}=30mA

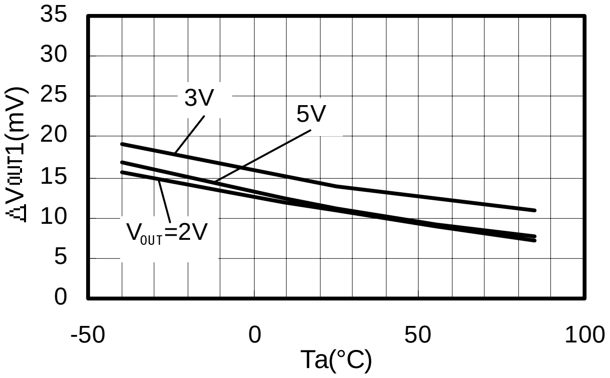


S-818A50A V_{IN}=6V, I_{OUT}=30mA



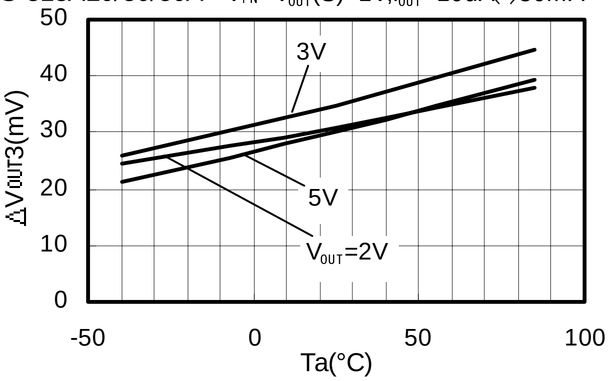
(6) LINE REGULATION TEMPERATURE DEPENDENCE

S-818A20/30/50A $V_{IN}=V_{OUT}(S)+0.5\leftrightarrow 10V, I_{OUT}=30mA$



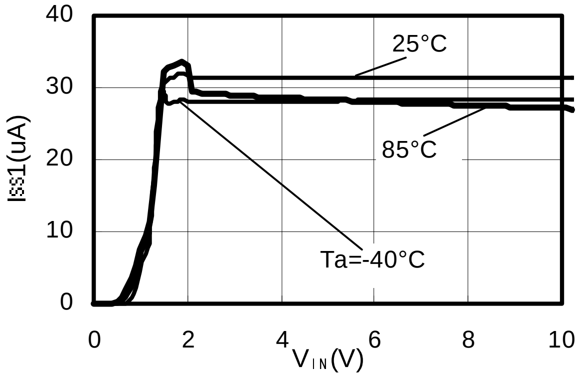
(7) LOAD REGULATION TEMPERATURE DEPENDENCE

S-818A20/30/50A $V_{IN}=V_{OUT}(S)+1V, I_{OUT}=10uA\leftrightarrow 80mA$

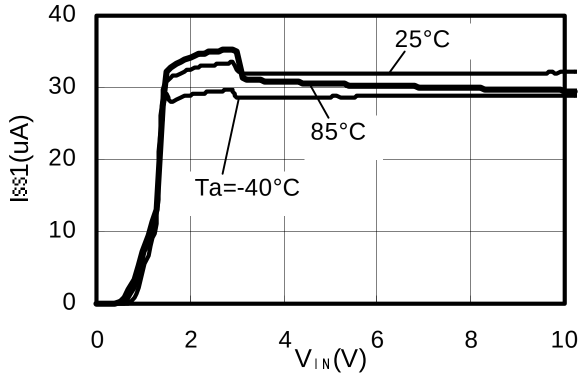


(8) CURRENTCONSUMPTION vs. INPUT VOLTAGE

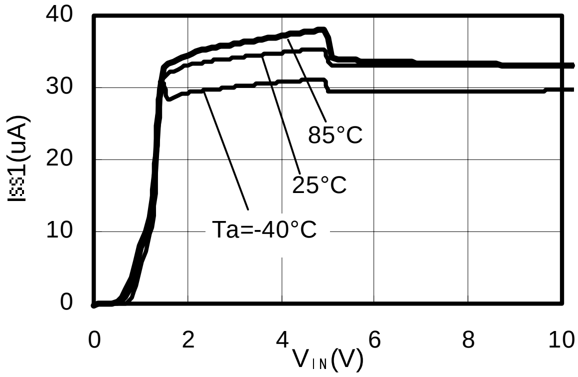
S-818A20A



S-818A30A

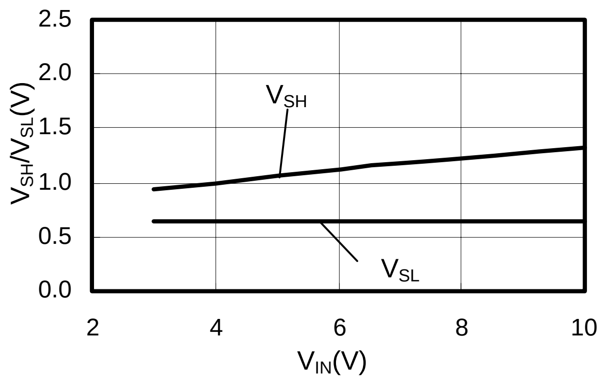


S-818A50A

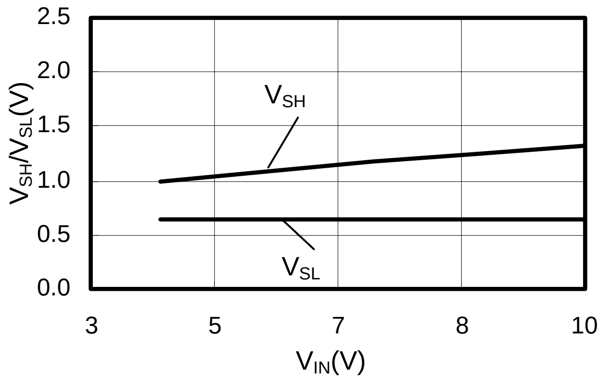


(9) THRESHOLD VOLTAGE OF POWER OFF PIN vs. INPUT VOLTAGE

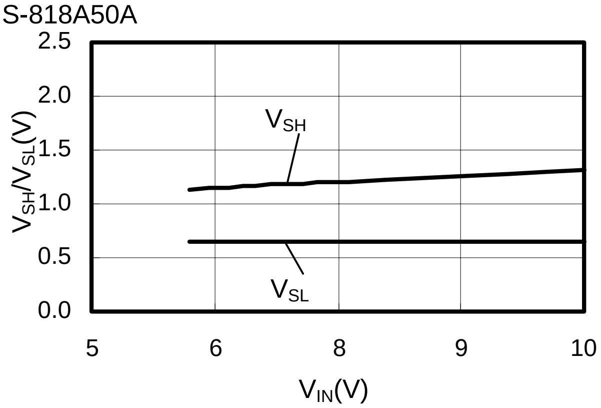
S-818A20A



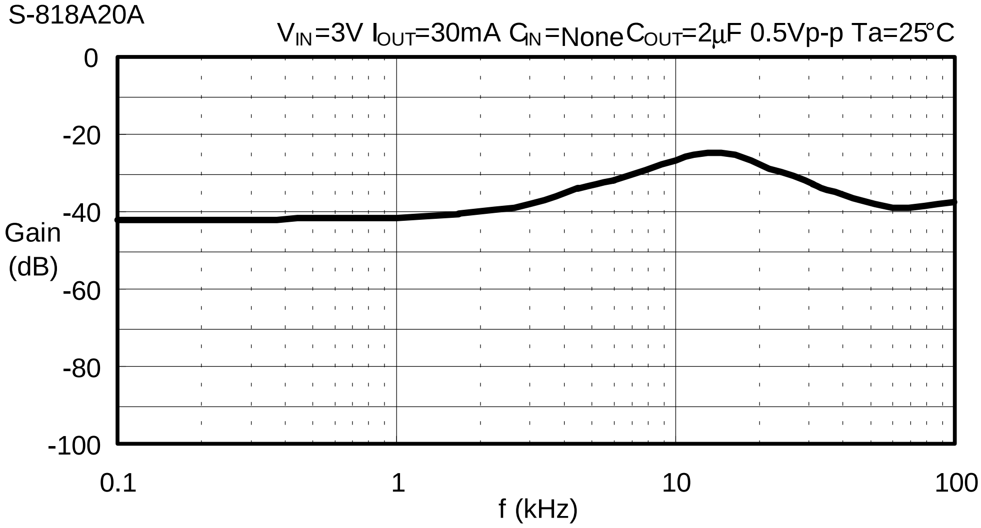
S-818A30A

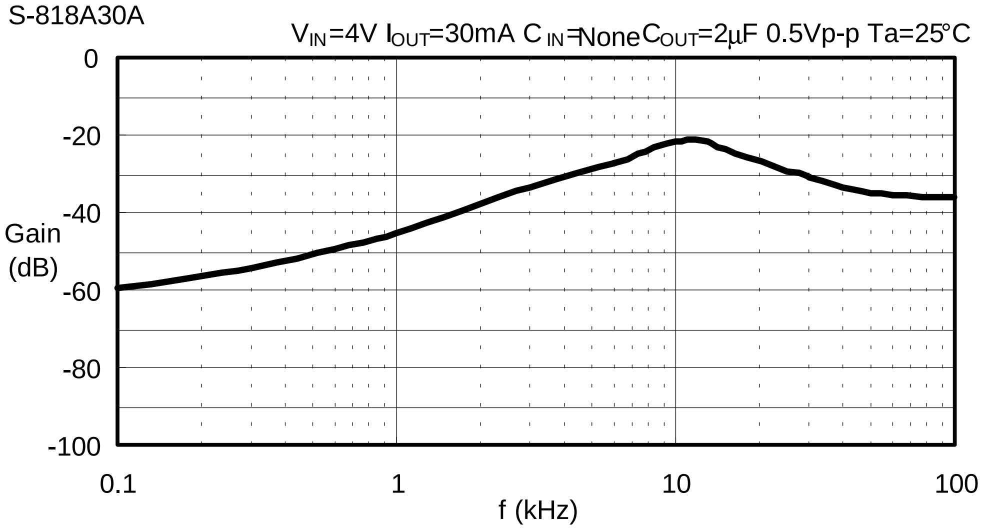


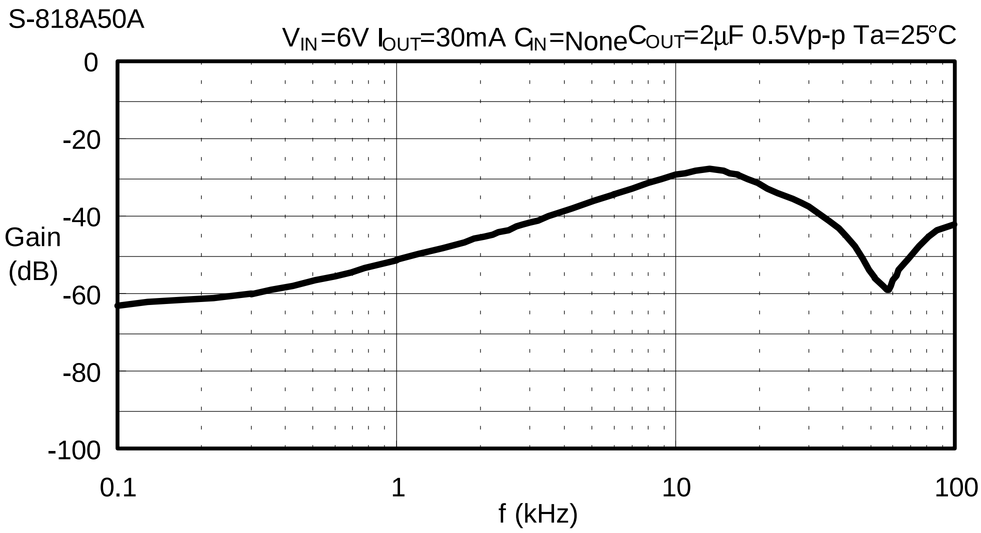
S-818A50A



(10) RIPPLE REDUCTION RATE

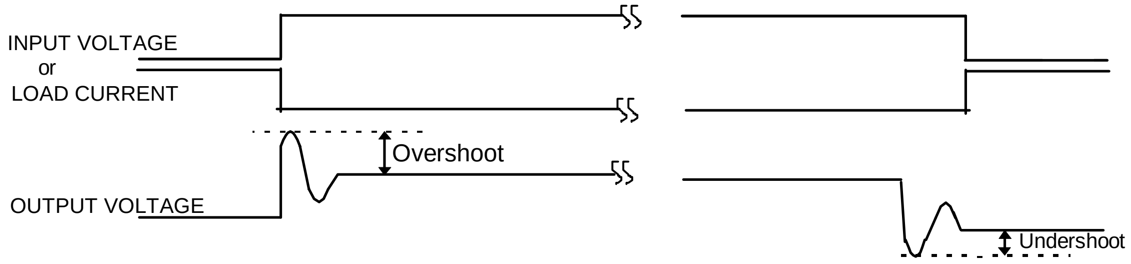




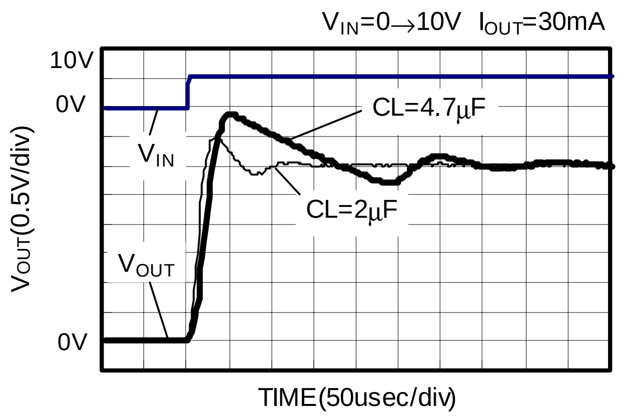


REFERENCE DATA

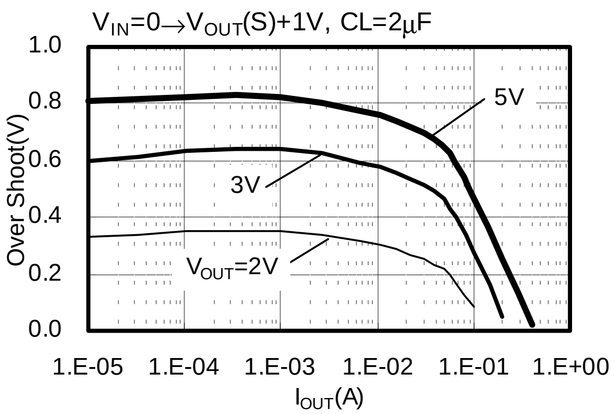
■ TRANSIENT RESPONSE CHARACTERISTICS (S-818A30A, Typical data: Ta=25°C)



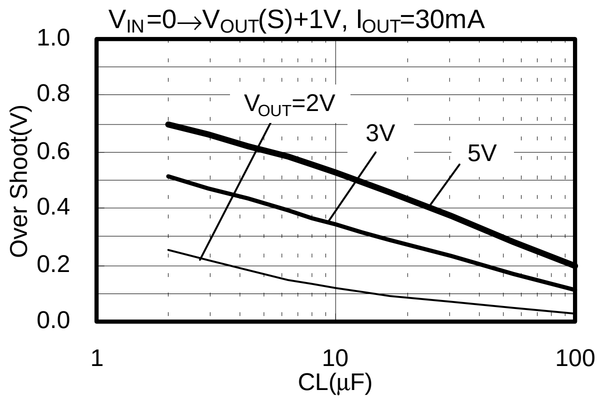
(1) Power on



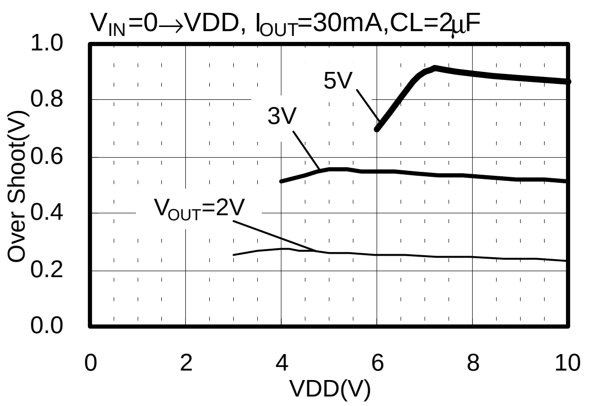
Load dependence of overshoot



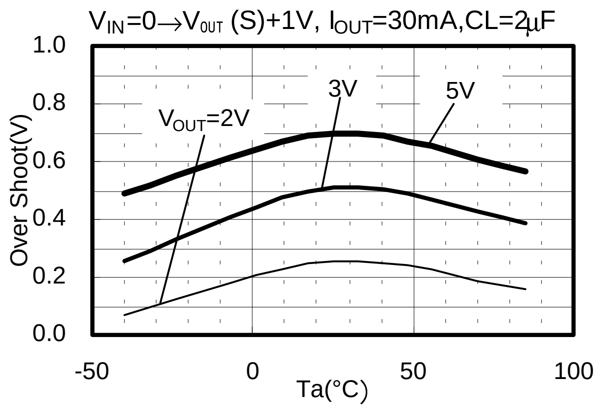
Output capacitor (CL) dependence of overshoot



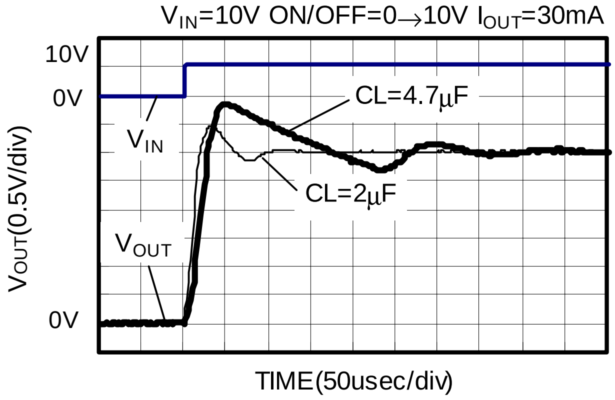
VDD dependence of overshoot



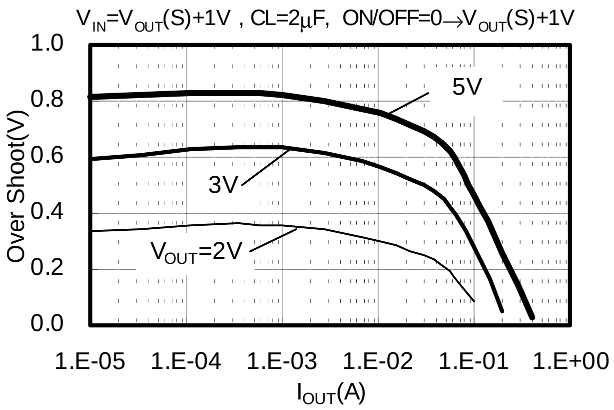
Temperature dependence of overshoot



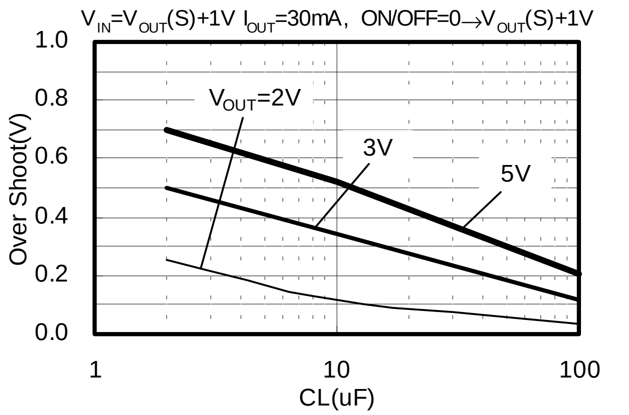
(2) Power on/off control



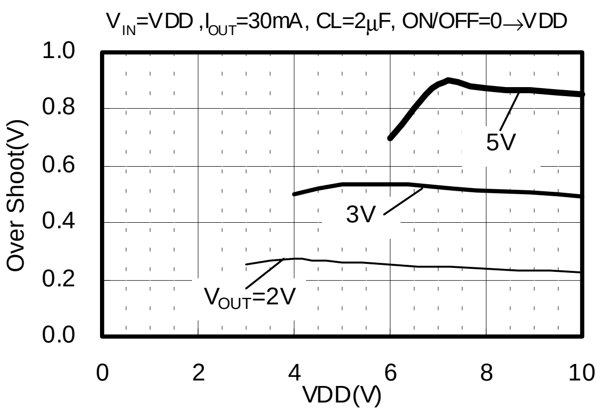
Load dependence of overshoot



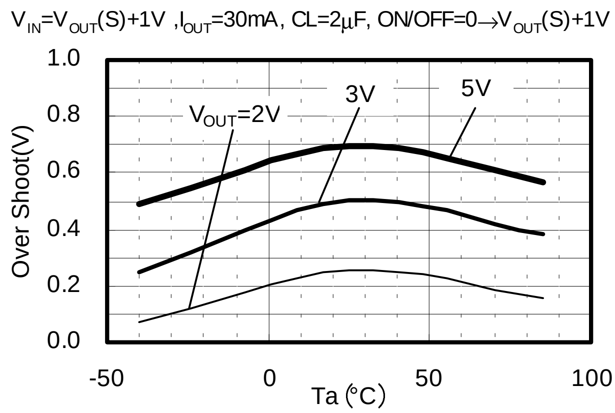
Output capacitor (CL) dependence of overshoot



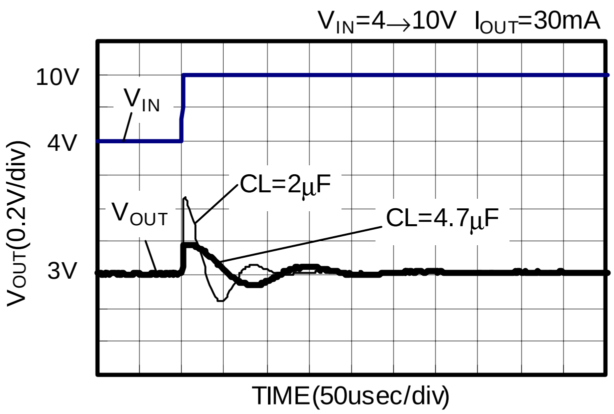
VDD dependence of overshoot

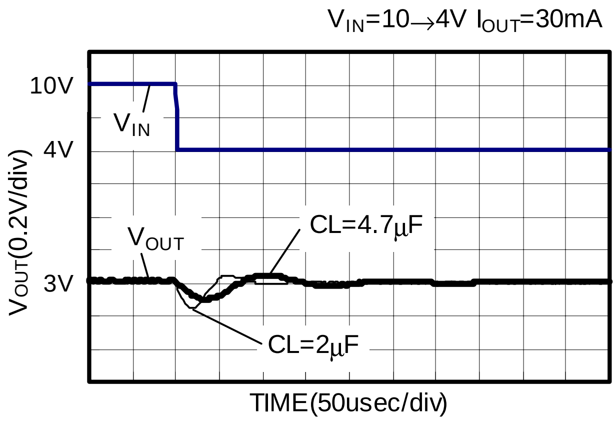


Temperature dependence of overshoot

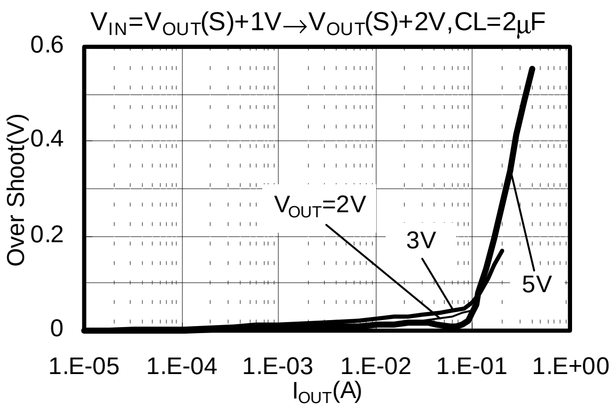


(3) Power fluctuation

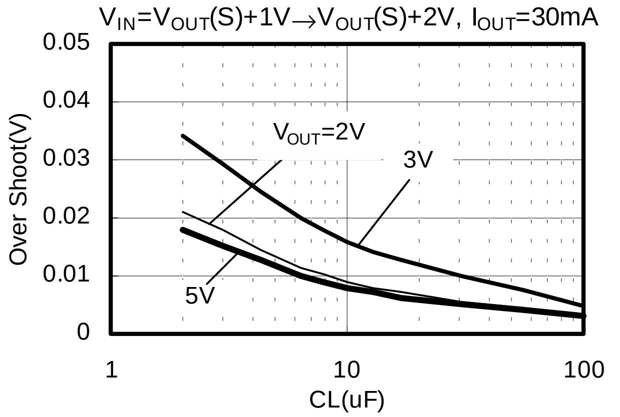




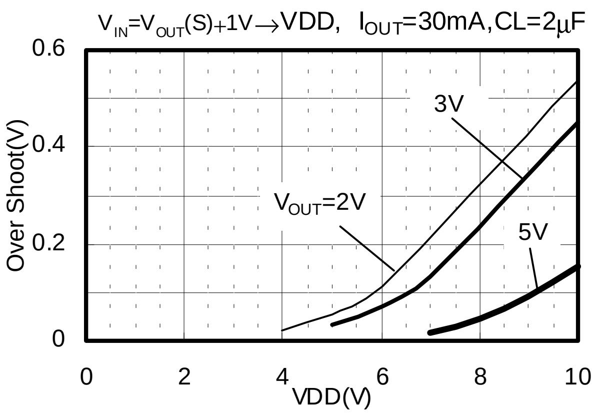
Load dependence of overshoot



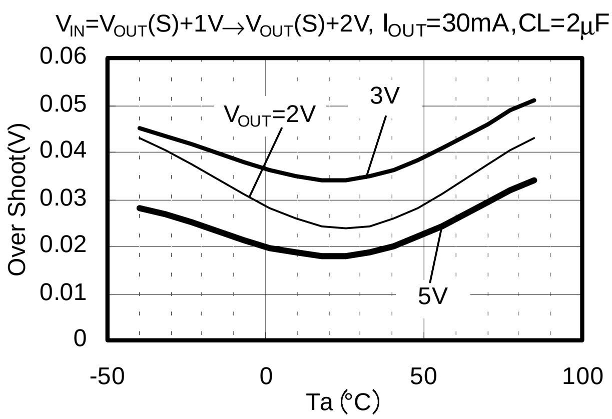
Output capacitor (CL) dependence of overshoot



VDD dependence of overshoot

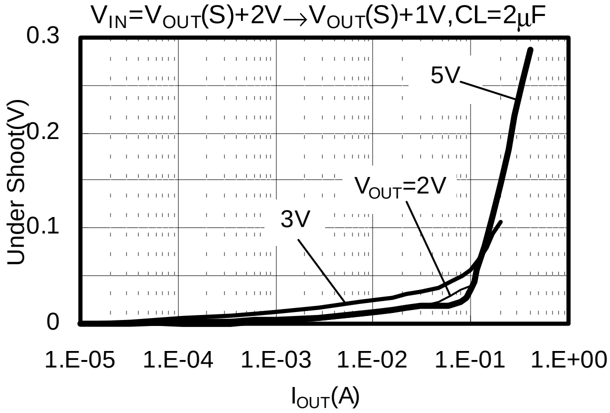


Temperature dependence of overshoot



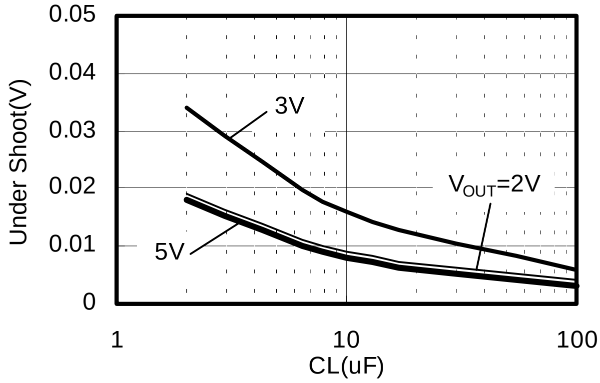
Load dependence of undershoot

$V_{IN}=V_{OUT}(S)+2V \rightarrow V_{OUT}(S)+1V, CL=2\mu F$



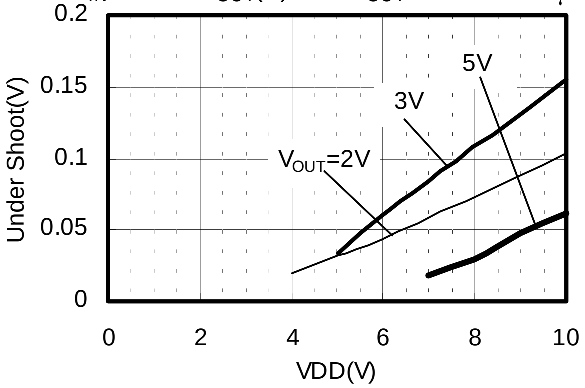
Output capacitor (CL) dependence of undershoot

$V_{IN}=V_{OUT}(S)+2V \rightarrow V_{OUT}(S)+1V, I_{OUT}=30mA$



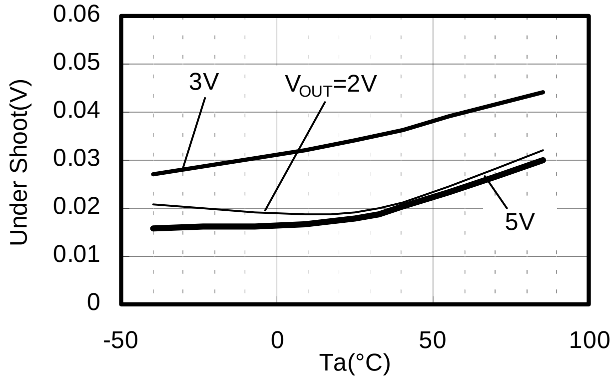
VDD dependence of undershoot

$V_{IN}=VDD \rightarrow V_{OUT}(S)+1V, I_{OUT}=30mA, CL=2\mu F$

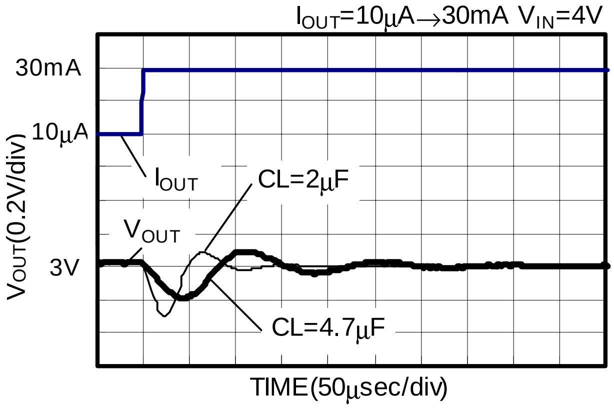


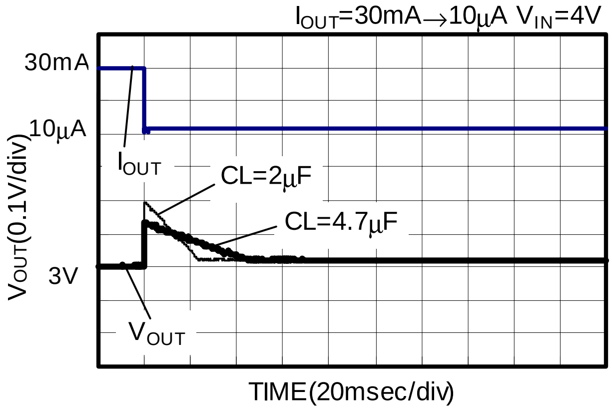
Temperature dependence of undershoot

$V_{IN}=V_{OUT}(S)+2V \rightarrow V_{OUT}(S)+1V, I_{OUT}=30mA, CL=2\mu F$



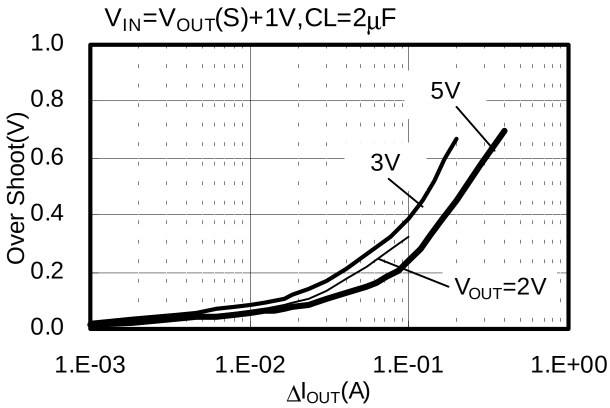
(4) Load fluctuation



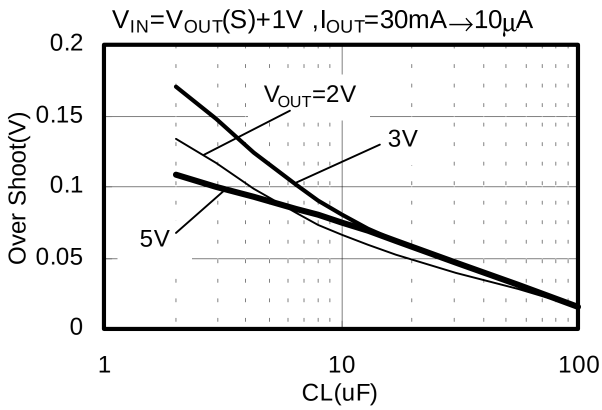


Load current dependence of load fluctuation overshoot

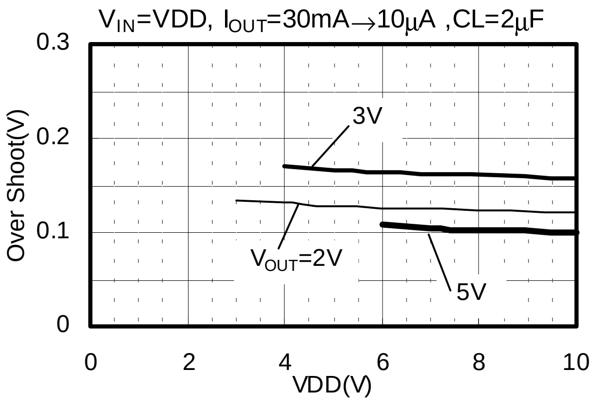
ΔI_{OUT} shows larger load current at load current fluctuation while smaller current is fixed to 10 μA. For example ΔI_{OUT}=1.E-02 (A) means load current fluctuation from 10 mA to 10 μA.



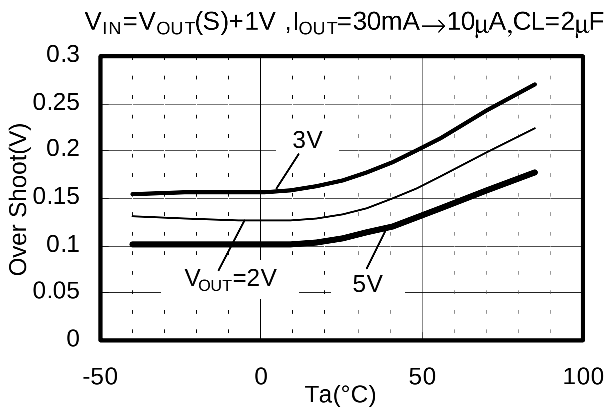
Output capacitor (CL) dependence of overshoot



VDD dependence of overshoot



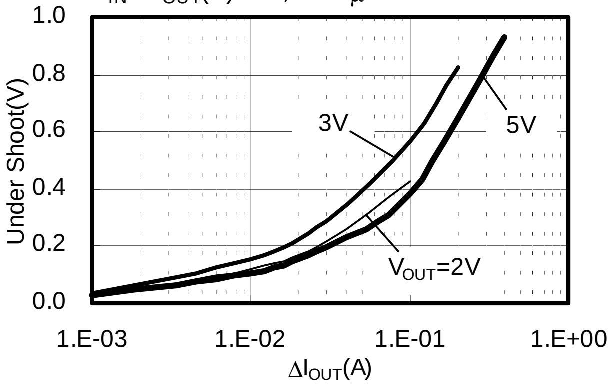
Temperature dependence of overshoot



Load current dependence of load fluctuation undershoot

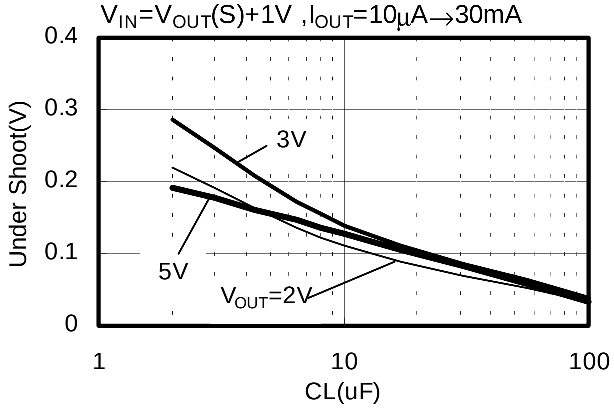
ΔI_{OUT} shows larger load current at load current fluctuation while smaller current is fixed to 10 µA. For example ΔI_{OUT}=1.E-02 (A) means load current fluctuation from 10 µA to 10 mA.

$V_{IN}=V_{OUT}(S)+1V$, CL=2µF



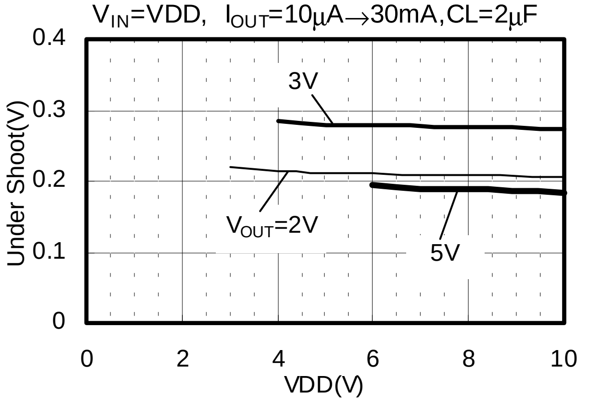
Output capacitor (CL) dependence of undershoot

$V_{IN}=V_{OUT}(S)+1V$, I_{OUT}=10µA→30mA



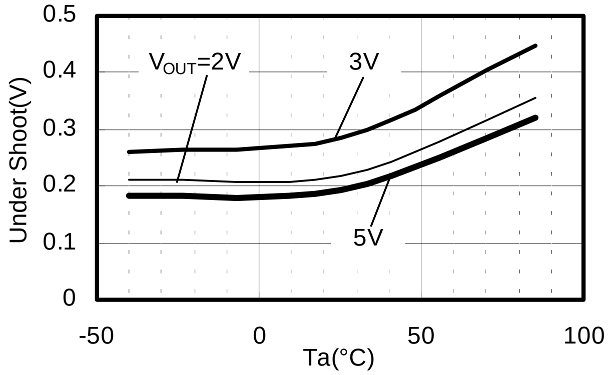
VDD dependence of undershoot

V_{IN}=VDD, I_{OUT}=10µA→30mA, CL=2µF



Temperature dependence of undershoot

$V_{IN}=V_{OUT}(S)+1V$, I_{OUT}=10µA→30mA, CL=2µF

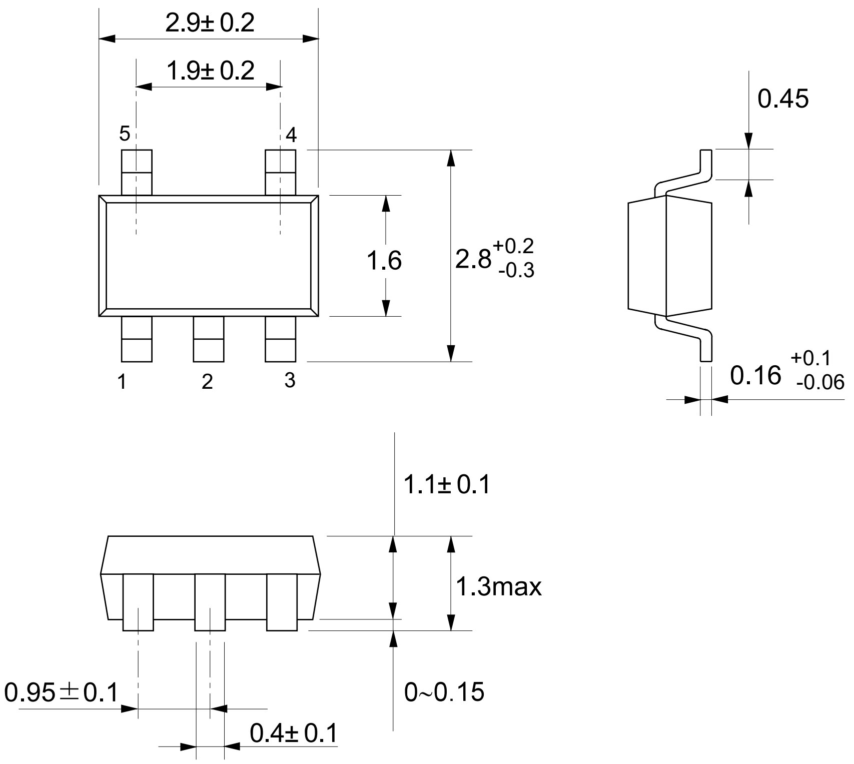


■ SOT-23-5

MP005-A 991105

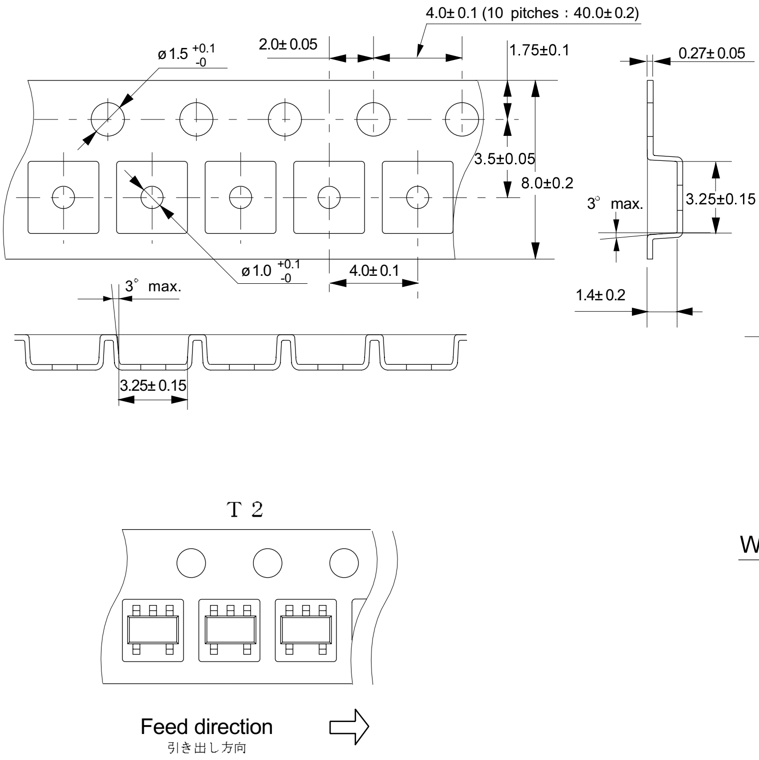
● Dimensions 外形図

Unit：mm



No.：MP005−A−P−SD−1.1

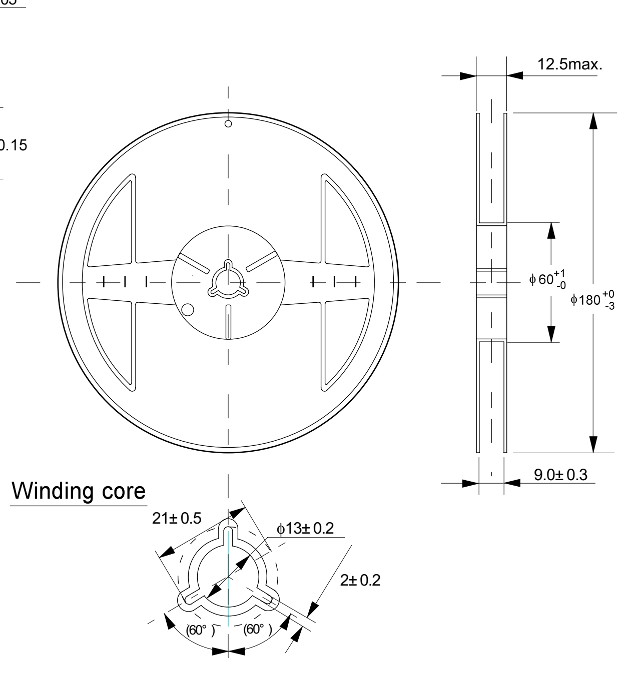
● Taping Specifications テーピング図



No.：MP005−A−C−SD−1.0

● Reel Specifications リール図

3000 pcs./reel



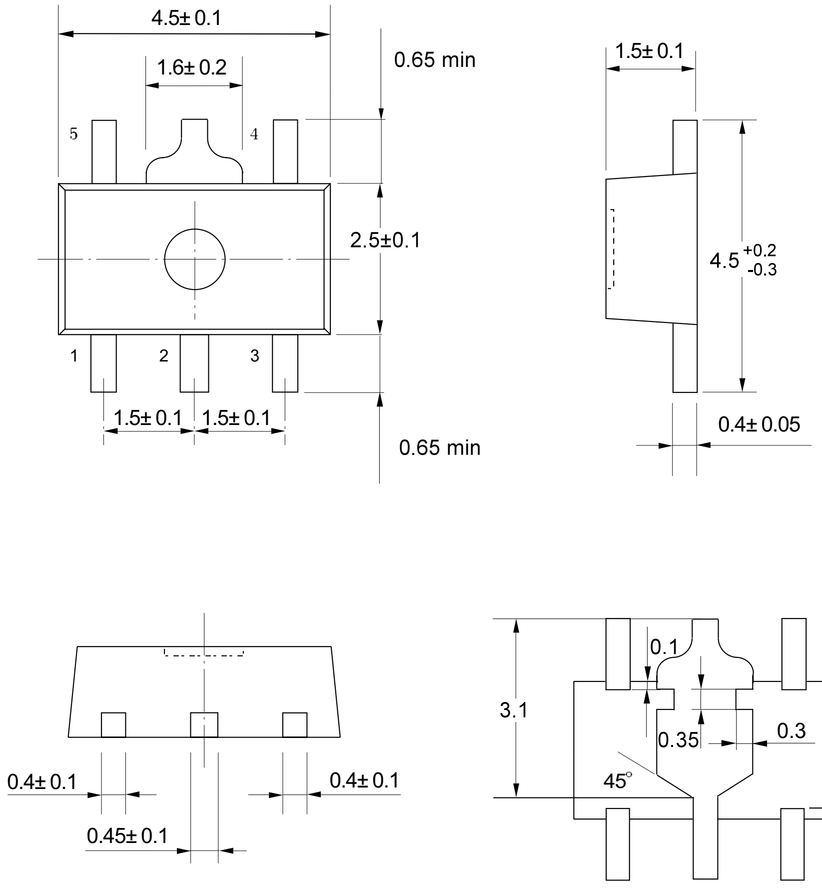
No.：MP005−A−R−SD−1.0

■ SOT-89-5

UP005-A 990531

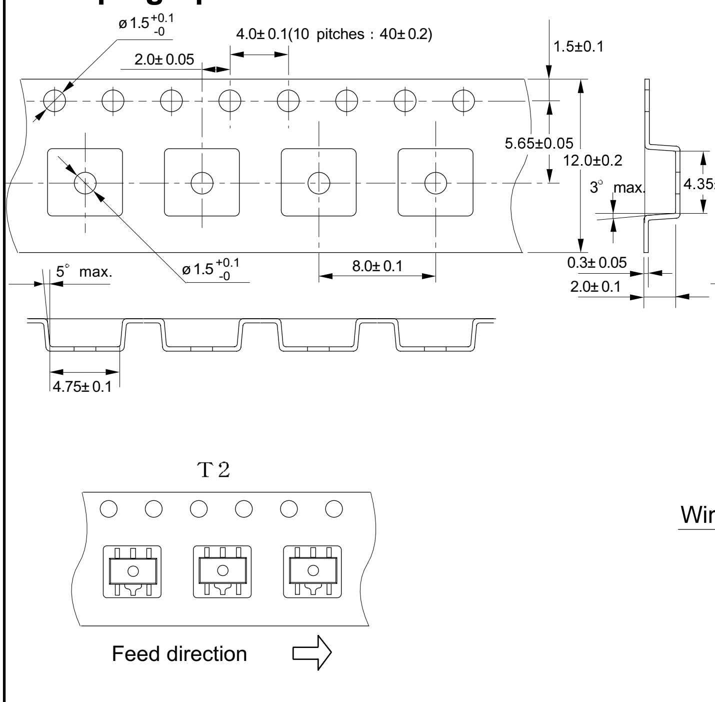
Unit : mm

● Dimensions



No. : UP005－A－P－SD－1. 1

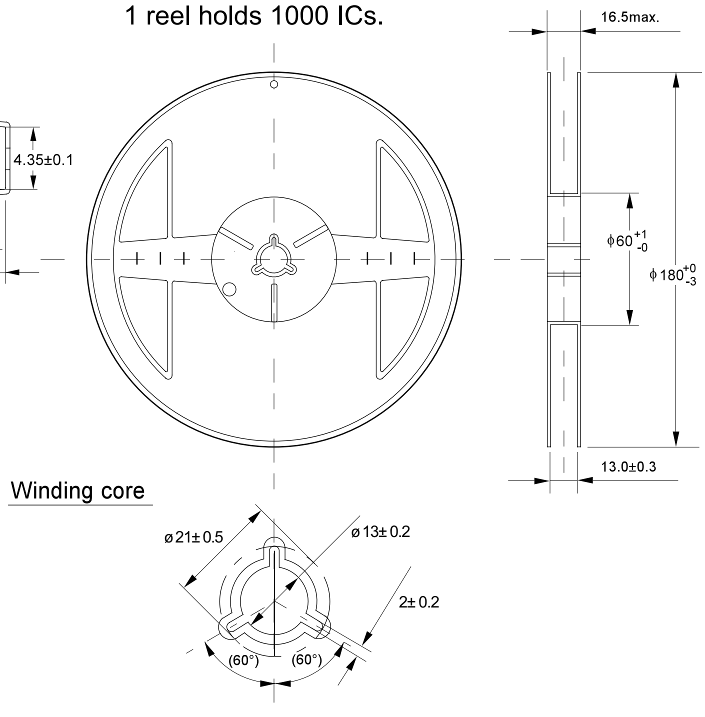
● Taping Specifications



No. : UP005－A－C－SD－1. 0

● Reel Specifications

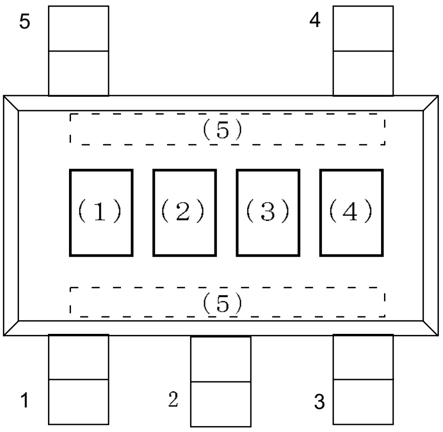
1 reel holds 1000 ICs.



No. : UP005－A－R－SD－1. 0

■Markings

● SOT-23-5



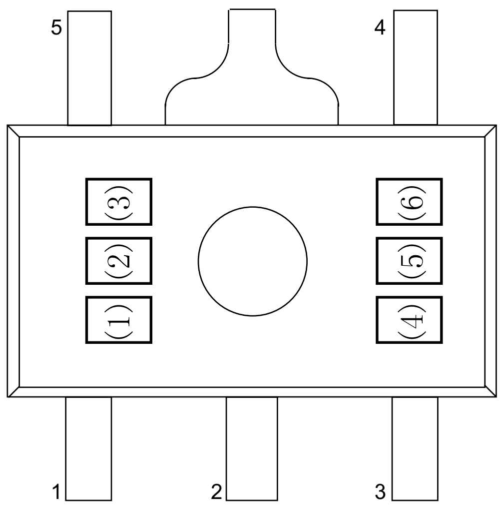
(1) to (3) : Product name (abbreviation)

(4) : Month of assembly

(5) : Dot on one side (Year and week of assembly)

No. : MP005−A−M−S1−1. 0

● SOT-89-5



(1) to (3) : Product name (abbreviation)

(4) : Year of assembly

(5) : Month of assembly

(6) : Week of assembly

No. : UP005−A−M−S1−1. 0