STK14CA8

128K x 8 *AutoStore*™ nvSRAM *QuantumTrap*™ CMOS Nonvolatile Static RAM Preliminary

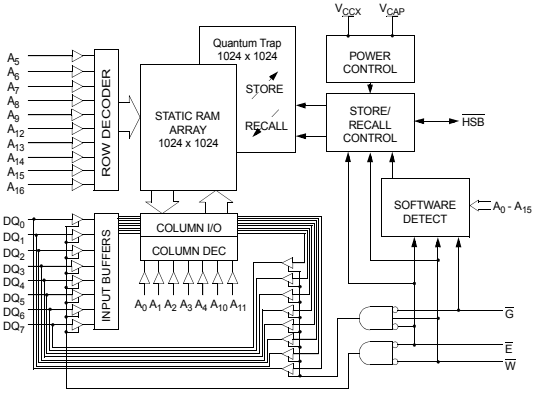
FEATURES

- **25ns, 35ns and 45ns Access Times**
- **"Hands-off" Automatic *STORE* with External 10μF Capacitor on Power Down**
- ***STORE* to *QuantumTrap*™ Nonvolatile Elements is Initiated by Software or *AutoStore*™ on Power Down**
- ***RECALL* to SRAM Initiated by Software or Power Restore**
- **5mA Typical I_{CC} at 200ns Cycle Time**
- **Unlimited READ, WRITE and *RECALL* Cycles**
- **1,000,000 *STORE* Cycles to Quantum Trap**
- **100-Year Data Retention to Quantum Trap**
- **Single 3V +20%, -10% Operation**
- **Not Sensitive to Power On/Off Ramp Rates**
- **Commercial and Industrial Temperatures**
- **SOIC, SSOP and DIP Packages**

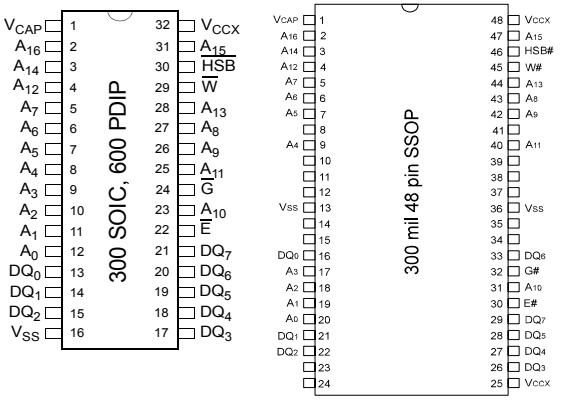
DESCRIPTION

The Simtek STK14CA8 is a fast static RAM with a nonvolatile element in each static memory cell. The embedded nonvolatile elements incorporate Simtek's *QuantumTrap*™ technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the nonvolatile elements. Data transfers from the SRAM to the nonvolatile elements (the *STORE* operation) can take place automatically on power down or under software control. A 10μF or larger capacitor tied from V_{CAP} to ground guarantees the *STORE* operation, regardless of power-down slew rate or loss of power from "hot swapping". Transfers from the nonvolatile elements to the SRAM (the *RECALL* operation) take place automatically on restoration of power or under software control.

BLOCK DIAGRAM



PIN CONFIGURATIONS



(not to scale)

PIN NAMES

A_0 - A_{16}	DQ_0 -DQ_7	$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{HSB}$	V_{CCX}	V_{CAP}	V_{SS}
Address Inputs	Data In/Out	Chip Enable	Write Enable	Output Enable	Hardware Store Busy (I/O)	Power (+ 3.3V)	Capacitor	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Power Supply Voltage . . . . . –0.5V to +3.9V
Voltage on Input Relative to V_{SS} . . . . . –0.5V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} . . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under Bias. . . . . –55°C to 125°C
Storage Temperature . . . . . –65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 3.0V +20%, -10%)[e]

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}[b]	Average V_{CC} Current		50 40 35		55 45 35	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns
I_{CC_2}[c]	Average V_{CC} Current during *STORE*		1.5		1.5	mA	All Inputs Don't Care, V_{CC} = max
I_{CC_3}[b]	Average V_{CC} Current at t_{AVAV} = 200ns 3V, 25°C, Typical		5		5	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I_{CC_4}[c]	Average V_{CAP} Current during *AutoStore*™ Cycle		0.5		0.5	mA	All Inputs Don't Care
I_{SB}[d]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		1		1	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.0	V_{CC} + .3	2.0	V_{CC} + .3	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –2mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 4mA
T_A	Operating Temperature	0	70	–40	85	°C	

Note b: I_{CC_1} and I_{CC_3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: I_{CC_2} and I_{CC_4} are the average currents required for the duration of the respective *STORE* cycles (t_{STORE}).
Note d: $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.
Note e: V_{CC} reference levels throughout this datasheet refer to V_{CCX}.

AC TEST CONDITIONS

Input Pulse Levels . . . . . 0V to 3V
Input Rise and Fall Times. . . . . ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

CAPACITANCE[f] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note f: These parameters are guaranteed but not tested.

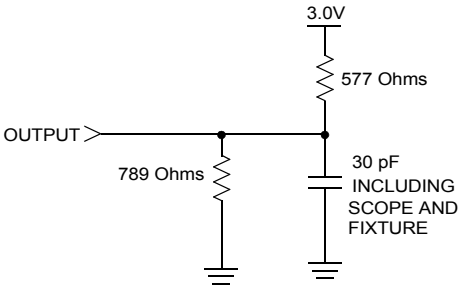


Figure 1: AC Output Loading

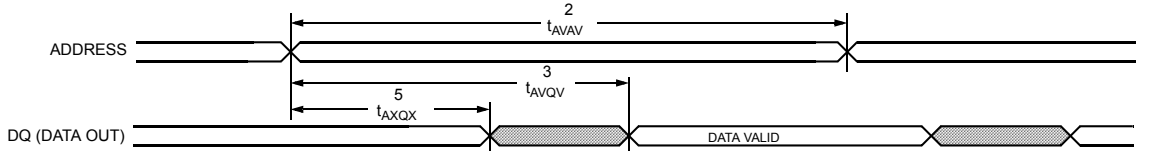
SRAM READ CYCLES #1 & #2

(V_{CC} = 3.0V +20%, -10%)[e]

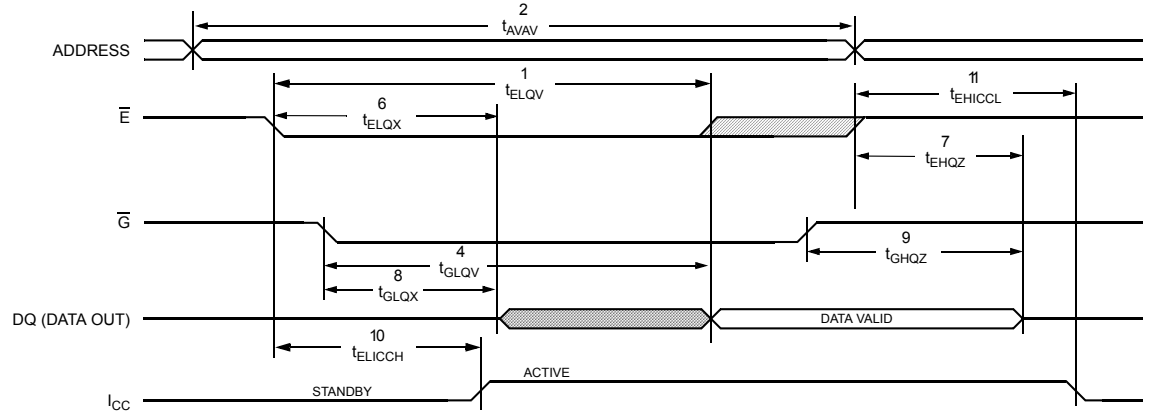
NO.	SYMBOLS		PARAMETER	STK14CA8-25		STK14CA8-35		STK14CA8-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}[g]	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}[h]	t_{AA}	Address Access Time		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20	ns
5	t_{AXQX}[h]	t_{OH}	Output Hold after Address Change	3		3		3		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	3		3		3		ns
7	t_{EHQZ}[i]	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}[i]	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10	t_{ELICCH}[f]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	t_{EHICCL}[f]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Note g: $\overline{W}$ and $\overline{HSB}$ must be high during SRAM READ cycles.
Note h: Device is continuously selected with $\overline{E}$ and $\overline{G}$ both low.
Note i: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled[g, h]



SRAM READ CYCLE #2: $\overline{E}$ Controlled[g]



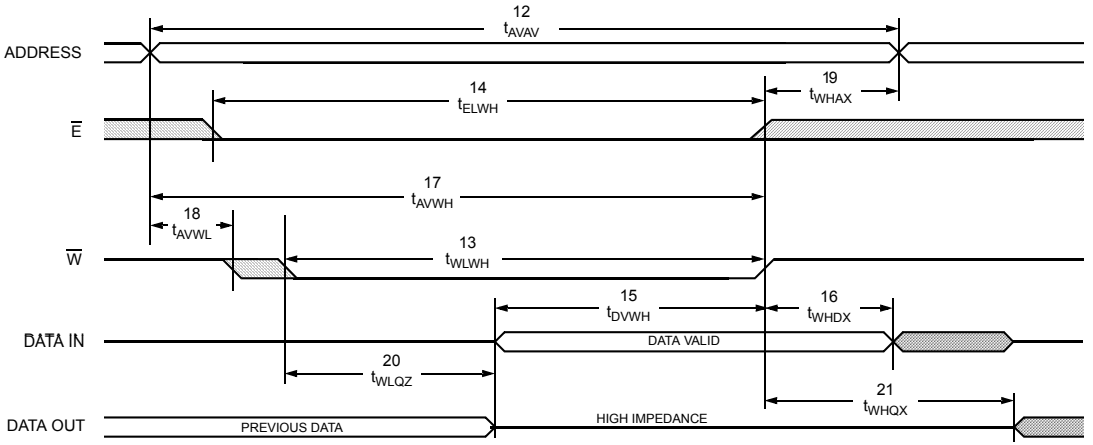
SRAM WRITE CYCLES #1 & #2

(V_{CC} = 3.0V +20%, -10%)[e]

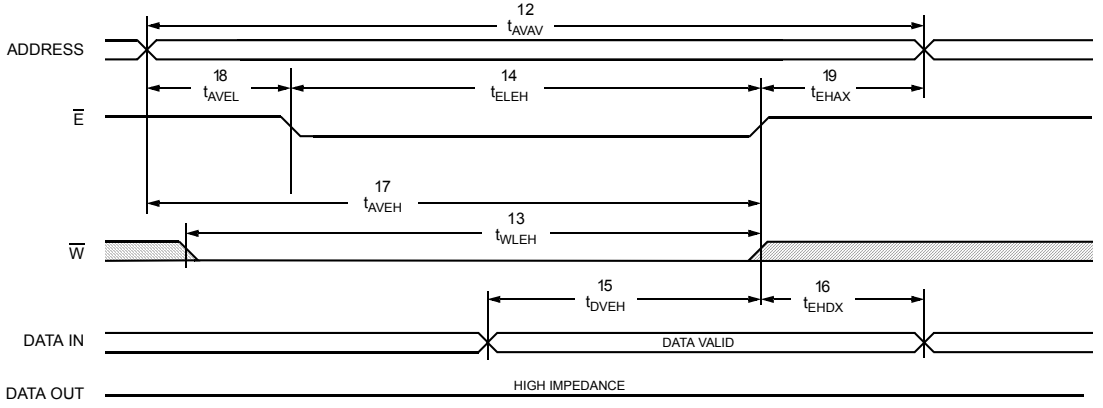
NO.	SYMBOLS			PARAMETER	STK14CA8-25		STK14CA8-35		STK14CA8-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns
20	t_{WLQZ}[i, j]		t_{WZ}	Write Enable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	3		3		3		ns

Note j: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
Note k: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note l: $\overline{HSB}$ must be high during SRAM WRITE cycles.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[k, l]



SRAM WRITE CYCLE #2: $\overline{E}$ Controlled[k, l]



MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{G}$	A_{15} - A_0 (hex)	MODE	I/O	POWER	NOTES
H	X	X	X	Not Selected	Output High Z	Standby	
L	H	L	X	Read SRAM	Output Data	Active	
L	L	X	X	Write SRAM	Input Data	Active	
L	H	L	4E38 B1C7 83E0 7C1F 703F 8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Autostore Inhibit	Output Data Output Data Output Data Output Data Output Data Output Data	Active	m, n, o
L	H	L	4E38 B1C7 83E0 7C1F 703F 4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Autostore inhibit off	Output Data Output Data Output Data Output Data Output Data Output Data	Active	m, n, o
L	H	L	4E38 B1C7 83E0 7C1F 703F 8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC_2}	m, n, o
L	H	L	4E38 B1C7 83E0 7C1F 703F 4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active	m, n, o

Note m: The six consecutive addresses must be in the order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.
Note n: While there are 17 addresses on the STK14CA8, only the lower 16 are used to control software modes.
Note o: I/O state depends on the state of $\overline{G}$. The I/O table shown assumes $\overline{G}$ low.

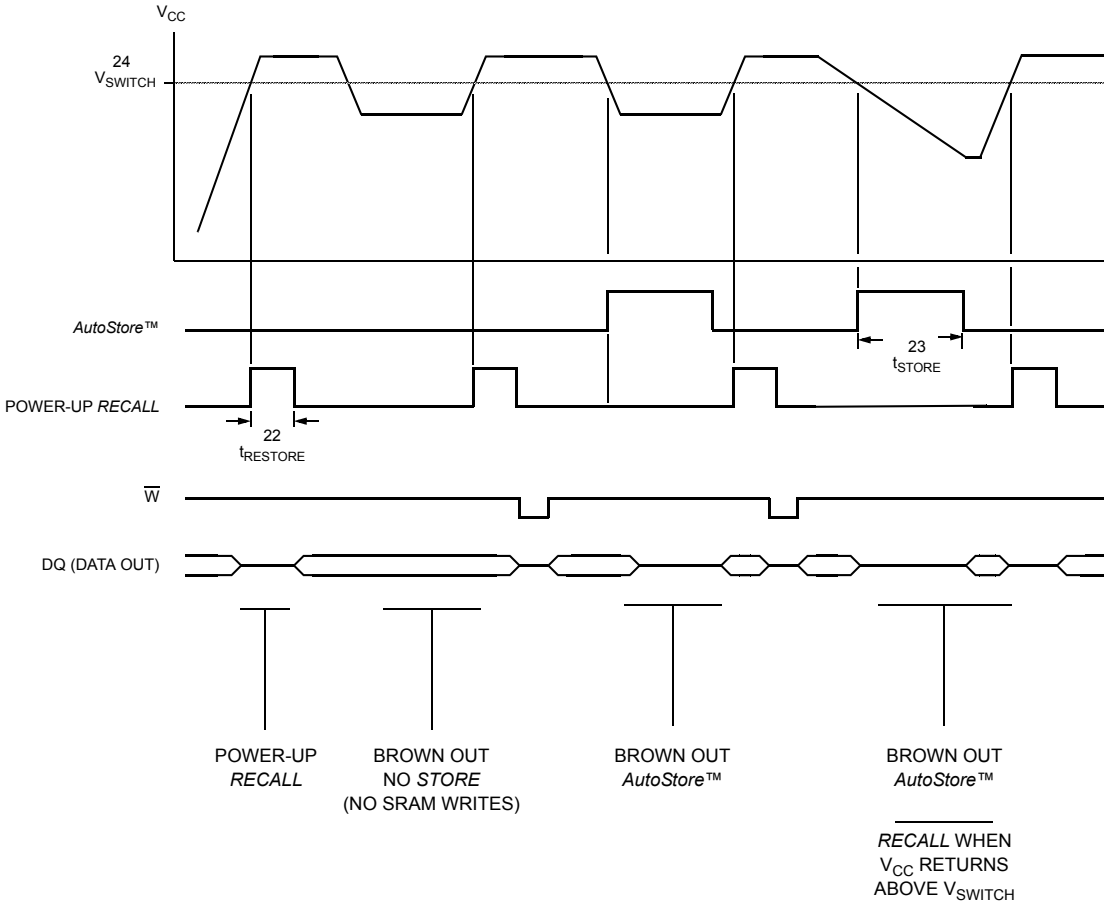
AutoStore™/POWER-UP *RECALL*

(V_{CC} = 3.0V +20%, -10%)[e]

NO.	SYMBOLS		PARAMETER	STK14CA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	$t_{RESTORE}$		Power-up *RECALL* Duration		5	ms	p
23	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		10	ms	q
24	V_{SWITCH}		Low Voltage Trigger Level	2.55	2.65	V	

Note p: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.
Note q: If an SRAM WRITE has not taken place since the last nonvolatile cycle, no *STORE* will take place.

AutoStore™/POWER-UP *RECALL*

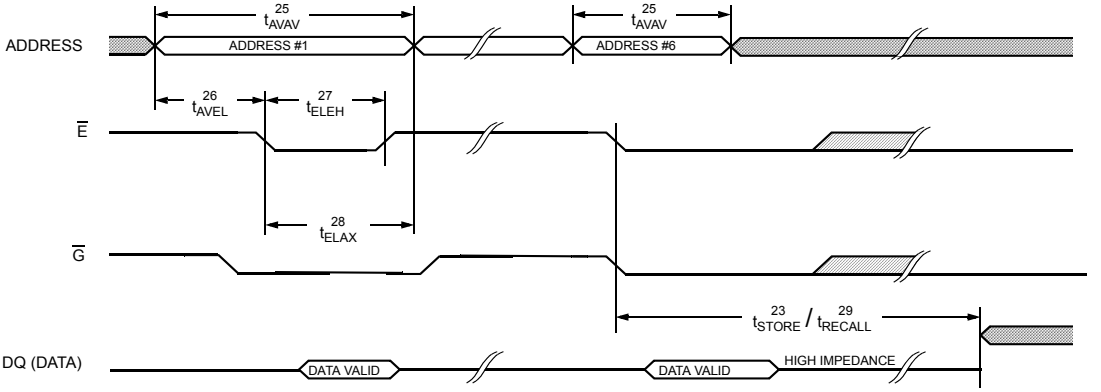


SOFTWARE-CONTROLLED *STORE*/*RECALL* CYCLE[t] (V_{CC} = 3.0V +20%, -10%)[e]

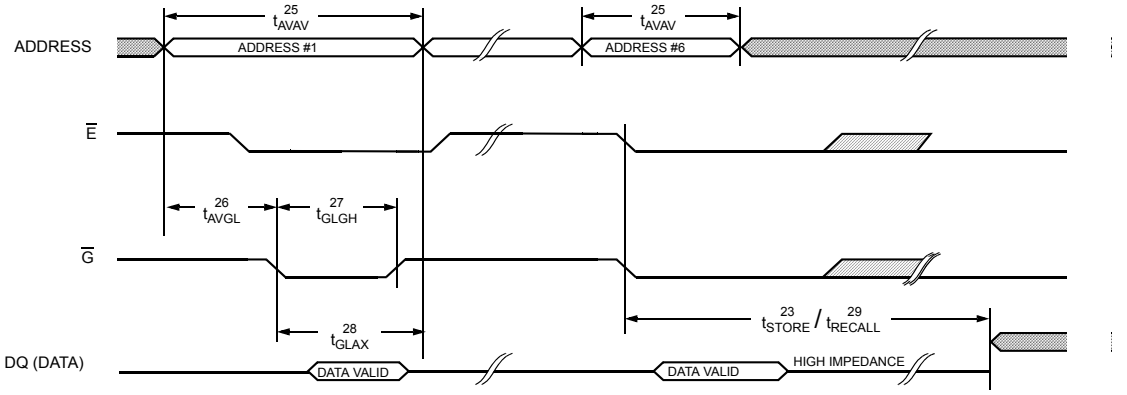
NO.	SYMBOLS			PARAMETER	STK14CA8-25		STK14CA8-35		STK14CA8-45		UNITS	NOTES
	$\overline{E}$ cont	$\overline{G}$ cont	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
25	t_{AVAV}	t_{AVAV}	t_{RC}	*STORE*/*RECALL* Initiation Cycle Time	25		35		45		ns	s
26	t_{AVEL}	t_{AVGL}	t_{AS}	Address Set-up Time	0		0		0		ns	
27	t_{ELEH}	t_{GLGH}	t_{CW}	Clock Pulse Width	20		25		30		ns	
28	t_{ELAX}	t_{GLAX}		Address Hold Time	20		20		20		ns	
29	t_{RECALL}	t_{RECALL}		*RECALL* Duration		20		20		20	µs	

Note r: The software sequence is clocked with $\overline{E}$ controlled READs or $\overline{G}$ controlled READs.
Note s: The six consecutive addresses must be in the order listed in the Hardware Mode Selection Table: (4E38, B1C7, 83E0, 7C1F, 703F, 8FC0) for a *STORE* cycle or (4E38, B1C7, 83E0, 7C1F, 703F, 4C63) for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE *STORE*/*RECALL* CYCLE: $\overline{E}$ CONTROLLED[s]



SOFTWARE *STORE*/*RECALL* CYCLE: $\overline{G}$ CONTROLLED[s]

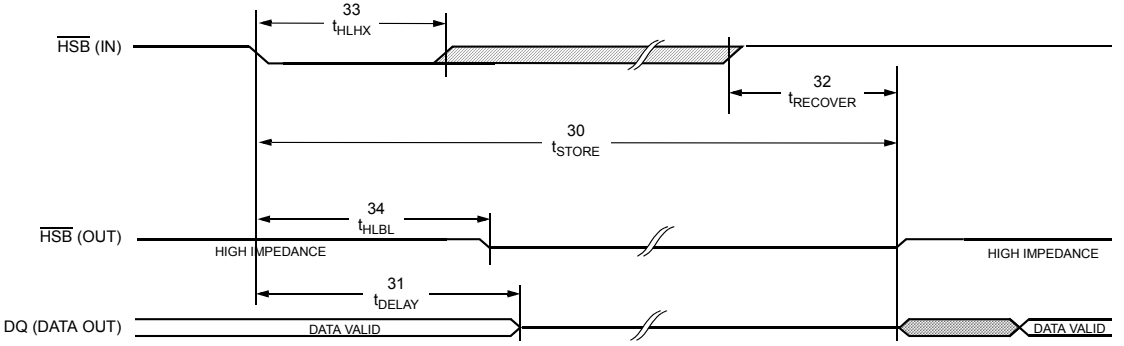


HARDWARE *STORE* CYCLE[t] (V_{CC} = 3.0V +20%, -10%)[e]

NO.	SYMBOLS		PARAMETER	STK14CA8		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
30	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		10	ms	i
31	t_{DELAY}	t_{HLQZ}	Time Allowed to Complete SRAM Cycle	1		µs	i
32	$t_{RECOVER}$	t_{HHQX}	Hardware *STORE* High to Inhibit Off		100	ns	t
33	t_{HLHX}		Hardware *STORE* Pulse Width	15		ns	
34	t_{HLBL}		Hardware *STORE* Low to *STORE* Busy		300	ns	

Note t: $t_{RECOVER}$ is only applicable after t_{STORE} is complete.

HARDWARE *STORE* CYCLE



DEVICE OPERATION

The STK14CA8 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to the nonvolatile elements (the *STORE* operation) or from the nonvolatile elements to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

SRAM READ

The STK14CA8 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ and $\overline{HSB}$ are high. The address specified on pins A_{0-16} determines which of the 131,072 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high, or $\overline{W}$ or $\overline{HSB}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low and $\overline{HSB}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

AutoStore™ OPERATION

The STK14CA8 can be powered in one of three modes.

During normal operation, the STK14CA8 will draw current from V_{CCX} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single *STORE* operation. After power up, when the voltage on the V_{CCX} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CCX} and initiate a *STORE* operation.

Figure 2 shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of between 10µF and 100µF (± 20%) rated at 5V should be provided.

In order to prevent unneeded *STORE* operations, automatic *STORE*s as well as those initiated by externally driving $\overline{HSB}$ low, will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle. Software initiated *STORE* cycles are performed regardless of whether a WRITE operation has taken place. $\overline{HSB}$ can be used to signal the system that the *AutoStore*™ cycle is in progress.

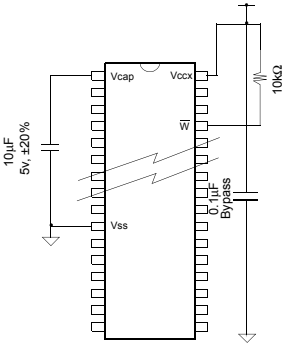


Figure 2: *AutoStore*™ Mode

If $\overline{HSB}$ is not used it should be left unconnected

$\overline{HSB}$ OPERATION

The STK14CA8 provides the $\overline{HSB}$ pin for controlling and acknowledging the *STORE* operations. The $\overline{HSB}$ pin can be used to request a hardware *STORE* cycle. When the $\overline{HSB}$ pin is driven low, the STK14CA8 will conditionally initiate a *STORE* operation after t_{DELAY}; an actual *STORE* cycle will only begin if a WRITE to the SRAM took place since the last *STORE* or *RECALL* cycle. The $\overline{HSB}$ pin also acts as an open drain driver that is internally driven low to indicate a busy condition while the *STORE* (initiated by any

means) is in progress.

SRAM READ and WRITE operations that are in progress when $\overline{HSB}$ is driven low by any means are given time to complete before the *STORE* operation is initiated. After $\overline{HSB}$ goes low, the STK14CA8 will continue SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{HSB}$ is pulled low it will be allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes low will be inhibited until $\overline{HSB}$ returns high.

The $\overline{HSB}$ pin can be used to synchronize multiple STK14CA8s while using a single larger capacitor. To operate in this mode the $\overline{HSB}$ pin should be connected together to the $\overline{HSB}$ pins from the other STK14CA8s. An external pull-up resistor to + 3.3V is required since $\overline{HSB}$ acts as an open drain pull down. The V_{CAP} pins from the other STK14CA8 parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the STK14CA8s detects a power loss and asserts $\overline{HSB}$, the common $\overline{HSB}$ pin will cause all parts to request a *STORE* cycle (a *STORE* will take place in those STK14CA8s that have been written since the last nonvolatile cycle).

During any *STORE* operation, regardless of how it was initiated, the STK14CA8 will continue to drive the $\overline{HSB}$ pin low, releasing it only when the *STORE* is complete. Upon completion of the *STORE* operation the STK14CA8 will remain disabled until the $\overline{HSB}$ pin returns high.

If $\overline{HSB}$ is not used, it should be left unconnected.

POWER-UP *RECALL*

During power up, or after any low-power condition ($V_{CCX} < V_{SWITCH}$), an internal *RECALL* request will be latched. When V_{CAP} once again exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

If the STK14CA8 is in a WRITE state at the end of power-up *RECALL*, the WRITE will be inhibited and $\overline{E}$ or $\overline{W}$ must be brought high and then low for a write to initiate.

SOFTWARE NONVOLATILE *STORE*

The STK14CA8 software *STORE* cycle is initiated by executing sequential $\overline{E}$ controlled READ cycles from six specific address locations. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

1.	Read address	4E38 (hex)	Valid READ
2.	Read address	B1C7 (hex)	Valid READ
3.	Read address	83E0 (hex)	Valid READ
4.	Read address	7C1F (hex)	Valid READ
5.	Read address	703F (hex)	Valid READ
6.	Read address	8FC0 (hex)	Initiate *STORE* cycle

The software sequence may be clocked with $\overline{E}$ controlled READs or $\overline{G}$ controlled READs .

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE *RECALL*

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of $\overline{E}$ controlled READ operations must be performed:

1.	Read address	4E38 (hex)	Valid READ
2.	Read address	B1C7 (hex)	Valid READ
3.	Read address	83E0 (hex)	Valid READ
4.	Read address	7C1F (hex)	Valid READ
5.	Read address	703F (hex)	Valid READ
6.	Read address	4C63 (hex)	Initiate *RECALL* cycle

Internally, *RECALL* is a two-step procedure. First, the

SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

HARDWARE PROTECT

The STK14CA8 offers hardware protection against inadvertent *STORE* operation and SRAM WRITEs during low-voltage conditions. When $V_{CCX} < V_{SWITCH}$, all externally initiated *STORE* operations and SRAM WRITEs will be inhibited.

PREVENTING STORES

The *AutoStore*™ function can be disabled on the fly by initiating an *AutoStore Inhibit* sequence. A sequence of read operations is performed in a manner similar to the software *STORE* initiation. To initiate the *AutoStore Inihibit* sequence, the following sequence of $\overline{E}$ controlled read operations must be performed:

1.	Read address	4E38 (hex)	Valid READ
2.	Read address	B1C7 (hex)	Valid READ
3.	Read address	83E0 (hex)	Valid READ
4.	Read address	7C1F (hex)	Valid READ
5.	Read address	703F (hex)	Valid READ
6.	Read address	8B45 (hex)	*AutoStore Inhibit*

Once the *AutoStore*™ inhibit has been initiated, it will remain active until an *AutoStore*™ inhibit off sequence has been performed, regardless of potential power cycling of the device.

The *AutoStore Inhibit* can be disabled by initiating an *AutoStore Inhibit Off* sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the *AutoStore Inhibit Off* sequence, the following sequence of E controlled read operations must be performed:

1.	Read address	4E38 (hex)	Valid READ
2.	Read address	B1C7 (hex)	Valid READ
3.	Read address	83E0 (hex)	Valid READ
4.	Read address	7C1F (hex)	Valid READ
5.	Read address	703F (hex)	Valid READ
6.	Read address	4B46 (hex)	*AutoStore Inhibit Off*

NOISE CONSIDERATIONS

The STK14CA8 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CCX} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

LOW AVERAGE ACTIVE POWER

The STK14CA8 draws significantly less current when it is cycled at times longer than 50ns. Figure 3 shows the relationship between I_{CC} and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 3.6V, 100% duty cycle on chip enable). Figure 4 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK14CA8 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READs to WRITEs; 5) the operating temperature; 6) the V_{cc} level; and 7) I/O loading.

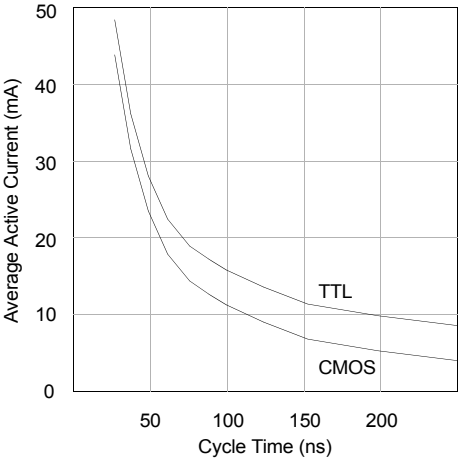


Figure 3: I_{cc} (max) Reads

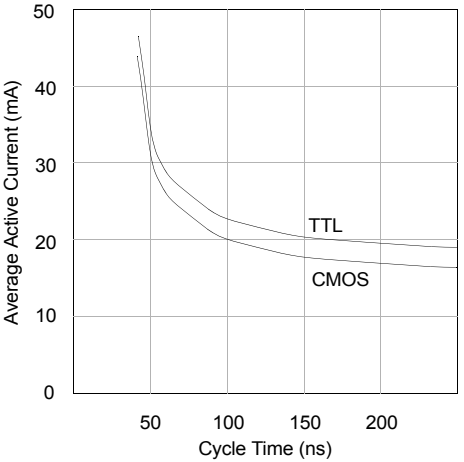


Figure 4: I_{cc} (max) Writes

ORDERING INFORMATION

STK14CA8 - N F 45 I

Temperature Range
- Blank = Commercial (0 to 70°C)
- I = Industrial (-40 to 85°C)

Access Time
- 25 = 25ns
- 35 = 35ns
- 45 = 45ns

Lead Finish
- Blank = 85%Sn/15%Pb
- F = 100% Sn (Matte Tin)

Package
- N = Plastic 32-pin 300 mil SOIC (50 mil pitch)
- W = Plastic 32-pin 600 mil DIP (100 mil pitch)
- R = Plastic 48-pin 300 mil SSOP (25 mil pitch)

Document Revision History

Revision	Date	Summary
0.0	January 2003	Publish new datasheet
0.1	May 2003	Add 48 pin SSOP, Modify AutoStore drawing (Figure 2), Update Mode Selection Table and Absolute Maximum Ratings, Added $\overline{G}$ control software store
0.2	September 2003	Added lead-free lead finish