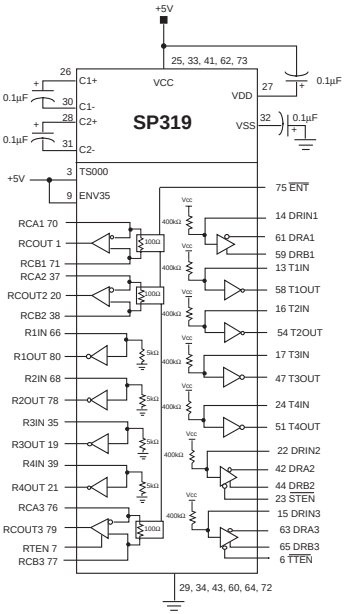
20Mbps, +5V-Only V.35 Interface with RS-232 (V.28) Control Lines

- 20Mbps V.35 Data Throughput
- +5V-Only, Single Supply Operation
- 3 Drivers, 3 Receivers – V.35
- 4 Drivers, 4 Receivers – RS-232
- Improved V.35 Receiver Propagation Delays
- No External V.35 Termination Resistors Required
- Termination Disable for V.35
- 80-pin QFP Surface Mount Packaging
- Pin Compatible with SP320

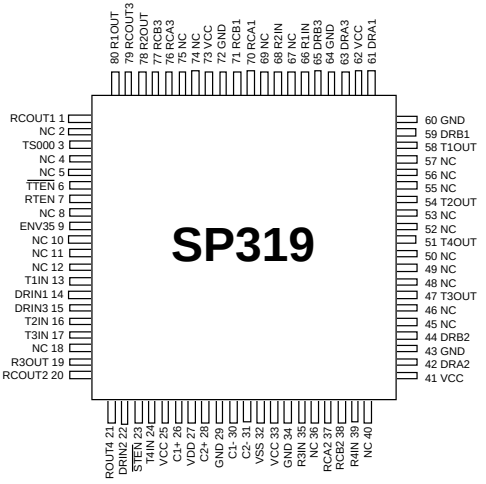
DESCRIPTION

The **SP319** is a complete V.35 interface transceiver offering 3 drivers and 3 receivers for V.35, and 4 drivers and 4 receivers for RS-232 (V.28). A **Sipex** patented charge pump allows +5V only low power operation. RS-232 drivers and receivers are specified to operate at 120kbps, all V.35 drivers and receivers operate up to 10Mbps.

Typical Applications Circuit



Pinout



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}.....+7V
Input Voltages
Logic.....-0.3V to (V_{CC}+0.5V)
Drivers.....-0.3V to (V_{CC}+0.5V)
Receivers.....±30V at ≤100mA
Output Voltages
Logic.....-0.3V to (V_{CC}+0.5V)
Drivers.....±14V
Receivers.....-0.3V to (V_{CC}+0.5V)
Storage Temperature.....-65˚C to +150˚C

Power Dissipation per Package
80-pin QFP (derate 18.3mW/ºC above +70ºC).....1500mW

SPECIFICATIONS

T_{AMB} = T_{MIN} to T_{MAX} and V_{CC} = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.35 DRIVER					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Voltage Outputs					
Open Circuit Voltage			±1.2	Volts	Refer to *Figure 1*
Differential Outputs	±0.44	±0.55	±0.66	Volts	R_L=100Ω from A to B; *Figure 2*
Source Impedance	50	100	150	Ohms	*Figure 4*
Short Circuit Impedance	135	150	165	Ohms	Measured from A=B to Gnd, V_{OUT}=-2V to +2V; *Figure 5*; T_{AMB} = +25ºC
Voltage Output Offset	-0.6		+0.6	Volts	V_{Offset}={[V_A|+|V_B|]/2}; *Figure 3*
AC Characteristics					T_{AMB} = +25ºC for all AC parameters
Transition Time		40		ns	10% to 90%; *Figure 6*
Maximum Transmission Rate	10			Mbps	$V_{DIFF\ OUT}$= 0.55V±20% ; *Figure 9*
Propagation Delay					
t_{PHL}		80	100	ns	Measured from 1.5V of V_{IN} to 50% of V_{OUT}; *Figure 9*, *10*
t_{PLH}		80	100	ns	Measured from 1.5V of V_{IN} to 50% of V_{OUT}; *Figure 9*, *10*
V.35 RECEIVER					
TTL Output Levels					
V_{OL}			0.4	Volts	I_{OUT}=-3.2mA
V_{OH}	2.4			Volts	I_{OUT}=1.0mA
Receiver Inputs					
Differential Input Threshold	-0.3		+0.3	Volts	
Input Impedance	90	100	110	Ohms	*Figure 7*
Short Circuit Impedance	135	150	165	Ohms	Measured from A=B to Gnd V_{IN}=-2V to +2V; *Figure 8*; T_{AMB} = +25ºC
AC Characteristics					T_{AMB} = +25ºC for all AC parameters
Maximum Transmission Rate	10			Mbps	V_{IN} = ±0.55V ±20%; *Figure 9*
Propagation Delay					
t_{PHL}		60	80	ns	Measured from 50% of V_{IN} to 1.5V of R_{OUT}; *Figure 9*, *11*
t_{PLH}		60	80	ns	Measured from 50% of V_{IN} to 1.5V of R_{OUT}; Figure 9, 11

SPECIFICATIONS (CONTINUED)

$T_{AMB} = T_{MIN}$ to T_{MAX} and V_{CC} = 5V±5% unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-232 DRIVER					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Voltage Outputs					
High Level Output	+5.0		+15.0	Volts	R_L= 3kΩ to Gnd; *Figure 13*
Low Level Output	-15.0		-5.0	Volts	R_L= 3kΩ to Gnd; *Figure 13*
Open Circuit Output	-15		+15	Volts	R_L= ∞; *Figure 12*
Short Circuit Current	-100		+100	mA	R_L= Gnd; *Figure 15*
Power Off Impedance	300			Ohms	V_{CC}= 0V; V_{OUT}= ±2V; *Figure 16*
AC Characteristics					
Slew Rate			30	V/µs	*Figure 14*
Maximum Transmission Rate	120			kbps	R_L= 3kΩ, C_L= 2500pF
Transition Time			1.56	µs	Rise/fall time, between ±3V R_L= 3kΩ, C_L= 2500pF; *Figure 17*
Propagation Delay					
t_{PHL}		2	8	µs	R_L= 3kΩ, C_L= 2500pF; From 1.5V of T_{IN} to 50% of V_{OUT}
t_{PLH}		2	8	µs	R_L= 3kΩ, C_L= 2500pF; From 1.5V of T_{IN} to 50% of V_{OUT}
RS-232 RECEIVER					
TTL Output Levels					
V_{OL}			0.4	Volts	I_{OUT} = -3.2mA
V_{OH}	2.4			Volts	I_{OUT} = 1.0mA
Receiver Input					
Input Voltage Range	-15		+15	Volts	
High Threshold		1.7	3.0	Volts	
Low Threshold	0.8	1.2		Volts	
Hysteresis	0.2	0.5	1	Volts	V_{CC}= 5V; T_A= +25˚C
Receiver Input Circuit Bias			+2.0	Volts	*Figure 19*
Input Impedance	3	5	7	kΩ	V_{IN}= ±15V; *Figure 18*
AC Characteristics					
Maximum Transmission Rate	120			kbps	
Propagation Delay					
t_{PHL}		0.1	1	µs	From 50% of R_{IN} to 1.5V of R_{OUT}
t_{PLH}		0.1	1	µs	From 50% of R_{IN} to 1.5V of R_{OUT}
POWER REQUIREMENTS					
No Load V_{CC} Supply Current		40	70	mA	No load; V_{CC}= 5.0V; T_A= 25˚C
Full Load V_{CC} Supply Current		60	80	mA	RS-232 drivers R_L= 3kΩ to Gnd; DC Input V.35 drivers R_L= 100Ω from A to B; DC Input
Shutdown Current		1.5	10	mA	TS000 = ENV35 = 0V

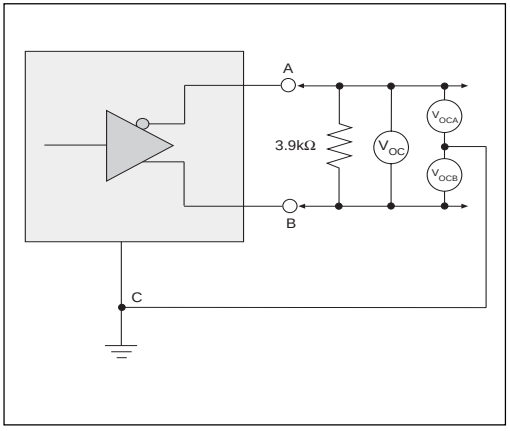


Figure 1. V.11 and V.35 Driver Output Open-Circuit Voltage

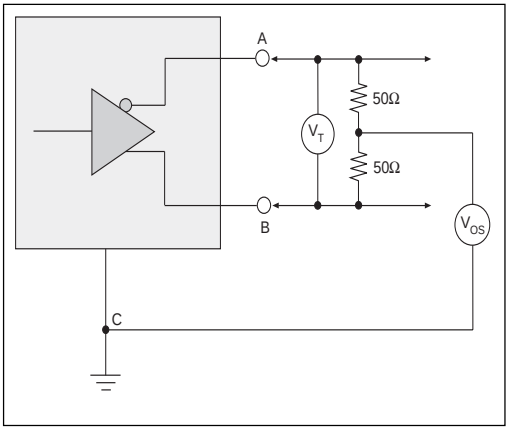


Figure 2. V.35 Driver Output Test Terminated Voltage

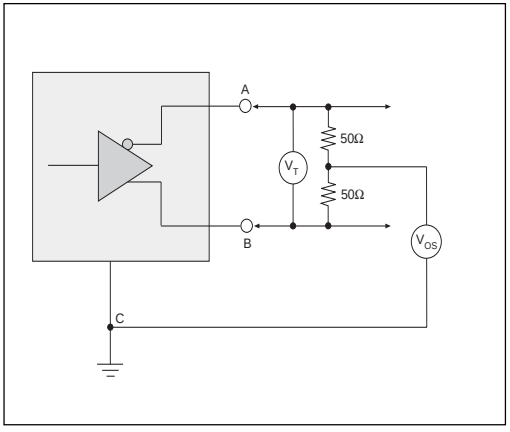


Figure 3. V.35 Driver Output Offset Voltage

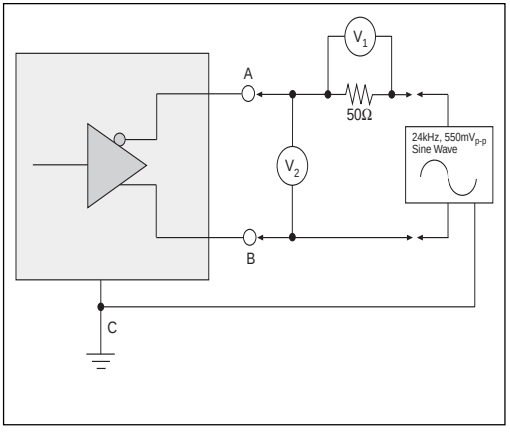


Figure 4. V.35 Driver Output Source Impedance

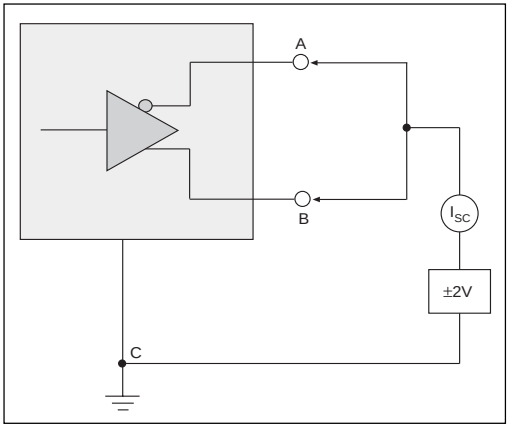


Figure 5. V.35 Driver Output Short-Circuit Impedance

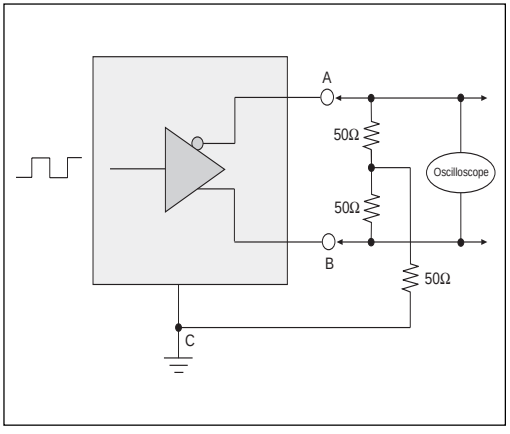


Figure 6. V.35 Driver Output Rise/Fall Time

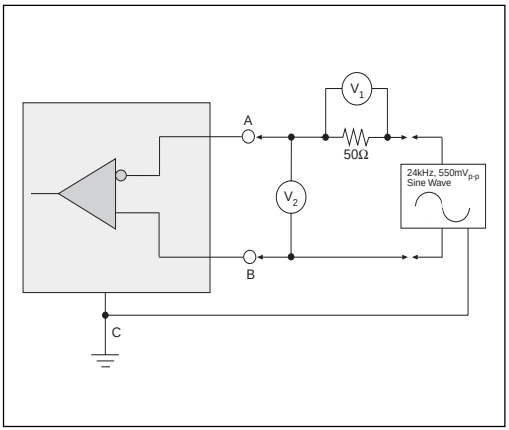


Figure 7. V.35 Receiver Input Source Impedance

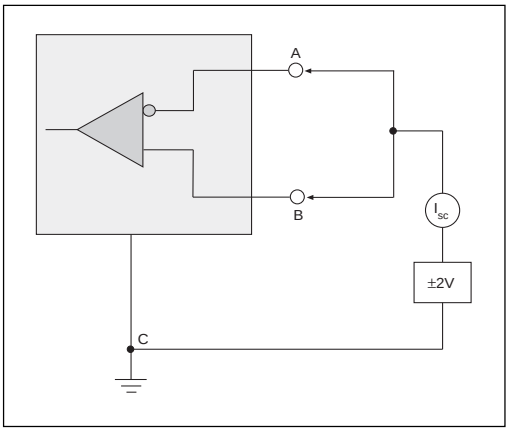


Figure 8. V.35 Receiver Input Short-Circuit Impedance

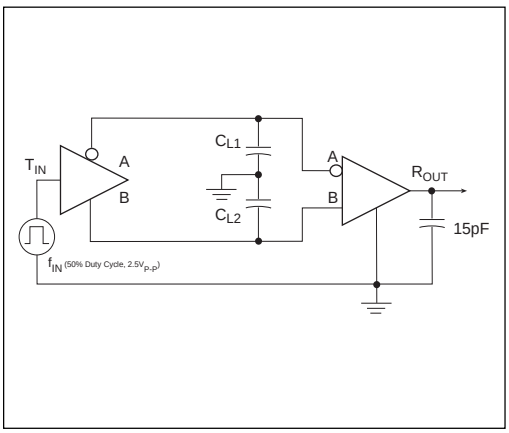


Figure 9. Driver/Receiver Timing Test Circuit

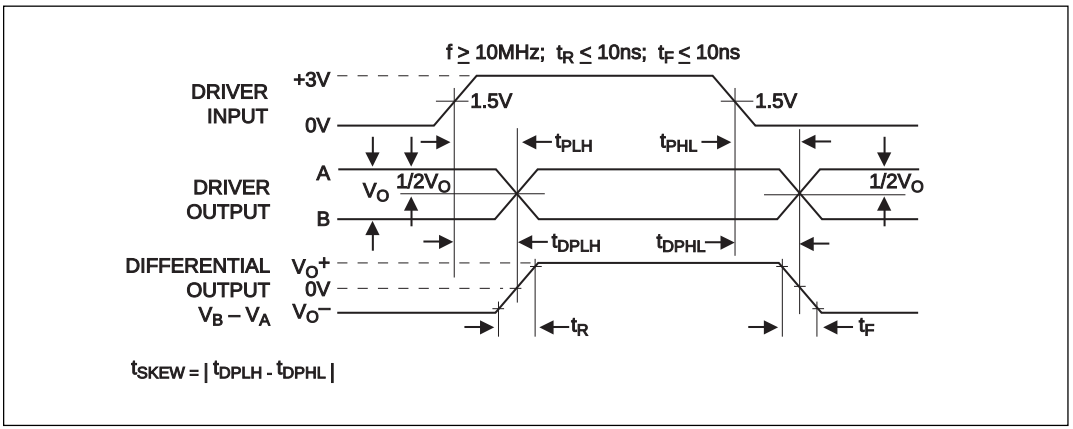


Figure 10. Driver Propagation Delays

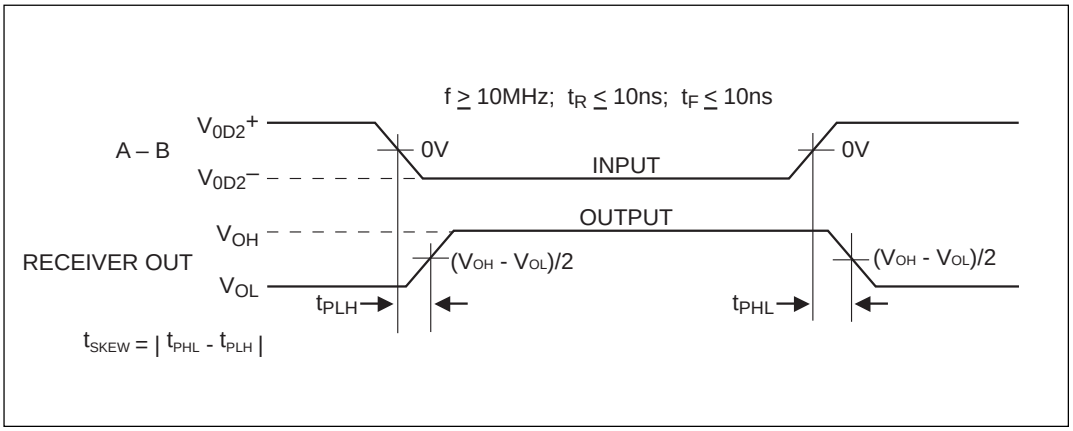


Figure 11. Receiver Propagation Delays

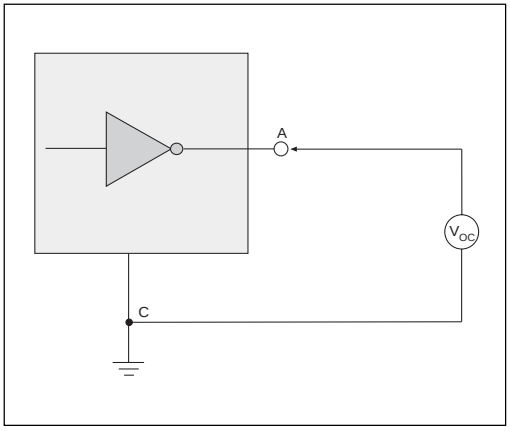


Figure 12. V.28 Driver Output Open Circuit Voltage

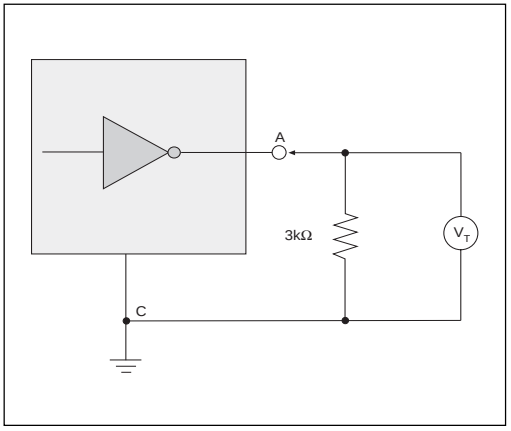


Figure 13. V.28 Driver Output Loaded Voltage

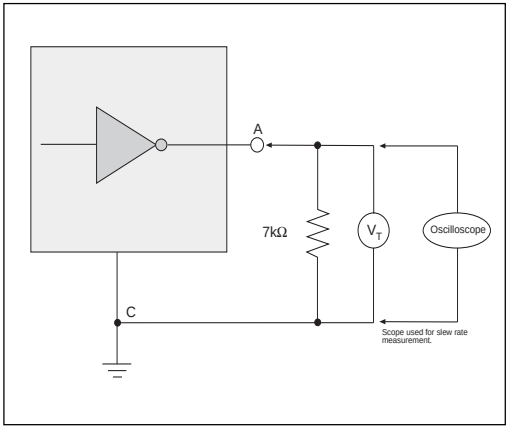


Figure 14. V.28 Driver Output Slew Rate

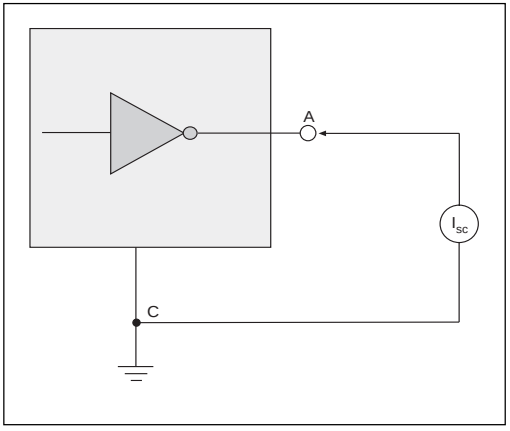


Figure 15. V.28 Driver Output Short-Circuit Current

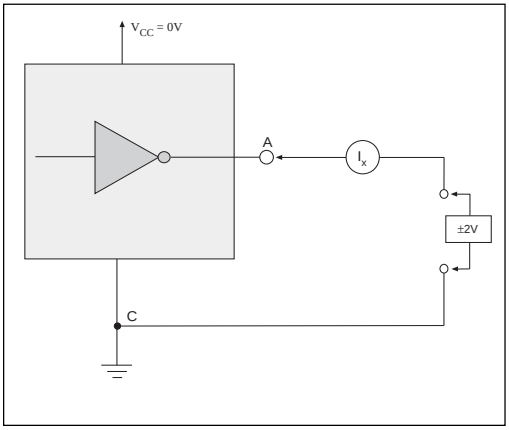


Figure 16. V.28 Driver Output Power-Off Impedance

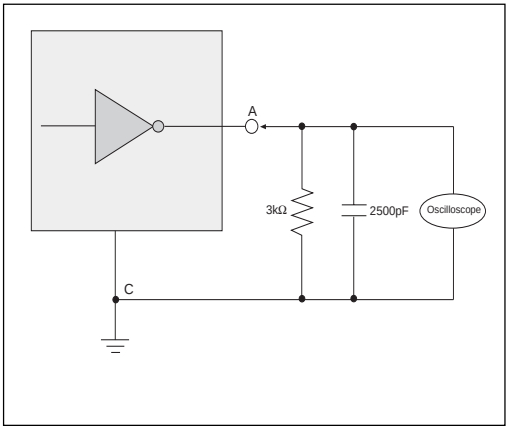


Figure 17. V.28 Driver Output Rise/Fall Times

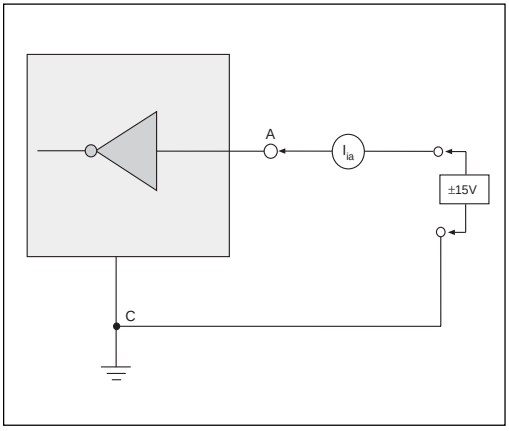


Figure 18. V.28 Receiver Input Impedance

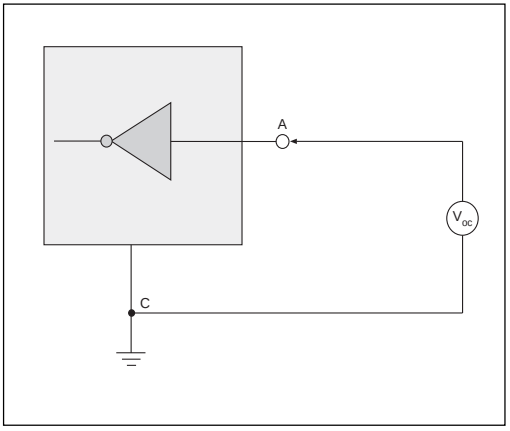


Figure 19. V.28 Receiver Input Open Circuit Bias

THEORY OF OPERATION

The **SP319** is a single chip +5V-only serial transceiver that supports all the signals necessary to implement a full V.35 interface. Three V.35 drivers and three V.35 receivers make up the clock and data signals. Four RS-232 (V.28) drivers and four RS-232 (V.28) receivers are used for control line signals for the interface.

V.35 Drivers

The V.35 drivers are +5V-only, low power voltage output transmitters. The drivers do not require any external resistor networks, and will meet the following requirements:

1. Source impedance in the range of 50Ω to 150Ω.

2. Resistance between short-circuited terminals and ground is 150Ω ±15Ω.

3. When terminated with a 100Ω resistive load the terminal to terminal voltage will be 0.55 Volts ±20% so that the A terminal is positive to the B terminal when binary 0 is transmitted, and the conditions are reversed to transmit binary 1.

4. The arithmetic mean of the voltage of the A terminal with respect to ground, and the B terminal with respect to ground will not exceed 0.6 Volts when terminated as in 3 above.

The V.35 drivers can operate at data rates as high as 5Mbps. The driver outputs are protected against short-circuits between the A and B outputs and short circuits to ground.

Two of the V.35 drivers, DRIN2 and DRIN3 are equipped with enable control lines. When the enable pins are high the driver outputs are disabled, the output impedance of a disabled driver will nominally be 300Ω. When the enable pins are low, the drivers are active.

V.35 Receivers

The V.35 receivers are +5V only, low power differential receivers which meet the following requirements:

1. Input impedance in the range of 100Ω ±10Ω.

2. Resistance to ground of 150Ω ±15Ω, measured from short-circuited terminals.

All of the V.35 receivers can operate at data rates as high as 5Mbps. The sensitivity of the V.35 receiver inputs is ±300mV.

RS-232 (V.28) Drivers

The RS-232 drivers are inverting transmitters, which accept either TTL or CMOS inputs and output the RS-232 signals with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is ±9V with no load, and ±5V minimum with full load. The transmitter outputs are protected against infinite short-circuits to ground without degradation in reliability.

In the power off state, the output impedance of the RS-232 drivers will be greater than 300Ω over a ±2V range. Should the input of a driver be left open, an internal 400kΩ pullup resistor to V_{CC} forces the input high, thus committing the output to a low state. The slew rate of the transmitter output is internally limited to a maximum of 30V/µs in order to meet the EIA standards. The RS-232 drivers are rated for 120kbps data rates.

RS-232 (V.28) Receivers

The RS-232 receivers convert RS-232 input signals to inverted TTL signals. Each of the four receivers features 500mV of hysteresis margin to minimize the effects of noisy transmission lines. The inputs also have a 5kΩ resistor to ground; in an open circuit situation the input of the receiver will be forced low, committing the output to a logic high state. The input resistance will maintain 3kΩ-7kΩ over a ±15V range. The maximum operating voltage range for the receiver is ±30V, under these conditions the input current to the receiver must be limited to less than 100mA. The RS-232 receivers can operate to beyond 120kbps.

CHARGE PUMP

The charge pump is a **Sipex** patented design (U.S. 5,306,954) that uses an innovative approach. The charge pump, with four external capacitors, uses a four-phase voltage shifting technique to attain a symmetrical ±10V power supply. The capacitors can be as low as 0.1µF with a 16 Volt rating. Either polarized or non-polarized capacitors can be used.

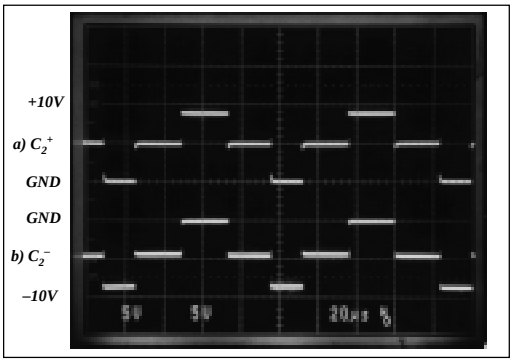


Figure 20. Charge Pump Waveforms

Figure 20 shows the waveforms on the positive and negative sides of capacitor C2 respectively. A free-running oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1: V_{SS} Charge Storage *(Figure 21)*
During this phase of the clock cycle, the positive side of capacitors C1 and C2 are charged to +5V. C1+ is switched to ground and the charge on C1- is transferred to C2-. Since C2+ is connected to +5V, the voltage potential across capacitor C2 becomes 10V.

Phase 2: V_{SS} Transfer *(Figure 22)*
Phase two of the clock connects the negative terminal of C2 to the Vss storage capacitor and the positive terminal of C2 to ground, and transfers the generated -10V to C3. Simultaneously, the positive side of capacitor C1 is switched to +5V and the negative side is connected to ground.

Phase 3: V_{DD} Charge Storage *(Figure 23)*
The third phase of the clock is identical to the first phase - the transferred charge on C1 produces -5V on the negative terminal of C1, which is applied to the negative side of capacitor C2. Since C2+ is at +5V, the voltage potential across C2 is +10V.

Phase 4: V_{DD} Transfer *(Figure 24)*
The fourth phase of the clock connects the negative terminal of C2 to ground and transfers the generated +10V across C2 to C4, the Vdd storage capacitor. The positive side of capacitor C1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V+ and V- are separately generated from Vcc in a no load condition, V+and V- will be symmetrical. Older charge pump approaches that generate V- from V+ will show a decrease in the magnitude of V- compared to V+ due to the inherent inefficiencies in design.

The clock rate for the charge pump typically operates at 15kHz with 0.1µF, 16V external capacitors.

Shutdown Mode

The **SP319** can be put into a low power shutdown mode by bringing both TS000 (pin 3) and ENV35 (pin 9) low. In shutdown mode, **SP319** draws less than 2mA. For normal operation, both pins should be connected to +5V.

Termination Enable

The **SP319** includes a termination enable pin that connects or disconnects the receiver input termination circuitry. A TTL logic LOW at $\overline{ENT}$ (pin 75) will connect the "Y" termination network to the V.35 receiver inputs. A TTL logic HIGH at $\overline{ENT}$ (pin 75) will disconnect the "Y" termination network and the receivers will operate as V.11 compliant receivers. The $\overline{ENT}$ pin has an internal pull-down resistor so that a floating input will enable the termination network. The **SP319** is compatible with the **SP320** since pin 75 on the **SP320** is designated as a no connect.

External Power Supplies

For applications where separate external supplies can be applied at the V+ and V- pins. The value of the external supply voltages should not exceed ±10V. It is critical the external power supplies provide a power supply sequence of : +10V, +5V, and then -10V.

Applications Information

The **SP319** is a single chip device that can implement a complete V.35 interface. Three (3) V.35 drivers and three (3) V.35 receivers are used for clock and data signals and four (4) RS-232 (V.28) drivers and four (4) RS-232 (V.28) receivers can be used for the control signals of the interface. Figures *25* and *28* show the **SP319** configured in DTE and DCE applications along with an ISO-2593 pin out.

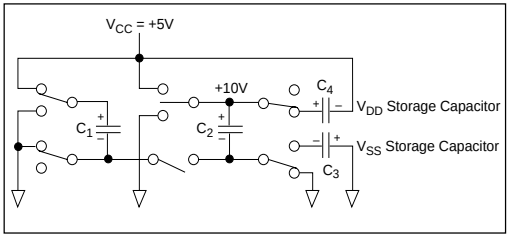


Figure 21. Charge Pump Phase 1

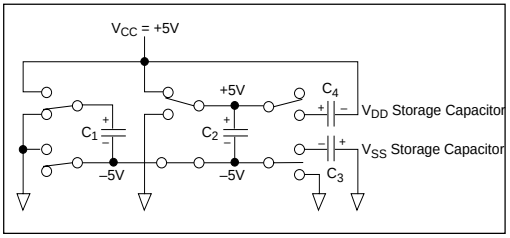


Figure 22. Charge Pump Phase 2

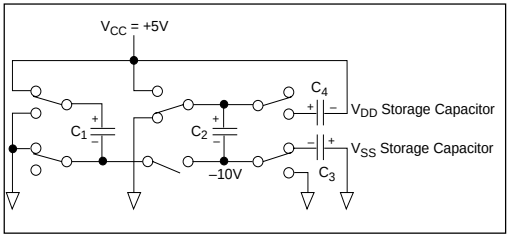


Figure 23. Charge Pump Phase 3

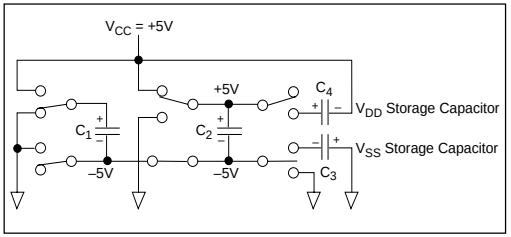


Figure 24. Charge Pump Phase 4

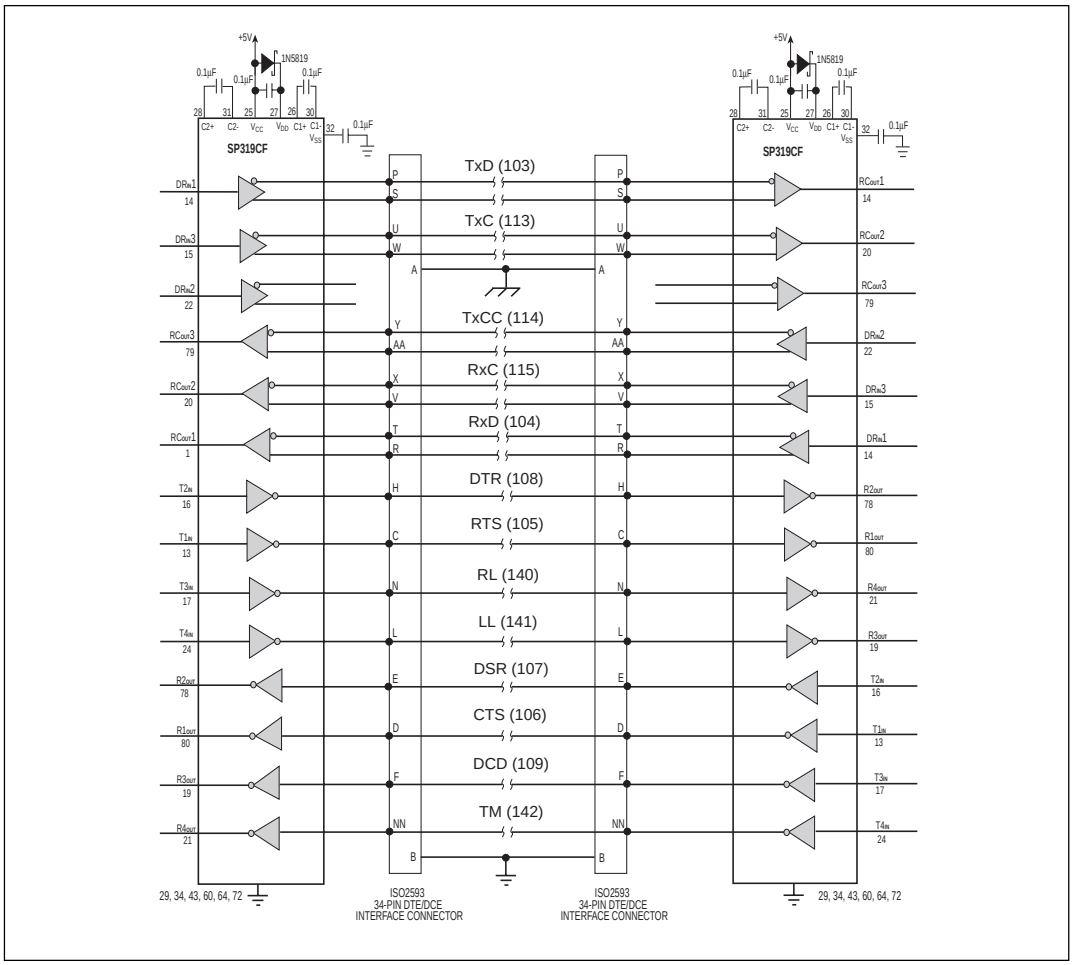


Figure 25. Typical DTE-DCE V.35 Connection using the SP319

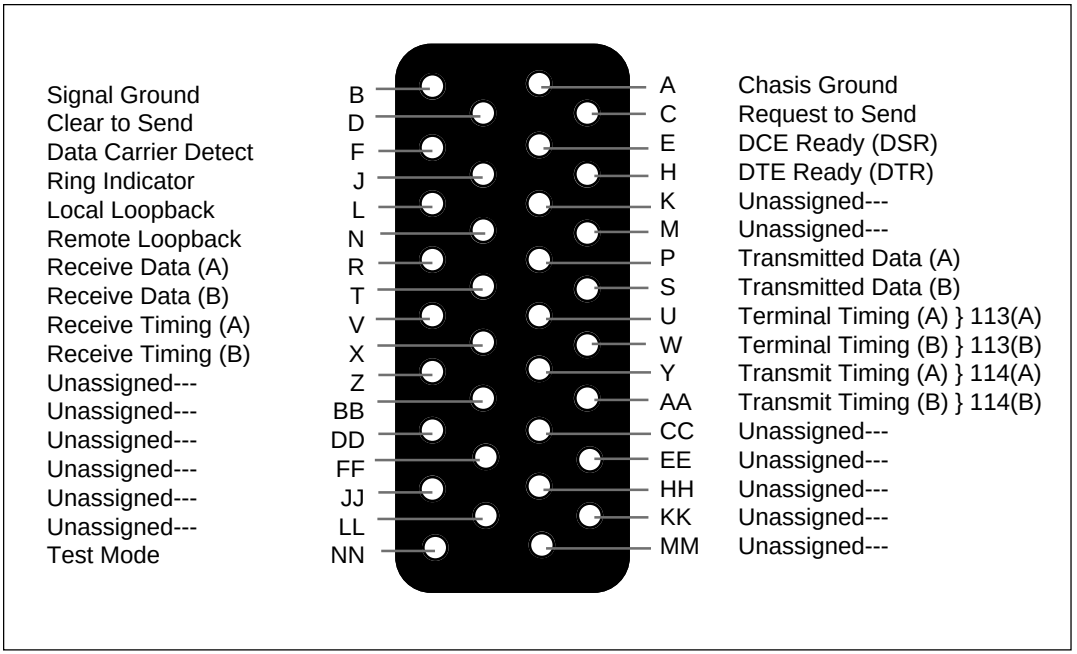


Figure 26. ISO-2593 Connector Pin Out

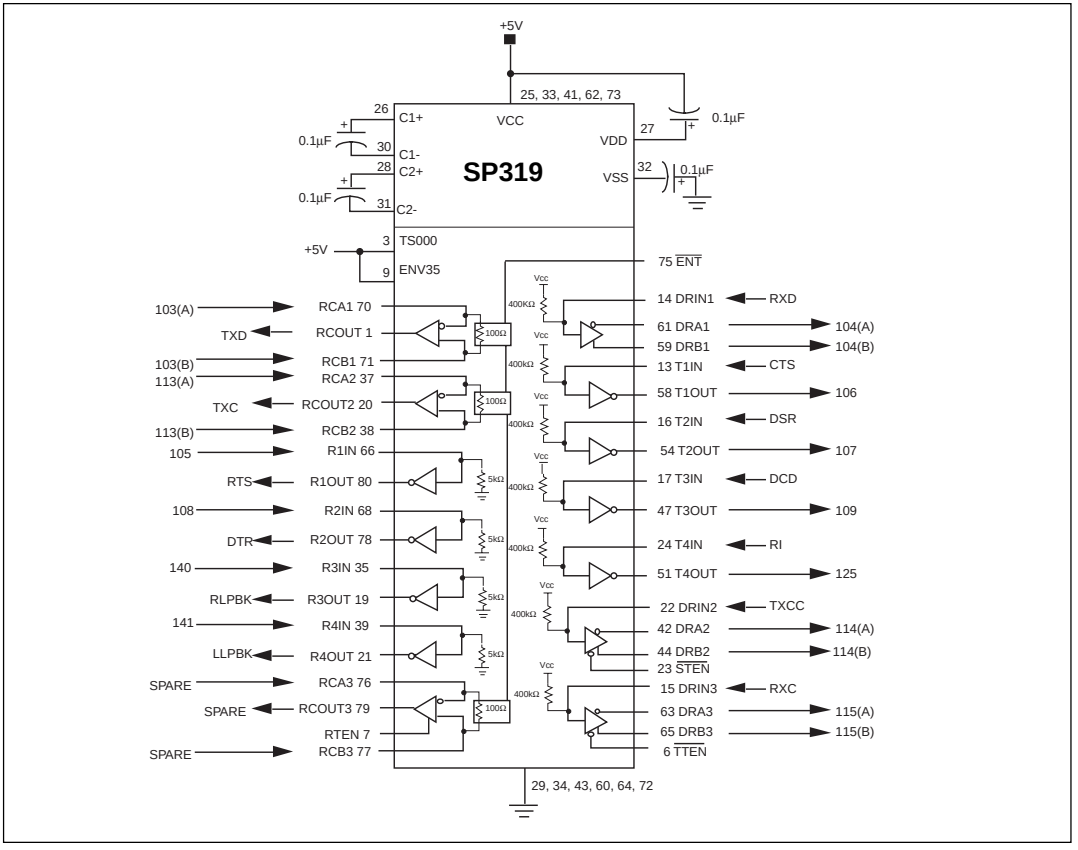


Figure 27. Typical DCE V.35 Interface

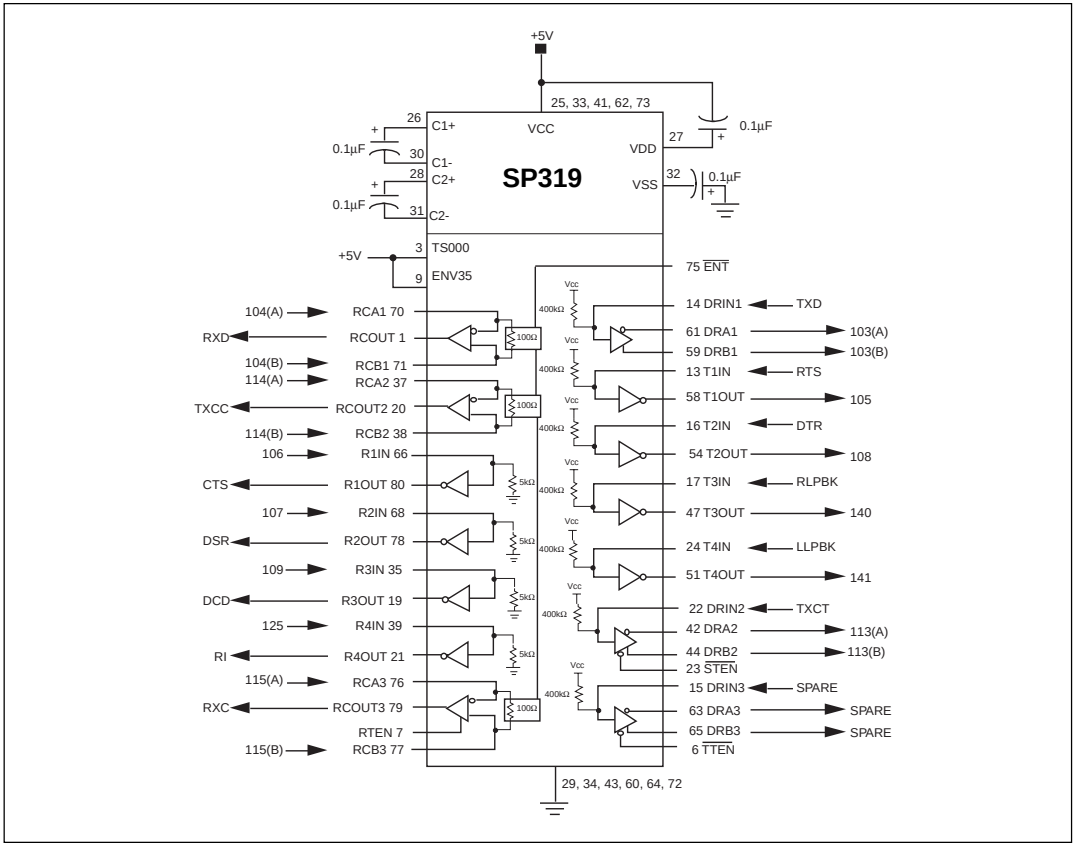
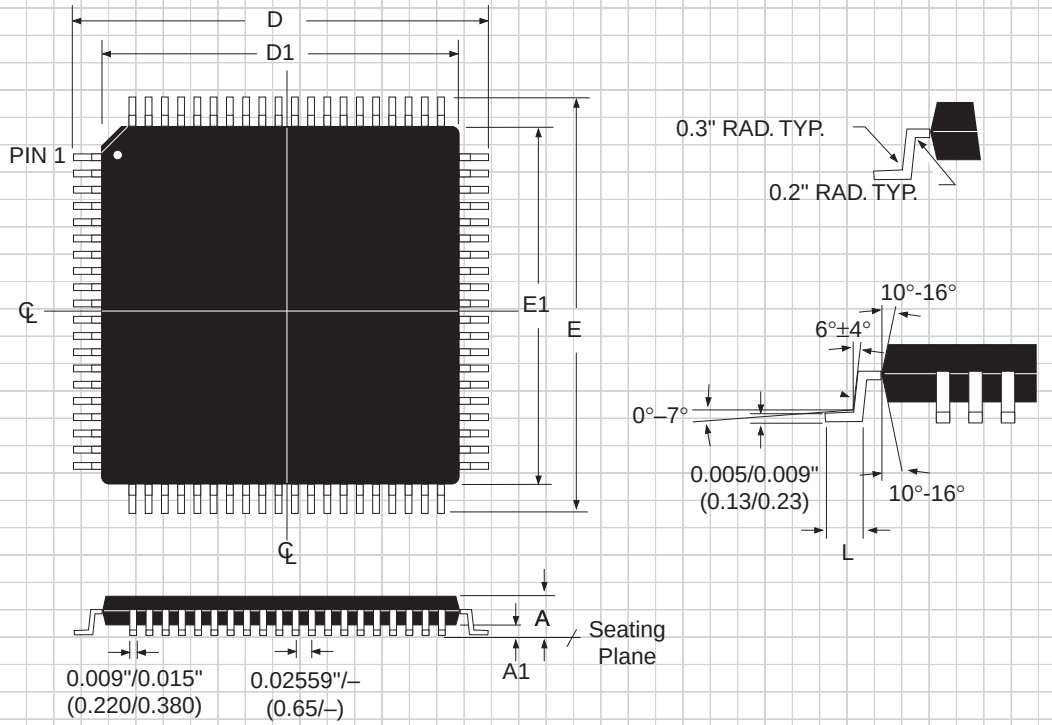


Figure 28. Typical DTE V.35 Interface

PACKAGE: QUAD FLATPACK
JEDEC "BE-2" OUTLINE



DIMENSIONS in Inches Minimum/Maximum (mm)	JEDEC BE-2 Outline 80–PIN
A	–/0.0925 (–/2.350)
A1	–/0.010 (–/0.250)
D	0.667/0.687 (16.950/17.450)
D1	0.547/0.555 (13.900/14.100)
E	0.667/0.687 (16.950/17.450)
E1	0.547/0.555 (13.900/14.100)
L	0.0255/0.0375 (0.650/0.950)

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP319CF	0˚C to +70˚C	80-pin JEDEC (BE-2 Outline) QFP

Please consult the factory for pricing and availability on a Tape-On-Reel option.

SIGNAL PROCESSING EXCELLENCE

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