

## Intelligent +3.0V to +5.5V RS-232 Transceivers

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Interoperable with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
- Minimum 250Kbps data rate under load
- Regulated Charge Pump Yields Stable RS-232 Outputs Regardless of  $V_{CC}$  Variations
- ESD Specifications:  
±2kV Human Body Model



### DESCRIPTION

The SP3249 device is an RS-232 transceiver solution intended for portable or hand-held applications such as notebook and palmtop computers. The SP3249 uses an internal high-efficiency, charge-pump power supply that requires only 0.1 $\mu$ F capacitors in 3.3V operation. This charge pump and Sipex's driver architecture allow the SP3249 device to deliver compliant RS-232 performance from a single power supply ranging from +3.0V to +5.0V. The SP3249 is a 5-driver/3-receiver device, ideal for laptop/notebook computer and PDA applications.

### SELECTION TABLE

Device	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	AUTO ON-LINE® Circuitry	TTL 3-State	No. of Pins
<b>SP3223</b>	+3.0V to +5.5V	2	2	4 capacitors	YES	YES	20
<b>SP3243</b>	+3.0V to +5.5V	3	5	4 capacitors	YES	YES	28
<b>SP3238</b>	+3.0V to +5.5V	5	3	4 capacitors	YES	YES	28
<b>SP3239</b>	+3.0V to +5.5V	5	3	4 capacitors	NO	YES	28
<b>SP3249</b>	+3.0V to +5.5V	5	3	4 capacitors	NO	NO	24

Applicable U.S. Patents - 5,306,954; and other patents pending.

## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

$V_{CC}$ .....	-0.3V to +6.0V
$V+$ (NOTE 1) .....	-0.3V to +7.0V
$V-$ (NOTE 1) .....	+0.3V to -7.0V
$V+ +  V- $ (NOTE 1) .....	+13V
$I_{CC}$ (DC $V_{CC}$ or GND current) .....	$\pm 100$ mA

## Input Voltages

$TxIN$ .....	-0.3V to +6.0V
$RxIN$ .....	$\pm 25$ V

## Output Voltages

$TxOUT$ .....	$\pm 13.2$ V
$RxOUT$ .....	-0.3V to ( $V_{CC} + 0.3$ )V

## Short-Circuit Duration

$TxOUT$ .....	Continuous
Storage Temperature .....	-65°C to +150°C

Note 1:  $V+$  and  $V-$  can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

## SPECIFICATIONS

$V_{CC} = +3.0$  to  $+5.5$ ,  $C1 - C4 = 0.1\mu F$  (tested at  $3.3V \pm 5\%$ ),  $C1 - C4 = 0.22\mu F$  (tested at  $3.3V \pm 10\%$ ),  $C1 = 0.047\mu F$ , and  $C2 - C4 = 0.33\mu F$  (tested at  $5.0V \pm 10\%$ ),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Supply Current		0.3	1.0	mA	$V_{CC}$ , no load
<b>LOGIC INPUTS AND RECEIVER OUTPUTS</b>					
Input Logic Threshold LOW HIGH	2.4		0.8	V	$V_{CC} = +3.3V$ or $+5.0V$ , $TxIN$
Input Leakage Current		$\pm 0.01$	$\pm 1.0$	$\mu A$	$TxIN$ , $T_A = 25^\circ C$
Output Voltage LOW			0.4	V	$I_{OUT} = 1.6mA$
Output Voltage HIGH	$V_{CC} - 0.6$	$V_{CC} - 0.1$		V	$I_{OUT} = -1.0mA$
<b>DRIVER OUTPUTS</b>					
Output Voltage Swing	$\pm 5.0$	$\pm 5.4$		V	All driver outputs loaded with $3K\Omega$ to GND
Output Resistance	300			$\Omega$	$V_{CC} = V+ = V- = 0V$ , $V_{OUT} = \pm 2V$
Output Short-Circuit Current		$\pm 35$	$\pm 60$	mA	$V_{OUT} = GND$
<b>RECEIVER INPUTS</b>					
Input Voltage Range	-25		25	V	
Input Threshold LOW	0.6	1.2		V	$V_{CC} = 3.3V$
Input Threshold LOW	0.8	1.5		V	$V_{CC} = 5.0V$
Input Threshold HIGH		1.5	2.4	V	$V_{CC} = 3.3V$
Input Threshold HIGH		1.8	2.4	V	$V_{CC} = 5.0V$
Input Hysteresis		0.5		V	
Input Resistance	3	5	7	$k\Omega$	

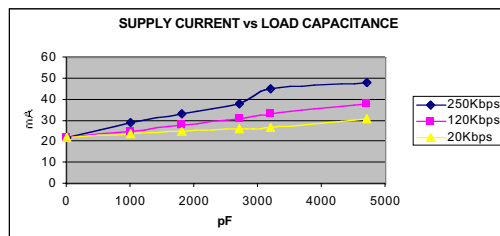
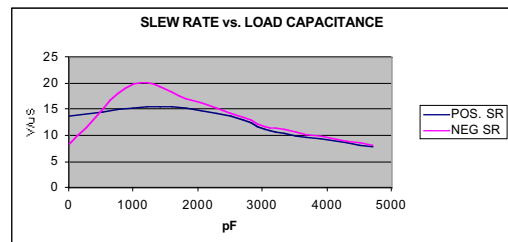
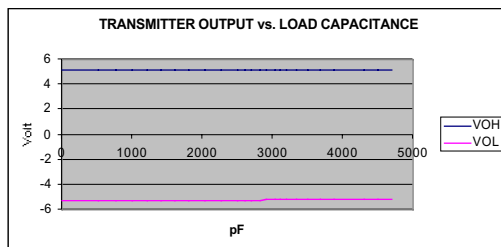
## SPECIFICATIONS

$V_{CC} = +3.0$  to  $+5.5$ ,  $C1 - C4 = 0.1\mu F$  (tested at  $3.3V \pm 5\%$ ),  $C1 - C4 = 0.22\mu F$  (tested at  $3.3V \pm 10\%$ ),  $C1 = 0.047\mu F$ , and  $C2 - C4 = 0.33\mu F$  (tested at  $5.0V \pm 10\%$ ),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>TIMING CHARACTERISTICS</b>					
Maximum Data Rate	250			kbps	$R_L = 3k\Omega$ , $C_L = 1000pF$ , one driver switching
Receiver Propagation Delay $t_{PHL}$ $t_{PLH}$		0.15 0.15		$\mu S$	Receiver input to receiver output, $C_L = 150pF$
Receiver Output Enable Time		200		ns	Normal operation
Receiver Output Disable Time		200		ns	Normal operation
Driver Skew		100		ns	$ t_{PLH} - t_{PHL} $ , $T_A = 25^\circ C$
Receiver Skew		50		ns	$ t_{PLH} - t_{PHL} $
Transition-Region Slew Rate			30	$V/\mu s$	$V_{CC} = 3.3V$ , $R_L = 3k\Omega$ , $T_{AMB} = 25^\circ C$ , measurements taken from $-3.0V$ to $+3.0V$ or $+3.0V$ to $-3.0V$

## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for  $V_{CC} = +3.3V$ , 250kbps data rate, all drivers loaded with  $3k\Omega$ ,  $0.1\mu F$  charge pump capacitors, and  $T_{AMB} = +25^\circ C$ .



**Figure 3. Supply Current VS. Load Capacitance when Transmitting Data**

## PIN DESCRIPTION

NAME	FUNCTION	PIN NO.
C2+	Positive terminal of the symmetrical charge-pump capacitor C2.	1
GND	Ground.	2
C2-	Negative terminal of the symmetrical charge-pump capacitor C2.	3
V-	Regulated -5.5V output generated by the charge pump.	4
T <sub>1</sub> OUT	RS-232 driver output.	5
T <sub>2</sub> OUT	RS-232 driver output.	6
T <sub>3</sub> OUT	RS-232 driver output.	7
R <sub>1</sub> IN	RS-232 receiver input.	8
R <sub>2</sub> IN	RS-232 receiver input.	9
T <sub>4</sub> OUT	RS-232 driver output.	10
R <sub>3</sub> IN	RS-232 receiver input.	11
T <sub>5</sub> OUT	RS-232 driver output.	12
<del>T<sub>5</sub>IN</del>	TTL/CMOS driver input.	13
<u>R<sub>3</sub>OUT</u>	TTL/CMOS receiver output.	14
T <sub>4</sub> IN	TTL/CMOS driver input.	15
<u>R<sub>2</sub>OUT</u>	TTL/CMOS receiver output.	16
R <sub>1</sub> OUT	TTL/CMOS receiver output.	17
T <sub>3</sub> IN	TTL/CMOS driver input.	18
T <sub>2</sub> IN	TTL/CMOS driver input.	19
T <sub>1</sub> IN	TTL/CMOS driver input.	20
C1-	Negative terminal of the symmetrical charge-pump capacitor C1.	21
V <sub>CC</sub>	+3.0V to +5.5V supply voltage.	22
V+	Regulated +5.5V output generated by the charge pump.	23
C1+	Positive terminal of the voltage doubler charge-pump capacitor C1	24

**Table 1. Device Pin Description**

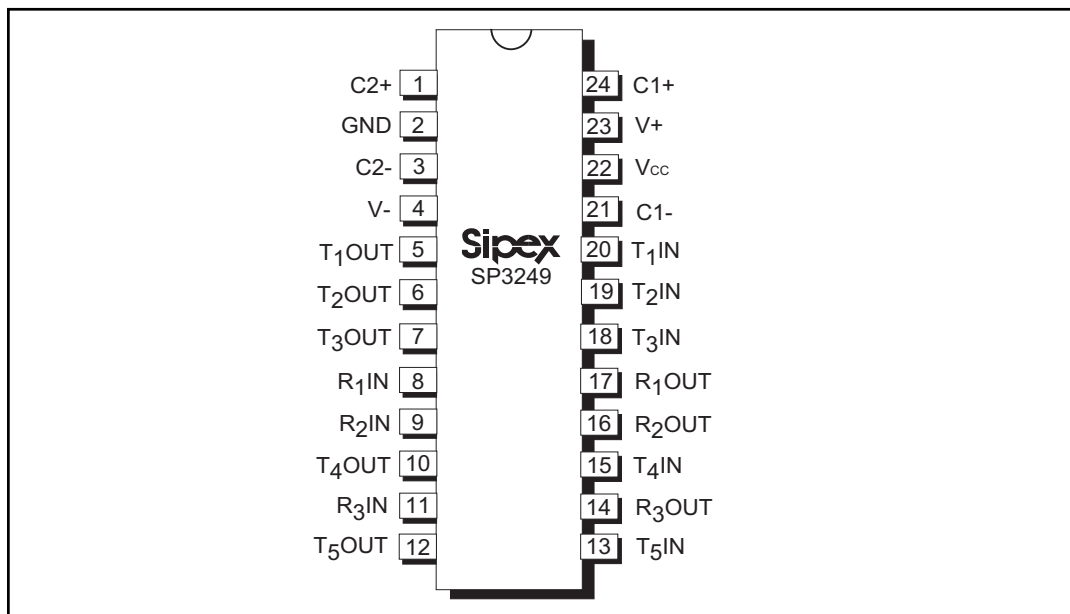


Figure 4. SP3249 Pinout Configuration

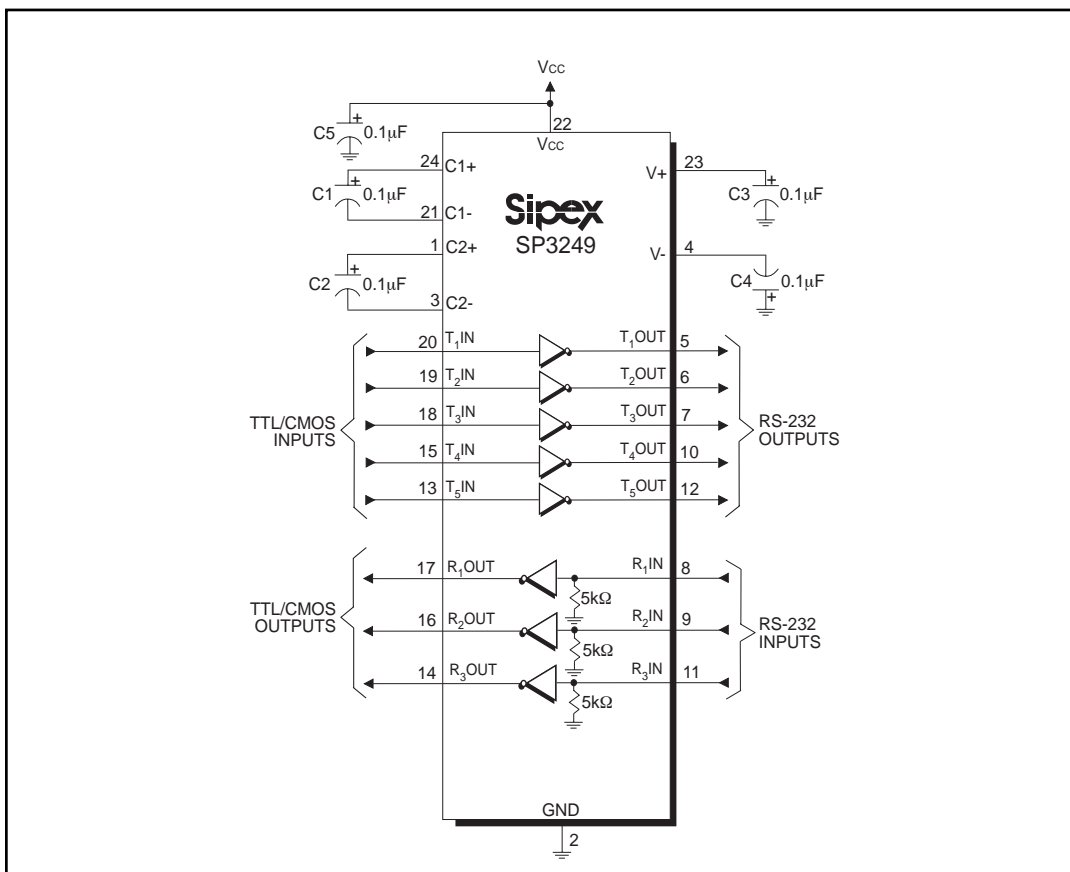


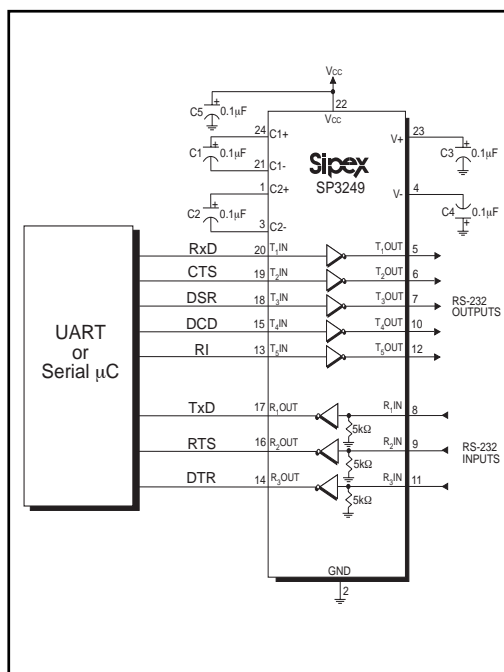
Figure 5. SP3249 Typical Operating Circuit

## DESCRIPTION

The SP3249 device meets the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The SP3249 device features Sipex's proprietary and patented (U.S. #5,306,954) on-board charge pump circuitry that generates  $\pm 5.5\text{V}$  RS-232 voltage levels from a single  $+3.0\text{V}$  to  $+5.5\text{V}$  power supply. The SP3249 device can operate at a data rate of 250kbps fully loaded.

The SP3249 is a 5-driver/3-receiver device, ideal for portable or hand-held applications.

The SP3249 device is an ideal choice for power sensitive designs.



**Figure 6. Interface Circuitry Controlled by Microprocessor Supervisory Circuit**

## THEORY OF OPERATION

The SP3249 device is made up of four basic circuit blocks: 1. Drivers, 2. Receivers, 3. the Sipex proprietary charge pump, and

### Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is  $\pm 5.4\text{V}$  with no load and  $\pm 5\text{V}$  minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232F and all previous RS-232 versions. All unused driver inputs must be connected to  $V_{CC}$  or GND.

The drivers can guarantee a data rate of 250kbps fully loaded with  $3\text{k}\Omega$  in parallel with  $1000\text{pF}$ , ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver output is internally limited to a maximum of  $30\text{V}/\mu\text{s}$  in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

Figure 7 shows a loopback test circuit used to test the RS-232 Drivers. Figure 8 shows the test results of the loopback circuit with all five drivers active at 120kbps with typical RS-232 loads in parallel with  $1000\text{pF}$  capacitors. Figure 6 shows the test results where one driver was active at 250kbps and all five drivers loaded with an RS-232 receiver in parallel with a  $1000\text{pF}$  capacitor. A solid RS-232 data transmission rate of 120kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

## Receivers

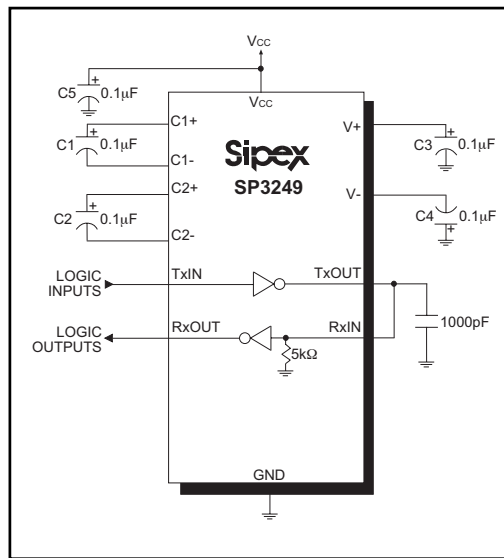
The receivers convert  $\pm 5.0\text{V}$  EIA/TIA-232 levels to TTL or CMOS logic output levels.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal  $5\text{k}\Omega$  pulldown resistor to ground will commit the output of the receiver to a HIGH state.

## Charge Pump

The charge pump is a Sipex-patented design (U.S. #5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage ( $V_{CC}$ ) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the

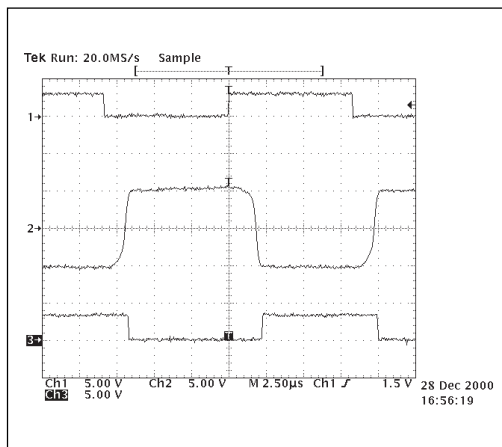


**Figure 7. Loopback Test Circuit for RS-232 Driver Data Transmission Rates**

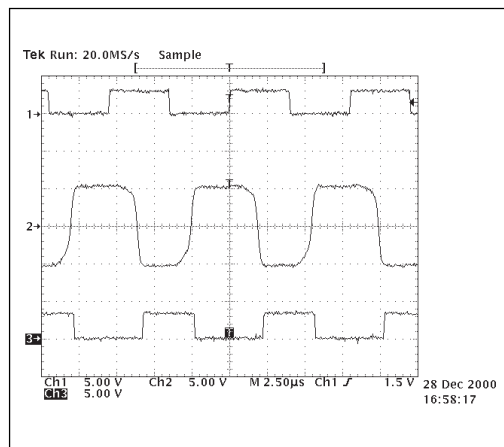
charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting (Figure 13). A description of each phase follows.

### Phase 1 (Figure 11)

—  $V_{SS}$  charge storage — During this phase of the clock cycle, the positive side of capacitors  $C_1$  and  $C_2$  are initially charged to  $V_{CC}$ .  $C_1+$  is then switched to GND and the charge in  $C_1-$  is transferred to  $C_2-$ . Since  $C_2+$  is connected to  $V_{CC}$ , the voltage potential across capacitor  $C_2$  is now 2 times  $V_{CC}$ .



**Figure 8. Loopback Test Circuit Result at 120kbps (All Drivers Fully Loaded)**



**Figure 9. Loopback Test Circuit result at 250kbps (All Drivers Fully Loaded)**

### Phase 2 (Figure 12)

—  $V_{SS}$  transfer — Phase two of the clock connects the negative terminal of  $C_2$  to the  $V_{SS}$  storage capacitor and the positive terminal of  $C_2$  to GND. This transfers a negative generated voltage to  $C_3$ . This generated voltage is regulated to a minimum voltage of  $-5.5V$ . Simultaneous with the transfer of the voltage to  $C_3$ , the positive side of capacitor  $C_1$  is switched to  $V_{CC}$  and the negative side is connected to GND.

### Phase 3 (Figure 14)

—  $V_{DD}$  charge storage — The third phase of the clock is identical to the first phase — the charge transferred in  $C_1$  produces  $-V_{CC}$  in the negative terminal of  $C_1$ , which is applied to the negative side of capacitor  $C_2$ . Since  $C_2^+$  is at  $V_{CC}$ , the voltage potential across  $C_2$  is 2 times  $V_{CC}$ .

### Phase 4 (Figure 15)

—  $V_{DD}$  transfer — The fourth phase of the clock connects the negative terminal of  $C_2$  to GND, and transfers this positive generated voltage across  $C_2$  to  $C_4$ , the  $V_{DD}$  storage capacitor. This voltage is regulated to  $+5.5V$ . At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to  $C_4$ , the positive side of capacitor  $C_1$  is switched to  $V_{CC}$  and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both  $V^+$  and  $V^-$  are separately generated from  $V_{CC}$ , in a no-load condition  $V^+$  and  $V^-$  will be symmetrical. Older charge pump approaches that generate  $V^-$  from  $V^+$  will show a decrease in the magnitude of  $V^-$  compared to  $V^+$  due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 500kHz. The external capacitors can be as low as  $0.1\mu F$  with a 16V breakdown voltage rating.



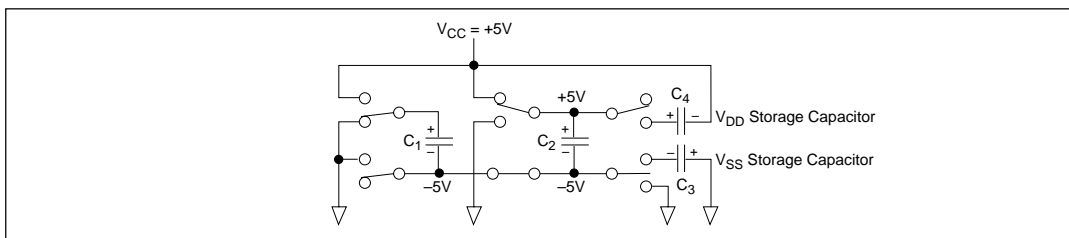


Figure 10. Charge Pump — Phase 1

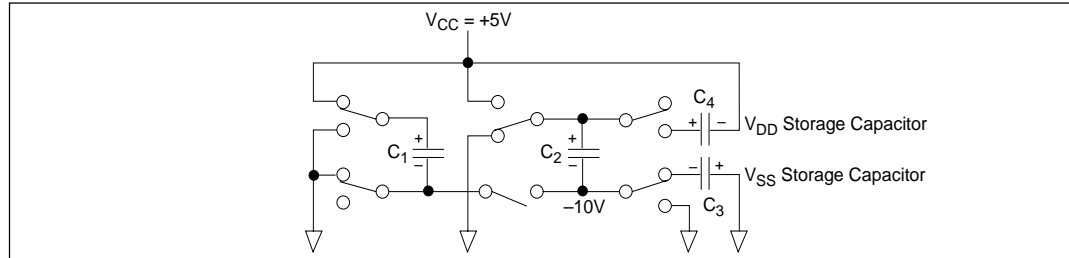


Figure 11. Charge Pump — Phase 2

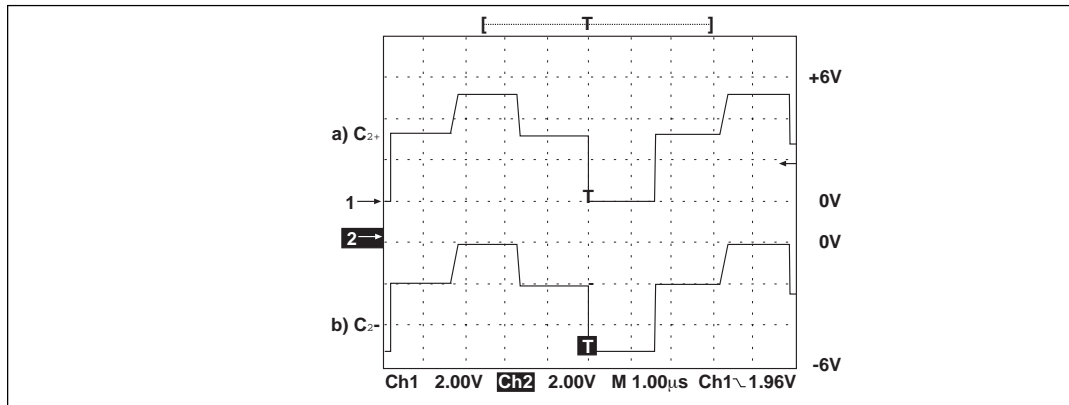


Figure 12. Charge Pump Waveforms

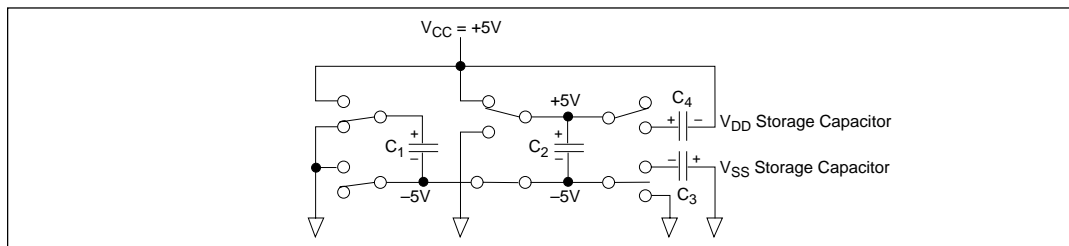


Figure 13. Charge Pump — Phase 3

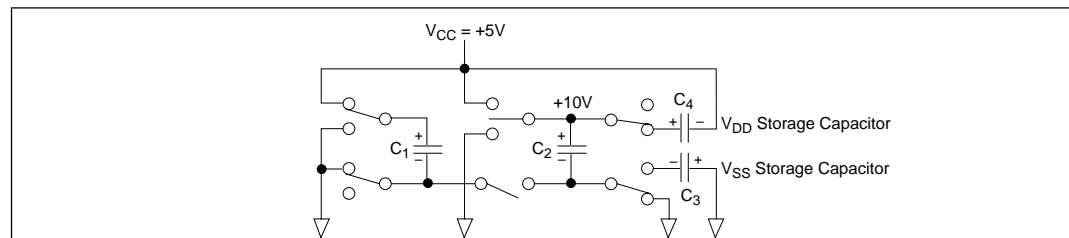


Figure 14. Charge Pump — Phase 4

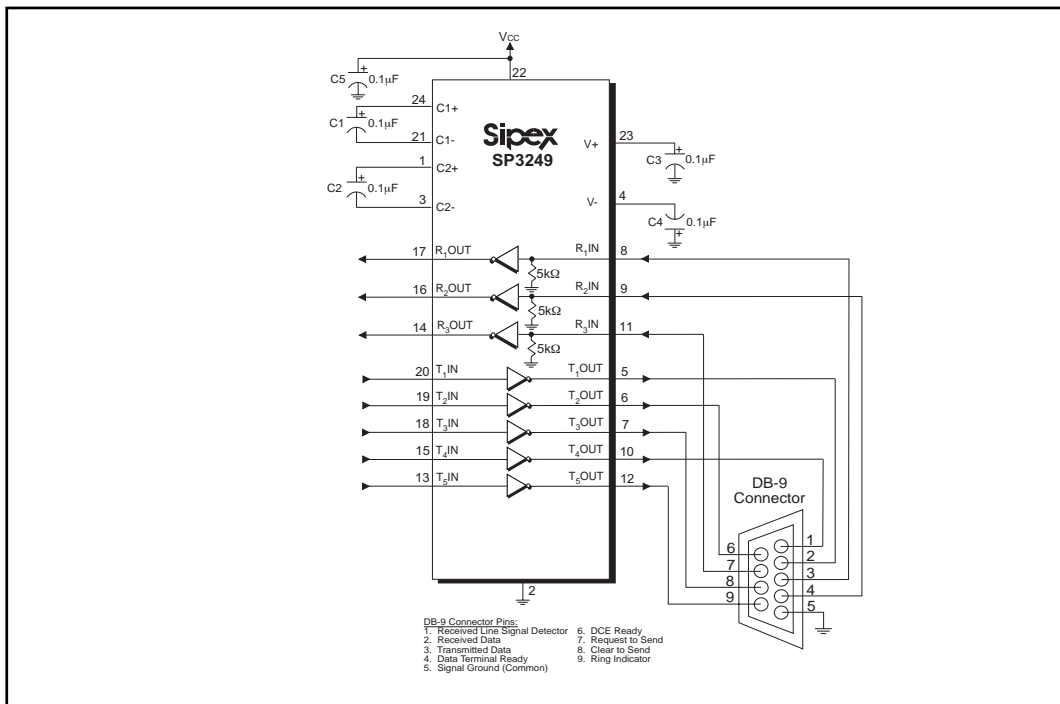


Figure 15. Circuit for the connectivity of the SP3249 with a DB-9 connector

## ESD TOLERANCE

The SP3249 device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients.

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's

potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 16. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

For the Human Body Model, the current limiting resistor ( $R_s$ ) and the source capacitor ( $C_s$ ) are  $1.5k\Omega$  and  $100pF$ , respectively.

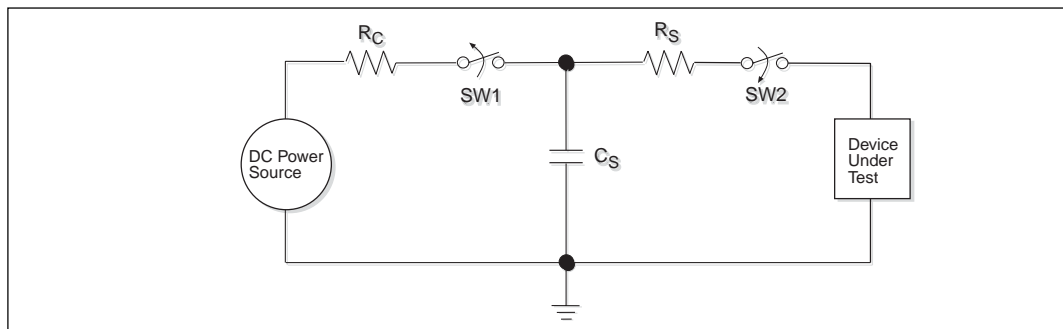
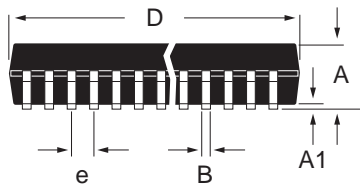
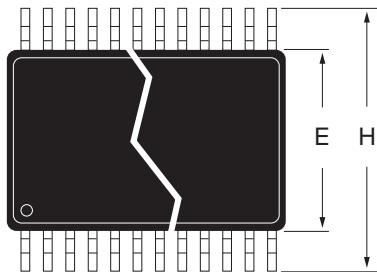


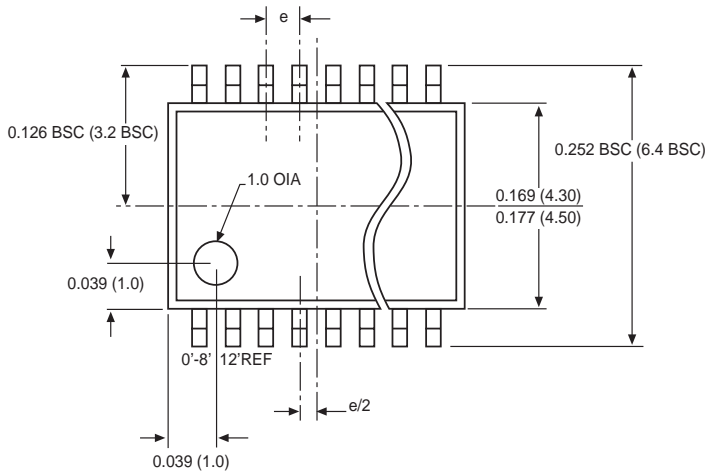
Figure 16. ESD Test Circuit for Human Body Model

# **PACKAGE: PLASTIC SHRINK SMALL OUTLINE (SSOP)**

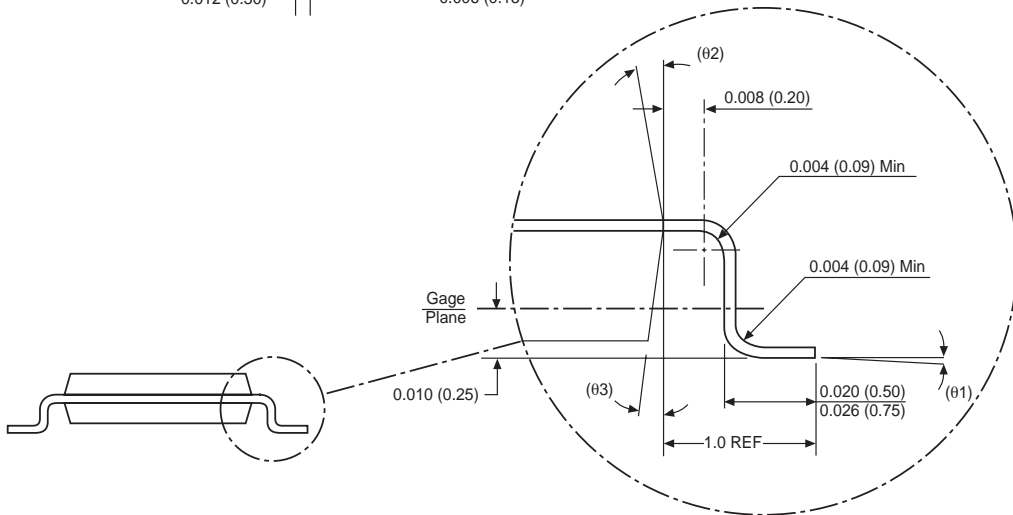
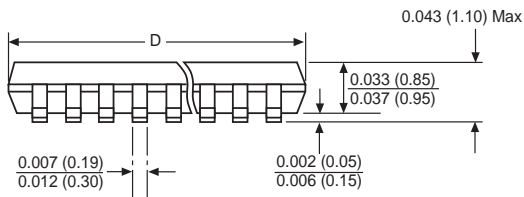


<b>DIMENSIONS (Inches) Minimum/Maximum (mm)</b>	<b>28-PIN</b>
<b>A</b>	<b>0.068/0.078 (1.73/1.99)</b>
<b>A1</b>	<b>0.002/0.008 (0.05/0.21)</b>
<b>B</b>	<b>0.010/0.015 (0.25/0.38)</b>
<b>D</b>	<b>0.397/0.407 (10.07/10.33)</b>
<b>E</b>	<b>0.205/0.212 (5.20/5.38)</b>
<b>e</b>	<b>0.0256 BSC (0.65 BSC)</b>
<b>H</b>	<b>0.301/0.311 (7.65/7.90)</b>
<b>L</b>	<b>0.022/0.037 (0.55/0.95)</b>
<b>Ø</b>	<b>0°/8° (0°/8°)</b>

# PACKAGE: PLASTIC THIN SMALL OUTLINE (TSSOP)



DIMENSIONS in inches (mm) Minimum/Maximum	
Symbol	28 Lead
D	0.378/0.386 (9.60/9.80)
e	0.026 BSC (0.65 BSC)



## ORDERING INFORMATION

Model	Temperature Range	Package Types
SP3249CA . . . . .	0°C to +70°C . . . . .	.28-pin SSOP
SP3249CY . . . . .	0°C to +70°C . . . . .	.28-pin TSSOP
SP3249EA . . . . .	-40°C to +85°C . . . . .	.28-pin SSOP
SP3249EY . . . . .	-40°C to +85°C . . . . .	.28-pin TSSOP

Please consult the factory for pricing and availability on a Tape-On-Reel option.



ANALOG EXCELLENCE

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