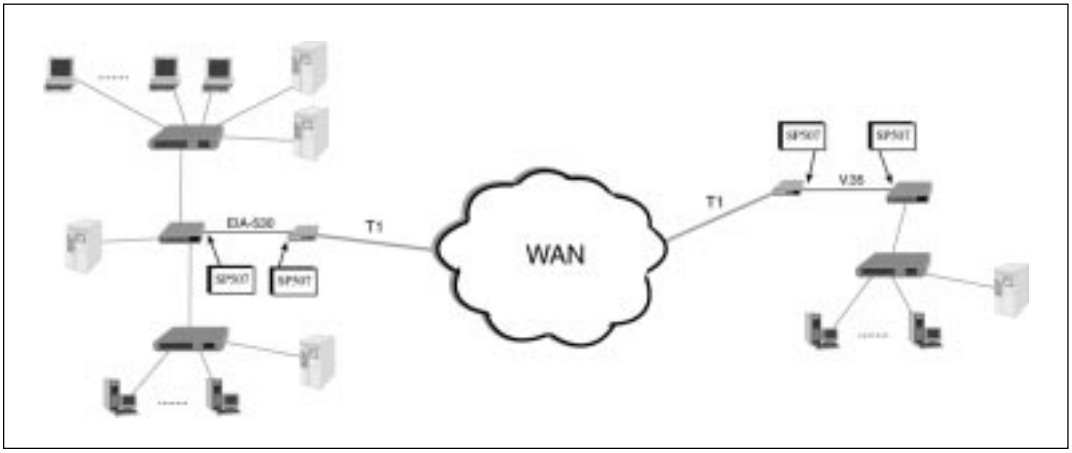
Designing with the SP505, SP506, & SP507 Multi-Protocol Serial Transceivers

The **SP50x** family of multi-protocol transceivers are designed for applications using serial ports in networking equipment such as routers, DSU/CSUs, multiplexors, access devices, and other networking equipment. This application note discusses and illustrates various configuration options, and other helpful hints about designing with the **SP505** and the newer **SP506** and **SP507** products.

These one-chip serial port transceiver products supports seven popular serial interface standards for Wide Area Network (WAN) connectivity. With a built-in DC-DC charge pump converter, the **SP505**, **SP506** and **SP507** operate on +5V only. The seven drivers and seven receivers can be configured via software for RS-232, X.21, EIA-530, EIA-530A, RS-449, V.35, and V.36 interface modes at any time.

Unlike other discrete solutions or other multi-chip transceivers, the **SP505**, **SP506** and **SP507** require no additional external circuitry for compliant operation other than the charge pump capacitors. All necessary resistor termination networks are integrated within the **SP505**, **SP506** and **SP507**, and are switchable when in EIA-530, EIA-530A, RS-449, V.35, V.36, and X.21 modes.

The **SP505**, **SP506** and **SP507** provide individual driver disable for easy DTE/DCE configurations. The **SP507** offers four receiver enable lines for even easier DTE/DCE programmability. The newer **SP506** is pin compatible with the **SP505** except with improved AC performance. Refer to the **SP505**, **SP506** and **SP507** datasheets for electrical parameter and configuration details.



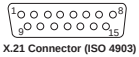
DTE Configuration to a DB-25 Serial Port

The **SP505**, **SP506** and **SP507** can easily be configured as a DTE in all serial communication applications. The **SP505**, **SP506** and **SP507** contain seven drivers and seven receivers to support most of the signals required for proper serial communications. *Figure 1* summarizes the usual signals used in synchronous serial communications. The basic configuration shown in *Figure 2* illustrates a connection to a DB-25 D-sub connector commonly used for EIA-530 and RS-232.

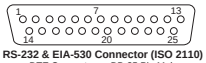
For other serial interface protocols, the decoder can be used to select the physical layer interface. The DEC_{0-3} of the **SP505** and **SP506** will program its internal drivers and receivers to electrically adhere to the appropriate interface. The **SP507** decoder is slightly different and uses 3-bits to select the desired interface. For the appropriate physical connection, a "daughter" cable can be attached to the DB-25 connector (female pins on cable) and transfer the signals to the physically compliant connector. For example, a V.35 interface will have a ISO-2593 34-pin connector. For a V.35 DTE interface, the **SP505**, **SP506** and **SP507** can be programed to V.35 mode and a daughter cable, having a DB-25 female connector on one end and a V.35 34-pin male connector on the other end, will allow the equipment to have an electrically and physically complaint V.35 interface.

		EIA-232		EIA-530		EIA-449		V.35		X.21	
Signal Name	Source	Mnemonic	Pin	Mnemonic	Pin	Mnemonic	Pin	Mnemonic	Pin	Mnemonic	Pin
Shield	—	—	1	—	1	—	1	—	A	—	1
Transmitted Data	DTE	BA	2	BA (A)	2	SD (A)	4	103	P	Circuit T(A)	2
				BA (B)	14	SD (B)	22	103	S	Circuit T(B)	9
Received Data	DCE	BB	3	BB (A)	3	RD (A)	6	104	R	Circuit R(A)	4
				BB (B)	16	RD (B)	24	104	T	Circuit R(B)	11
Request To Send	DTE	CA	4	CA (A)	4	RS (A)	7	105	C	Circuit C(A)	3
				CA (B)	19	RS (B)	25			Circuit C(B)	10
Clear To Send	DCE	CB	5	CB (A)	5	CS (A)	9	106	D	Circuit I(A)	5
				CB (B)	13	CS (B)	27			Circuit I(B)	12
DCE Ready (DSR)	DCE	CC	6	CC (A)	6	DM (A)	11	107	E		
				CC (B)	22	DM (B)	29				
DTE Ready (DTR)	DTE	CD	20	CD (A)	20	TR (A)	12	108	H *		
				CD (B)	23	TR (B)	30				
Signal Ground	—	AB	7	AB	7	SG	19	102	B	Circuit G	8
Recv. Line Sig. Det. (DCD)	DCE	CF	8	CF (A)	8	RR (A)	13	109	F		
				CF (B)	10	RR (B)	31				
Trans. Sig. Elemt. Timing	DCE	DB	15	DB (A)	15	ST (A)	5	114	Y	Circuit B(A)**	7
				DB (B)	12	ST (B)	23	114	AA	Circuit B(B)**	14
Recv. Sig. Elemt. Timing	DCE	DD	17	DD (A)	17	RT (A)	8	115	V	Circuit S(A)	6
				DD (B)	9	RT (B)	26	115	X	Circuit S(B)	13
Local Loopback	DTE	LL	18	LL	18	LL	10	141	L *		
Remote Loopback	DTE	RL	21	RL	21	RL	14	140	N *		
Ring Indicator	DCE	CE	22	—	—	—	—	125	J *		
Trans. Sig. Elemt. Timing	DTE	DA	24	DA (A)	24	TT (A)	17	113	U *	Circuit X(A)**	7
				DA (B)	11	TT (B)	35	113	W *	Circuit X(B)**	14
Test Mode	DCE	TM	25	TM	25	TM	18	142	NN *		

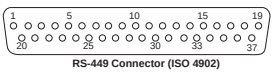
* - Optional signals
** - Only one of the two X.21 signals, Circuit B or X, can be implemented and active at one time.



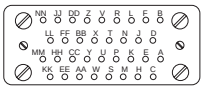
X.21 Connector (ISO 4903)
DTE Connector — DB-15 Pin Male
DCE Connector — DB-15 Pin Female



RS-232 & EIA-530 Connector (ISO 2110)
DTE Connector — DB-25 Pin Male
DCE Connector — DB-25 Pin Female

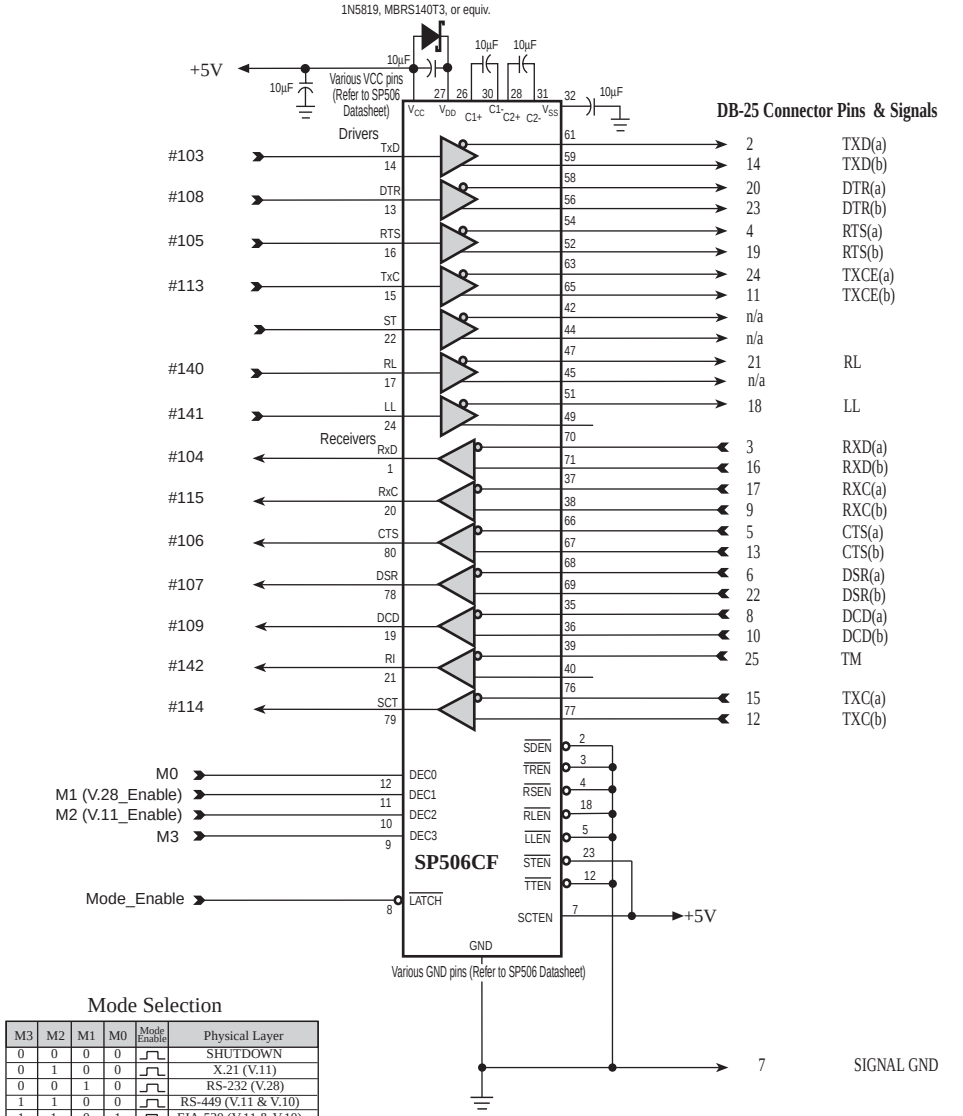


RS-449 Connector (ISO 4902)
DTE Connector Face — DB-37 Pin Male
DCE Connector Face – DB-37 Pin Female



V.35/ISO 2593 Connector
DTE Connector Face — 34 Pin Male
DCE Connector Face — 34 Pin Female

Figure 1. Signals and Connector Allocation Table



Mode Selection

M3	M2	M1	M0	Mode Enable	Physical Layer
0	0	0	0	⎍	SHUTDOWN
0	1	0	0	⎍	X.21 (V.11)
0	0	1	0	⎍	RS-232 (V.28)
1	1	0	0	⎍	RS-449 (V.11 & V.10)
1	1	0	1	⎍	EIA-530 (V.11 & V.10)
1	1	1	0	⎍	V.35 (V.35 & V.28)
1	1	1	1	⎍	EIA-530A (V.11 & V.10)

Figure 2. SP506 DTE Configuration

DCE Configuration to a DB-25 Serial Port

The **SP505**, **SP506** and **SP507** can also be easily configured as a DCE in all serial communication applications. *Figure 1* summarizes the usual signals used in synchronous serial communications. However when sourcing the signal by the DCE, the transceiver must be configured as a driver. The basic configuration shown in *Figure 3* illustrates the connection to a DB-25 D-sub connector.

Programmable DTE/DCE Configuration to a DB-25 Serial Port

The **SP505**, **SP506** and **SP507** can also be conveniently configured so that the interface is programmable for either DTE or DCE. Extra attention must be paid to the direction of the signals since there may be bidirectional signals present. *Figure 4* and *5* illustrate a connection to a DB-25 D-sub connector using the **SP506** and **SP507**, respectively.

When bidirectional signals are needed, this usually means a driver and receiver are half-duplexed together. In other words, the driver outputs are connected to the receiver inputs. This requires the driver outputs to be disabled and at a high impedance state. The receiver does not require a disable function as long as the inputs are high enough impedance so that the driver signals are not attenuated. A half-duplexed receiver without a disable function will still produce a signal at its output when the driver is active and communicating with the receiver at the other end of the cable. This signal can be ignored unless the receiver output is tied to the driver input. If this is the case, then the receiver output should a buffered with a latch or 2:1 mux in order to direct the driver input or receiver output into the HDLC device. The **SP507** has additional receivers with enable lines for easier DTE/DCE implementation.

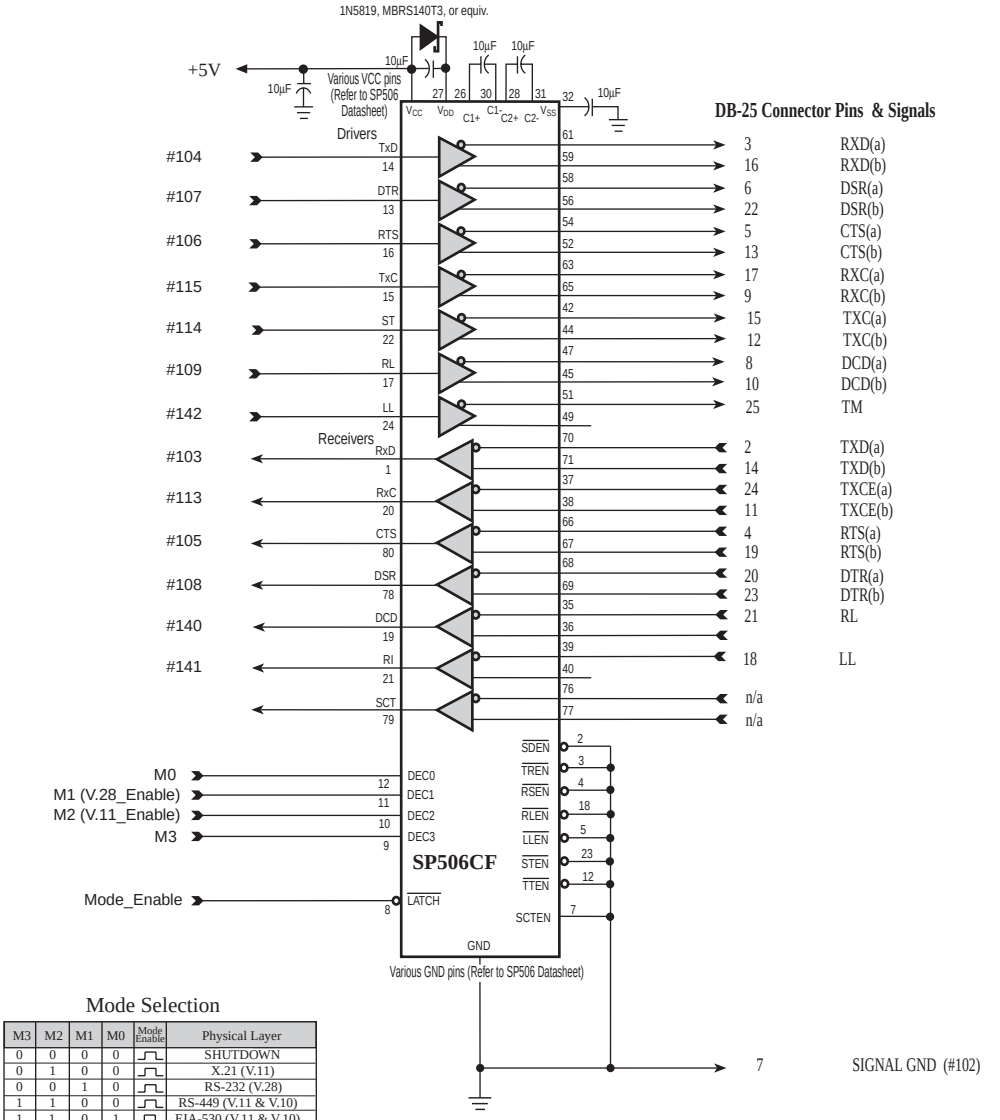
The **SP505**, **SP506** and **SP507** can be configured on the equipment as either DTE or DCE to the DB-25 connector. For the illustration on *Figure 4*, DTE is used with the **SP506**. Since only a DB-25 connector is used as the equipment's serial port, daughter cables are still needed for the other connector types. In addition, to support DCE on this serial port, crossover cables are used. Thus, the equipment will need to provide a DTE V.35 cable and a DCE V.35 cable, for example.

Crossover cables merely reroute the signals to the appropriate connector pin assignment. For DTE in V.35 mode, pins P and S are used for Transmit Data (ITU#103), and pins R and T are used for Receive Data (ITU#104). Pins P and S are connected to the driver outputs since they are sourced from the DTE. Pins R and T are connected to the receiver inputs since they are sourced for the DCE. To convert the serial port to a DCE configuration, the crossover cable swaps the signals to those pins. Specifically, the DB-25 will have pins 2 and 14 connected to the driver and pins 3 and 16 connected to the receiver. This is a normal DTE allocation. However, by the time these signals reach the other end of the cable to the ISO2593 V.35 connector, the pins 2 and 14 now go to R and T, respectively. Pins 3 and 16 on the DB-25 side now go to pins P and S, respectively. Therefore, pins R and T are now generating the data and thus, connected to the driver output. Similarly for pins P and S, now connected to the receiver inputs.

The configuration on *Figure 5* uses the **SP507** in a popular DTE/DCE configuration. The TxC signal is half-duplex and bidirectional. The DCE_ST driver is active during DCE mode while the DTE_ST receiver is active during DTE mode. The STEN and SCTEN enable lines are connected together for common DCE/DTE control. Similarly with the RL/DCD pair and the LL/TM pair. The DCD signal is used for this driver labelled RL in this case. The Remote Loopback function is not available in this configuration. The same goes for the Test Mode function where the TM receiver is used for Local Loopback when in DCE mode.

On-Board Programmable DTE/DCE Configuration (Without Crossover Cables)

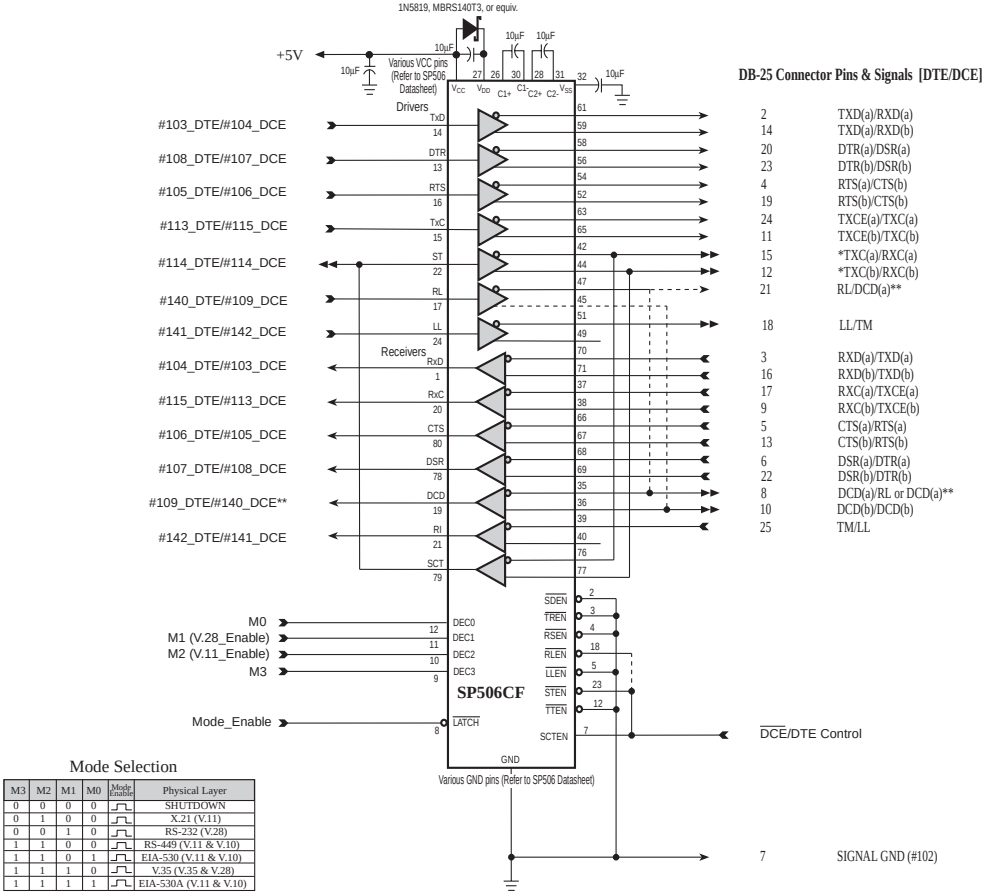
DTE/DCE programmability can also be achieved without using crossover cables. Instead, the selection can be designed in the circuitry. This requires a bidirectional serial port for all signals, not just TxC and DCD. An "on-board" solution would need to have circuitry allocated for DTE and circuitry allocated for DCE. The transceiver portion would need to address disable functions, low leakage currents, and specific timing issues when joined together in a half-duplex configuration.



Mode Selection

M3	M2	M1	M0	Mode Enable	Physical Layer
0	0	0	0		SHUTDOWN
0	1	0	0		X.21 (V.11)
0	0	1	0		RS-232 (V.28)
1	1	0	0		RS-449 (V.11 & V.10)
1	1	0	1		EIA-530 (V.11 & V.10)
1	1	1	0		V.35 (V.35 & V.28)
1	1	1	1		EIA-530A (V.11 & V.10)

Figure 3. SP506 DCE Configuration



Mode Selection

M3	M2	M1	M0	Mode Enable	Physical Layer
0	0	0	0		SHUTDOWN
0	1	0	0		X.21 (V.11)
0	0	1	0		RS-232 (V.28)
1	1	0	0		RS-449 (V.11 & V.10)
1	1	0	1		EIA-530 (V.11 & V.10)
1	1	1	0		V.35 (V.35 & V.28)
1	1	1	1		EIA-530A (V.11 & V.10)

* - Driver applies for DCE only on pins 24 and 11. Receiver applies for DTE only on pins 24 and 11.

** - RL may not be required in some applications and DCD may be required to be bi-directional. If RL is not required The RL is replaced by DCD(a) and the #140_DCE is replaced by #109_DCE. The RL driver of the SP505 will not be in use during DCE mode in this case.

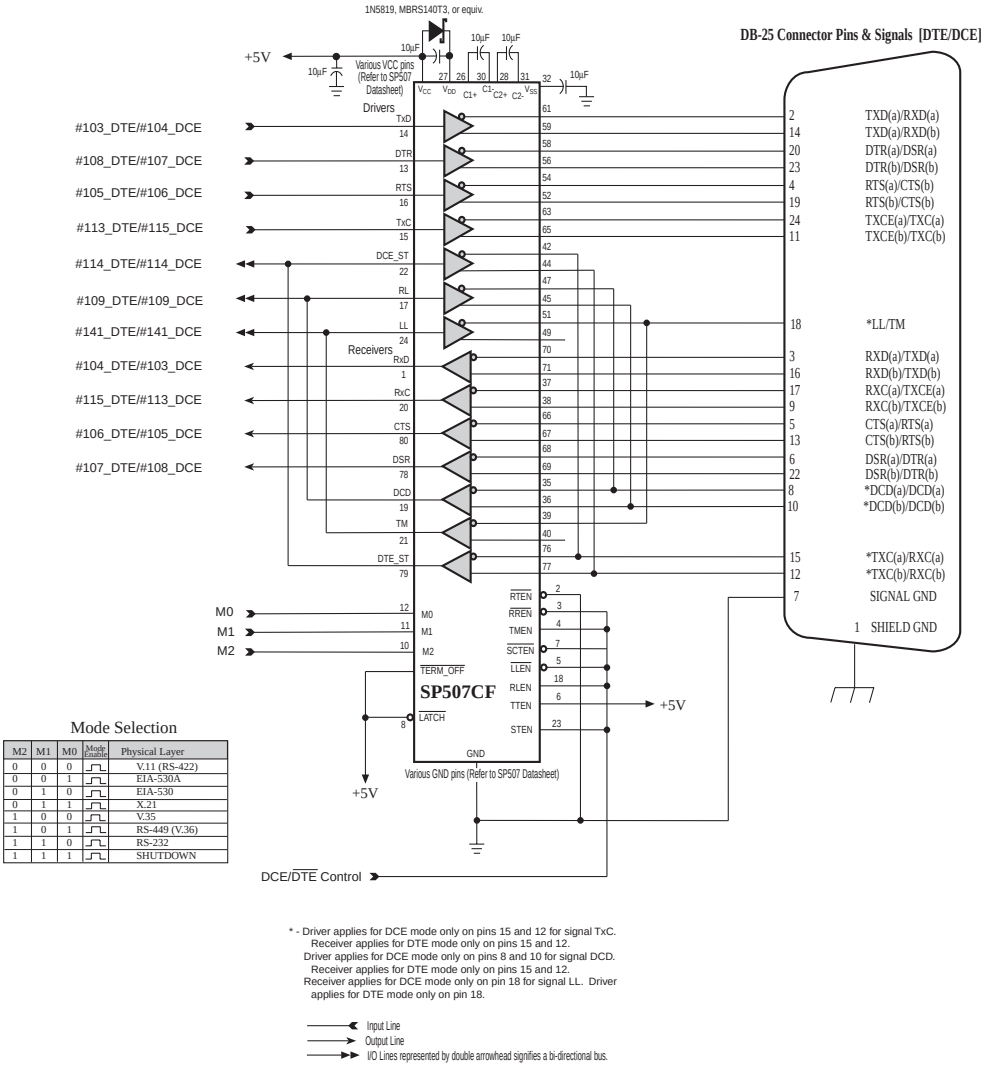
Input Line

Output Line

I/O Lines represented by double arrowhead signifies a bi-directional bus.

Optional bi-directional line; if RL (#140) is used, the driver output, RL(a), can go directly to pin. 21, Remote Loopback, of the DB-25. The RLEN enable pin, if RL is used, can be permanently enabled by tying it to GND.

Figure 4. SP506 DTE/DCE Programmable Configuration



Mode Selection

M2	M1	M0	Mode Enable	Physical Layer
0	0	0		V.11 (RS-422)
0	0	1		EIA-530A
0	1	0		EIA-530
0	1	1		X.21
1	0	0		V.35
1	0	1		RS-449 (V.36)
1	1	0		RS-232
1	1	1		SHUTDOWN

* - Driver applies for DCE mode only on pins 15 and 12 for signal TxC. Receiver applies for DTE mode only on pins 15 and 12. Driver applies for DCE mode only on pins 8 and 10 for signal DCD. Receiver applies for DTE mode only on pins 15 and 12. Receiver applies for DCE mode only on pin 18 for signal LL. Driver applies for DTE mode only on pin 18.

Input Line
Output Line
I/O Lines represented by double arrowhead signifies a bi-directional bus.

Figure 5. SP507 DTE/DCE Programmable Configuration (Similar configuration to competitor's 3-chip solution.)

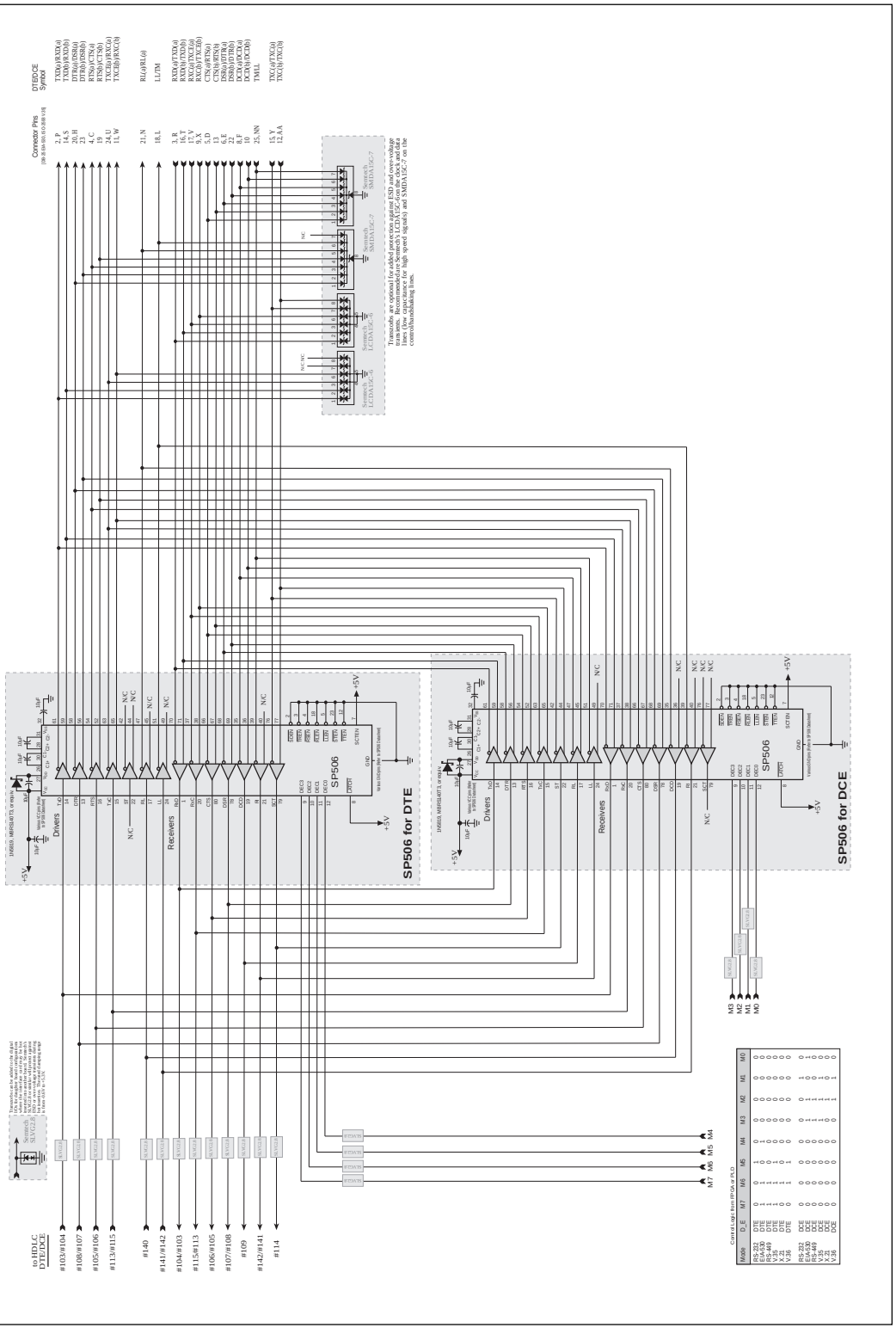


Figure 6. Complete DTE/DCE Programmable Serial Port w/o Crossover Cables

The **SP505**, **SP506** and **SP507** can be easily designed to support this type of configuration. *Figure 6* shows a typical circuit illustrating two **SP506** devices connected in a half-duplex configuration. The top circuit is dedicated to DTE and the bottom **SP506** is dedicated to DCE. Note that only one device is active at any given time. For DTE, the decoder for the DCE device should be off (0000), and vice versa. During the shutdown or off state of the **SP506**, the driver output typically draws 100µA of leakage current. Even with the maximum **SP506** leakage current of 500µA, the receiver input impedance would only change by 500Ω. This is important for RS-232 since the input voltage range can be up to 15V and the typical RS-232 receiver input impedance is 5kΩ. For V.11 differential receivers, the maximum range is ±7V and typical input impedance is 10kΩ. Thus for V.28 receivers, the drivers would be effectively driving into 5kΩ in parallel with the disabled receiver with 10kΩ input impedance. The resultant impedance is 3.3kΩ. For V.11 mode, the drivers will drive into either a terminated receiver of 120Ω or unterminated receiver at 3.9kΩ. These two values in parallel with the disabled 10kΩ receiver will yield 118Ω and 2.8kΩ, respectively, and will not degrade the V.11 driver performance. The receiver outputs are typically at 1µA when disabled.

The **SP505**, **SP506** and **SP507** adds convenience by incorporating the V.11 and V.35 termination resistors inside the device. For this type of 2-chip DTE/DCE configuration, the termination resistors would need to be disabled along with the receivers. A "0000" code into the **SP505** and **SP506** will automatically disable all termination networks as well as the transceivers. A "111" code into the **SP507** performs the same function. In the shutdown mode, the IC will draw less than 10mA of supply current.

Adding Additional Transceivers

To support additional signals, the SP522 can easily attach onto the **SP505**, **SP506** or **SP507** charge pump outputs, V_{DD} and V_{SS}. The SP522 adds two drivers and two receivers for supporting other signals such as RI and RL. In *Figure 7*, the SP522 is hardwired for RS-423 or ITU-T V.10 mode. This allows for the support of RI and RL in RS-449 or V.35 modes if necessary.

Schottky Diode on the SP50x

Sipex requires the installation of a Schottky rectifier placed between the V_{CC} and V_{DD} pins of the SP50x charge pump, where the anode is connected to V_{CC} and the cathode is connected to V_{DD}. It is required to bootstrap the charge pump's internal circuitry during power off conditions in presence of signals or voltages through the receiver inputs or driver outputs.

When placed in parallel with the charge pump capacitor, the diode will allow some of the V_{CC} current to flow into the V_{DD} regions of the device, which will partially bias the V_{DD} charged regions before the device charge pump is fully functioning. This prevents biasing of V_{DD} from other sources such as through the driver outputs or receiver inputs, typical of serial port connections to other powered-on equipment. Once the charge pump oscillator starts up and becomes functional, current flows from V_{DD} back into V_{CC} through the capacitor, ensuring that a rapidly rising V_{DD} does not rise too quickly above the V_{CC} regions before the V_{CC} regions have become fully charged.

The main characteristics of the Schottky diode necessary for this application is the forward voltage. The V_F of the 1N5819 type, which is the diode recommended, is 0.6V @ 1A. Surface mount versions are available from *Motorola*. The *MBRS130T3* from *Motorola* is used with our **SP505**, **SP506**, and **SP507** evaluation boards. Other options are *MBRS140T3* or *MBRS130LT3*, which are all in a "403A-03 SMB" package. The end-to-end length is 5.40mm typical and the width is 3.55mm typical.

Motorola also offers the Powermite™ line, which offers the Schottky rectifiers in a 1.1mm height, 3.75mm length, and 1.90mm width surface mount package. The part numbers recommended are MBRM120LT3, MBRM120ET3, and MBRM140T3. Specifics can be found in *Motorola Semiconductor's* web site (*http://mot-sps.com/products/index.html*). The Schottky rectifiers can be found in the discrete rectifier section and datasheets can be downloaded after searching for the part number.

Powermite™ is a trademark of Motorola.

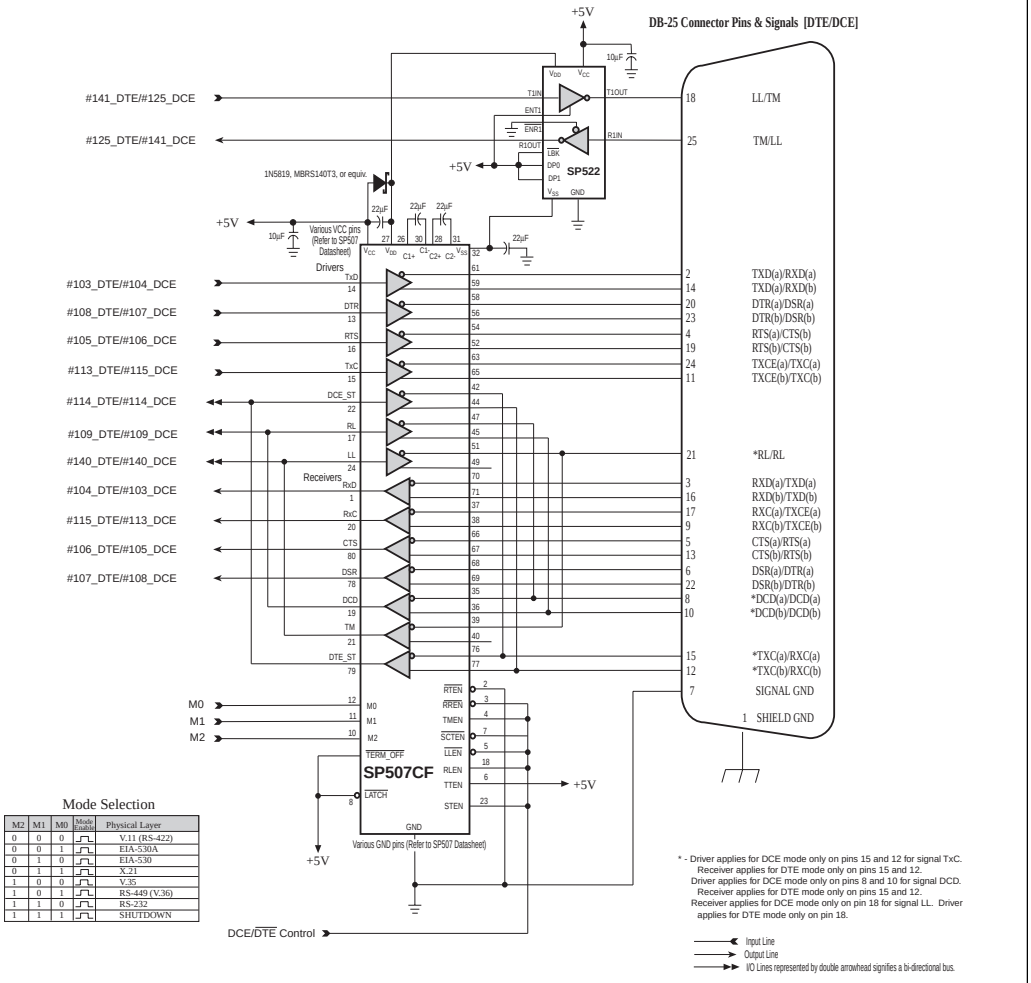


Figure 7. Adding the SP522 to the SP507 in a DTE/DCE Programmable Configuration

SP506 and SP507 Drive Capability

According to the ITU-T V.11 standard, the maximum cable length for a differential V.11 transmission is 4,000 feet (~1,000 meters). However, the standard also illustrates a derating graph of data rate versus cable length. So actually in a real application, the system would not be able to transmit 10Mbps over the full 4,000 feet of Category 3 or similar type cable. As cable parasitics add up over longer cable lengths, capacitance and other affects will degrade the signal, especially at higher frequencies.

The signal integrity depends mainly on the driver output strength or "drivability" and parasitic capacitance on the cable. RS-232 cabling is typically 50pF per foot, where as a good twisted pair type cable for X.21, RS-449, EIA-530, or V.35 will typically be 10pF per foot or less. Some better quality cables will have 3-5pF per foot.

Using a typical setup with a TTC Fireberd 6000A Bit Error Rate Tester (BERT) connected with our SP507 evaluation board as configured in *Figure 8* below, the driver output performance was characterized over various cable lengths. The 6000A BERT emulated the DCE, which provided the TXC clock pulse from 1.544Mbps to 12Mbps. The clock waveform was propagated through the serial cable to the SP507 evaluation board, which was configured as the DTE. The clock signal was then "echoed" through the TxCE (Transmit Clock Echo) driver across the cable and back the BERT. The clock signal input to the TxCE driver (CH3) and the differential driver output are measured with a oscilloscope to observe driver waveform integrity. The differential driver output was measured at the other end of the cable (M1 = A - B), as if the receiver would view the incoming signal. The data stream was generated by the DCE and was propagated through the SP507's RxC receiver and TxCE driver. The BERT also records the number of bit errors occurring during the infinite 1:1 data bit stream that is sent back through the cable.

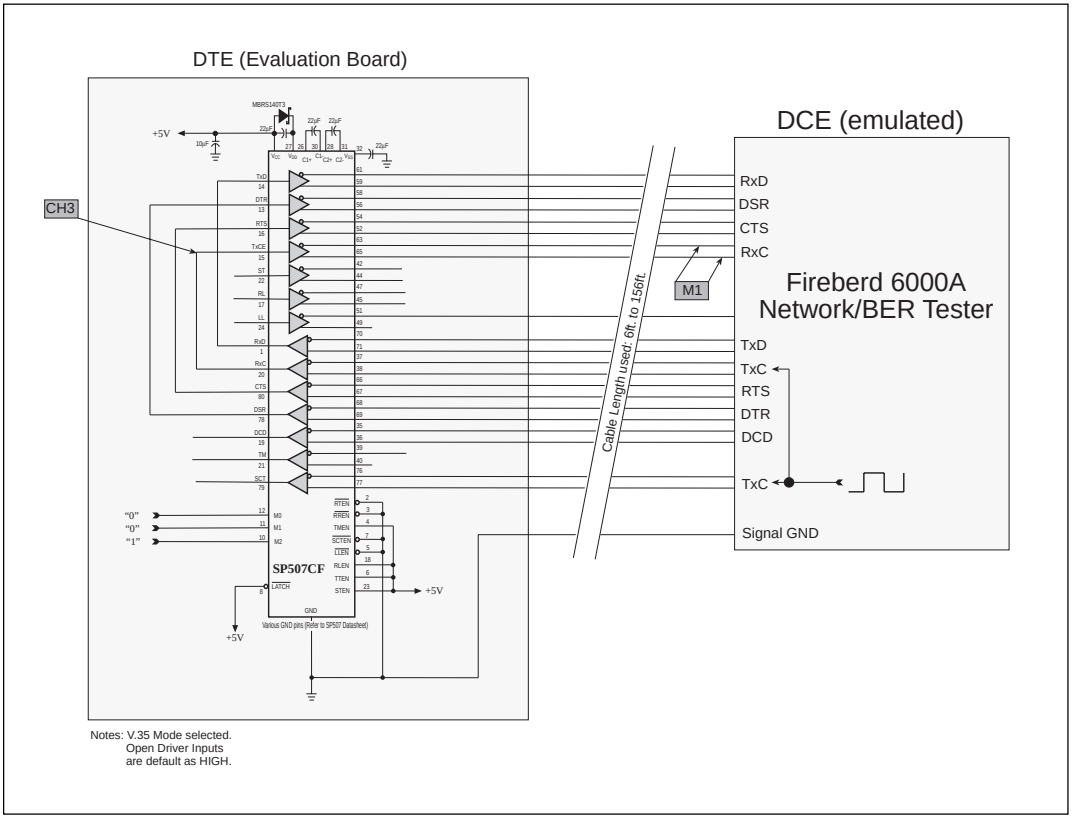


Figure 8. SP507 Cable Length Versus Throughput Circuit Configuration

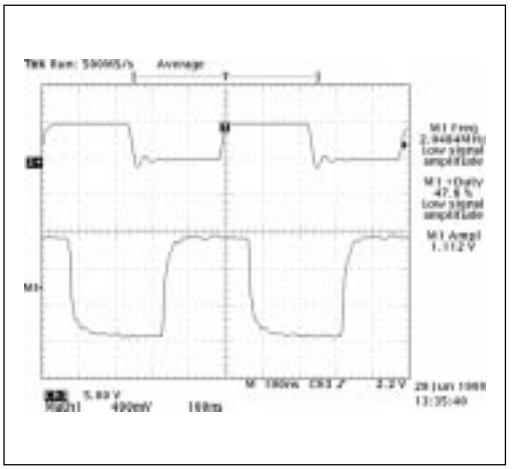


Figure 9. SP507 TxCE at 2.048MHz over 6ft.

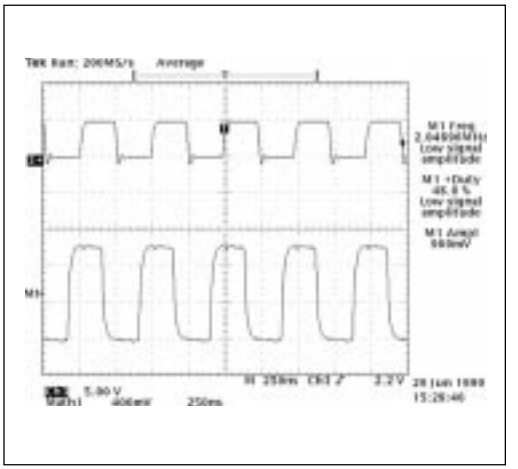


Figure 10. SP507 TxCE at 2.048MHz over 56ft.

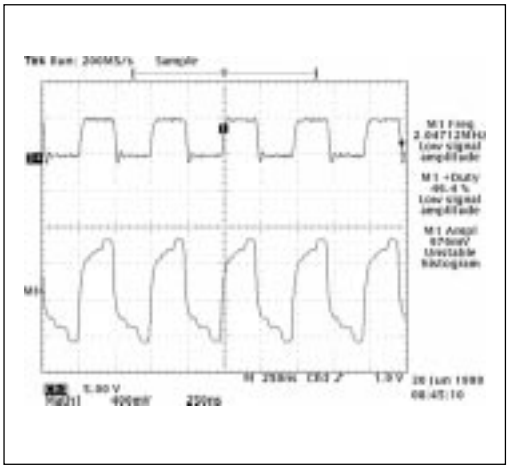


Figure 11. SP507 TxCE at 2.048MHz over 106ft.

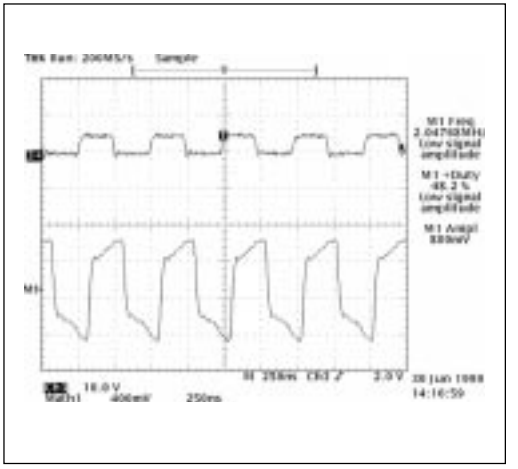


Figure 12. SP507 TxCE at 2.048MHz over 156ft.

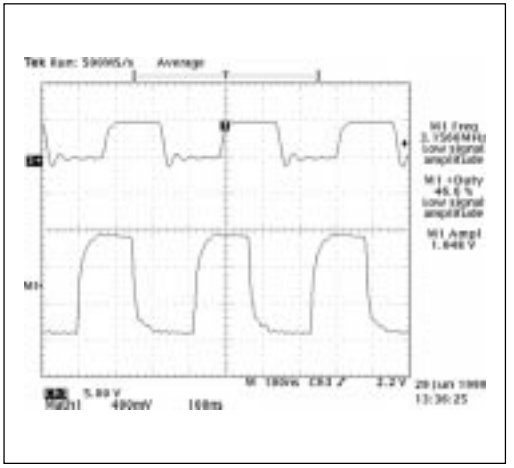


Figure 13. SP507 TxCE at 6.312MHz over 6ft.

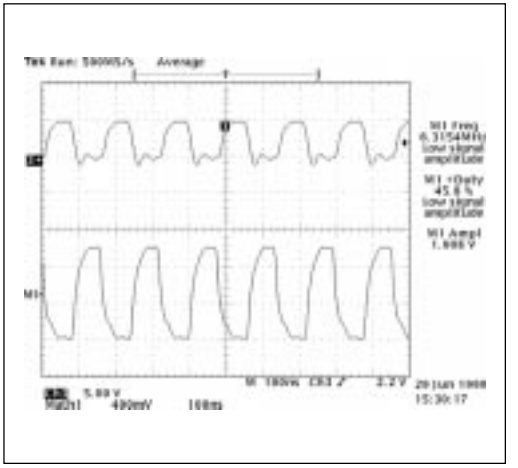


Figure 14. SP507 TxCE at 6.312MHz over 56ft.

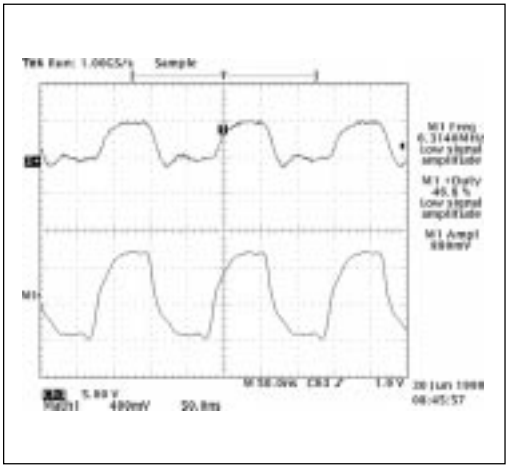


Figure 15. SP507 TxCE at 6.312MHz over 106ft.

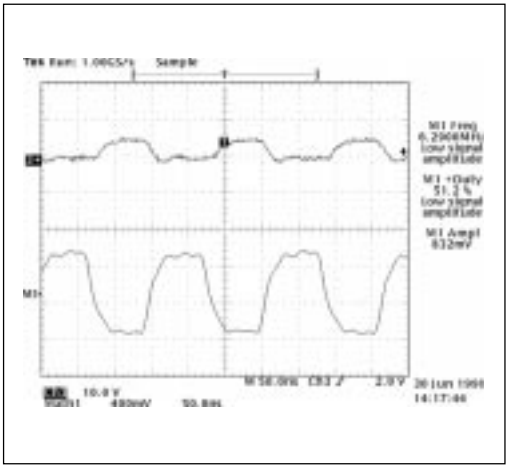


Figure 16. SP507 TxCE at 6.312MHz over 156ft.

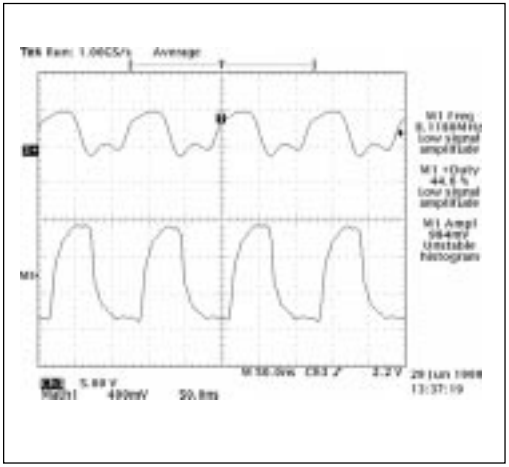


Figure 17. SP507 TxCE at 8.192MHz over 6ft.

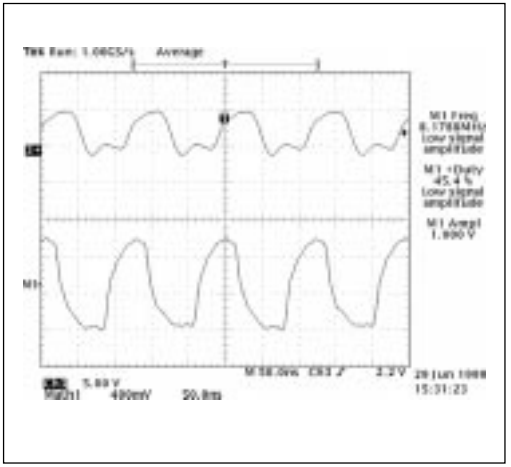


Figure 18. SP507 TxCE at 8.192MHz over 56ft.

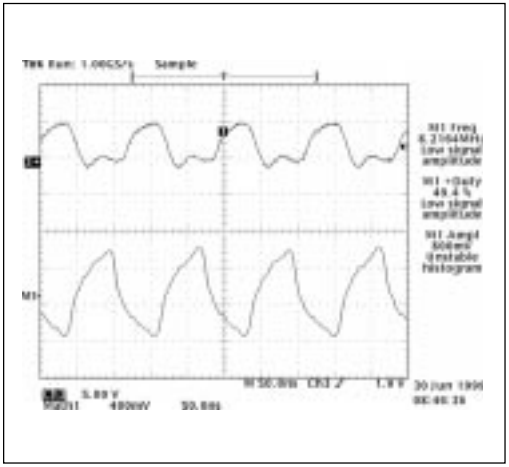


Figure 19. SP507 TxCE at 8.192MHz over 106ft.

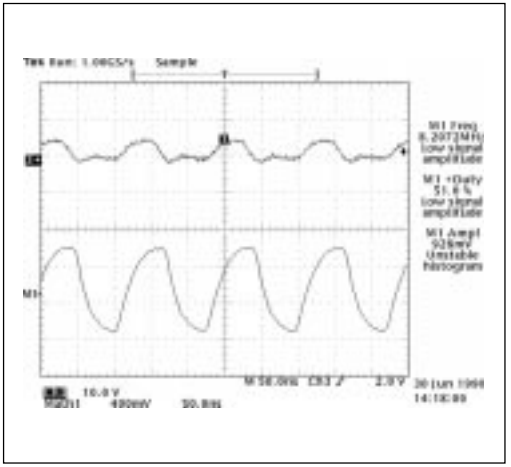


Figure 20. SP507 TxCE at 8.192MHz over 156ft.

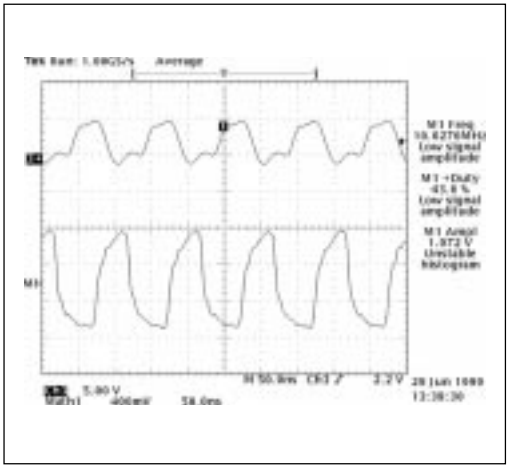


Figure 21. SP507 TxCE at 10MHz over 6ft.

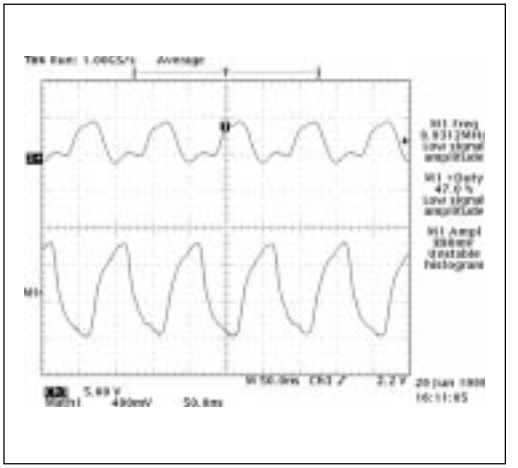


Figure 22. SP507 TxCE at 10MHz over 56ft.

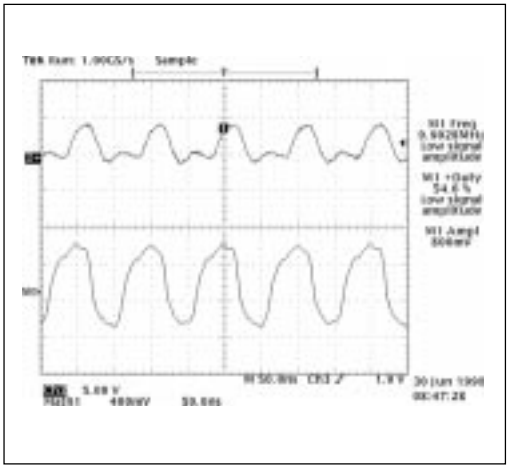


Figure 23. SP507 TxCE at 10MHz over 106ft.

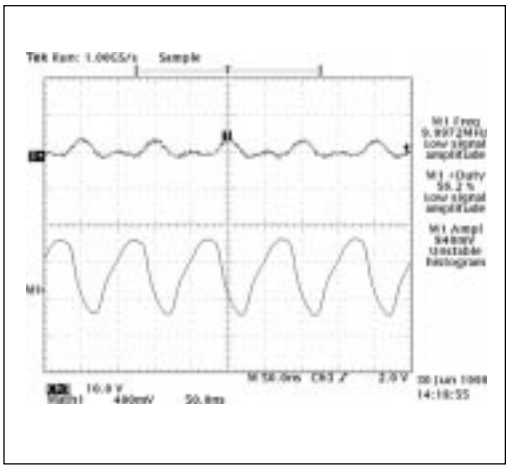


Figure 24. SP507 TxCE at 10MHz over 156ft.

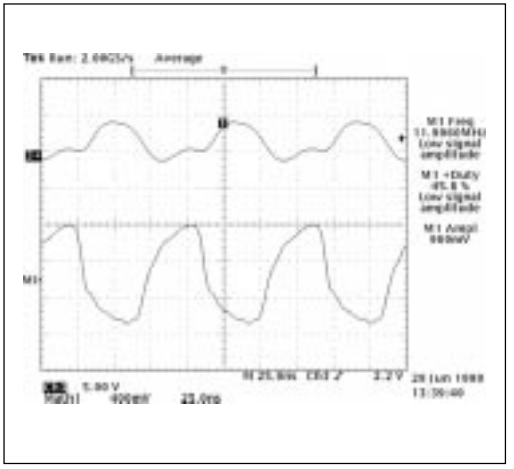


Figure 25. SP507 TxCE at 12MHz over 6ft.

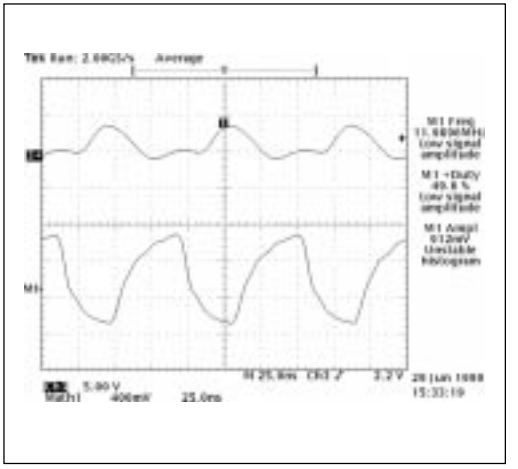


Figure 26. SP507 TxCE at 12MHz over 56ft.

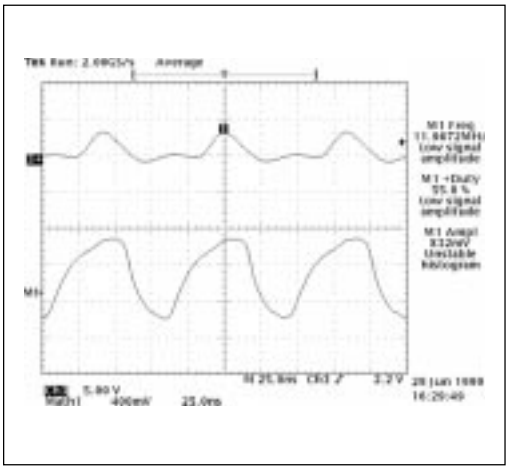


Figure 27. SP507 TxCE at 12MHz over 86ft.

The V.35 interface was selected because the V.35 signal has low voltage differential amplitude, which is more susceptible to noise compared to other higher amplitude signals such as V.11 or RS-485. The small amplitude of 0.55V can easily be affected by noise caused by various environmental effects.

SP506 and **SP507** driver performance was characterized over 6ft., 26ft., 56ft., 86ft, 106ft., 126ft., and 156ft. V.35 cable lengths. The frequency measured are from 1.544MHz, 2.048MHz, 3.152MHz, 6.312MHz, 8.192MHz, 9.600MHz, 10MHz, and 12MHz. The scope photos and graphs on *Figures 9* through *27* illustrate the some of these measurements.

The Fireberd 6000A was able to synchronize with the incoming TxCE clock signal and read the TxD output data stream up to a 12MHz clock without any bit errors. This implies that the clock source had sufficient amplitude and was stable enough for the DCE receiver to read back and synchronize the data on the clock's rising edge. The transmission was successful up to 12MHz with 86 feet of V.35 cable without bit errors. Further cable length degraded the signal to a point where the receiver was unable to capture the clock, thus not able to synchronize data and resulting in bit errors.

One important note is that the signal no longer adheres to the V.35 specification for Transmitter Differential Output with Termination (per CCITT V.35 Section II.3.c) of 0.44V minimum after 56 feet at 10MHz. However, longer cable lengths and even 12MHz signaling was still readable by the DCE. This is because the V.35 receiver input sensitivity is 200mV maximum. As the signal amplitude decays to approximately $400mV_P$ ($832mV_{P-P}$), there is still enough gain on the signal for the receiver to successfully read the clock. Although the AC performance across the system is worse as the receiver input sensitivity is higher.

The V.35 specification does not take into account any capacitive loading for the Terminated Transmitter Output measurement. Therefore it would be unfair to use the V.35 specification as a criteria for pass/fail in a real application environment. Signal monotonicity and duty cycle are the important, measurable elements to determining a clean and error-free clock transmission.

Note that these oscilloscope photos are a typical representation of the **SP507's** performance in presence of cabling using our in-house evaluation board. The system designer should test and characterize the system in order determine the cable distance versus speed allowance in the application.

ESD Protection and EMI Filtering

It is now a requirement for networking equipment, in order to receive the European "CE" mark, to withstand a certain amount of environmental hazards. Among these are ESD and EMI immunity as well as EMI emissions, which is the equipment's own generation of electromagnetic interference.

Electrostatic discharge and overvoltage transients are important to suppress in any system. The specification generally used for ESD immunity is EN61000-4-2 (formerly IEC1000-4-2), which specifies Air Discharge and Contact Discharge Methods. For "CE" approval, the acceptance level is generally "Level 2" per the IEC1000-4-2 specification, which is 4kV Air Discharge and 4kV Contact Discharge. While the **SP505**, **SP506**, and **SP507** has reasonable handling withstand voltages built in the I/O structures of the device, external protection is always a good idea.

One method of protection is incorporating TransZorbs™ or transient voltage suppression ICs, which are back-to-back Zener diodes connected on the line to ground. There are a variety of manufacturers such as Motorola, Siemens, Semtech, Protek Devices, and more. The key specifications are:

1) Reverse Standoff Voltage - normal circuit operating voltage. For RS-232, the maximum V_{RWM} = 15V.
2) Peak Pulse or Transient Current - expected transient current. (I_{PP})
3) Reverse Breakdown Voltage - device begins to avalanche and becomes a low impedance path to ground for the transient. (V_{BR})
4) Maximum Junction Capacitance - loading capacitance of the diode structure. More capacitance will affect the total AC performance. (C_J)

A variety of transzorbs were tested and all perform well in the presence of ESD transients. For faster data rates such as V.11 and V.35 signals, low capacitance is important since an additional 50pF load could add 5ns to the transition time and affect the overall transmission rate. The *Semtech LCDA15C-6* and *Protek Devices SM16LC15C* are especially designed for data communications because of the multichannel line support and the low junction capacitance.

Lower V_{RWM} values can be selected instead of 15V. If the configuration is straightforward, using 5V to 8V V_{RWM} values is fine for the driver outputs and receiver inputs. Using 5V V_{RWM} on the driver is fine since the clamping occurs at the reverse breakdown voltage(V_{BR}), which is 6V for most 5V transzorbs. However, during compliancy testing, the V.28 receiver may be subjected to 15V in order to test the input impedance. Applying a voltage exceeding the V_{RWM} rating will affect the input current measurement and thus fail the impedance test.

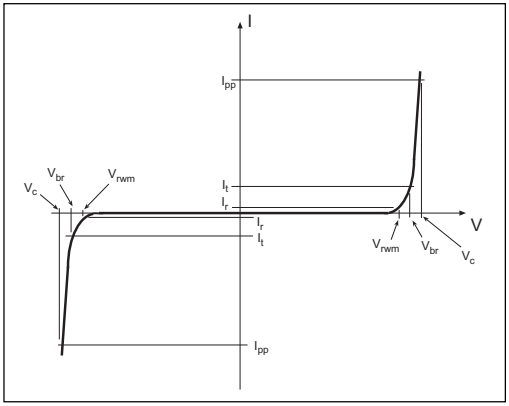


Figure 28. I-V Curve of a TVS diode

Figure 29 illustrates a TVS configuration using the *Semtech LCDA15C-6* connected to the clock and data signals of the **SP505**, **SP506** and **SP507**. The *LCDAC-6* was chosen due to its low junction capacitance of 20pF, which are important for high speed clock and data lines. *Protek's SM16LC15C* can also be used as the junction capacitance is 25pF. However, the two TVS devices are not pin compatible. *Protek's SM16LC15C* contains protection for eight lines and has a straight-through pinout. One side of the *SM16LC15C* is grounded. The *LCDAC-6* uses a 8-pin SOIC package as opposed to the 16-pin package with the *SM16LC15C*. Since two ICs are needed anyway for clock and data, the smaller package is usually preferred. Refer to each of the manufacturer's datasheet for details. *Figure 30* illustrates a TVS configuration to the handshaking signals. As these signals are for control and indication, they do not usually switch at high speed. The junction capacitance for these devices are less critical.

TransZorb is a trademark of General Semiconductor Industries.

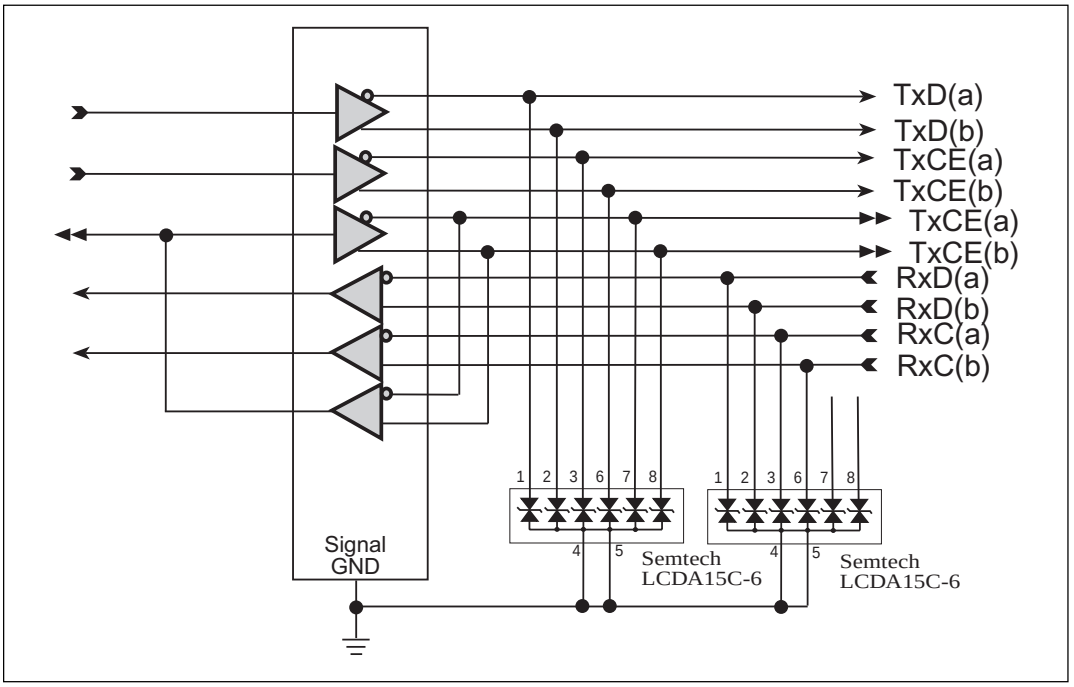


Figure 29. TVS Configuration to Clock and Data Lines of the SP505/SP506/SP507

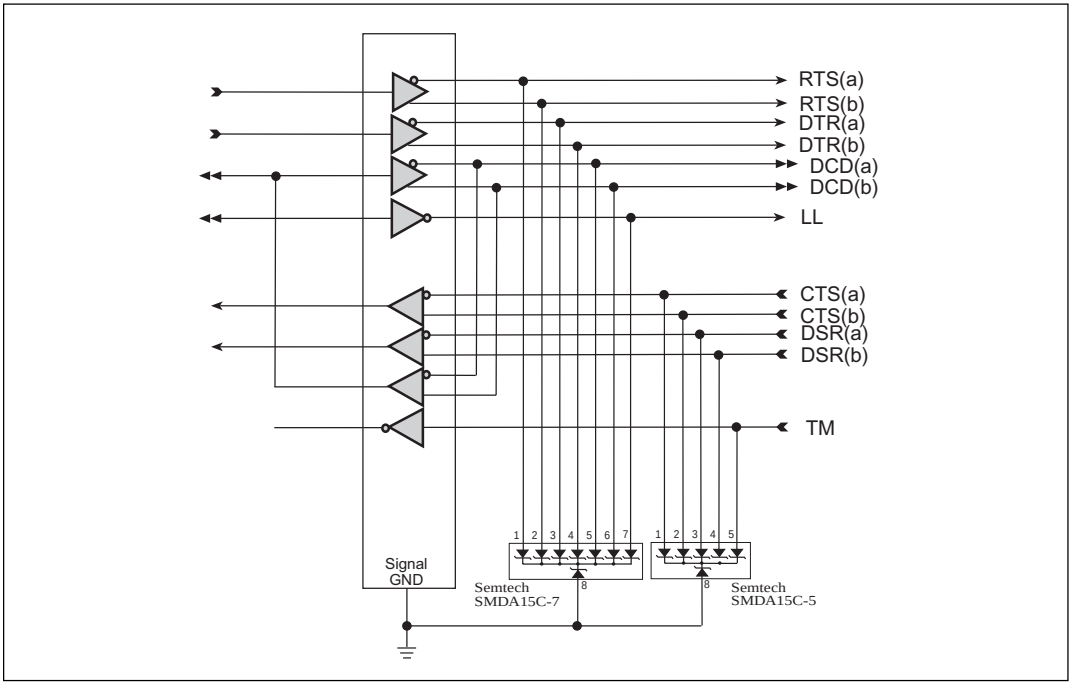


Figure 30. TVS Configuration to Handshaking Signal Lines of the SP505/SP506/SP507

Semtech's SMDA15C-7 is used in *Figure 30* to protect the handshaking signals. Since the *SMDA15C-7* only provides protection for seven lines, the *SMDA15C-5* is used for the remaining lines. Both are 8-pin SOIC packages. Other configurations or manufacturers can be used. Refer to the TVS datasheets. (*http://www.semtech.com/pdf/tvs/lcda15c6.pdf*)

Figure 6 also shows optional TransZorbs™ or TVS devices on the **SP506** to further protect the serial port from any ESD or overvoltage transients that may occur in any application. The **SP505**, **SP506** and **SP507** are internally rated for 8kV based on Human Body Model and 2kV Air Discharge per IEC1000-4-2. Adding transzorbs to the I/O lines will protect the serial port to over 15kV of ESD transients per IEC1000-4-2 Air Discharge and 8kV per Contact Discharge. The TVS devices on the driver inputs and receiver outputs are included for hot-insertion of the interface module/board applications.

The internal junction of the **SP505**, **SP506** and **SP507** receiver inputs and driver outputs are similar to the I-V curve on *Figure 28*. However, TVS devices are always recommended where ever possible as it is difficult to predict transient induced phenomena in any environment.

It is also important to know that these TVS devices are also specified for IEC1000-4-4 Electrical Fast Transients and IEC1000-4-5 Surge (Lightning) protection. Refer to the TVS datasheets from *Semtech* for details (*www.semtech.com*).

Electromagnetic Interference is also a concern for networking equipment. The EMI noise is cause by radiated emissions or power-line conducted emissions from the system. The equipment has to be characterized for both immunity and emissions. Immunity is the system's tolerance to incoming interference or disturbances generated from outside sources. Emissions are the system's own generation of these types of disturbances. Specifically, the documents EN61000-4-3 and EN61000-4-6 pertain to Radiated electric field test and Line Conducted electric field test, respectively, for immunity. The EN55022 specification pertains to emissions and specifies Line Conducted Emission, which are noise or disturbances generated from a power supply unit, conducted in the cables; and Radiated emissions, which pertain to noise or disturbances generated by the power supply unit and radiated out to the environment. For serial port datacom applications, both emissions and immunity must be carefully considered during the design-in phase.

The conducted emissions in the most single supply interface transceivers are generated from the internal charge pump. Although the charge pump is enhanced over previous generation pumps, the **SP506** and **SP507** charge pump architecture will inherently have small ripples on the V_{DD} and V_{SS} outputs. The ripples are due to the switching of the internal charge pump transistors that are transferring energy. The charge pump oscillates at 20kHz in standby mode (without loads to the drivers) and will automatically increase frequency to 300kHz when loaded. The ripples will coincide with the oscillator frequency. The driver output circuitry receives biasing from the charge pump outputs, V_{DD} and V_{SS}, for the V.28 and V.10 bipolar voltage swings. The V_{DD} or V_{SS} supply ripple could be superimposed onto the driver outputs, depending on the ripple amplitude. Larger capacitor values will suppress the ripple of the pump and thus, minimize the ripple amplitude on the data lines. For the **SP505**, **SP506**, and **SP507**, the amplitude of the ripple is below 100mV when using 22µF pump capacitors (refer to *Figure 34*).

Depending on the application requirements, EMI/EMC filtering may be needed. The **SP506** and **SP507** are usually not affected by radiated disturbance nor do they emit radiated noise/interference. But a shielded enclosure (Faraday Cage) will help the immunity from radiated disturbance as well as emissions of radiated noise. Conducted noise can be surpressed by using ferrite beads, low pass filters using RC circuits, inductor circuits, or common mode chokes on the signal lines.

One surface mount common-mode choke (CMC) designed for data signaling applications in the 10Mbps to 15Mbps band is *TDK's ZJYS51R5-4P*. This 8-pin SOIC package contains a two pairs of inductors for two differential signals. Since clock and data are switching most frequently, the number of pairs needed are two for DTE (TxD and TxCE drivers) or three for DCE (TxD, TxCE, TxC drivers), which means one IC for DTE and two ICs for DCE. Refer to *Figure 31* for connection and to TDK's datasheet for the ZJYS51R5-4P CMC.
(*http://www.tdk.co.jp/tefe02/e971_zjys.pdf*)

Another alternative is using conductive-EMI enhanced connectors that have ferrite cores around the pins. AMP and other connector manufacturers also offer specially built conductive-EMI filtered connectors. The *AMPLIMITE*™ Subminiature D-Sub connectors have a DB-15 through DB-37 connectors as well as high density connectors that have a distributed element filter using lossy ferrite core or a capacitive filter assembled around each pin. These connectors have right-angle, vertical, or stacked versions that all have the same PCB footprint as the regular non-filtered connectors.

Various filter types are available with these connectors. Once the serial protocol is defined and the operating frequency known, a filter type can be chosen using its 3dB point, which can be used as the maximum frequency. The filter will begin filtering above this 3dB point. One should be careful when using the capacitive filters as they will affect the overall AC performance of the driver, specifically driver rise/ fall time. Details of the *AMPLIMITE*™ filtered connectors can be found in AMP's home page (*http://connect.amp.com.*), which includes insertion loss (dB) versus frequency.

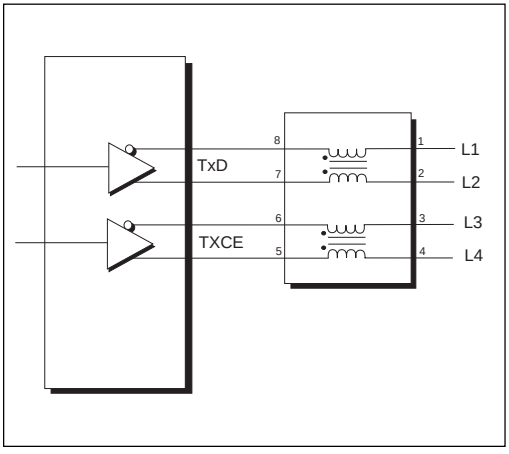


Figure 31. Common-Mode Choke Circuit with Drivers

AMPLIMITE™ is a trademark of AMP Inc.

Using Smaller Charge Pump Capacitors with the SP50x

The charge pump of the **SP505**, **SP506**, and **SP507** have been designed to drive the RS-232 voltage levels through the drivers using 22µF pump capacitors. However, the **SP505**, **SP506**, and **SP507** can use 10µF capacitors for operation while still maintaining the critical specifications.

There are two issues involved with lowering the charge pump capacitors; RS-232 driver output V_{OH} and V_{OL} levels, and output ripple.

Figure 32 shows the typical driver output (TxD in this case) in an unloaded condition using 10µF charge pump capacitors. *Figure 33* shows the same driver but loaded with 3kΩ and 2,500pF to ground. Running at a worse case speed of 120kHz, the driver output voltages shown in *Figure 34* clearly comply with the RS-232 and ITU-T V.28 specifications under these conditions.

Figures 34 and *35* show the driver output's ripple when a DC input is asserted. The ripple in *Figure 34* uses 22µF charge pump capacitors where as *Figure 35* uses 10µF capacitors. The ripple amplitude is increased from approximately 60mV to 400mV. Although the RS-232 voltages are within the specifications and the ripple amplitude is negligible compared to the RS-232 signal amplitude, the designer should examine the EMC consequences of reducing the charge pump capacitors.

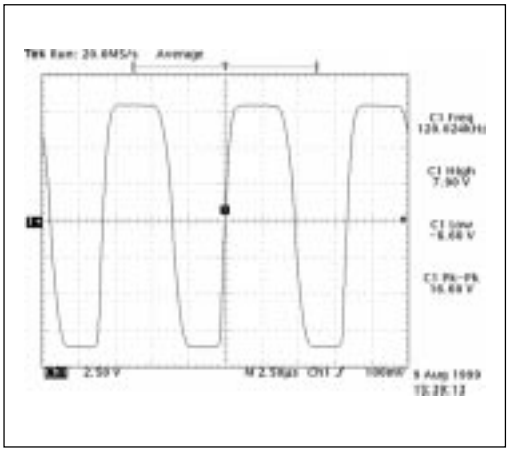


Figure 32. Unloaded Driver Output Using 10µF Pump Capacitors

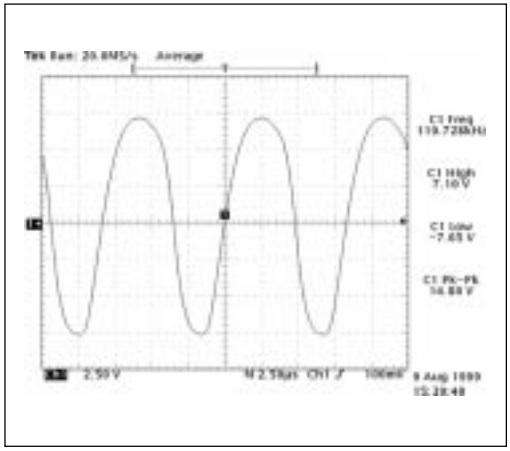


Figure 33. Driver Output Loaded w/ 3kΩ // 2,500pF Using 10µF Pump Capacitors

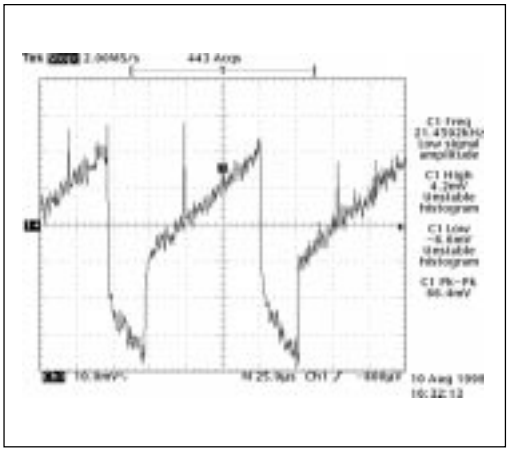


Figure 34. Charge Pump Ripple of Driver Output w/ 22µF Pump Capacitors

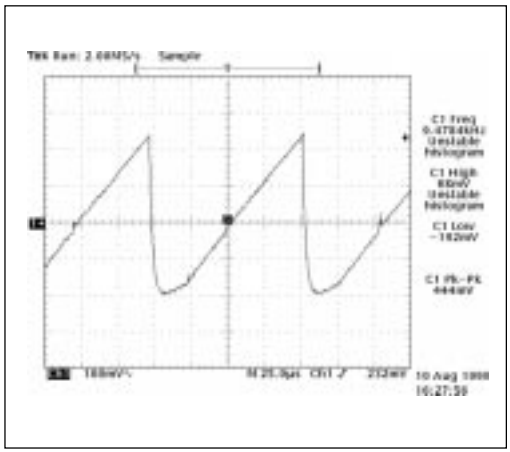


Figure 35. Charge Pump Ripple of Driver Output w/ 10µF Pump Capacitors

SP506 and SP507 Evaluation Boards

For easy bench testing of the **SP506** and **SP507**, evaluation boards are available. Similar to the **SP505EB**, the **SP506EB** and **SP507EB** offers a "breakout" type configuration that allows the user to access the driver's and receiver's I/Os. The evaluation boards have a DB-25 serial connector that is configured to a EIA-530 DTE pinout. This connector can be used to analyze any of the serial standards offered in the **SP506** and **SP507**. Translation cables may be needed from the DB-25 to the appropriate connector. Refer to *Figure 1* or the cabling schemes in the ***Design Guide for Multi-Protocol Serial Ports***. Refer to the ***SP504/SP505 Evaluation Board Manual*** for the **SP506EB**.

For the **SP507EB**, the probe pins or access points are arranged such that the drivers are on one side and the receivers are on the other. Each driver has three basic access points: the TTL input, inverting analog output, and non-inverting analog output. Additional access points are included for the driver outputs, thus a total of four access points for each driver. Similarly with the receiver with two analog inputs, inverting and non-inverting, and the TTL output. Receiver inputs have additional access points for convenience. There are additional ground points for convenient resistor or capacitor load connections to the driver output access points. There are also receiver ground points for convenience at each receiver.

The TTL control lines have DIP switches that allow the user to input a signal to enter a logic HIGH or logic LOW. The control lines include the driver and receiver enable lines and the mode select pins. For the **SP506EB**, the driver enable inputs are active LOW and have internal pull down resistors. The DIP switch position will either tie the inputs to a logic HIGH or leave the input open where the internal pull-down defines a LOW state.

For the **SP507EB**, the **SP507** uses a logic HIGH for its driver enable lines except for the LL driver, which

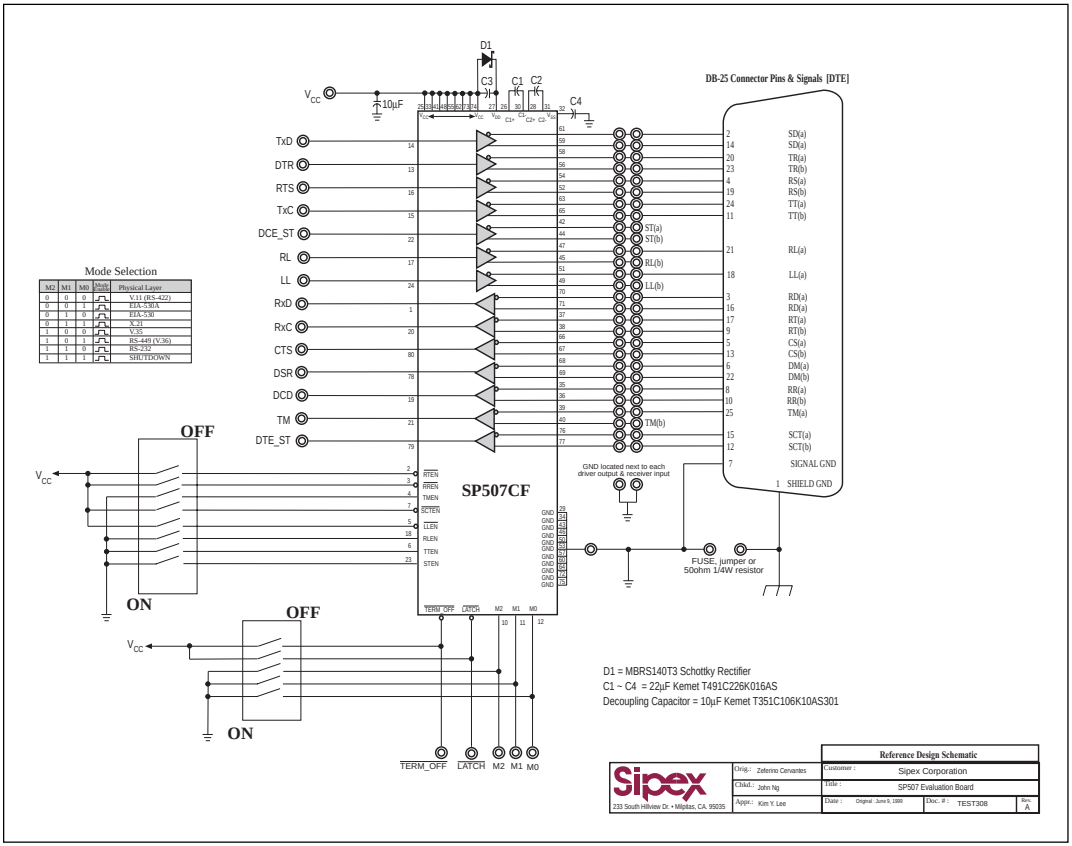


Figure 36. SP507EB Schematic

has a logic LOW enable. The receivers use a logic LOW enable for its receiver enable lines except for the TM receiver, which has a logic HIGH enable. The DIP switches for the SP507EB evaluation board is such that the "down" position of the switch will be considered "ON" and the "up" position will be considered "OFF", regardless up enable polarity. Note that the SP507EB Rev. A boards will have the label on the switches reversed. But the true state is all transceivers enabled when rocker switches are positioned down.

On the right side of the board with the driver inputs, there is a common bus named INPUT, which has access points next to each driver input. This bus is added on the board for convenience so that the driver inputs can all be connected together via jumper wires to this bus. The INPUT trace can be followed on the top layer of the board.

The other DIP switch will configure the physical layer protocol desired on the transceiver IC. The **SP507** uses three bits M0, M1, and M2. The decoder bits will be logic HIGH when the toggle position is "down" The /TERM_OFF will be logic LOW when in the rocker "down" position. The /LATCH pin will be logic HIGH in the rocker "down" position.

The "FUSE" connection on the board is included to connect the shield ground to the signal ground. A 1-Ω to 100Ω resistor can be placed into the FUSE position. EIA-530, EIA-530A, and RS-449 standards state that a 100Ω, 1/4W resistor should isolate the shield or earth ground from the signal ground on the DTE side.

Loopbacks and other testing can be easily performed by the use of jumper wires or cables. All necessary points on the boards are labelled. The **SP507 Evaluation Board** (Rev. A) schematic is shown on *Figure 36*. The **SP507EB** (Rev A.) layout plot is shown on *Figure 38*.

SP505, 506 and SP507 Retrofits

Along with our **SP506** Evaluation (**SP506EB**) and **SP507** Evaluation Boards (**SP507EB**), Sipex also offers **SP506** or **SP507** Retrofit Boards (**SP506RB** and **SP507RB**). Shown in *Figure 37*, these retrofit boards are design to map onto existing motherboards and replace an existing serial port platform. These boards are approximately 1.375" x 1.375" and contain the four charge pump capacitors and one Schottky diode needed for compliant operation. The boards also have the connections for driver inputs and outputs and receiver inputs and outputs. Using a ribbon type cable or "flex-board", the analog I/Os can be mapped to the appropriate pin assignment on the serial port connector and the TLL/CMOS I/Os to the HDLC serial controller IC. The equipment's existing serial transceiver ICs can be depopulated and replaced by the retrofit board.

Sipex usually prefers to perform the retrofitting in-house. But the experienced designer can also retrofit the serial port as well. Once connected properly, the functionality and electrical performance will be transparent to the user. **Sipex** will perform the necessary testing to ensure the retrofit is electrically transparent and complaint to the physical layer specifications. **Sipex** has already passed homologation testing per NET1/2 and TBR2 with this board retrofitted onto a router.

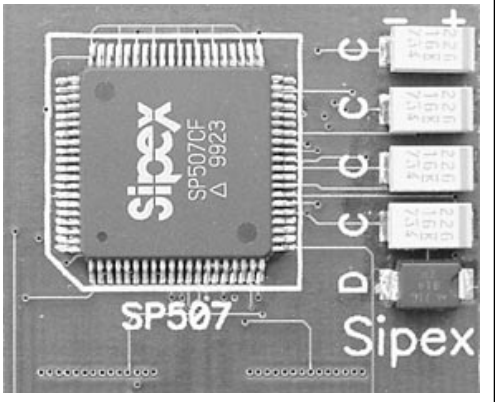


Figure 37. SP507 Retrofit Board

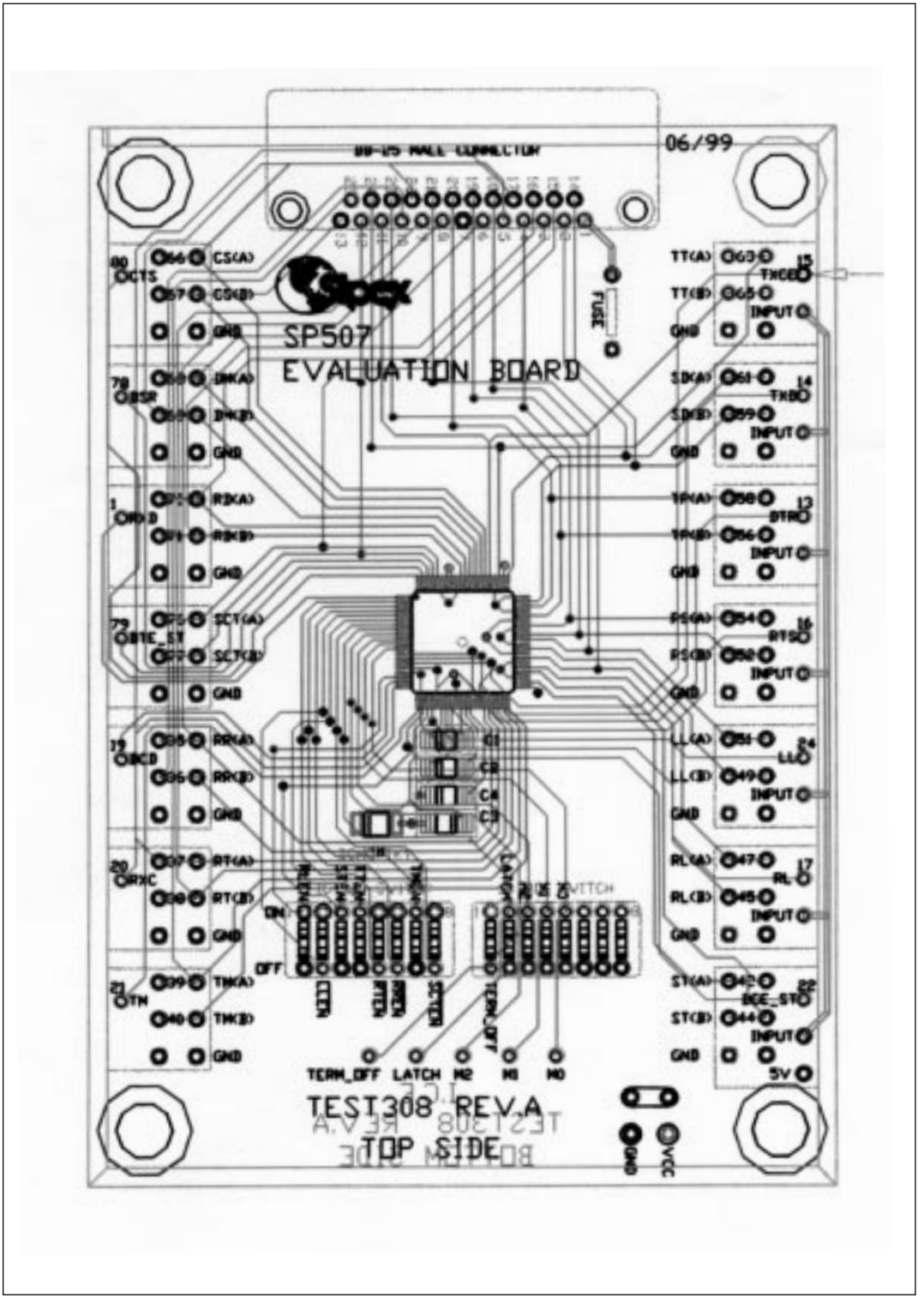


Figure 38. SP507 Evaluation Board Layout

More Compliancy....

In order for networking equipment to be connected in the European network or even offered in Europe, it must be thoroughly tested to a set of specifications. Serial ports are no exception to the rule and are tested to ensure compliancy to their respective ITU specifications. This is to ensure proper operation to the public network as the equipment is connected. This is a requirement in order to obtain the "CE" mark for European compliance.

In January of 1998, CTR1/CTR2 compliancy could officially be attained by using another test option called TBR2. The Technical Basis for Regulation specification was recently finalized and approved for use as a test criteria for certification. Similar to NET1/2, the testing ensures that the serial port adheres to the ITU-T V-Recommendations. It specifies the connector type and the signals required between the DTE and DCE. However, there are some minor testing differences.

Paragraph 6.3.1 – V.10 Interface

6.3.1.1 Generator open circuit output voltage

The single-ended generator or driver's output (point A), for either binary state, shall be less than or equal to 12.0V when terminated with a 3.9kΩ resistor to ground (point C).

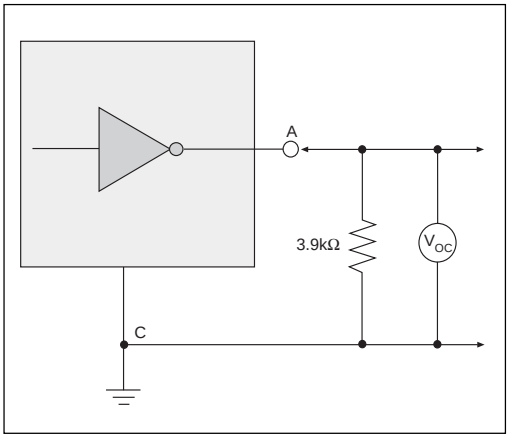


Figure 39. V.10 Driver Open Circuit Voltage

6.3.1.2 Generator terminated output voltage

The driver output's magnitude, for either binary state, shall be greater than or equal to 2.0V when terminated with a 450Ω resistor to ground.

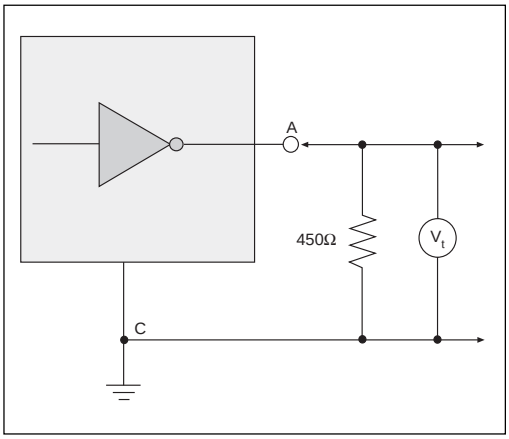


Figure 40. V.10 Driver Terminated Voltage

6.3.1.3 Generator output rise/fall time

The driver output's transition from one binary point to another shall be less than or equal to 0.3 of the nominal bit duration (t_b). This is measured between 10% and 90% of its steady state value and with a 450Ω resistor load to ground.

6.3.1.4 Generator polarities

The driver's single-ended output A shall be:
a) greater than point C ($V_{OUT} > 0V$) when the signal condition 0 is transmitted for data circuits, or ON for control circuits; and
b) less than point C ($V_{OUT} < 0V$) when the signal condition 1 is transmitted for data circuits, or OFF for control circuits.

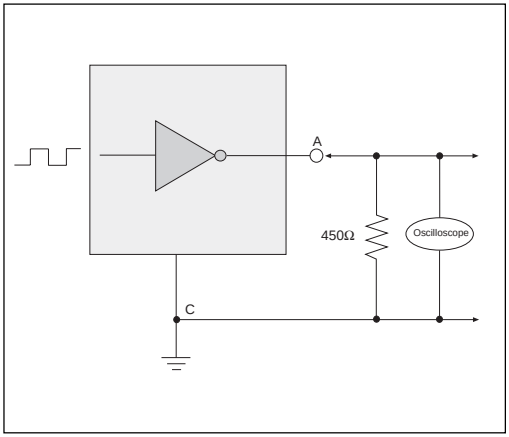


Figure 41. V.10 Driver Transition Time

Paragraph 6.3.2 – V.11 Circuits

6.3.2.1 Generator open circuit output voltage

The magnitude of the driver's outputs for:

a) between point A and point B

b) either point A or point B to point C

shall be less than or equal to 12.0V for either binary state when terminated with a 3.9kΩ resistor between points A and points B.

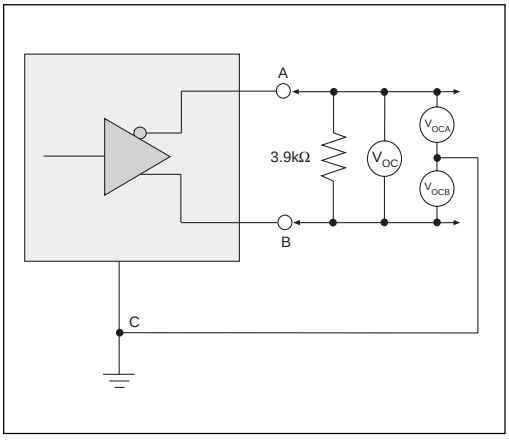


Figure 42. V.11 Driver Open Circuit Voltage

6.3.2.2 Generator terminated output voltage

The magnitude of the driver's outputs for:

a) between point A and point B

b) either point A or point B to point C

shall be greater than or equal to 2.0V for either binary state when terminated with two 50Ω resistors connected in series between point A and point B.

The center point of the two 50Ω resistors shall measure less than or equal to 3.0V with respect to point C.

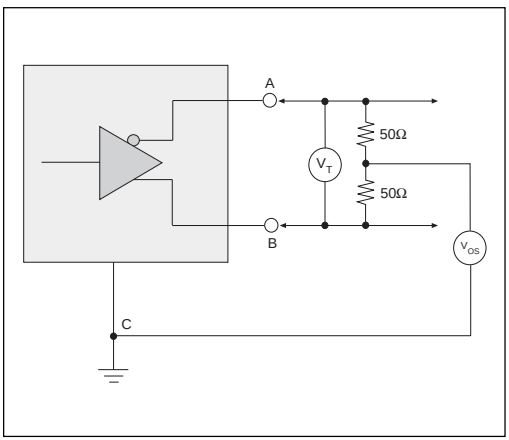


Figure 43. V.11 Driver Output Terminated Voltage

6.3.2.3 Generator output rise/fall time

The driver outputs' transition from one binary point to another shall be less than or equal to 0.3 of the nominal bit duration (t_b). This is measured between 10% and 90% of its steady state value and with a "Y" resistor configuration. The resistor network contains two 50Ω resistors in series with a center-tap 50Ω resistor between the two series resistors to ground.

6.3.2.4 Generator polarities

The driver's point A output shall be:

a) greater than point B (V_A–V_B > 0V) when the signal condition 0 is transmitted for data circuits, or ON for control circuits; and

b) less than point B (V_A–V_B < 0V) when the signal condition 1 is transmitted for data circuits, or OFF for control circuits.

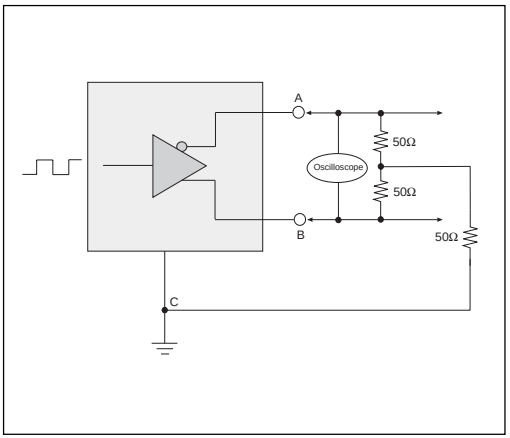


Figure 44. V.11 Transition Time

Paragraph 6.3.3 – V.28 Circuits

6.3.3.1 Generator open circuit output voltage

The single-ended generator or driver's output (point A), for either binary state, shall be less than or equal to 25.0V with respect to ground (point C).

6.3.1.2 Generator terminated output voltage

The driver output's magnitude, for either binary state, shall be greater than or equal to 3.0V when terminated with a 3kΩ resistor to ground.

6.3.1.3 Generator output rise/fall time

The driver output's transition from one binary point to another shall be less than or equal to 3% or 1.0ms, whichever is greater, of the nominal bit duration (t_b). This is measured between +3V and -3V of the transition and with 3kΩ resistor // 2500pF loads to ground.

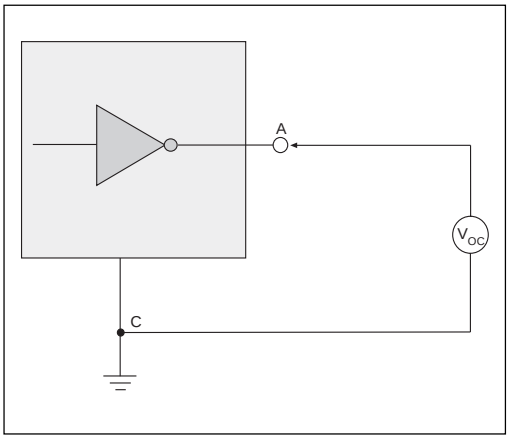


Figure 45. V.28 Driver Open Circuit Voltage

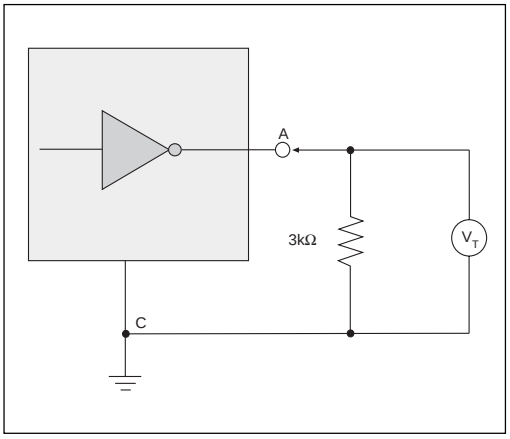


Figure 46. V.28 Driver Terminated Voltage

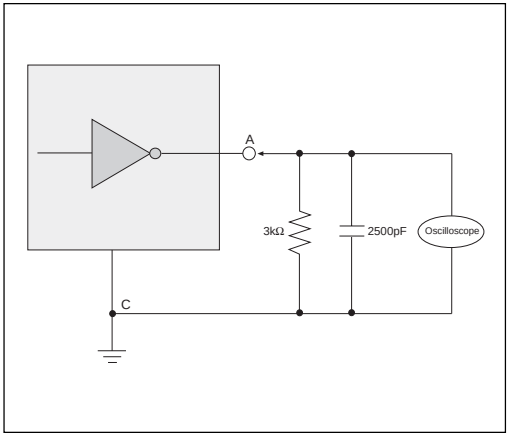


Figure 47. V.28 Transition Time

6.3.1.4 Generator polarities

The driver's single-ended output A shall be:
a) greater than point C (V_{OUT} > 0V) when the signal condition 0 is transmitted for data circuits, or ON for control circuits; and
b) less than point C (V_{OUT} < 0V) when the signal condition 1 is transmitted for data circuits, or OFF for control circuits.

6.3.3.5 Receiver maximum shunt capacitance

The total effective shunt capacitance shall be less than 2500pF at point A with respect to ground. This is measured by applying a $14V_P$ signal with 0V offset at 9.6kbps with 50% duty cycle through a 1.2kΩ resistor. The rise time measured from -3V to +3V at point A to point C (t_1) and the fall time measured from +3V to -3V at point A to point C (t_2) is measured and recorded.

Then replace the receiver with a 3kΩ resistor in parallel with a 2500pF capacitor and apply the same signal through the 1.2kΩ resistor. The new rise time (t_3) is recorded and compared to t_1 and t_2. The times t_1 and t_2 shall be less than or equal to t_3.

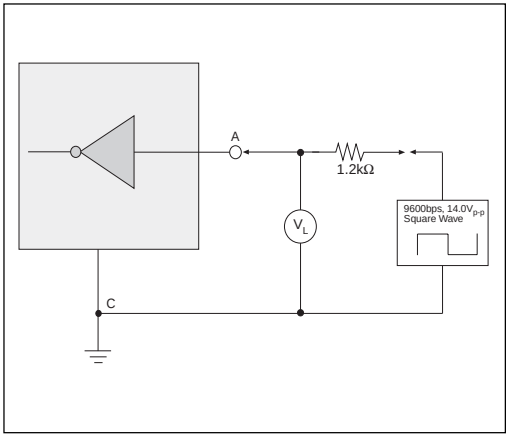


Figure 48. V.28 Receiver Effective Shunt Capacitance

Paragraph 6.3.4 – V.35 Circuits

6.3.4.1 Generator open circuit output voltage

The magnitude of the driver's outputs for:

a) between point A and point B

b) either point A or point B to point C

shall be less than or equal to 1.2V for either binary state when terminated with a 3.9kΩ resistor between points A and points B.

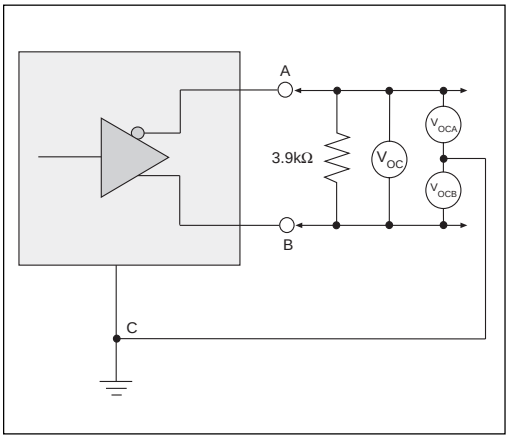


Figure 49. V.35 Driver Open Circuit Voltage

6.3.4.2 Generator terminated output voltage

The magnitude of the driver's outputs for:

a) between point A and point B

b) either point A or point B to point C

shall be 0.55V ±20% for either binary state when terminated with two 50Ω resistors connected in series between point A and point B.

The center point of the two 50Ω resistors shall measure less than or equal to 0.6V with respect to point C.

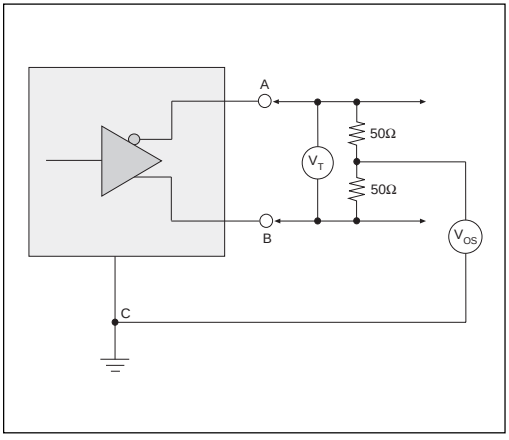


Figure 50. V.35 Driver Terminated Voltage

6.3.4.3 Generator output rise/fall time

The driver outputs' transition from one binary point to another shall be less than or equal to 0.1 of the nominal bit duration (t_b). This is measured between 20% and 80% of its steady state value and with a "Y" resistor configuration. The resistor network contains two 50Ω resistors in series with a center-tap 50Ω resistor between the two series resistors to ground.

6.3.4.4 Generator polarities

The driver's point A output shall be:

a) greater than point B ($V_A – V_B \geq 0V$) when the signal condition 0 is transmitted for data circuits, or ON for control circuits; and

b) less than point B ($V_A – V_B \geq 0V$) when the signal condition 1 is transmitted for data circuits, or OFF for control circuits.

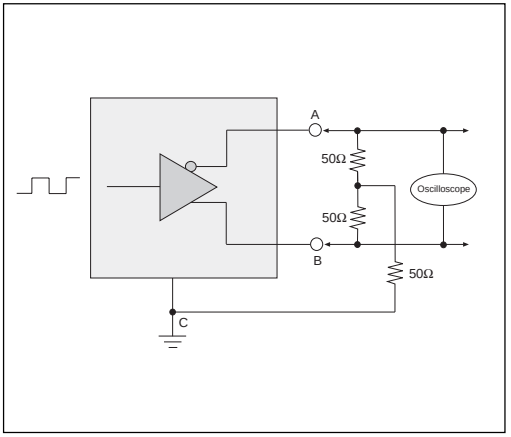


Figure 51. V.35 Transition Time

The **SP505** has been successfully tested to CTR1/CTR2 through TUV Telecom Services. The test was performed on the **SP505EB** Evaluation Board. The test report ***CTR2/052101/98*** can be furnished upon request. The **SP507** has also successfully passed the CTR1/CTR2 testing requirements through KTL using our **SP507EB**. The test report ***9D2566DEU1*** can also be furnished upon request.

Please contact Sipex Applications for details.

TÜV Rheinland

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Fax. +1 612 639-0873

TEST REPORT NO.

CTR2/052101/98

Date: June 12, 1998

Total Number of Pages: 25

Equipment: **Sipex SP505CF**

Client: **Sipex Corporation**
Address: **491 Fairview Way**
Milpitas, CA 95035
USA

European Harmonised Standard: **CTR 2**

Authorised Signature:

June 12, 1998	**D. Mueller**	**Chief Engineer**	
Date	Name	Title	Signature

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Registration No. S002E001

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Figure 52. Front Cover of the CTR1/CTR2 Test Report for the SP505

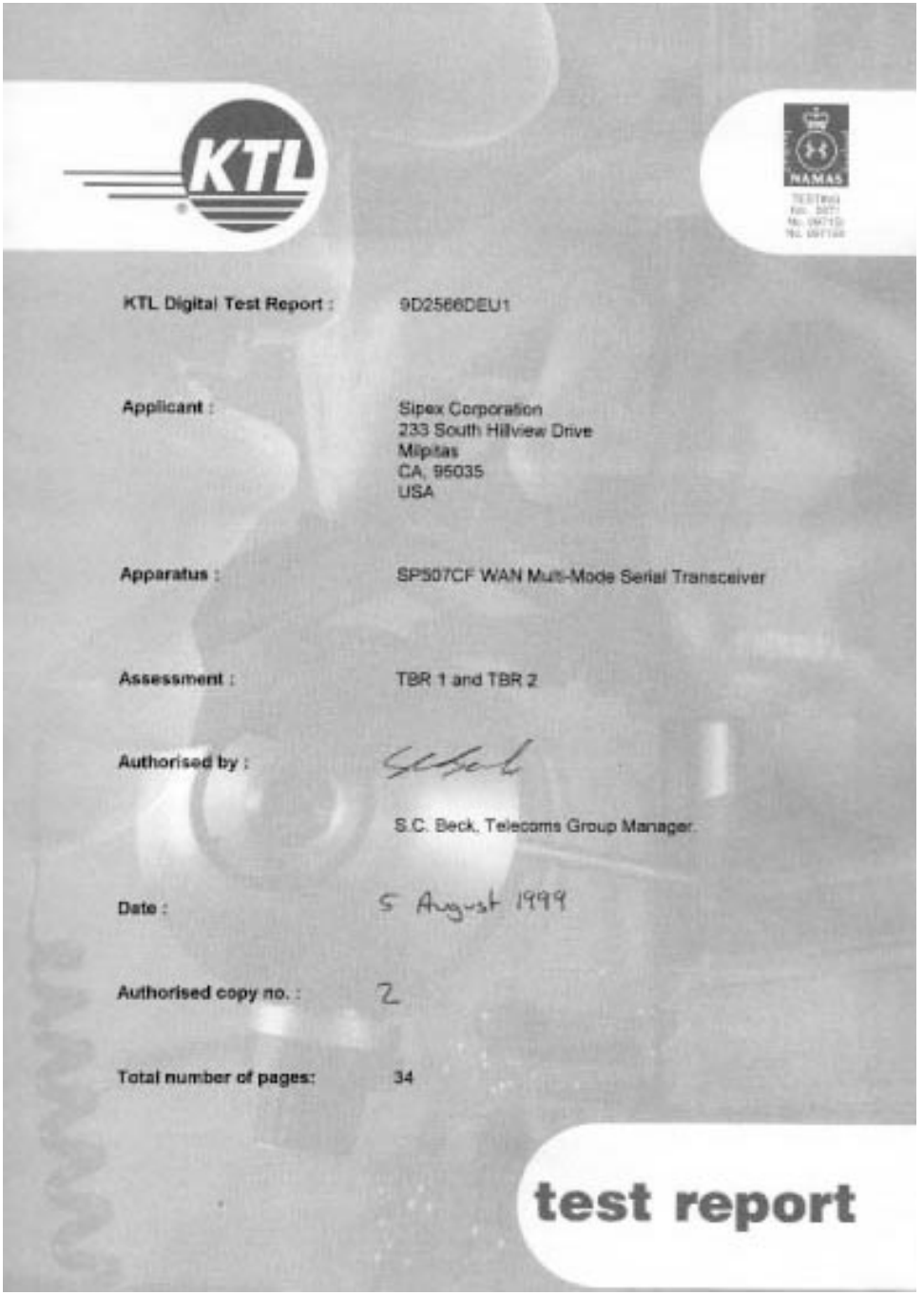

Figure 53. Front Cover of the CTR1/CTR2 Test Report for the SP507

ORDERING INFORMATION

Multi-Protocol Transceiver Products

Model	Temperature Range	Package Types
SP505CF	0°C to +70°C	80–pin JEDEC (BE-2 Outline) QFP
SP506CF	0°C to +70°C	80–pin JEDEC (BE-2 Outline) QFP
SP507CF	0°C to +70°C	80–pin JEDEC (BE-2 Outline) QFP

Evaluation and Retrofit Boards

Model	Description
SP505EB	SP505CF Evaluation Board
SP506EB	SP506CF Evaluation Board
SP507EB	SP507CF Evaluation Board
SP505RB	SP505CF Retrofit Board
SP506RB	SP506CF Retrofit Board
SP507RB	SP507CF Retrofit Board

Evaluation Kits
(Boxed with SP5xxEB, Product Datasheet, Application Note)

Model	Description
SP505EK	SP505CF Evaluation Kit
SP506EK	SP506CF Evaluation Kit
SP507EK	SP507CF Evaluation Kit

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