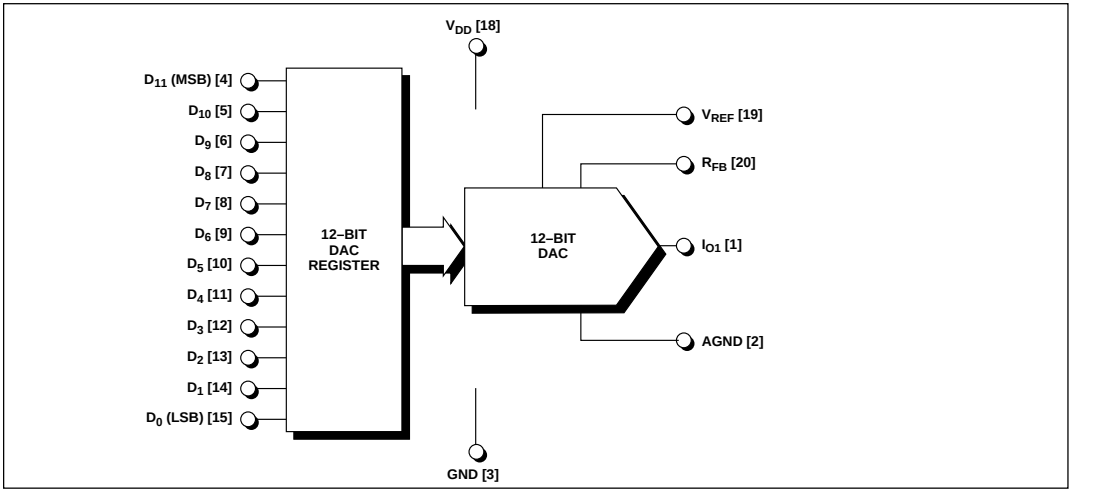
12–Bit, Buffered Multiplying DAC

- ±1.0 LSB Relative Accuracy Over Temperature
- Monotonic to 12–Bits Over Temperature
- High Stability, Segmented Architecture
- Proprietary, Low TCR Thin–Film Resistor Technology
- Operates With +5V to +15V Power Supplies
- On-Board, Level–Triggered Latches
- 2kVESD Protection on all Digital Inputs

DESCRIPTION…

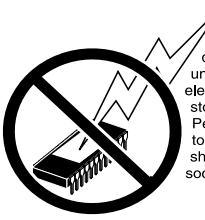
The **SP7545** is a low–cost, high stability 12–bit CMOS multiplying DAC with on–board data latches. The **SP7545** is constructed using a proprietary low–TCR thin–film process that requires no laser–trimming to achieve 12–bit performance. With no laser–trimming, inherent high stability, and a segmented (decoded) DAC architecture, the **SP7545** retains its performance over time and temperature. The **SP7545** is available for use in commercial and industrial temperature ranges. It is available in 20–pin plastic DIP and PLCC packages.



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted.)
These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{DD} to GND ..... –0.3V, +17V
Digital Input Voltage to GND ..... –0.3V, V_{DD}+0.3V
V_{REF} or V_{RFB} to GND ..... ±25V
Output Voltage (Pin 1, Pin 2) ..... –0.3V, V_{DD}+0.3V
Power Dissipation (Any Package to +75°C) 450mW
Derates above 75°C by ..... 6mW/°C
Dice Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 seconds) ..... +300°C



CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

(T_A=25°C; V_{DD} =+5V or +15V as noted; V_{REF} = +10V; I_{O1} = AGND = GND = 0V; unipolar unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
STATIC PERFORMANCE					
Resolution	12			Bits	
Integral Non-Linearity					Note 6
–J			±2.0	LSB	Note 5; 11-bit relative accuracy
–K			±1.0	LSB	Note 5; 12-bit relative accuracy
Differential Non-Linearity					Note 7
–J			±4.0	LSB	Note 5; monotonic to 12-bits
–K			±1.0	LSB	Note 5; monotonic to 12-bits
Gain Error					Note 16
–J			±20	LSB	V_{DD} = +5V; Note 5
			±25	LSB	V_{DD} = +15V
–K			±10	LSB	V_{DD} = +5V
			±15	LSB	V_{DD} = +15V
Output Leakage Current			±10	nA	At I_{O1} (Pin 1); Note 5 and 17
AC PERFORMANCE CHARACTERISTICS					Output Amplifier HOS-050; Note 10
Propagation Delay			300	ns	V_{DD} = +5V; Note 11
			250	ns	V_{DD} = +15V; Note 11
Current Settling Time			2.0	µs	Full scale transition; Note 12
Output Capacitance		50	200	pF	WR, CS = 0V; data inputs V_{DD}
			200	pF	Note 5; data inputs V_{DD}
		25	70	pF	Data inputs 0V
			70	pF	Note 5; data inputs 0V
Glitch Energy		250		nV-s	Note 13
Multiplying Feedthrough Error		2.0		mV_{P-P}	Measured at output I_{O1}; Note 14
		0.2		mV_{P-P}	Measured at output I_{O1}; Note 15
STABILITY					
Gain Error TC		±1.0	±2.0	ppm/°C	
			±2.0	ppm/°C	Note 5
Integral Non-Linearity TC		±0.1	±1.0	ppm/°C	
			±1.0	ppm/°C	Note 5
Differential Non-Linearity TC		±0.1	±1.0	ppm/°C	
			±1.0	ppm/°C	Note 5
Power Supply Rejection		±0.002	±0.01	%/%	%/0.005% change in power supply voltage
			±0.02	%/%	Note 5
REFERENCE INPUT					
Input Resistance	7	10	15	KΩ	Pin 19 to GND
Input Resistance TC		±150		ppm/°C	
Voltage Range			±25	Volts	Note 5 and 8

SPECIFICATIONS (continued)

(T_A=25°C; V_{DD} =+5V, V_{REF} = +10V; I_{O1} = AGND = GND = 0V; unipolar unless otherwise noted.)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DIGITAL INPUTS					
Logic Levels					
V_{IH}	2.4		V_{DD}	Volts	V_{DD} = +5V
			2.4	Volts	V_{DD} = +5V; Note 5
	13.5		V_{DD}	Volts	V_{DD} = +15V
			13.5	Volts	V_{DD} = +15V; Note 5
V_{IL}	-0.3		0.8	Volts	V_{DD} = +5V
			0.8	Volts	V_{DD} = +5V; Note 5
	-0.3		1.5	Volts	V_{DD} = +15V
			1.5	Volts	V_{DD} = +15V; Note 5
Input Current			±1.0	µA	V_{IN} = 0V or V_{DD}
			±10	µA	Note 5 and 9
Input Capacitance					V_{IN} = 0; Note 5 and 8
Bits 1—12			5	pF	
WR, CS			20	pF	
Coding					
Unipolar		Binary			
Bipolar		Offset Binary			
POWER REQUIREMENTS					
Supply Current			2.0	mA	All digital inputs V_{IL} or V_{IH}
			2.0	mA	Note 5; all digital inputs V_{IL} or V_{IH}
			0.5	mA	Note 18
				mA	Note 5 and 18
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
Commercial	0		+70	°C	
Industrial	-40		+85	°C	
Storage Temperature	-65		+150	°C	
Package	20–pin Plastic DIP 20–pin Plastic LCC				

Notes and Cautions:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal other than V_{REF} or V_{RFB}.
2. The digital inputs are diode-clamp protected against ESD damage. However, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation at or above these specifications is not implied. Exposure to the above maximum rated conditions for extended periods may affect device reliability.
5. From T_{MIN} to T_{MAX}.
6. End-point linearity
7. Differential Non-linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
8. Guaranteed by design, but not production tested.
9. Logic inputs are MOS gates. I_{IN} typically is less than 1nA @ 25°C.
10. AC performance characteristics are included for design guidance only and are subject to sample testing only.
11. R_L = 100Ω, C_{EXT} = 13pF; all data inputs 0V to V_{DD} or V_{DD} to 0V; from 50% digital input change to 90% of final analog output.
12. Settling to ±0.01% FSR (strobed); all data inputs 0V to V_{DD} or V_{DD} to 0V.
13. V_{REF} = 0V, DAC register alternatively loaded with all 0’s and all 1’s.
14. V_{REF} = $20V_{P-P}$; F = 10kHz sinewave.
15. V_{REF} = $20V_{P-P}$; F = 1kHz sinewave.
16. Measured using internal feedback resistor with DAC loaded with all 1’s.
17. All digital inputs = 0V.
18. All digital inputs 0V or V_{DD}.

ORDERING INFORMATION

Model	Integral Linearity	Package
0°C to +70°C Operating Temperature		
SP7545JCN	±2LSB	20–pin, 0.3" Plastic DIP
SP7545JCL	±2LSB	20–pin PLCC
SP7545KCN	±1LSB	20–pin, 0.3" Plastic DIP
SP7545KCL	±1LSB	20–pin PLCC
–40°C to +85°C Operating Temperature		
SP7545JIN	±2LSB	20–pin, 0.3" Plastic DIP
SP7545JIL	±2LSB	20–pin PLCC
SP7545KIN	±1LSB	20–pin, 0.3" Plastic DIP
SP7545KIL	±1LSB	20–pin PLCC