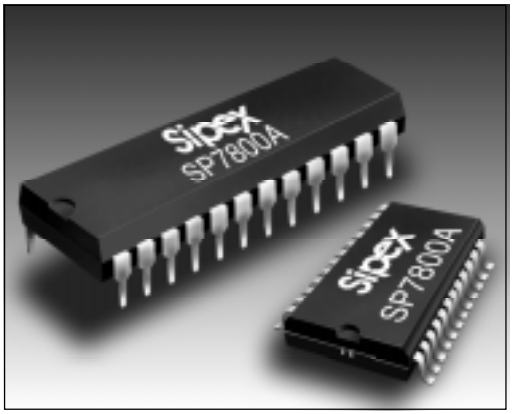
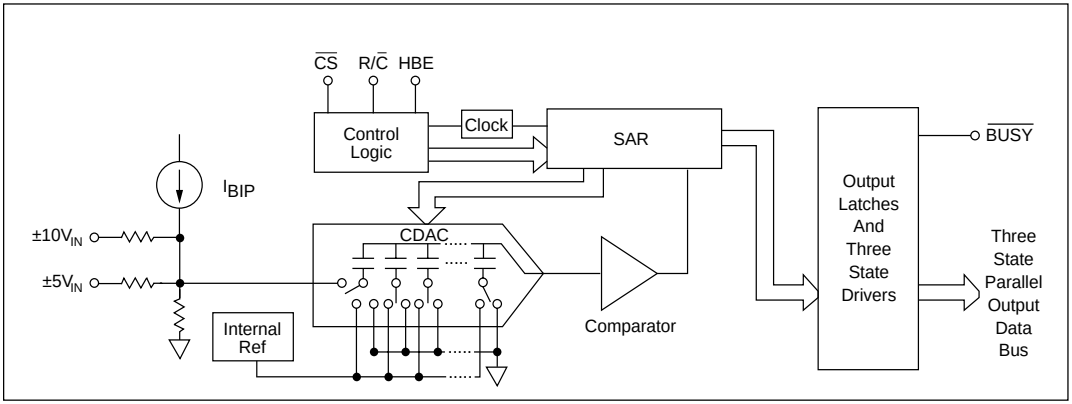
12-Bit 3µs Sampling A/D Converter

- 333k Samples Per Second
- Standard ±10V and ±5V Input
- No Missing Codes Over Temperature
- AC Performance Over Temperature
  - 71.5dB Signal–to–Noise Ratio at Nyquist
  - 85dB Spurious–free Dynamic Range at 49KHz
  - –81dB Total Harmonic Distortion at 49KHz
- Internal Sample/Hold, Reference, Clock, and 3-State Outputs
- Power Dissipation: 90mW
- 24–Pin Narrow DIP and 24–Lead SOIC
- Enhanced Single (+5V) Supply Version of ADS7800



DESCRIPTION…

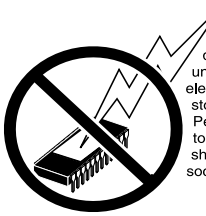
The **SP7800A** is a complete 12-bit sampling A/D converter using state–of–the–art CMOS structures. It contains a complete 12–bit successive approximation A/D converter with internal sample/hold, reference, clock, digital interface for microprocessor control, and three–state output drivers. AC and DC performance are completely specified. Two grades based on linearity and dynamic performance are available to provide the optimum price/performance fit in a wide range of applications.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_S to Digital Common ..... +7V
Pin 23 (V_{SO}) to Pin 24 (V_{SA}) ..... ±0.3V
Analog Common to Digital Common ..... ±0.3V
Control Inputs to Digital Common ..... –0.3 to V_S + 0.3 V
Analog Input Voltage ..... ±20V
Maximum Junction Temperature ..... 160°C
Internal Power Dissipation 750mW
Lead Temperature (soldering, 10s) ..... +300°C
Thermal Resistance. $Ø_{JA}$:
Plastic DIP ..... 50°C/W
SOIC ..... 100°CC/W



CAUTION: ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

T_A = 25°C, Sampling Frequency, f_8, = 333kHz, V_S = +5V, unless otherwise specified.

PARAMETER	MIN .	TYP.	MAX .	UNITS	CONDITIONS
RESOLUTION			**12**	**BITS**	
ANALOG INPUT					
Voltage Ranges		±10V/±5V		V	
Impedance					
±10V Range	4.7	6.7	8.7	kΩ	$T_{MIN} \le T_A \le T_{MAX}$
±5V Range	2.7	3.9	5.1	kΩ	$T_{MIN} \le T_A \le T_{MAX}$
THROUGHPUT SPEED					
Conversion Time		2.6	2.7	µs	Conversion alone
Complete Cycle			333	µs	Acquisition plus conversion
Throughput Rate	3.0			kHz	
DC ACCURACY					$T_{MIN} \le T_A \le T_{MAX}$
Full Scale Error					Note 1
–J			±0.50	%	
–K			±0.35	%	
Integral Linearity Error					Note 2
–J			±1	LSB	
–K			±½	LSB	
Differential Linearity Error					
–J			±1	LSB	
–K			±¾	LSB	
No Missing Codes		Guaranteed			
Bipolar Zero					Note 1
–J			±4	LSB	
–K			±2	LSB	
Power Supply Sensitivity					Note 3
–J		±.1		LSB	
–K		±0.5		LSB	
AC ACCURACY					$T_{MIN} \le T_A \le T_{MAX}$
Spurious-Free Dynamic Range					
–J	74	77		dB	Note 4; f_{IN} = 47kHz
–K	77	80		dB	
Total Harmonic Distortion					f_{IN} = 47kHz
–J		–77	–74	dB	
–K		–80	–77	dB	
Two-tone Intermod. Distortion					f_{IN1} = 24.4kHz (–6dB); f_{IN2} = 28.5kHz (-6dB)
–J		–77	–74	dB	
–K		–80	–77	dB	

SPECIFICATIONS (continued)

T_A = 25°C, Sampling Frequency, f_s, = 333kHz, V_S = +5V, unless otherwise specified.

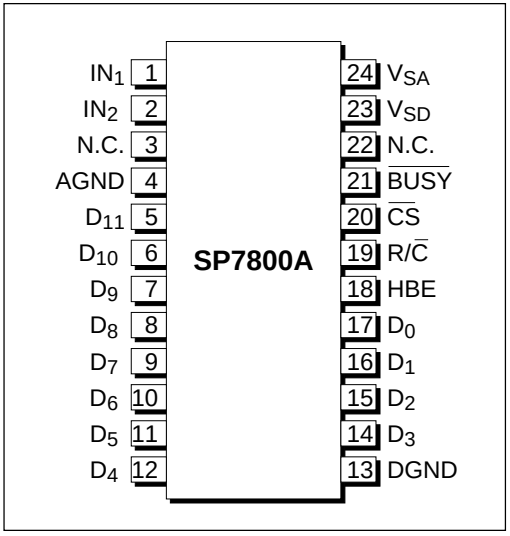
PARAMETER	MIN .	TYP.	MAX .	UNITS	CONDITIONS
AC ACCURACY					$T_{MIN} \le T_A \le T_{MAX}$
Signal to (Noise + Distortion) Ratio					f_{IN} = 47kHz
–J	67	70		dB	
–K	69	71.0		dB	
Signal to Noise Ratio (SNR)					f_{IN} = 47kHz
–J	68	71		dB	
–K	70	71.5		dB	
SAMPLING DYNAMICS					
Aperture Delay		13		ns	
Aperture Jitter		150		ps, rms	
Transient Response					Note 5
–J		130		ns	
–K		150		ns	
Overvoltage Recovery		150		ns	Note 6
DIGITAL INPUTS					$T_{MIN} \le T_A \le T_{MAX}$
Logic Levels					
V_{IL}	–0.3		+0.8	V	
V_{IH}	+2.4		+5.3	V	
I_{IL}	–5			µA	
I_{IH}	+5			µA	
DIGITAL OUTPUTS					
Data Format	Parallel; 12-bit or 8-bit/4-bit				
Data Coding	Binary; Offset Binary				
V_{OL}	DGND		+0.4	V	I_{SINK} = 1.6mA
V_{OH}	+2.4		V_{DD}	V	I_{SOURCE} = 1.6mA
$I_{LEAKAGE}$ (High-Z State)		±0.1	±5	µA	
POWER SUPPLY REQUIREMENTS					
Rated Voltage	+4.75	+5.0	+5.25	V	V_S (V_{SA} and V_{SD})
Current		18	21	mA	I_S
Power Consumption		90		mW	
ENVIRONMENTAL AND MECHANICAL					
Specification					
–J, –K	0		+70	°C	
Storage	–65		+150	°C	
Package					
–_N	24–pin Narrow DIP				
–_S	24–pin SOIC				

NOTES

1. Adjustable to zero with external potentiometer.
2. LSB means Least Significant Bit. For SP7800A, 1LSB = 2.44mV for ±5V range, 1 LSB = 4.88mV for ±10V range.
3. Measured at mid-range, between 4.75 < V_S < 5.25 volts.
4. All specifications in dB are referred to a full-scale input, either ±10V or ±5V.
5. For full-scale step input, 12-bit accuracy attained in specified time.
6. Recovers to specified performance in specified time after 2 x F_S input overvoltage.

OBSOLETE - HISTORICAL REFERENCE ONLY

PINOUT



PIN ASSIGNMENT

Pin 1 — IN_1 — ±10V Analog Input. Connected to AGND for ±5V range.

Pin 2 — IN_2 — ±5V Analog Input. Connected to AGND for ±10V range.

Pin 3 — N.C. — This pin is not internally connected.

Pin 4 — AGND — Analog Ground. Connect to pin 13 at the device.

Pin 5 — D_{11} — Data Bit 11. Most Significant Bit (MSB).

Pin 6 — D_{10} — Data Bit 10.

Pin 7 — D_9 — Data Bit 9.

Pin 8 — D_8 — Data Bit 8.

Pin 9 — D_7 — Data Bit 7 if HBE is LOW; LOW if HBE is HIGH.

Pin 10 — D_6 — Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.

Pin 11 — D_5 — Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.

Pin 12 — D_4 — Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.

Pin 13 — DGND — Digital Ground. Connect to pin 4 at the device.

Pin 14 — D_3 — Data Bit 3 if HBE is LOW; Data Bit 11 if HBE is HIGH.

Pin 15 — D_2 — Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.

Pin 16 — D_1 — Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.

Pin 17 — D_0 — Data Bit 0 if HBE is LOW. Least Significant Bit (LSB). Data Bit 8 if HBE is HIGH.

Pin 18 — HBE — High Byte Enable, When held LOW, data output as 12-bits in parallel. When held HIGH, four MSBs presented on pins 14–17, pins 9 – 12 output LOWs. Must be LOW to initiate conversion.

Pin 19 — R/$\overline{C}$ — Read/$\overline{Convert}$. Falling edge initiates conversion when $\overline{CS}$ is LOW, HBE is LOW, and $\overline{BUSY}$ is HIGH.

Pin 20 — $\overline{CS}$ — Chip Select. Outputs in Hi-Z state when HIGH. Must be LOW to initiate conversion or read data.

Pin 21 — $\overline{BUSY}$. Output LOW during conversion. Data valid on rising edge in Convert Mode.

Pin 22 — N.C. — This pin is not internally connected.

Pin 23 — V_{SD} — Positive Digital Power Supply, +5V. Connect to pin 24, and bypass to DGND.

Pin 24 — V_{SA} — Positive Analog Power Supply. +5V. Connect to pin 23, and bypass to AGND.

FEATURES...

The **SP7800A** is specified at a 333kHz sampling rate. Conversion time is factory set for 2.70µs max over temperature, and the high-speed sampling input stage insures a total acquisition and conversion time of 3µs max over temperature. Precision, laser–trimmed scal-

ing resistors provide industry–standard input ranges of ±5V or ±10V. The 24-pin **SP7800A** is available in plastic DIP, and SOIC packages and it operates from a single +5V supply. The **SP7800A** is available in grades specified over the 0°C to +70°C commercial temperature ranges.

OPERATION...

Basic Operation

Figure 1 shows the simple hookup circuit required to operate the **SP7800A** in a ±10V range in the Convert Mode. A convert command arriving on R/$\overline{C}$, (a pulse taking R/$\overline{C}$ LOW for a minimum of 40ns) puts the **SP7800A** in the HOLD mode, and a conversion is started. The falling edge of R/$\overline{C}$ establishes the sampling instant of the A/D; it must therefore have very low jitter. $\overline{BUSY}$ will be held LOW during the conversion, and rises only after the conversion is completed and the data has been transferred to the output drivers. Thus, the rising edge can be used to read the data from the conversion. Also, during conversion, the $\overline{BUSY}$ signal puts the output data lines in Hi-Z states and inhibits the input lines. This means that pulses on R/$\overline{C}$ are ignored, so that new conversions cannot be initiated during a conversion, either as a result of spurious signals or to short-cycle the **SP7800A.**

In the Read Mode, the input to R/$\overline{C}$ is kept normally LOW, and a HIGH pulse is used to read data and initiate a conversion. In this mode, the rising edge of R/$\overline{C}$ will enable the output data pins, and the data from the previous conversion becomes valid. The falling edge then puts the **SP7800A** in a hold mode, and initiates a new conversion.

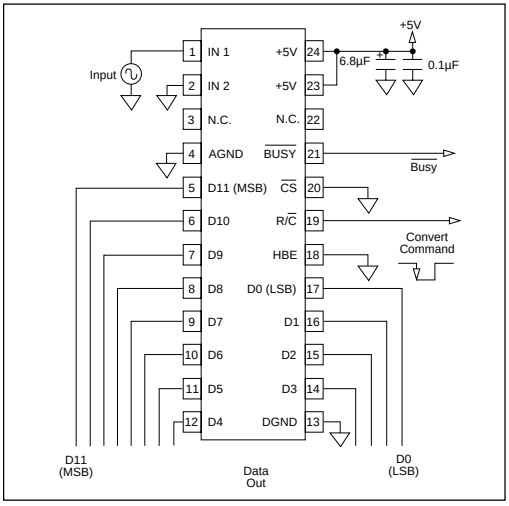


Figure 1. Basic ±10V Operation

The **SP7800A** will begin acquiring a new sample just prior to $\overline{BUSY}$ output rising, and will track the input signal until the next conversion is started.

For use with an 8-bit bus, the data can be read out in two bytes under the control of HBE. With a LOW input on HBE, at the end of a conversion, the 8 LSBs of data are loaded into the output drivers D_7 – D_4 and D_3–D_0. Taking HBE HIGH then loads the 4 MSBs on output drivers D_3–D_0, with D_7–D_4 being forced LOW.

Analog Input Ranges

The **SP7800A** offers two standard bipolar input ranges: ±10V and ±5V. If a ±10V range is required, the analog input signal should be connected to pin 1. A signal requiring a ±5V range should be connected to pin 2. In either case, the other pin of the two must be grounded or connected to the adjustment circuits described in the section on calibration.

Controlling The SP7800A

The **SP7800A** can be easily interfaced to most microprocessor-based and other digital systems. The microprocessor may take full control of each conversion, or the **SP7800A** may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of initiating the conversion and reading the output data at user command, transmitting data either all 12-bits in one parallel word, or in two 8-bit bytes. The three control inputs ($\overline{CS}$, R/$\overline{C}$ and HBE) are all TTL/CMOS compatible. The functions of the control lines are shown in *Table 1*.

For stand-alone operation, control of the **SP7800A** is accomplished by a single control line connected to R/$\overline{C}$. In this mode, $\overline{CS}$ and HBE are connected to GND. The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a HIGH-to-LOW transition

CS	R/$\overline{C}$	HBE	BUSY	OPERATION
1	X	X	1	None – outputs in Hi-Z state.
0	1 ↓ 0	0	1	Holds signal and initiates conversion.
0	1	0	1	Output three-state buffers enabled once conversion has finished.
0	1	1	1	Enable hi-byte in 8-bit bus mode.
0	1 ↓ 0	1	1	Inhibit start of conversion.
0	0	1	1	None – outputs in Hi-Z state.
X	X	X	0	Conversion in progress. Outputs Hi-Z state. New conversion inhibited until present conversion has finished.

Table 1. Control Line Functions

on R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is HIGH and $\overline{BUSY}$ is HIGH. Thus, there are two possible modes of operation: conversion can be initiated with either positive or negative pulses. In either case, the R/$\overline{C}$ pulse must remain LOW a minimum of 40ns.

Figure 5 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes LOW and returns HIGH during the conversion. In this case (Convert Mode), the three-state outputs go into the Hi-Z state in response to the falling edge of R/$\overline{C}$, and are enabled for external access to the data after completion of the conversion.

Figure 6 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode (Read Mode), the output data from the previous conversion is enabled during the HIGH portion of R/$\overline{C}$. A new conversion starts on the falling edge of R/$\overline{C}$, and the three-state outputs return to the Hi-Z state until the next occurrence of a HIGH on R/$\overline{C}$.

Conversion Start

A conversion is initiated on the **SP7800A** only by a negative transition occurring on R/$\overline{C}$, as shown in *Table 2*. No other combination of states or transitions will initiate a conversion. Conversion is inhibited if either $\overline{CS}$ or HBE are HIGH, or if $\overline{BUSY}$ is LOW. $\overline{CS}$ and HBE should be stable a minimum of 25ns prior to the transition on R/$\overline{C}$. Timing relationships for start of conversion are illustrated in *Figure 7*.

The $\overline{BUSY}$ output indicates the current state of the converter by being LOW only during conversion. During this time the three-state output buffers remain in a Hi-Z state, and therefore data cannot be read during conversion. During this period, additional transitions on the three digital inputs ($\overline{CS}$, R/$\overline{C}$ and HBE) will be ignored, so that conversion cannot be prematurely terminated or restarted.

Internal Clock

The **SP7800A** has an internal clock that is factory trimmed to achieve a typical conversion time of 2.6µs, and a maximum conversion time over the full operating temperature range of 2.7µs. No external adjustments are required, and with the guaranteed maximum acquisition time of 300ns, throughput performance is assured with convert pulses as close as 3µs.

Reading Data

After conversion is initiated, the output buffers remain in a Hi-Z state until the following three logic conditions are simultaneously met: R/$\overline{C}$ is HIGH, $\overline{BUSY}$ is HIGH and $\overline{CS}$ is LOW. Upon satisfying these conditions, the data lines are enabled according to the state of HBE. See *Figure 7* for timing relationships and specifications.

CALIBRATION...
Optional External Gain And Offset Trim

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the **SP7800A** as shown in *Figure 3*.

If adjustment of offset and full scale is not required, connections as shown in *Figure 2* should be used.

Calibration Procedure

Apply a precision input voltage source to your chosen input range (±10V range at pin1 or ±5V at pin 2). Set the A/D to convert continuously. Monitor the output code. Trim the offset first, then gain. Use the appropriate input voltages and output target codes for your chosen input range as follows. The recommended offset calibration voltage values eliminate interaction between the offset and gain calibration.

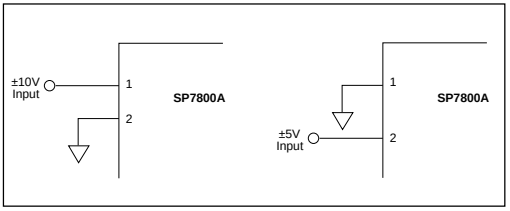


Figure 2. a) ±10V Range b) ±5V Range — Without Trims

INPUT VOLTAGE RANGE AND LSB VALUES			
Input Voltage Range Defined As:		±10V	±5V
Analog Input Connected to Pin		1	2
Pin Connected to GND		2	1
One Least Significant Bit (LSB)	$FSR/2^{12}$	$20V/2^{12}$ 4.88mV	$10V/2^{12}$ 2.44mV
OUTPUT TRANSITION VALUES			
FFEH TO FFFH	+ FULL SCALE	+10V–3/2LSB +9.9927V	+5V–3/2LSB +4.9963V
7FFH TO 800H	Mid Scale (Bipolar Zero)	0V–1/2LSB –2.44mV	0V–1/2LSB –1.22mV
000H to 001H	–Full Scale	–10V+1/2LSB -9.9976V	–5V+1/2LSB -4.9988V

Table 2. Input Voltages, Transition Voltages and LSB Values

±5V Range Offset and Gain

Offset — Apply 1.5637V to the ±5V input at pin 2. Adjust the offset potentiometer until the LSB toggles on and off at code $1010\ 1000\ 0000_{BIN} = A80_H = 2688_{DEC}$.

Gain — Apply 4.9963V to the ±5V input at pin 2. Adjust the gain potentiometer until the LSB toggles on and off at code $1111\ 1111\ 1110_{BIN} = FFE_H = 4094_{DEC}$.

±10V Range Offset and Gain

Offset — Apply 1.2622V to the ±10V input at pin 1. Adjust the offset potentiometer until the LSB toggles on and off at code $1001\ 0000\ 0010_{BIN} = 902_H = 2306_{DEC}$.

Gain — Apply 9.9927V to the ±10V input at pin 1. Adjust the gain potentiometer until the LSB toggles on and off at code $1111\ 1111\ 1110_{BIN} = FFE_H = 4094_{DEC}$.

Layout Considerations

Because of the high resolution and linearity of the **SP7800A**, system design problems such as ground path resistance and contact resistance become very important.

The input resistance of the **SP7800A** is 6.3kΩ or 4.2KΩ (for the ±10V and ±5V ranges respectively). To avoid introducing distortion, the source resistance must be very low, or constant with signal level. The output impedance provided by most op amps is ideal. Pins 23 (V_{SD}) and 24 (V_{SA}) are not connected internally on the **SP7800A**, to maximize accuracy on the chip. They should be connected together as close as possible to the unit. Pin 24 may be slightly more sensitive than pin 23 to supply variations, but to maintain

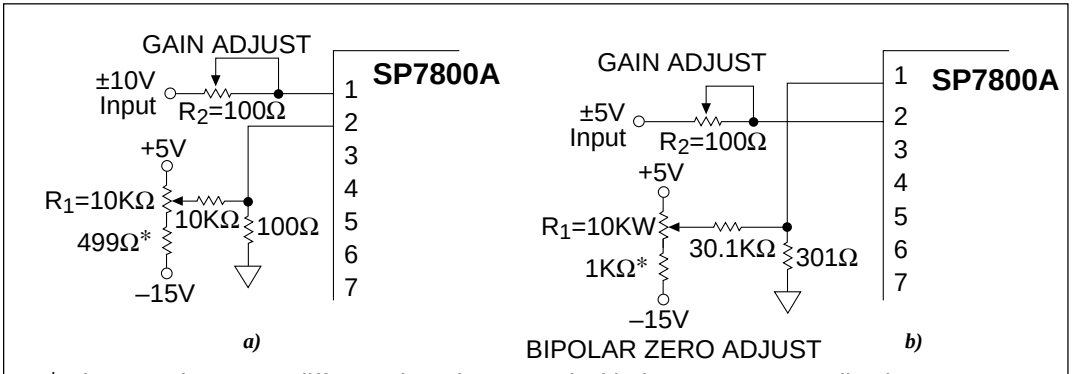


Figure 3. a) ±10V Range b) ±5V Range — With External Trims

maximum system accuracy, both should be well–isolated from digital supplies with wide load variations.

To limit the effects of digital switching elsewhere in a system on the analog performance of the system, it often makes sense to run a separate +5V supply conductor from the supply regulator to any analog components requiring +5V, including the **SP7800A.** If the **SP7800A** traces cannot be separated back to the power supply terminals, and therefore share the same trace as the logic supply currents, then a 10 Ohm isolating resistor should be used between the board supply and pin 24 (V_{DA}) and its bypass capacitors to keep V_{DA} glitch–free. The V_S pins (23 and 24) should be connected together and bypassed with a parallel combination of a 6.8µF Tantalum capacitor and a 0.1µF ceramic capacitor located close to the converter to obtain noise-free operation. (See *Figure 1*). Noise on the power supply lines can degrade converter performance, especially noise and spikes from a switching power supply. Appropriate supplies or filters must be used.

The GND pins (4 and 13) are also separated internally, and should be directly connected to a ground plane under the converter. A ground plane is usually the best solution for preserving dynamic performance and reducing noise coupling into sensitive converter circuits. Where any compromises must be made, the common return of the analog input signal should be referenced to pin 4, AGND, on the **SP7800A,** which prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

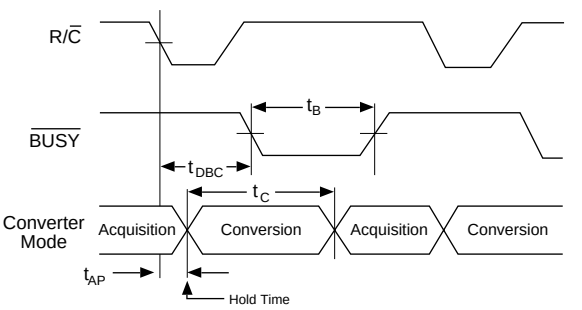
If external full scale and offset potentiometers are used, the potentiometers and related resistors should be located as close to the **SP7800A** as possible.

"Hot Socket" Precaution

Two separate +5V V_S pins, 23 and 24, are used to minimize noise caused by digital transients. If one pin is powered and the other is not, the **SP7800A** may draw excessive current. In normal operation, this is not a problem because both pins will be soldered together. However, during evaluation, incoming inspection, repair, etc., where the potential of a "Hot Socket" exists, care should be taken to apply power to the **SP7800A** only after it has been socketed.

Minimizing "Glitches"

Coupling of external transients into an analog-to-digital converter can cause errors which are difficult to debug. In addition to the discussions earlier on layout considerations for supplies, bypassing and grounding, there are several other useful steps that can be taken to get the best analog performance out of a system using



SYMBOL/PARAMETER		MIN	TYP	MAX	UNITS
t_{DBC}	BUSY delay from R/C		80	150	ns
t_B	BUSY Low		2.5	2.7	µs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.47	2.70	µs

Figure 4. Acquisition and Conversion Timing

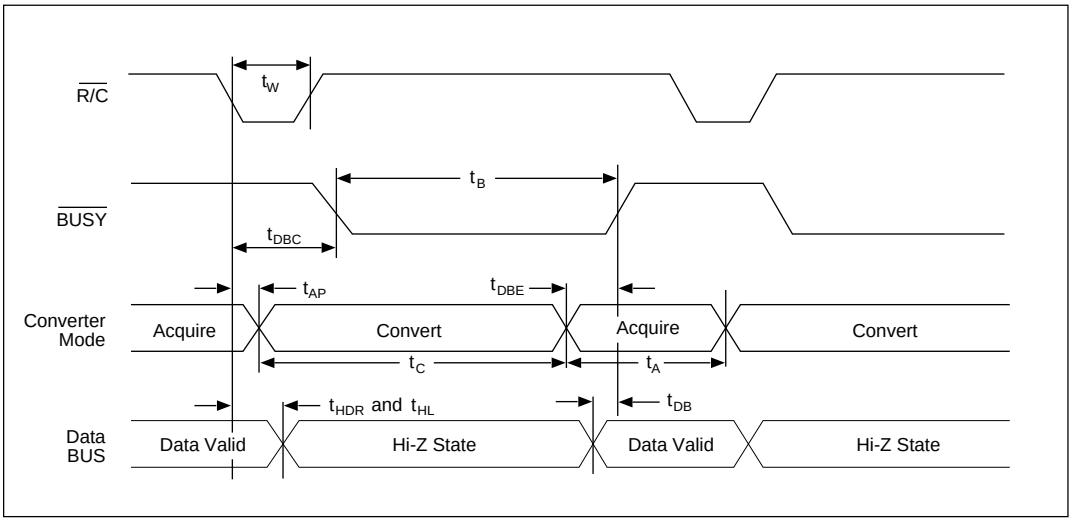


Figure 5. Convert Mode Timing — R/$\overline{C}$ Pulse LOW, Outputs Enabled After Conversion

the **SP7800A.** These potential system problem sources are particularly important to consider when developing a new system, and looking for the causes of errors in breadboards.

First, care should be taken to avoid glitches during critical times in the sampling and conversion process. Since the **SP7800A** has an internal sample/hold function, the signal that puts it into the hold state (R/$\overline{C}$ going LOW) is critical, as it would be on any sample/hold amplifier. The R/$\overline{C}$ falling edge should be sharp (5 to 10ns), have low jitter and minimal ringing, especially during the 20ns after it falls.

Although not normally required, it is also good practice to avoid glitches from coupling to the **SP7800A** while bit decisions are being made. Since the above discussion calls for a fast, clean rise and fall on R/$\overline{C}$, it makes sense to keep the rising edge of the convert pulse outside the time when bit decisions are being made. In other words, the convert pulse should either be short (under 100ns so that it transitions before the MSB decision), or relatively long (over 2.75µs to transition after the LSB decision).

Next, although the data outputs are forced into a Hi-Z state during conversion, fast bus transients can still be capacitively coupled into the **SP7800A.** If the data bus experiences fast transients during conversion, these transients can be attenuated by adding a logic buffer to the data outputs. The $\overline{BUSY}$ output can be used to enable the buffer.

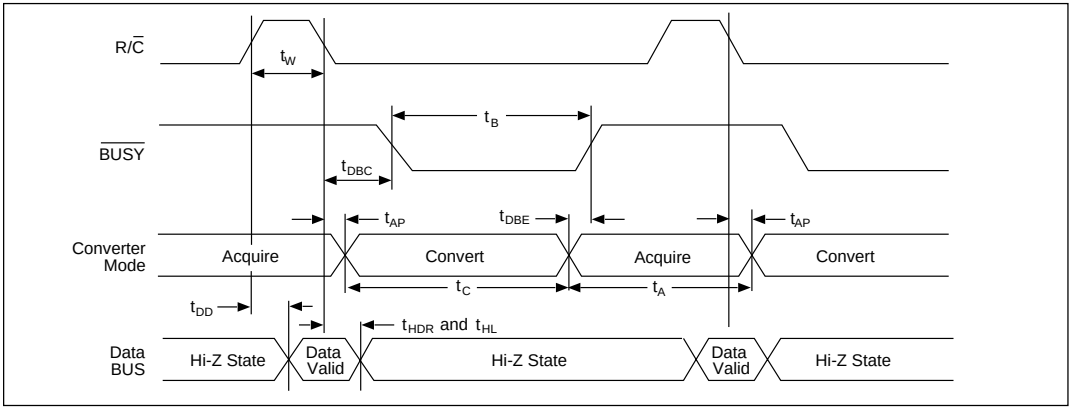


Figure 6. Read Mode Timing — R/$\overline{C}$ Pulse HIGH, Outputs Enabled Only When R/$\overline{C}$ is High

AC DYNAMIC TIMING DATA

SYMBOL/PARAMETER		MIN	TYP	MAX	UNITS
t_W	R/$\overline{C}$ Pulse Width	40	10		ns
t_{DBC}	$\overline{BUSY}$ delay from R/$\overline{C}$		80	150	ns
t_B	$\overline{BUSY}$ LOW		2.47	2.7	µs
t_{AP}	Aperture Delay		13		ns
Δt_{AP}	Aperture Jitter		150		ps, rms
t_C	Conversion Time		2.5	2.70	µs
t_{DBE}	$\overline{BUSY}$ from End of Conversion		100		ns
t_{DB}	$\overline{BUSY}$ Delay after Data Valid	25	75	200	ns
t_A	Acquisition Time		130	300	ns
$t_A + t_C$	Throughput Time	3.0			µs
t_{HDR}	Valid Data Held After R/$\overline{C}$ LOW	20	50		ns
t_S	$\overline{CS}$ or HBE LOW before R/$\overline{C}$ Falls	25	5		ns
t_H	$\overline{CS}$ or HBE LOW after R/$\overline{C}$ Falls	25	0		ns
t_{DD}	Data Valid from $\overline{CS}$ LOW, R/$\overline{C}$ HIGH, and HBE in Desired State (Load = 100pF)		65	150	ns
t_{HL}	Delay to Hi-Z State after R/$\overline{C}$ Falls or $\overline{CS}$ Rises (3KΩ Pullup or Pulldown		50	150	ns
All parameters Guaranteed By Design					

Naturally, transients on the analog input signal are to be avoided, especially at times within ±20ns of R/$\overline{C}$ going LOW, when they may be trapped as part of the charge on the capacitor array. This requires careful layout of the circuit in front of the **SP7800A.**

Finally, in multiplexed systems, the timing relative to when the multiplexer is switched may affect the analog performance of the system. In most applications, the multiplexer can be switched as soon as R/$\overline{C}$ goes LOW (with appropriate delays), but this may affect the conversion if the switched signal shows glitches or significant ringing at the **SP7800A** input. Whenever possible, it is safer to wait until the conversion is completed before switching and multiplexer. The extremely fast acquisition time and conversion time of the **SP7800A** make this practical in many applications.

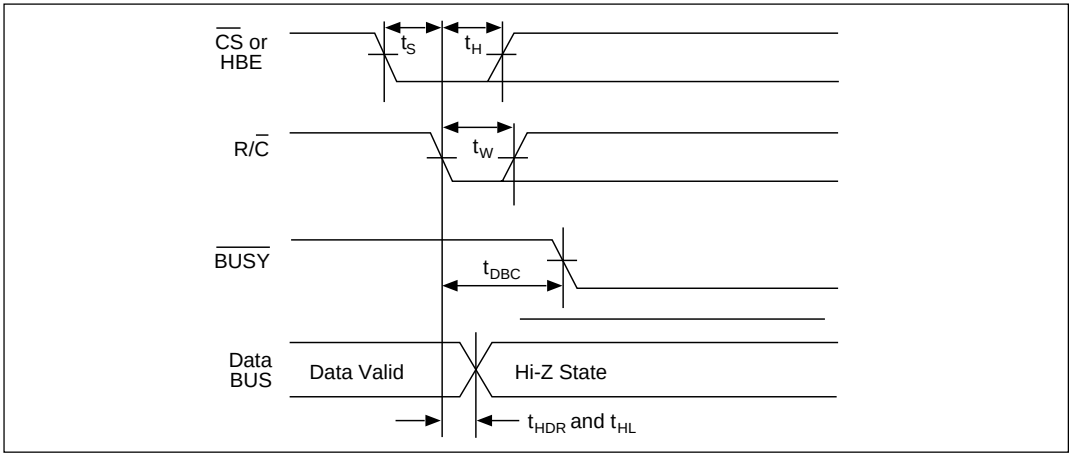
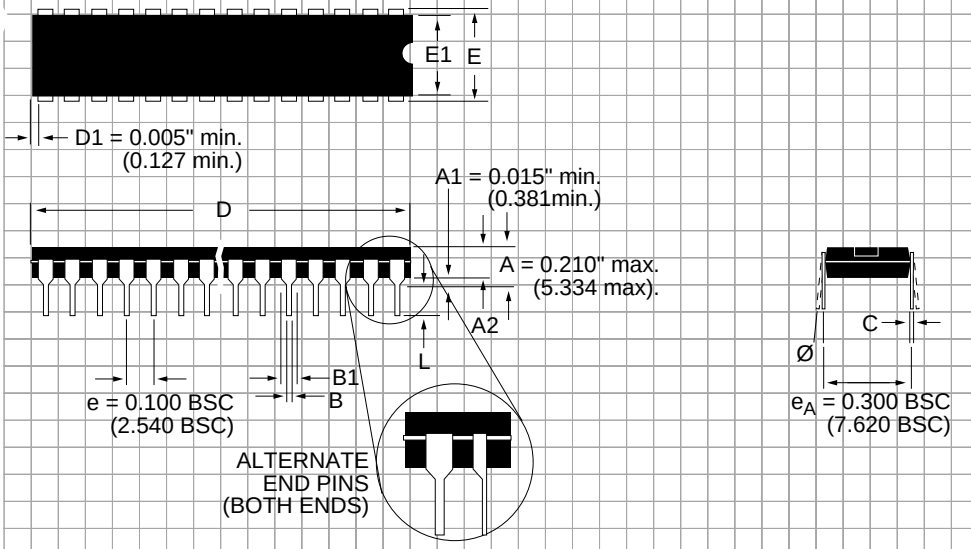


Figure 7. Conversion Start Timing

OBSOLETE - HISTORICAL REFERENCE ONLY

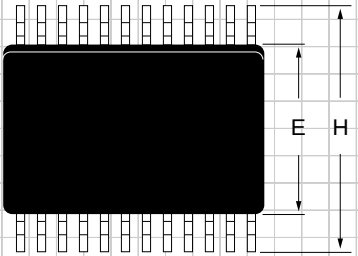
PACKAGE: PLASTIC DUAL–IN–LINE (NARROW)

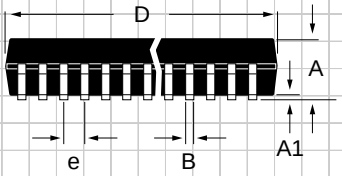


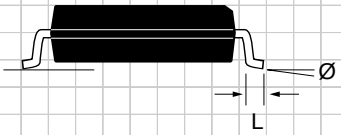
DIMENSIONS (Inches) Minimum/Maximum (mm)	24–PIN	28–PIN				
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)				
B	0.014/0.023 (0.356/0.584)	0.014/0.022 (0.356/0.559)				
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)				
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)				
D	1.155/1.280 (29.33/32.51)	1.385/1.454 (35.17/36.90)				
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)				
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)				
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)				
Ø	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)				

OBSOLETE - HISTORICAL REFERENCE ONLY

PACKAGE: PLASTIC SMALL OUTLINE (SOIC)







DIMENSIONS (Inches) Minimum/Maximum (mm)	14–PIN	16–PIN	18–PIN	20–PIN	24–PIN	28–PIN
A	0.090/0.104 (2.29/2.649))	0.090/0.104 (2.29/2.649)	0.090/0.104 (2.29/2.649))	0.090/0.104 (2.29/2.649)	0.090/0.104 (2.29/2.649)	0.090/0.104 (2.29/2.649)
A1	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)
D	0.348/0.363 (8.83/9.22)	0.398/0.413 (10.10/10.49)	0.447/0.463 (11.35/11.74)	0.496/0.512 (12.60/13.00)	0.599/0.614 (15.20/15.59)	0.697/0.713 (17.70/18.09)
E	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC))	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

ORDERING INFORMATION

0°C to +70°C	Linearity	Package
SP7800AJN	±1 LSB INL	24–pin, 0.3" PDIP
SP7800AKN	±1/2 LSB INL	24–pin, 0.3" PDIP
SP7800AJS	±1LSB INL	24–pin, 0.3" SOIC
SP7800AKS	±1/2 LSB INL	24–pin, 0.3" SOIC

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